

# Non-BELLE applications

## Multigate DEPFETs – future trends and possible applications

19<sup>th</sup> international workshop on DEPFET detectors

Seon monastery

11.5.2007

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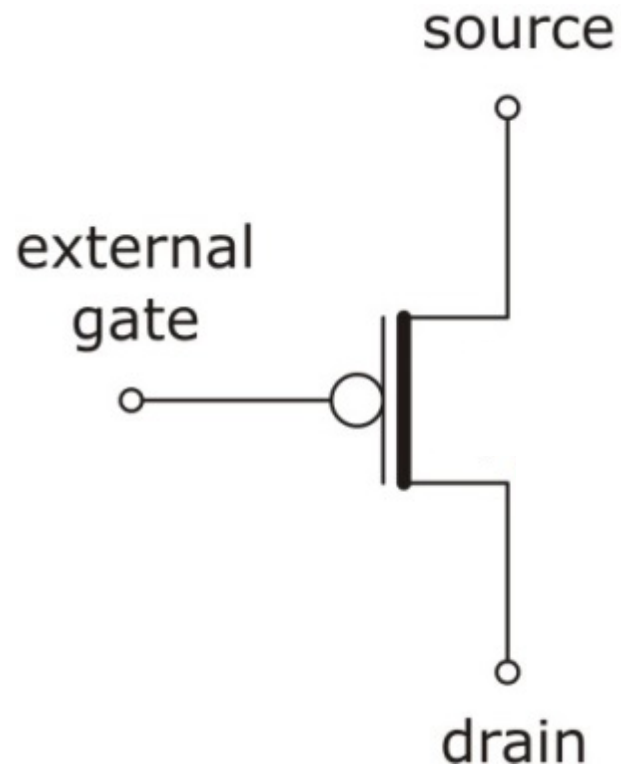
- Standard DEPFET
- GPIX:
  - GPIX Barrier gate
  - GPIX Blindgate
- Infinipix variants:
  - Infinipix
  - Infinipix Quad (IQ)
  - Central Anode (IQCA)
- DEPFET RNDR
- RNDR GPIx
- RNDR INFINIPIX
- Application prospects

**BORING!**

Welcome to...



# DEPFET

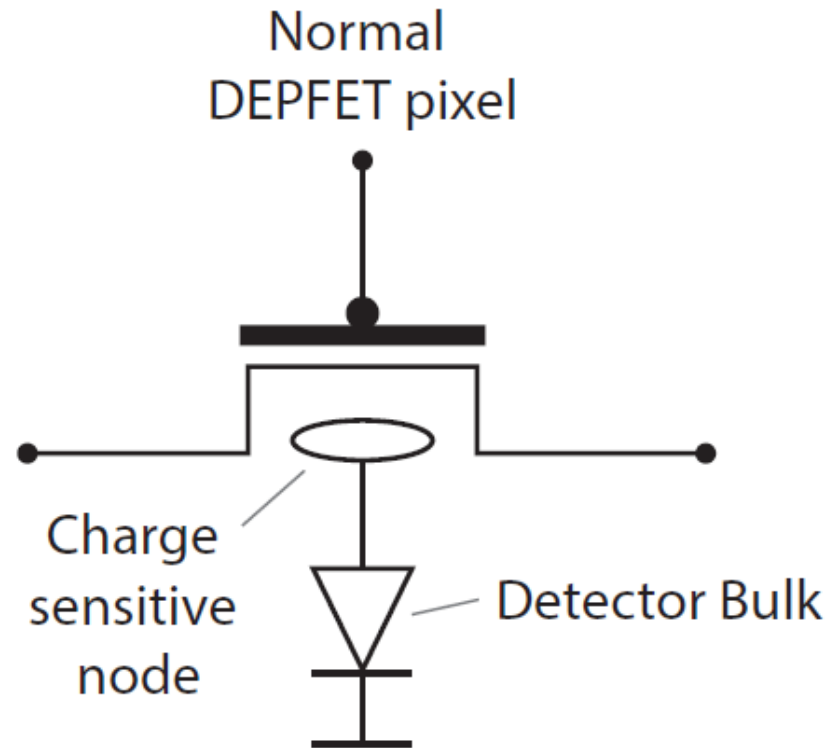


# Multigate DEPFET

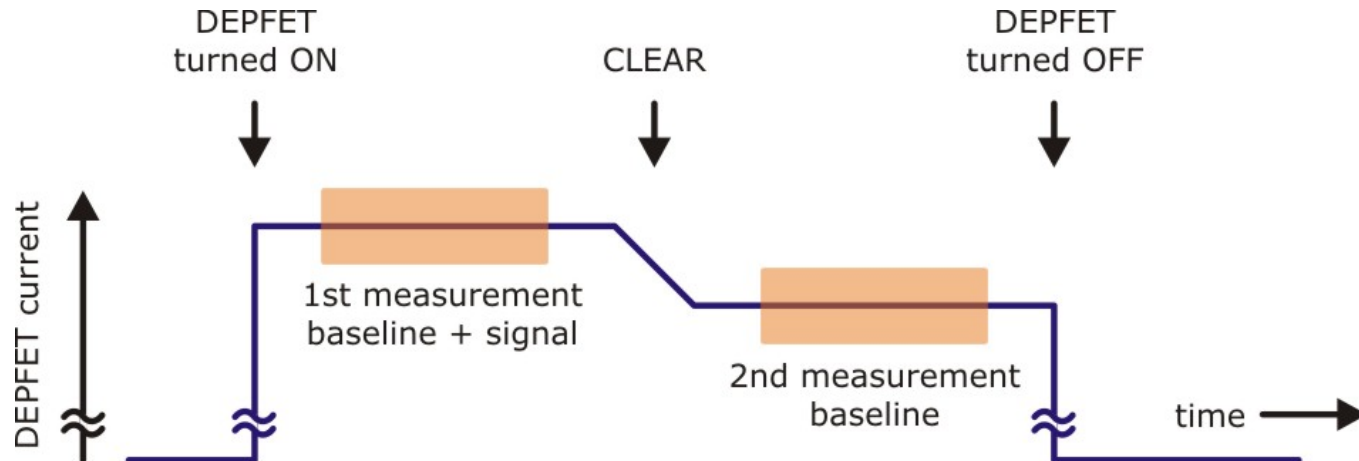
Introduction of additional gate electrodes to implement more functionality into one DEPFET (super-)pixels



# DEPFET

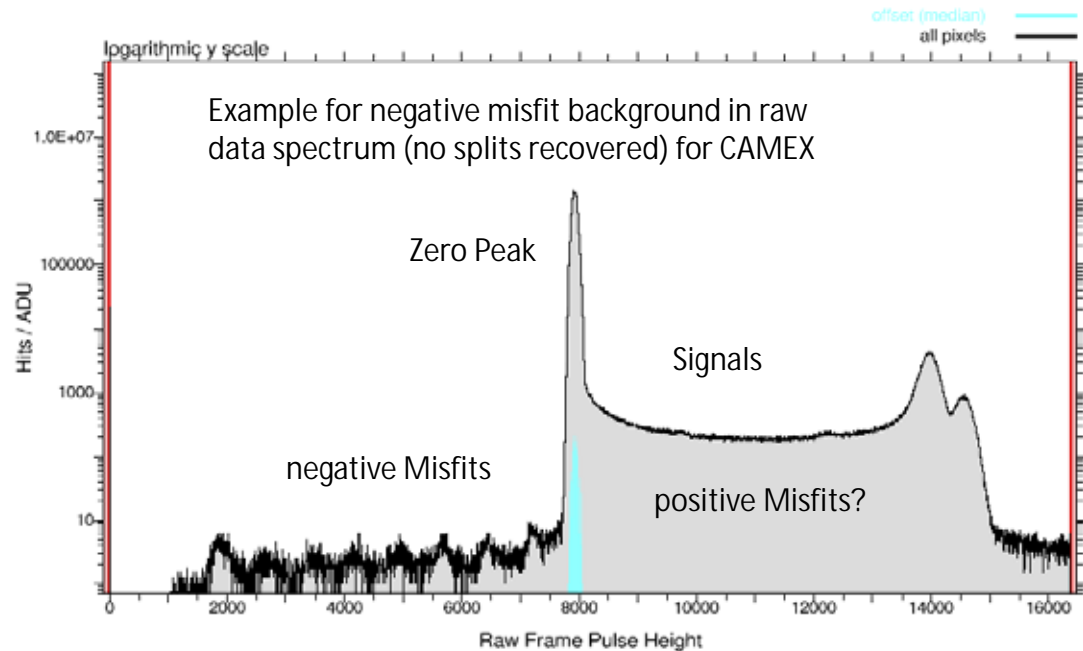


# Problem I: Misfits

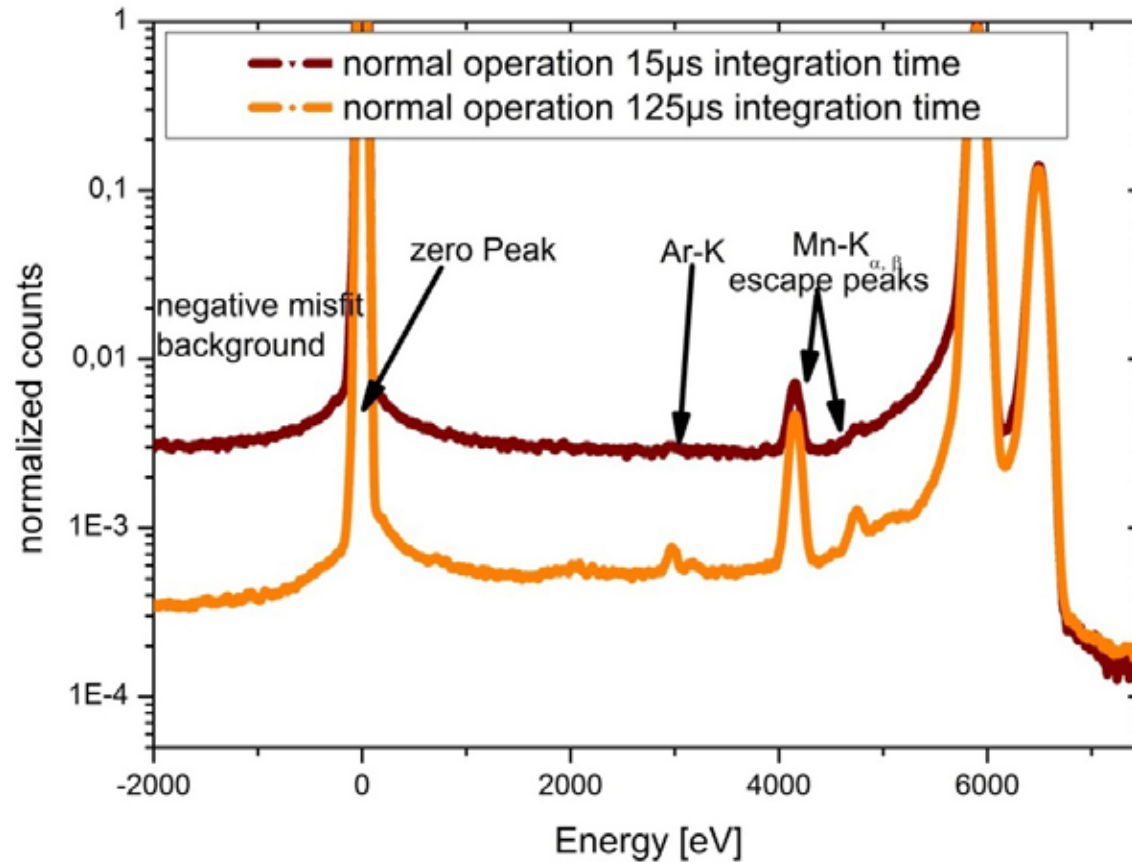


## Measurement of signal:

- Measure signal levels
- Measure „mean values“ both before and after clear
- Calculate the difference of mean values = „Charge Signal“
- Hit during integration phase distorts signal



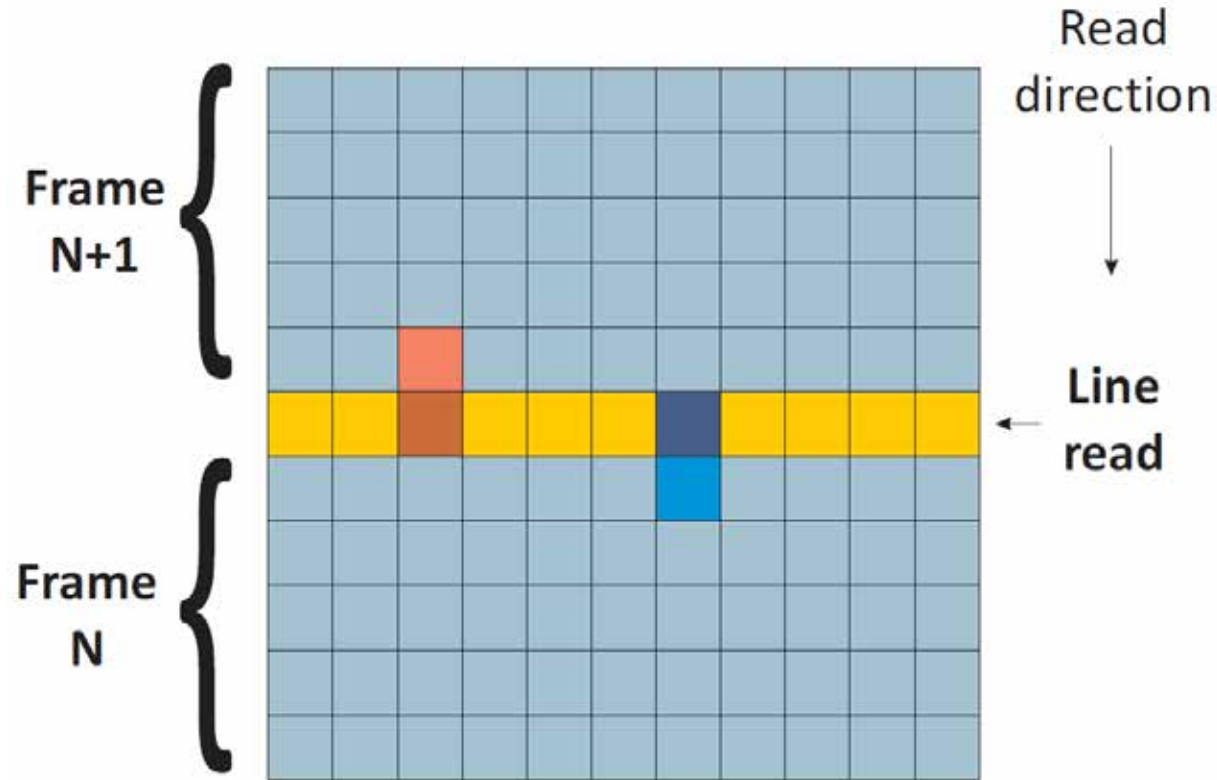
# Problem I: Misfits



## Signal processing of 4.2µs:

- P/B=280, FWHM=129eV @15µs signal integration
- P/B=1600, FWHM=133eV @125µs signal integration

# Problem II: Broken patterns



- Broken patterns due to rolling shutter effect
- "Lost" split partners / allocated to different frames
- Red case: Positive misfit causes broken pattern
- Blue case: Negative misfit causes broken pattern



# Multigate DEPFET

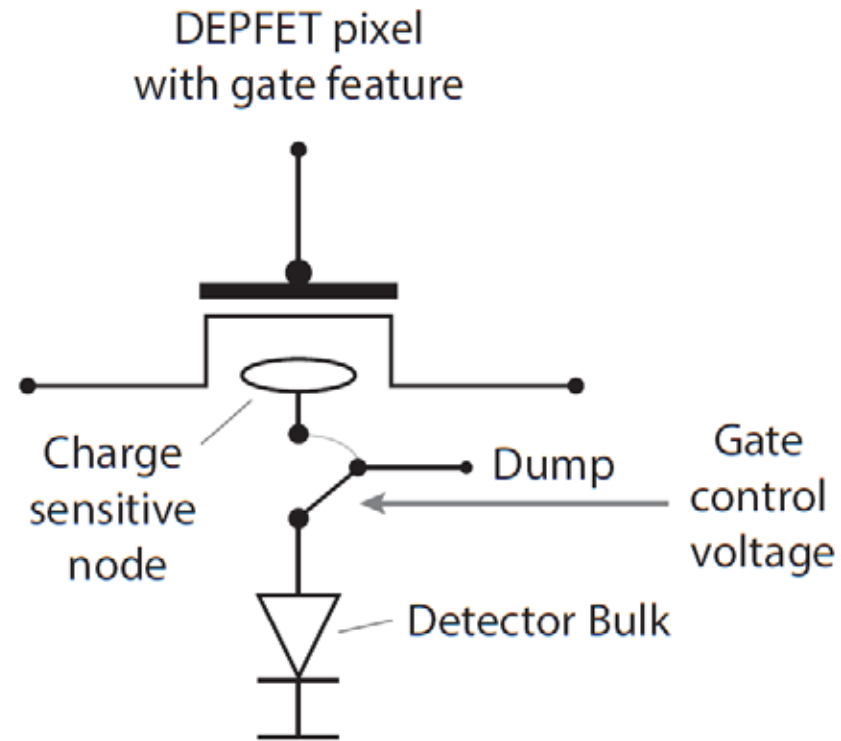
Turn off sensitivity of DEPFET  
during readout

Dump unwanted bulk generated  
charge to dedicated electrode

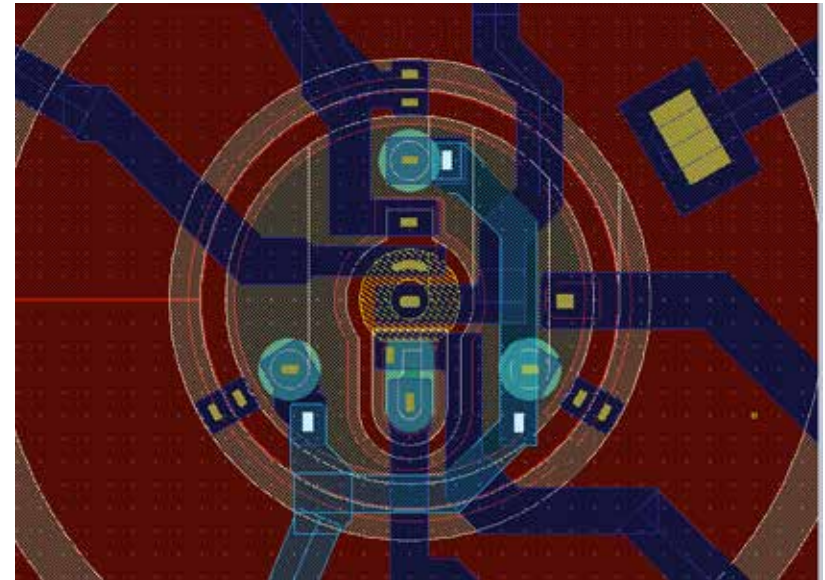
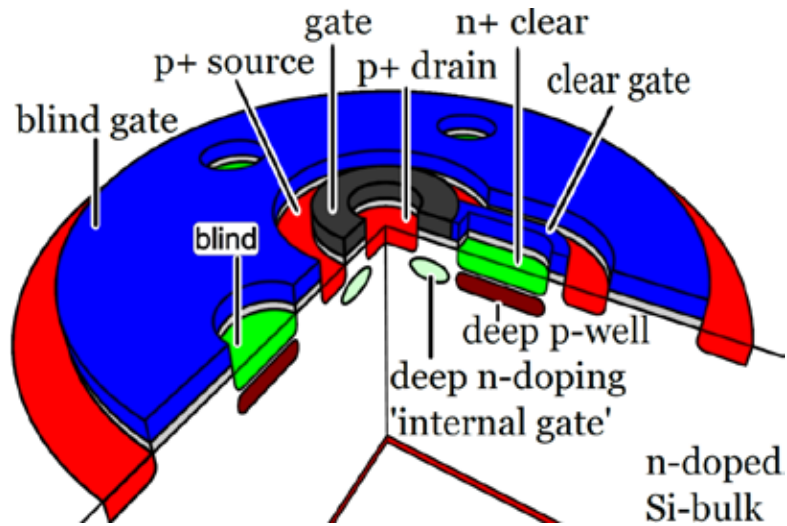


"Global shutter" functionality  
with precise timing

# GPIX device

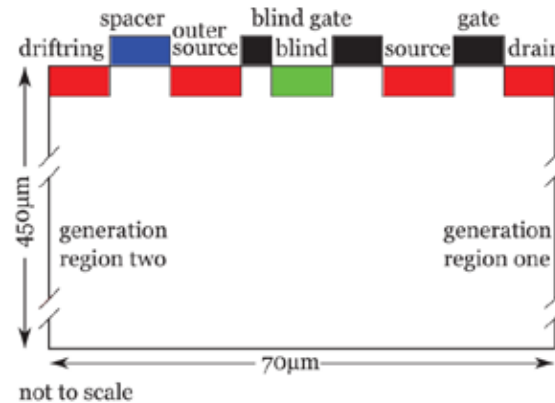


# GPIX



- Critical parameters:
  - Charge retention (similar to CHC)
  - Charge suppression  $> 5 \times 10^{-4}$
  - Shutter speed  $< 100$  ns

# Simulations

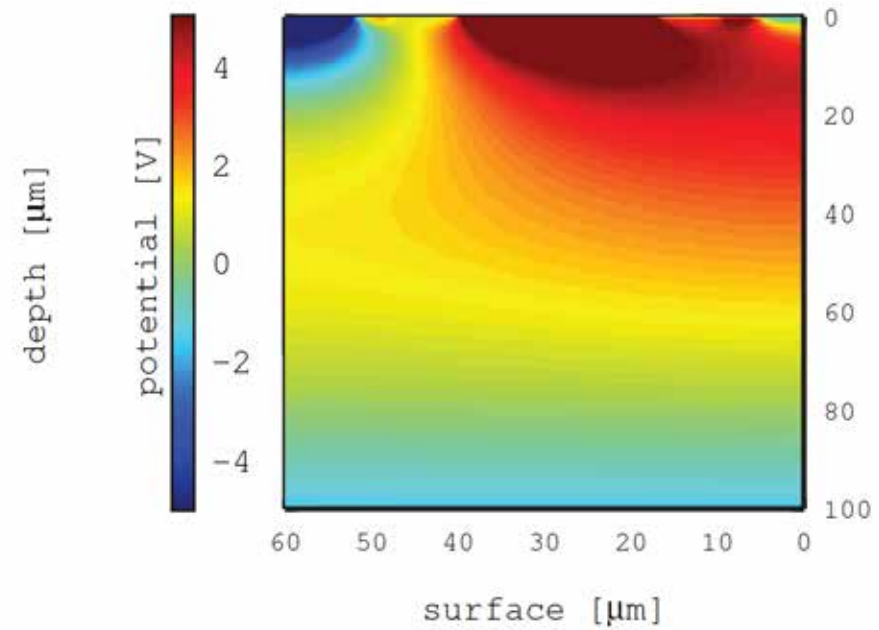
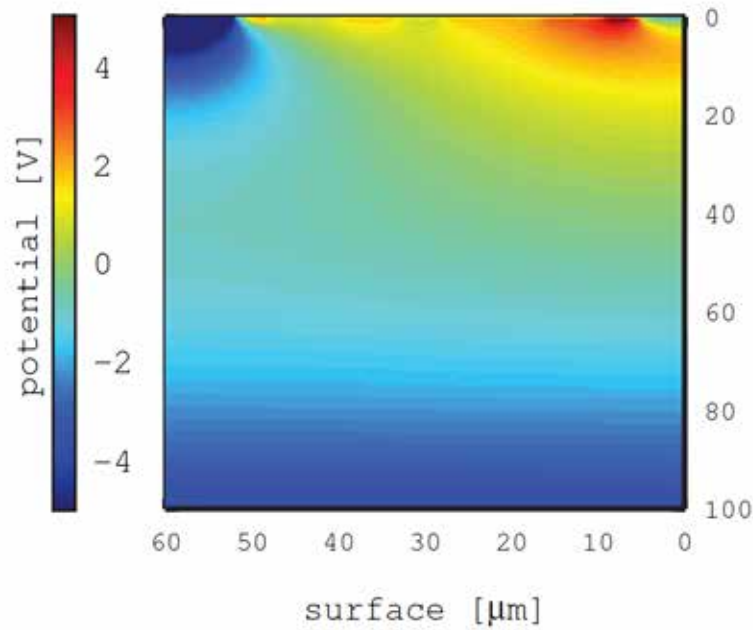


## Collection mode:

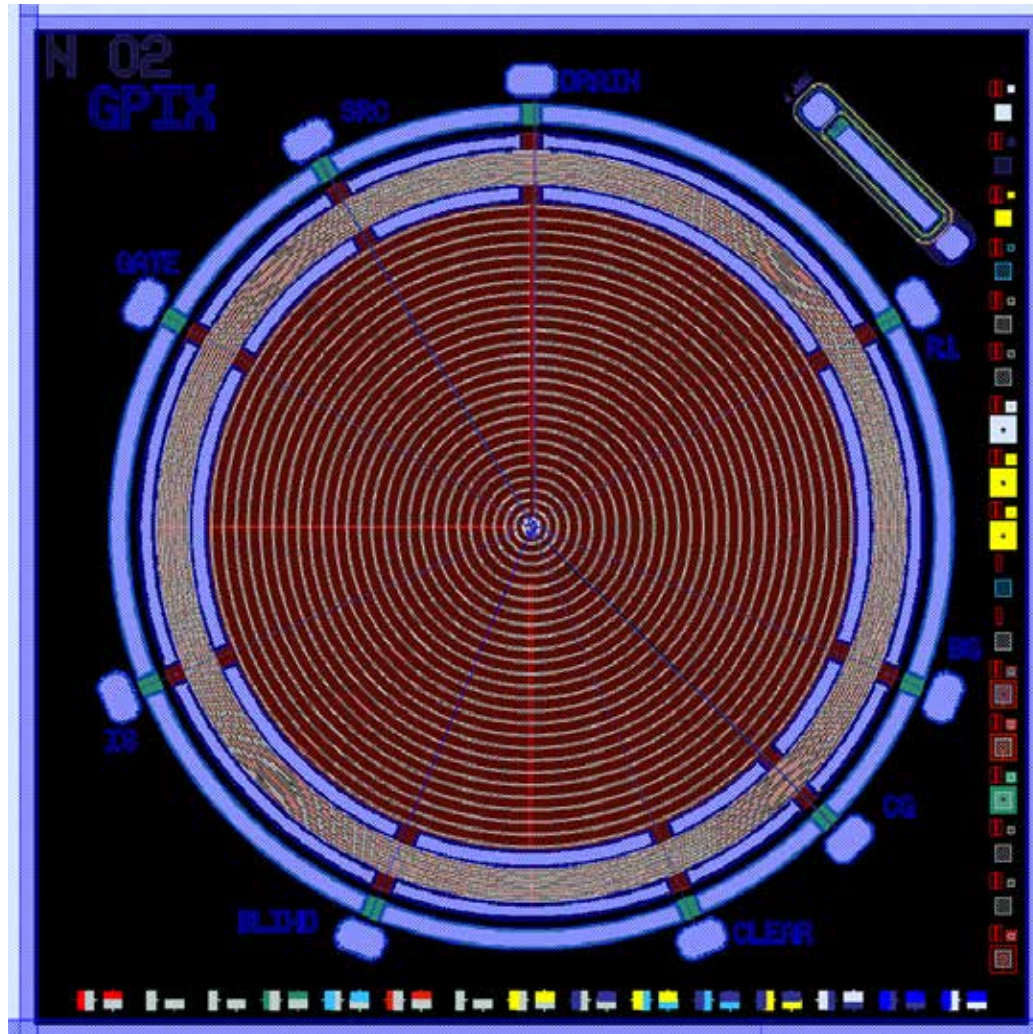
- Blind and blindgate low

## Blinded mode:

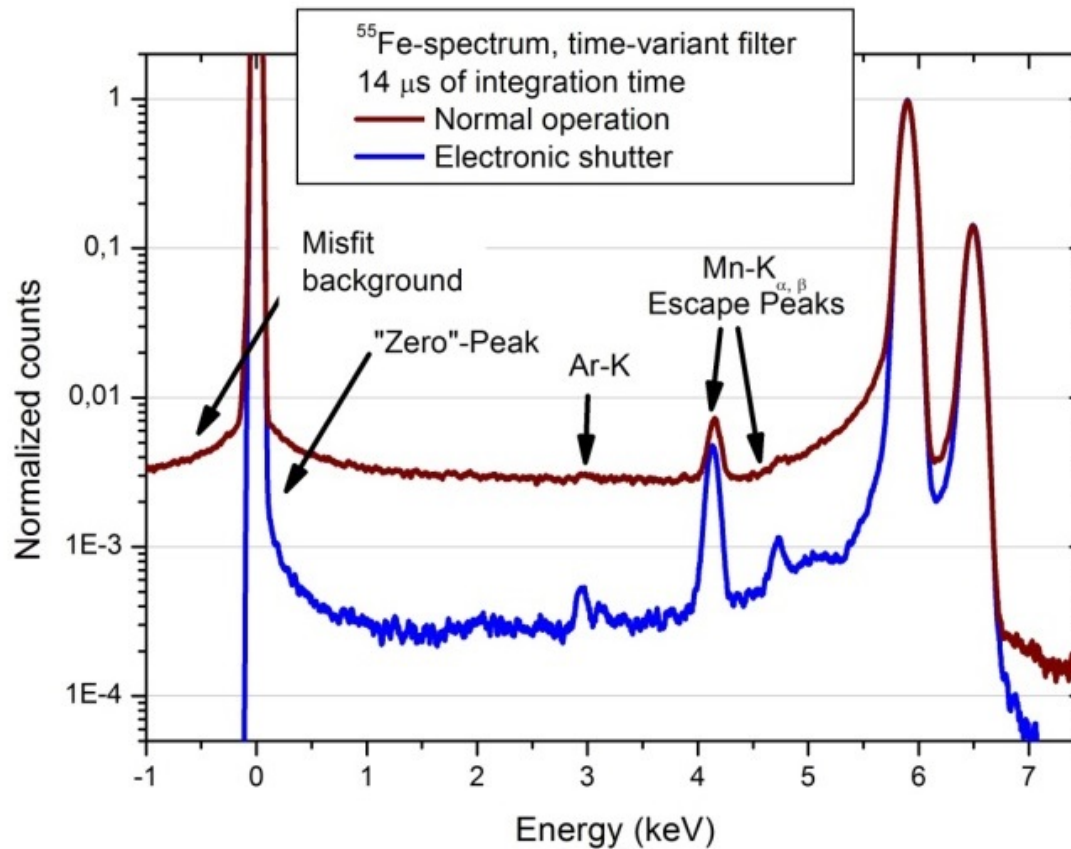
- Blind and blindgate high



# Prototype device



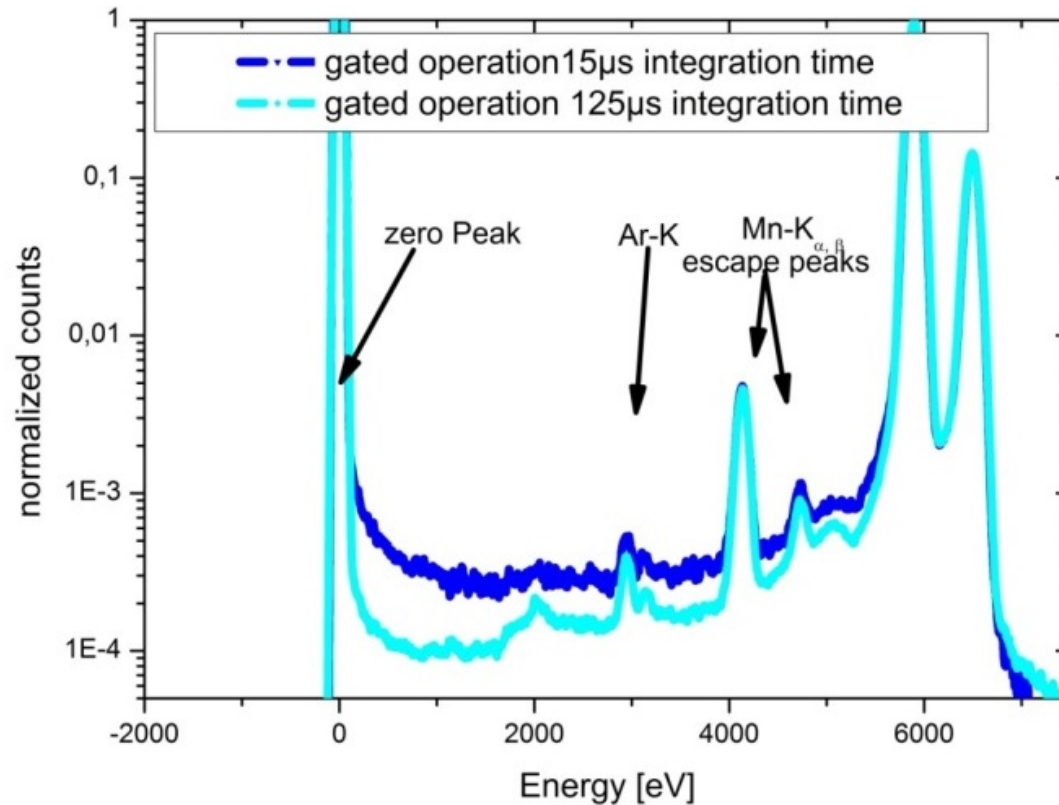
# Results



## Signal processing of 4.2 $\mu$ s:

- P/B=280, FWHM=129eV @15 $\mu$ s signal integration
- P/B=3100, FWHM=129eV @125 $\mu$ s signal integration

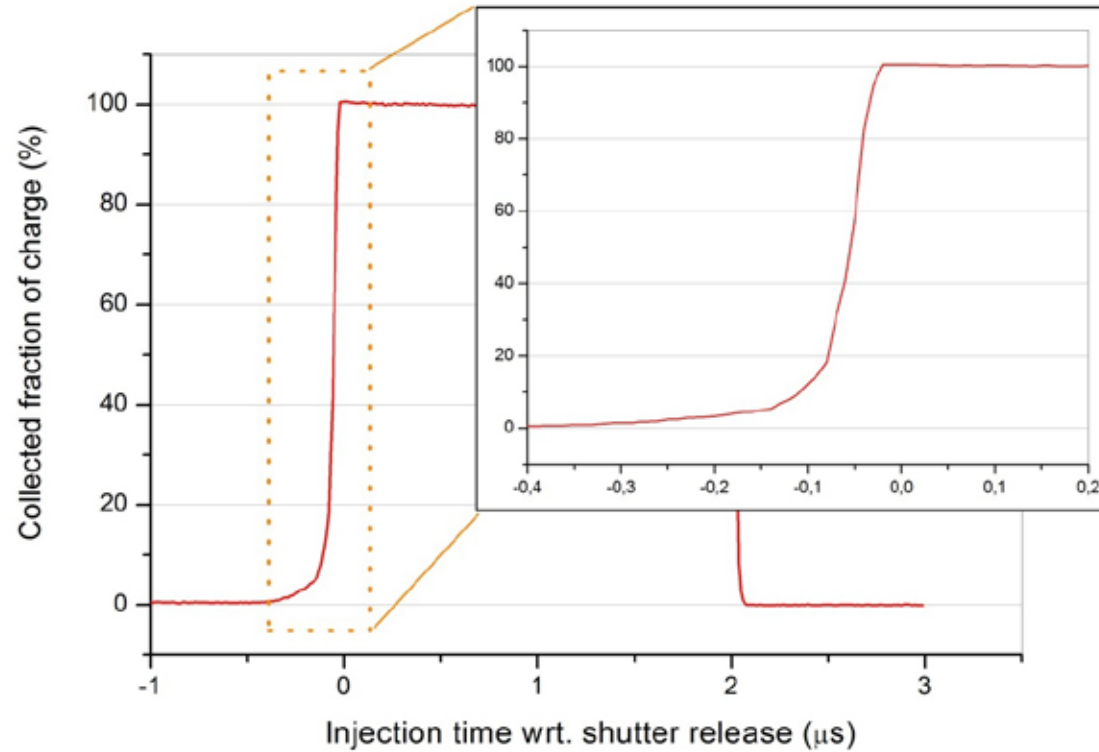
# Results



## Signal processing of 4.2µs:

- P/B=3100, FWHM=129eV @15µs signal integration
- P/B=1100, FWHM=133eV @125µs signal integration

# Results



## Timing:

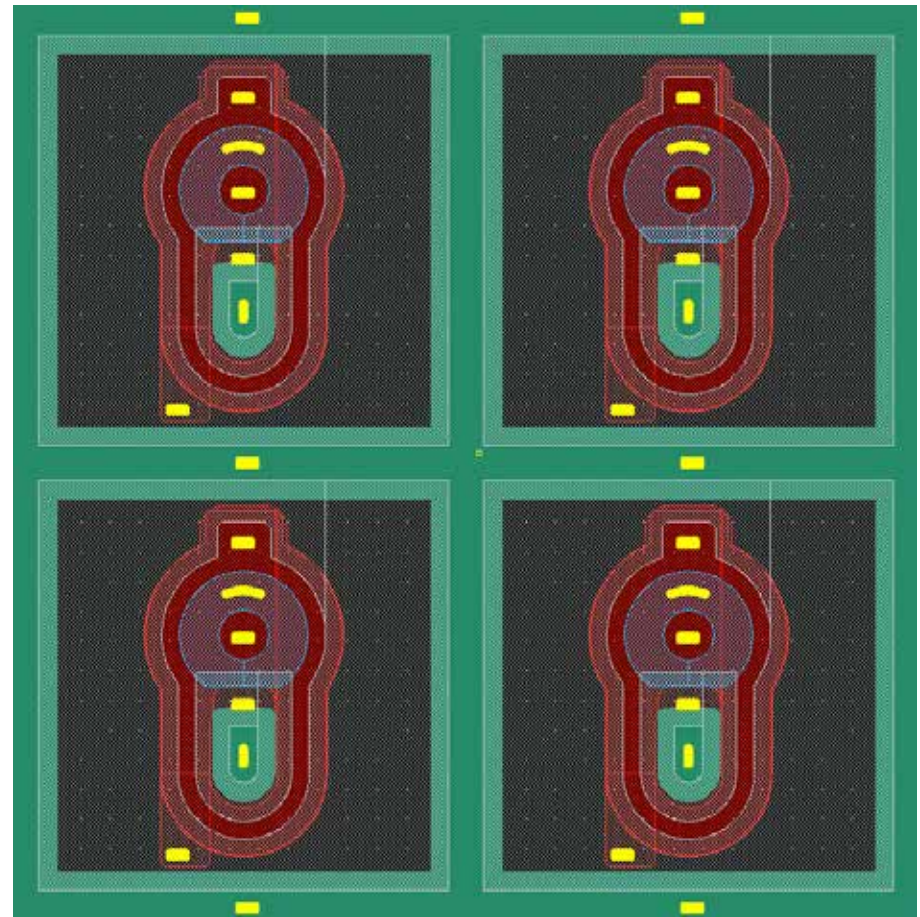
- Rise time 10% - 90 % < 100 ns



# Matrix device

## Prototype matrix:

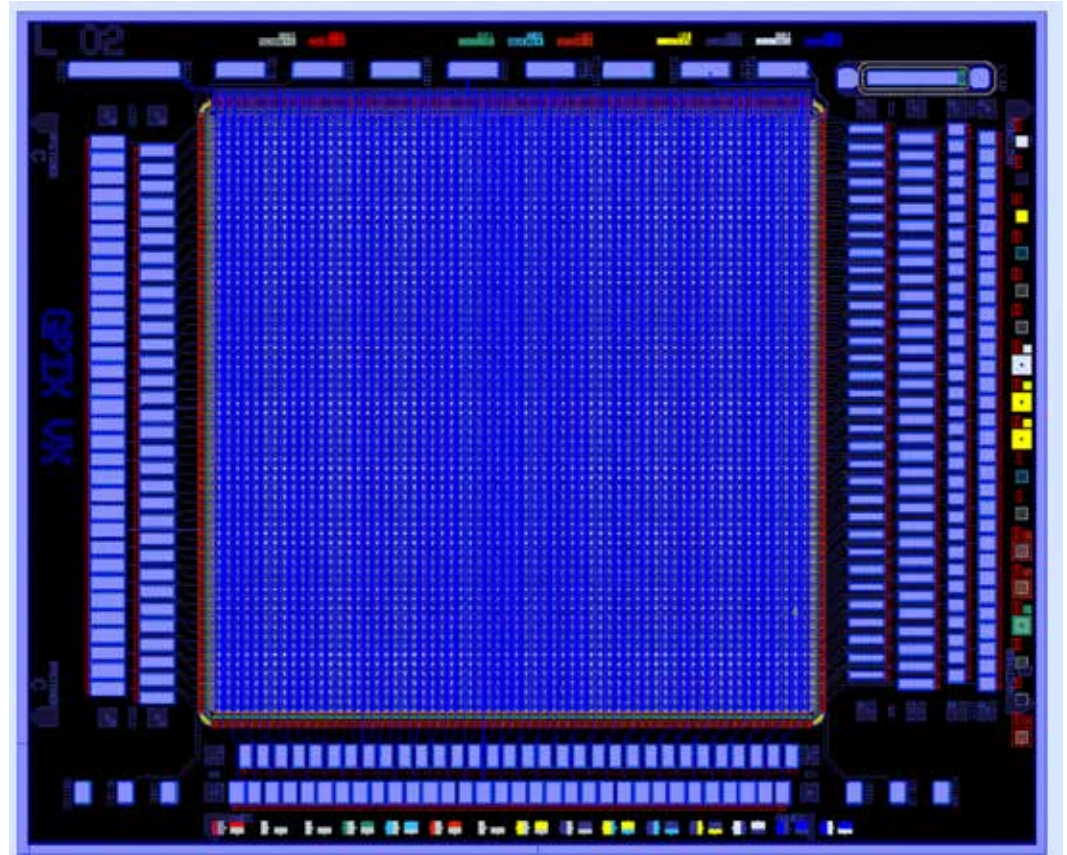
- Global shutter:
  - Global Blind
  - Global Blindgate
- Blind and collection mode can alternate with arbitrary timing
- Matrix can be read during blind mode
- Source follower readout
- Normal "rolling shutter" r/o
- No misfit or broken pattern issues
- Source width issue



# Matrix device

## Prototype matrix devices:

- 64 x 64 pixels
- 75 x 75  $\mu\text{m}^2$  size
- Sensitive area: 4.8 x 4.8  $\text{mm}^2$
- Backside illuminated
- "Optical" entrance window
- Chip size: 8.5 x 7  $\text{mm}^2$
- PXD 7 technology (spectroscopy grade)
- Available for evaluation!



# Problem: Dead time



# Multigate DEPFET

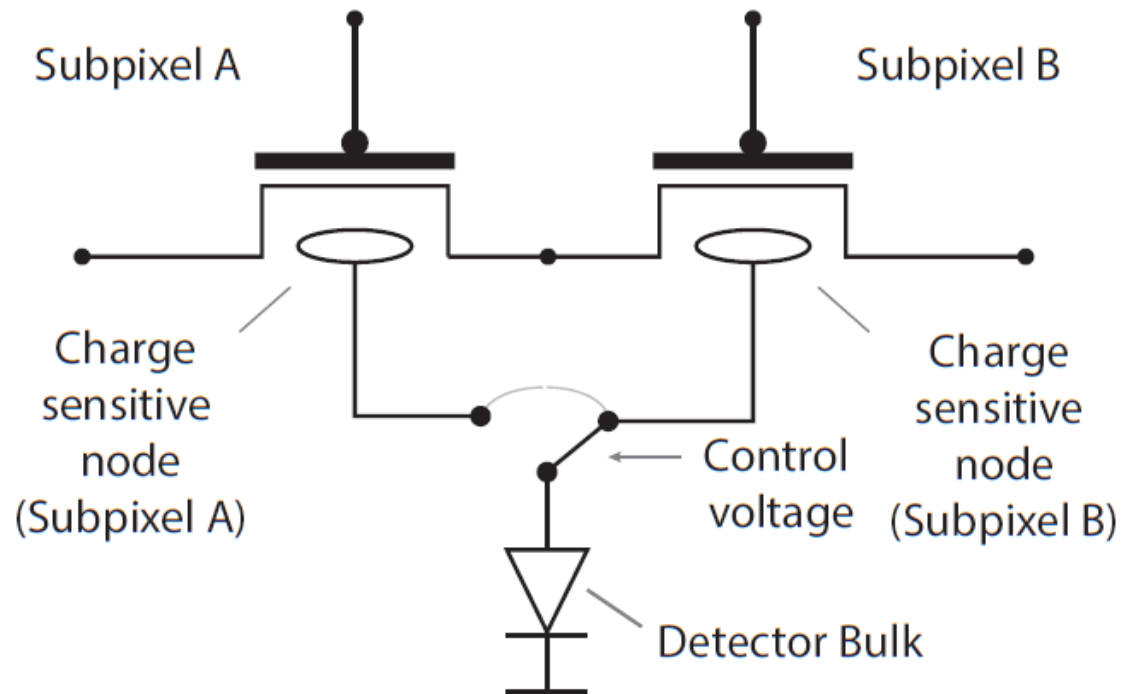
Turn off sensitivity of DEPFET  
during readout

Do not dump charge, but deviate  
charge to neighboring pixel

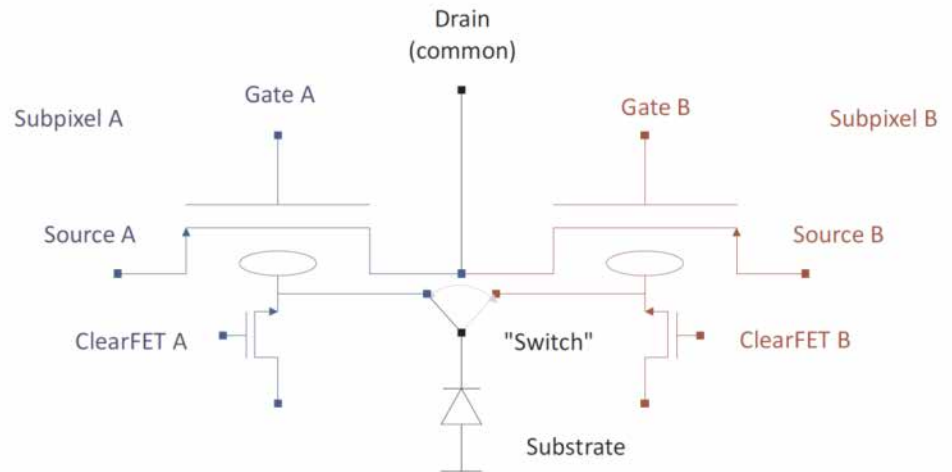
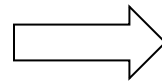
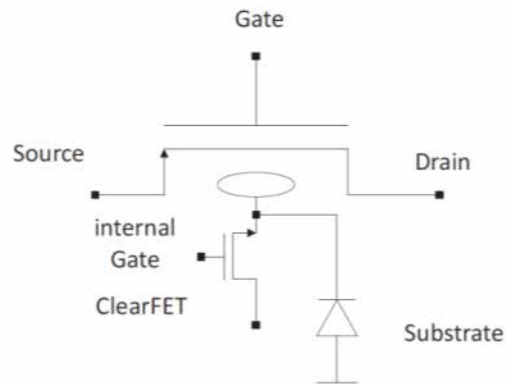


# Infinipix

Deadtimeless DEPFET Infinipix  
Superpixel with two subpixels

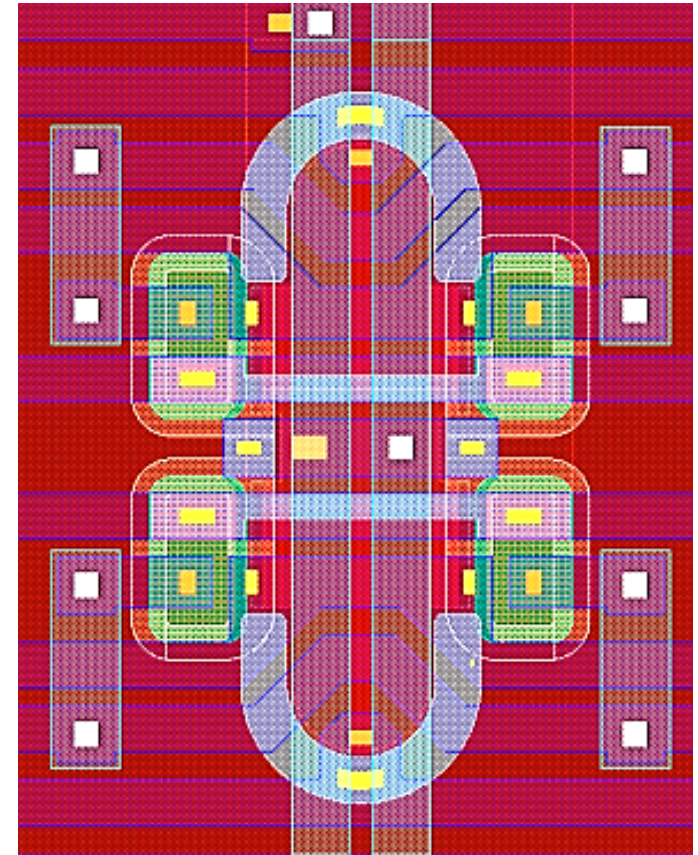
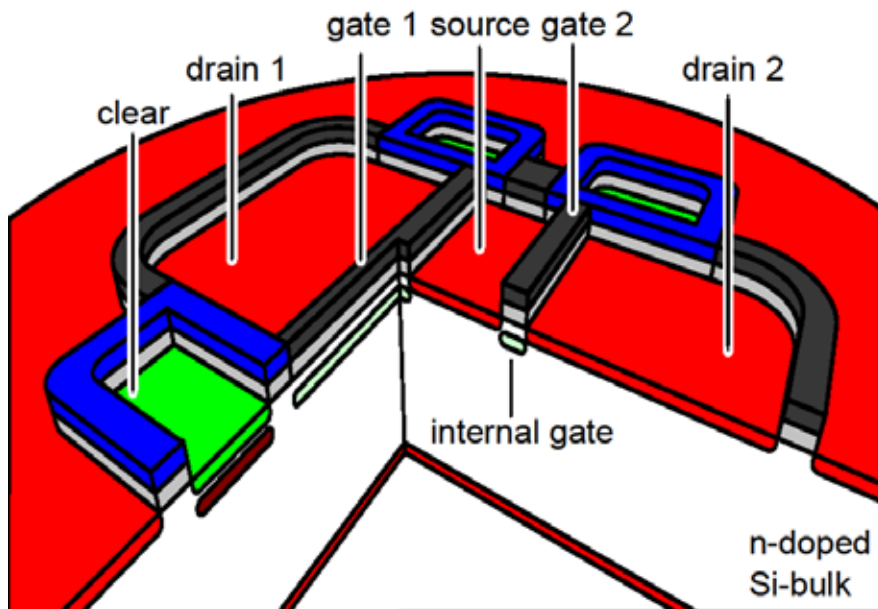


# Infinipix



- Superpixel consist of two subpixels
- Charge is deviated to one of the subpixels by using the drain potential
- Only insensitive pixel can be read out
- Strong suppression of MISFIT induced background
- Elimination of broken pattern background due to Rolling Shutter effect
- Benefit larger in case of fast timing
- Optimum case corresponds to **fully parallel readout**

# Infinipix

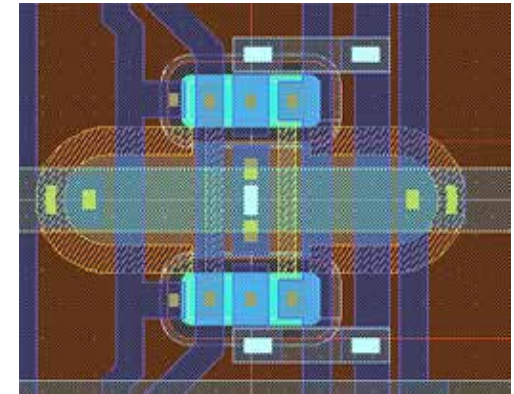


- Critical parameters:
  - Charge retention (similar to CHC)
  - Charge selectivity  $> 5 \times 10^{-4}$
  - Switch speed  $< 100$  ns

# Infinipix

## Matrix operation:

- Interconnection generates two independent subframes
- Interleaved storage of images in alternating subframes
- Charge integration in "sensitive" subframe
- Readout of insensitive subframe
- Only insensitive subframe can be read out



$$\lim_{n \rightarrow \infty} a_n = \infty$$

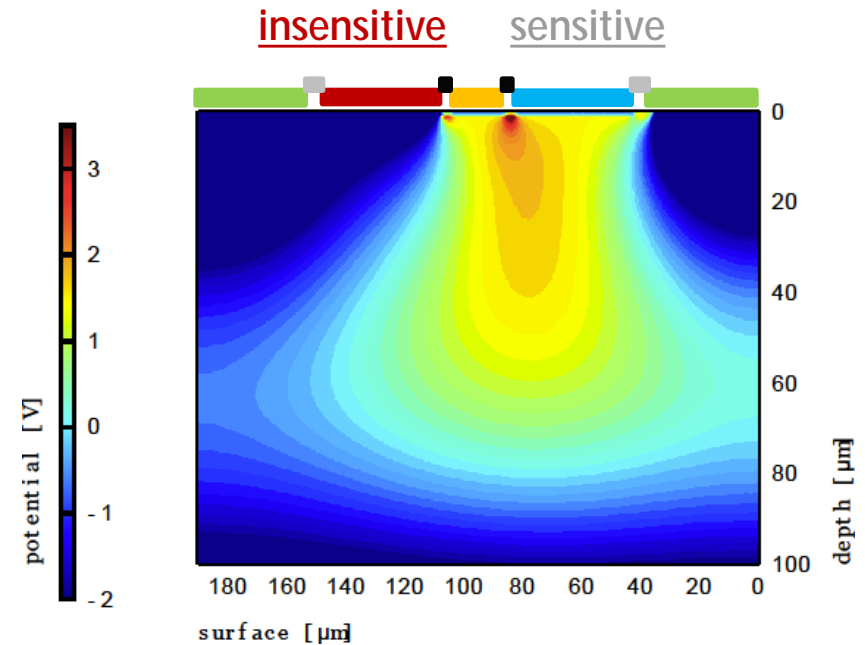
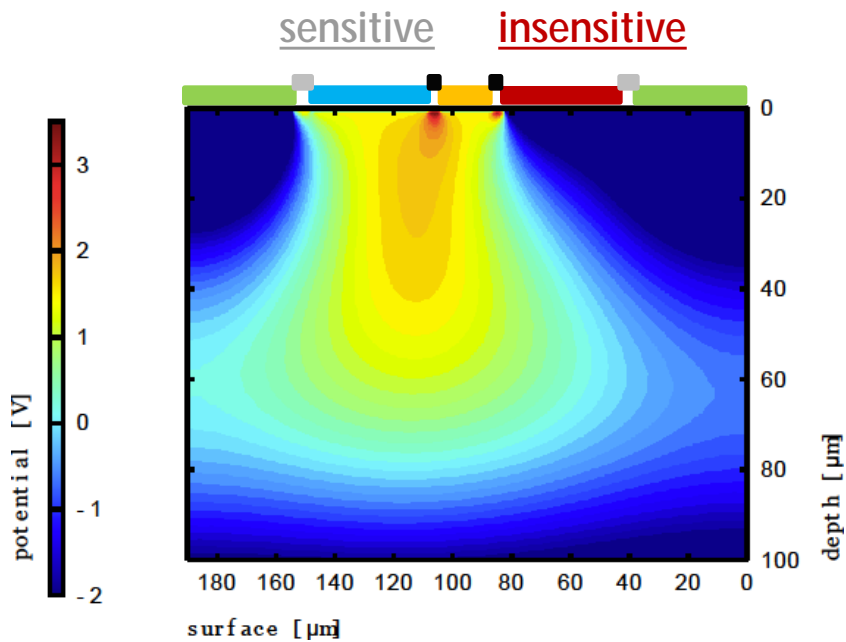
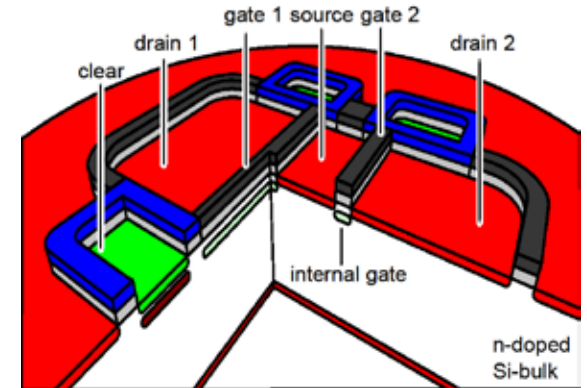
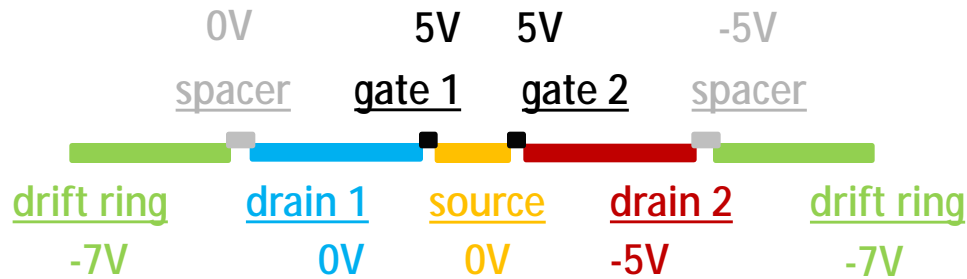
## The working title "InfiniPix" was chosen because

- Infinipix design resembles 'infinity' symbol and Moebius strip

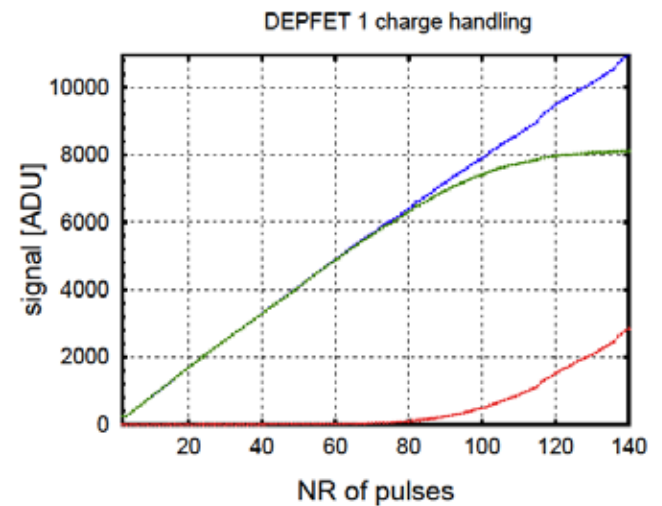
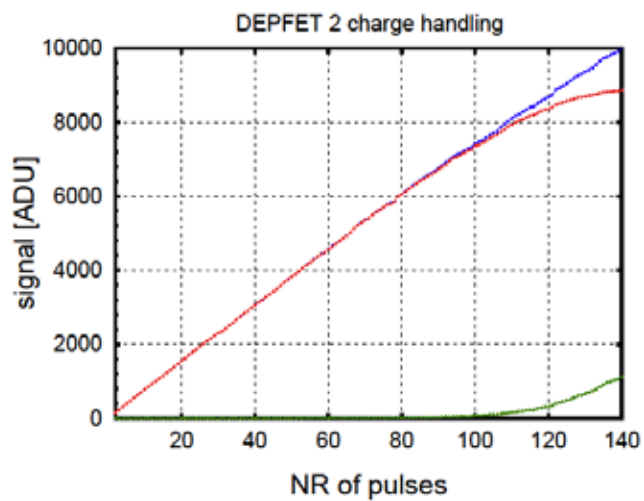
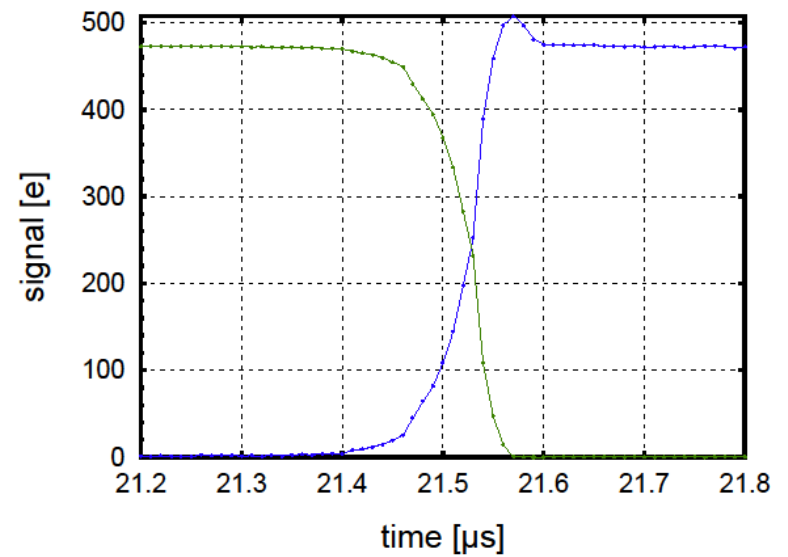
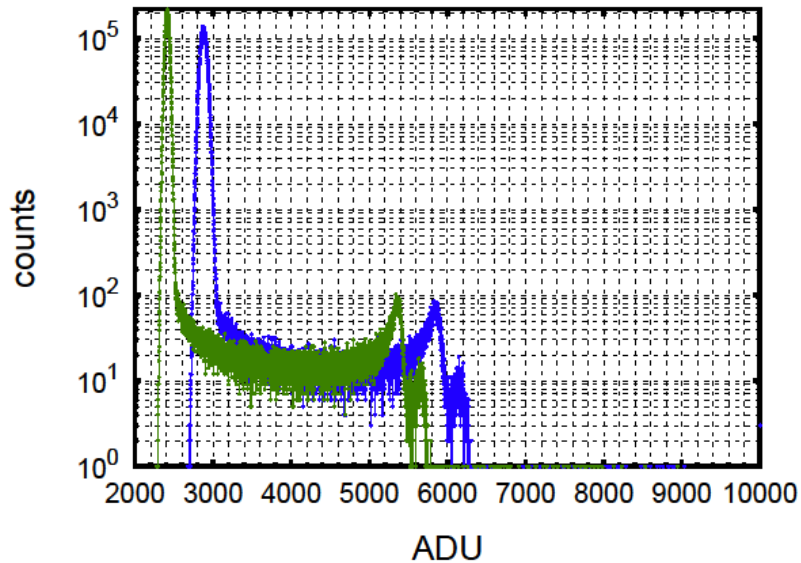




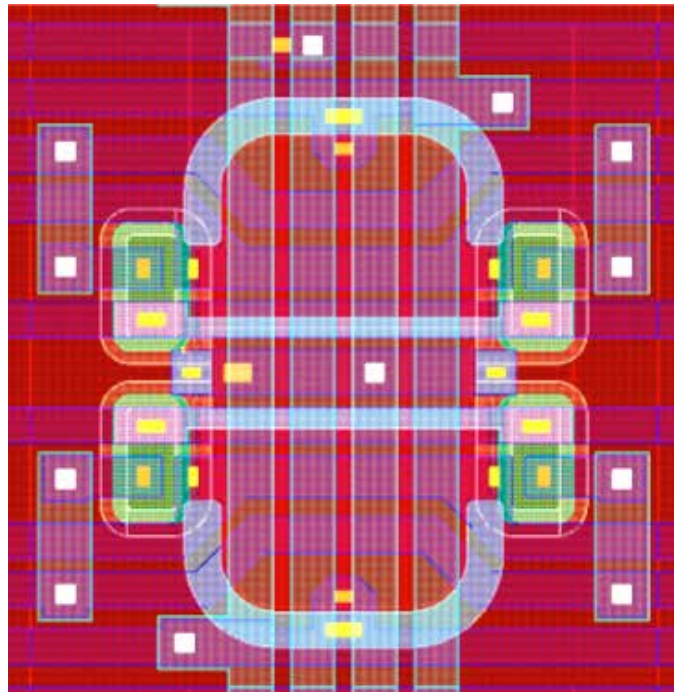
# Simulations



# Measurements

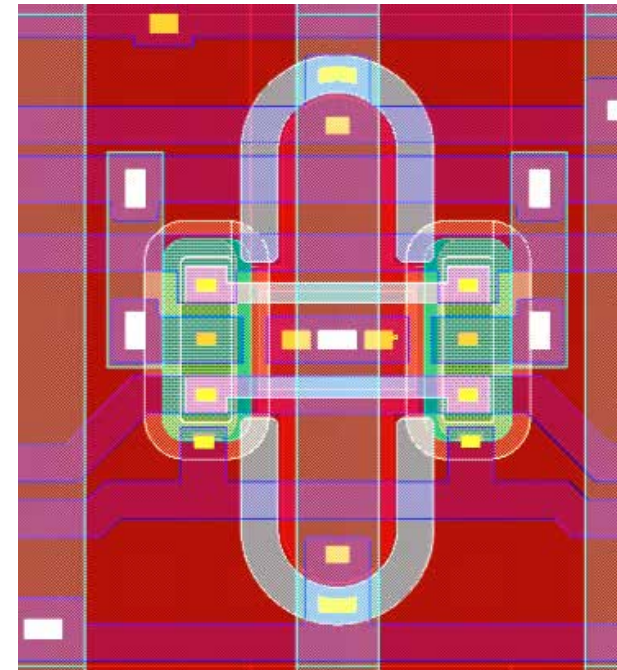


# Matrix devices



## Infinipix 5 large:

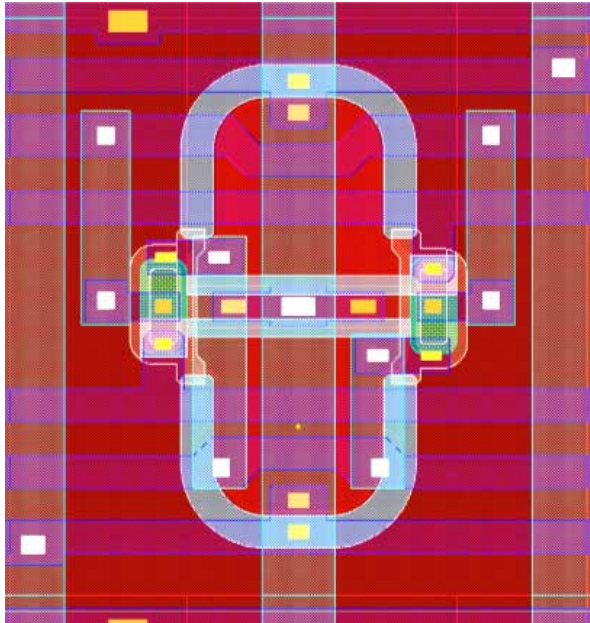
- Dual Clear
- $L(\text{Source}) = 16 \text{ mm}$ ,  $L(\text{Drain}) = 42 \text{ mm}$ ,  
 $L(\text{gate}) = 4.5 \text{ mm}$
- $W = 30 \text{ mm}$  (Infinipix 5),  $W = 60 \text{ mm}$   
(Infinipix 5 large)



## Infinipix 6:

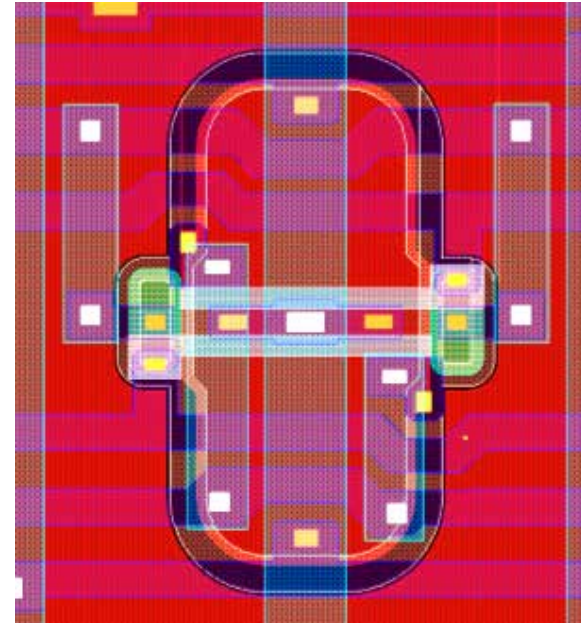
- Single Clear
- $L(\text{Source}) = 16 \text{ mm}$ ,  $L(\text{Drain}) = 42 \text{ mm}$ ,  
 $L(\text{gate}) = 4.5 \text{ mm}$
- $W = 30 \text{ mm}$

# Matrix devices



## Infineon 7:

- New design with optimized dimensions according to simulations
- Single Clear
- $L(\text{Source}) = 8 \text{ mm}$ ,  $L(\text{Drain}) = 44 \text{ mm}$ ,  
 $L(\text{gate}) = 4.5 \text{ mm}$
- $W = 42 \text{ mm}$



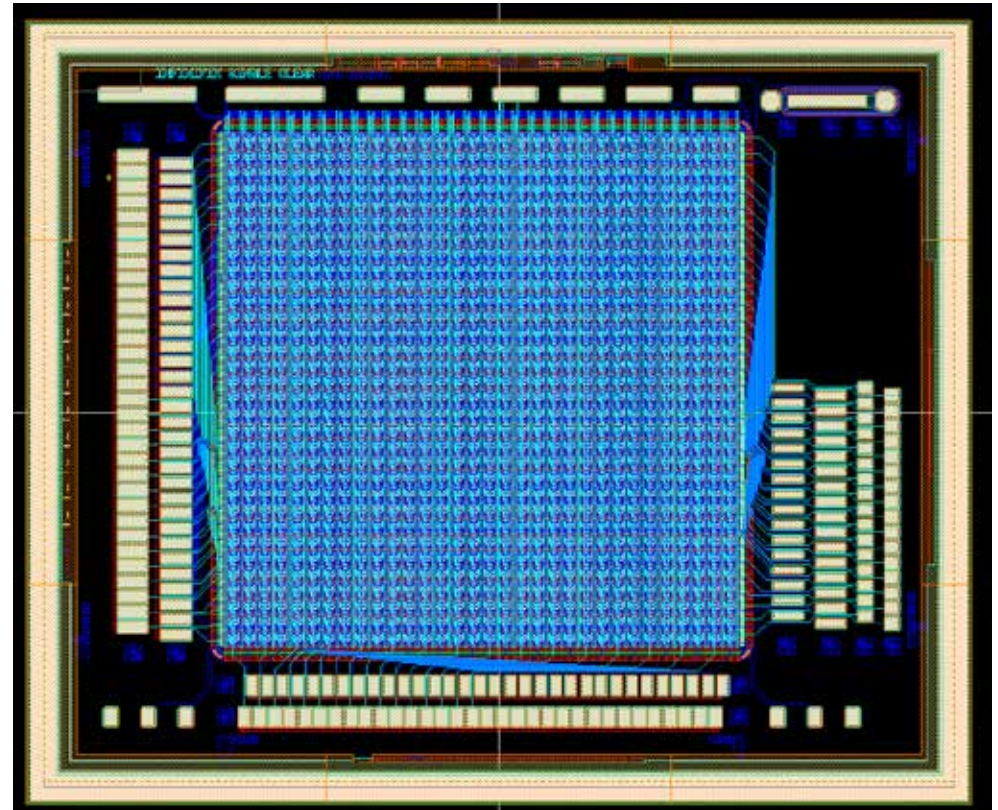
## Infineon Omega:

- New design with optimized dimensions according to simulations
- Single Clear / Cleagate separator
- $L(\text{Source}) = 8 \text{ mm}$ ,  $L(\text{Drain}) = 44 \text{ mm}$ ,  
 $L(\text{gate}) = 4.5 \text{ mm}$
- $W = 42 \text{ mm}$

# Matrix devices

## Prototype matrix:

- 32 x 32 pixels
- 150 x 150 mm<sup>2</sup> size
- Sensitive area: 4.8 x 4.8 mm<sup>2</sup>
- Backside illuminated
- "Optical" entrance window
- Chip size: 8.5 x 7 mm<sup>2</sup>
- PXD 8 / PXD 11 technology (spectroscopy grade)
- PXD 8 devices under investigation
- PXD 11 devices in fabrication
- Soon: New production dedicated to Infinipix devices



# Idea

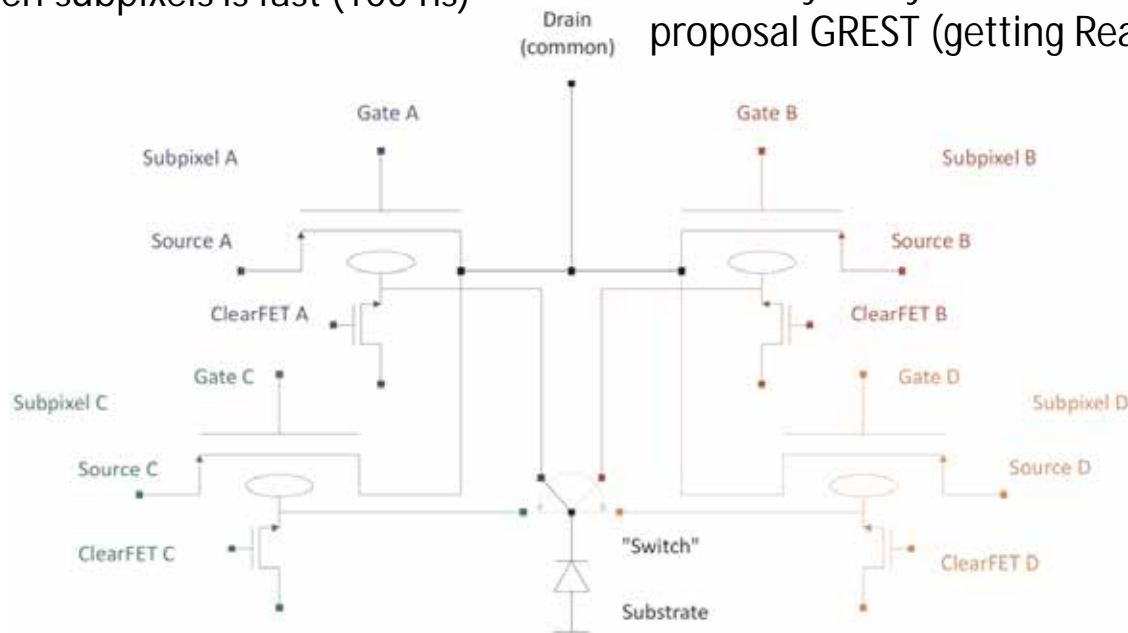
Why only two  
subframes?



# Infinipix Quad (IQ) structures

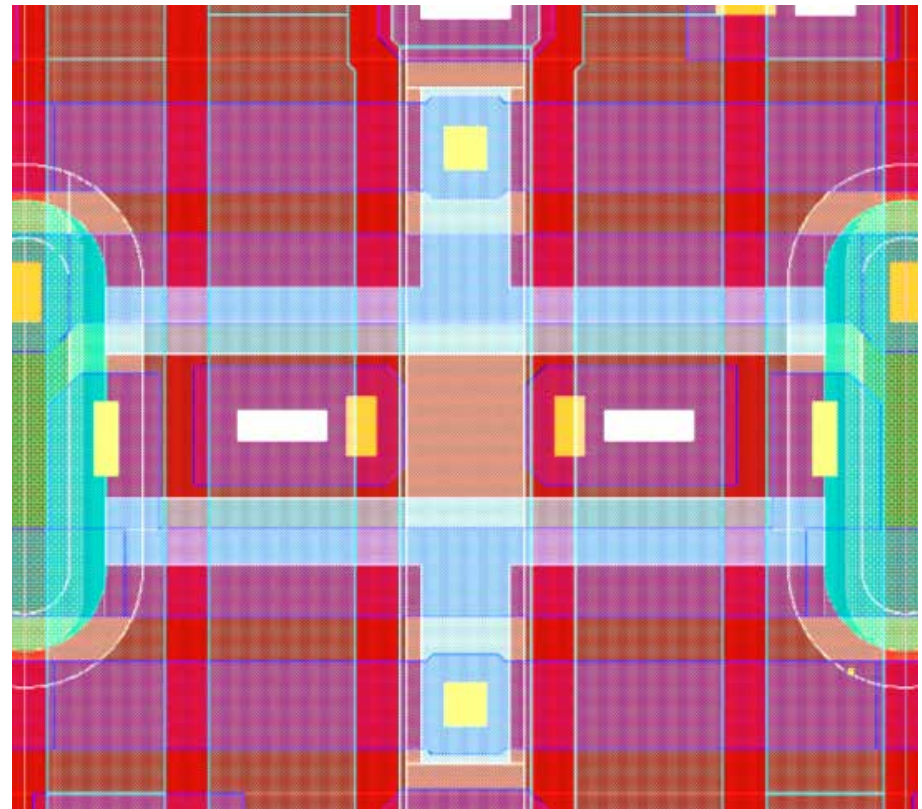
## Application driven:

- Infinipix subframe / subpixel counts higher than 2
- Infinipix superpixels with 4 subpixels suitable for future (solar) polarimeter (See talk by A. Feller)
- Integrated charge for one of four polarization states (Stokes vector components) is stored in one associated subpixel
- Switching between subpixels is fast (100 ns)
- Due to large charge handling capacitance, large numbers of images can be integrated
- Readout noise is accounted only once
- Very high duty cycle
- Very high modulation rate
- Very low noise
- Feasibility study within the scope of H2020 proposal GREST (getting Ready for EST)



# IQ Structures

- **Simplified structure:**
  - Common clear
  - Two gates instead of 4
  - Two sources
  - Source follower
  - Device can be sensitive with Gate off
  - Shutter speed < 100 ns
  
- **Critical parameters:**
  - Charge retention (similar to CHC)
  - Charge selectivity >  $5 \times 10^{-4}$  ?
  - Switch speed < 100 ns
  - **New: Spatial conformity!**

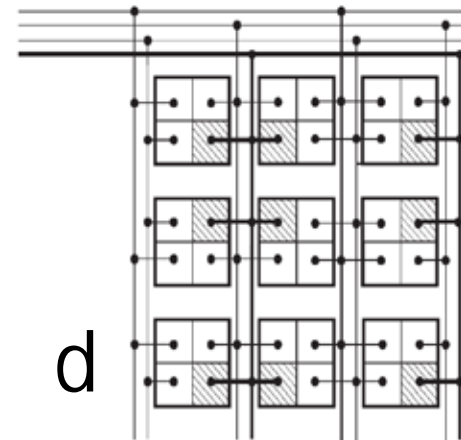
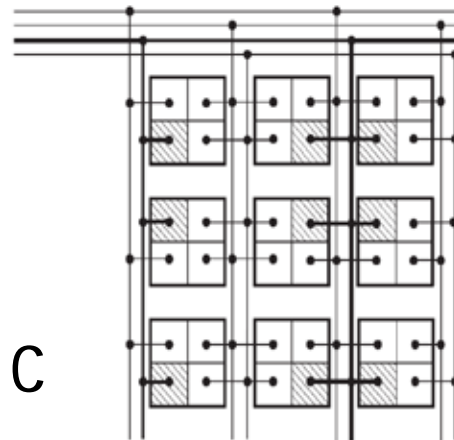
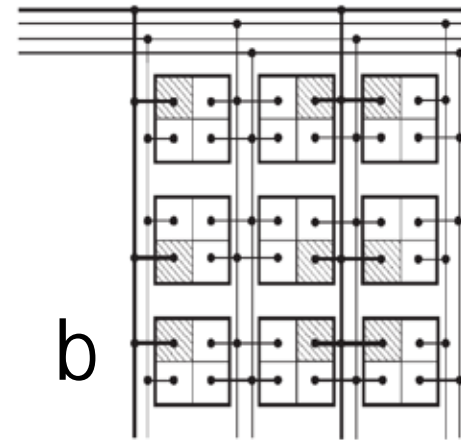
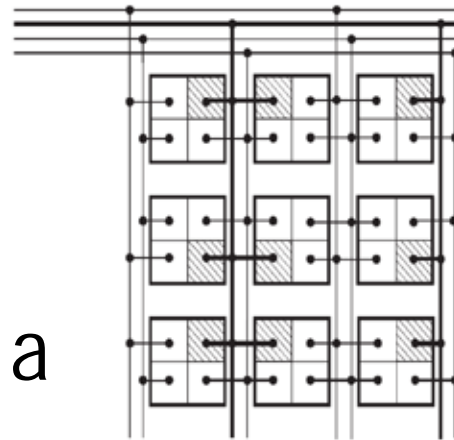


"Standard" IQ (Infinipix Quad) structure

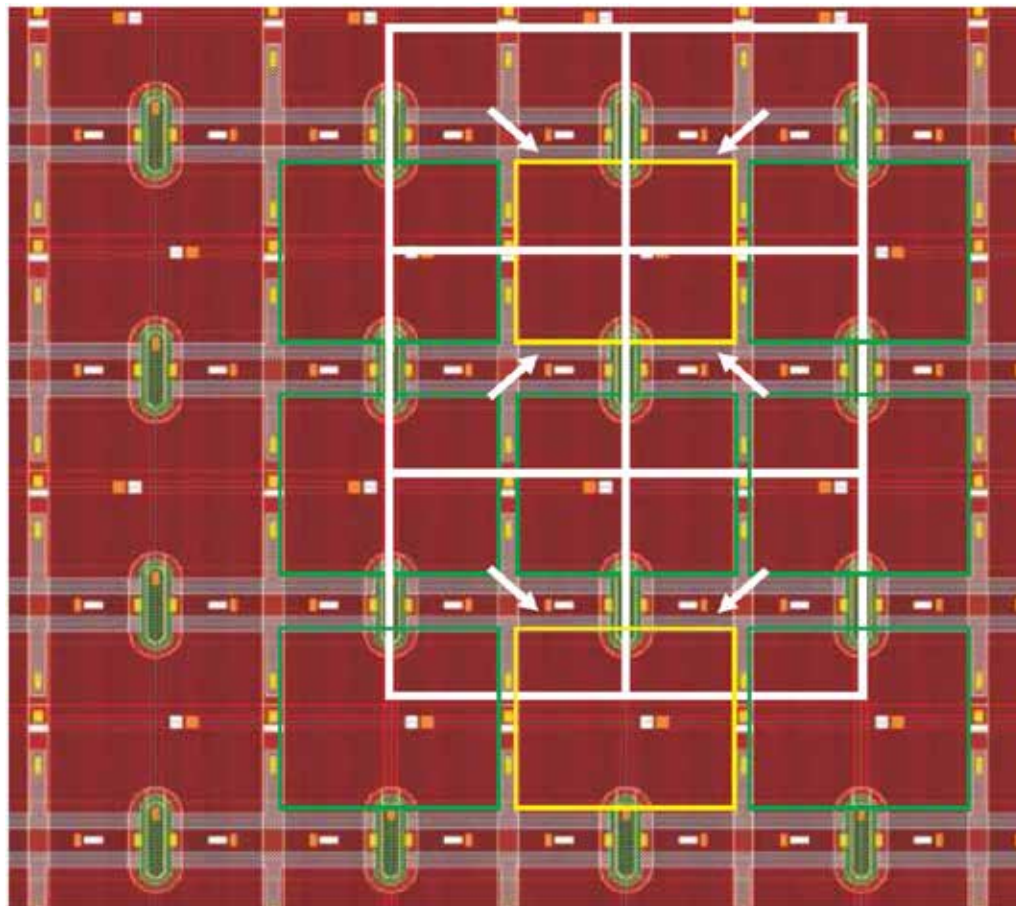


# Infinipix device

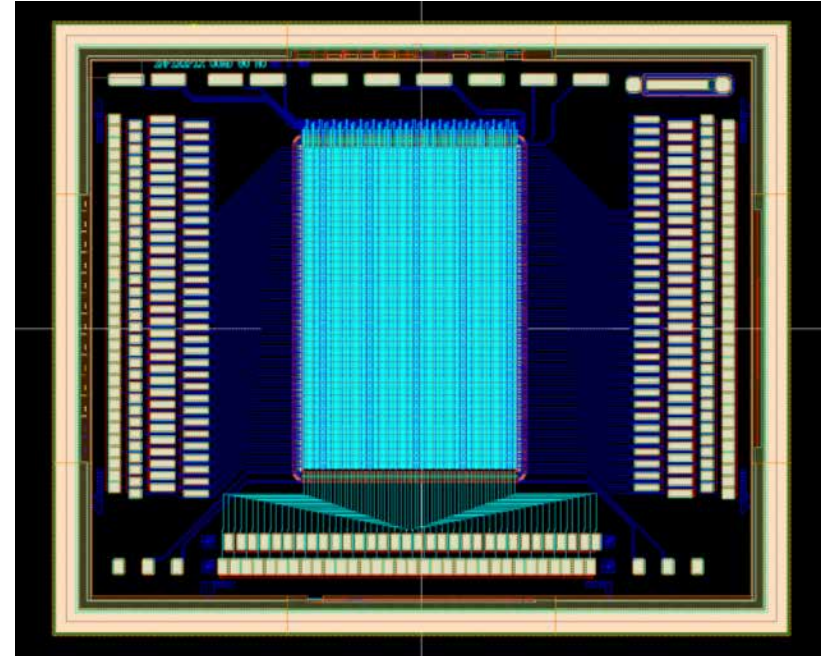
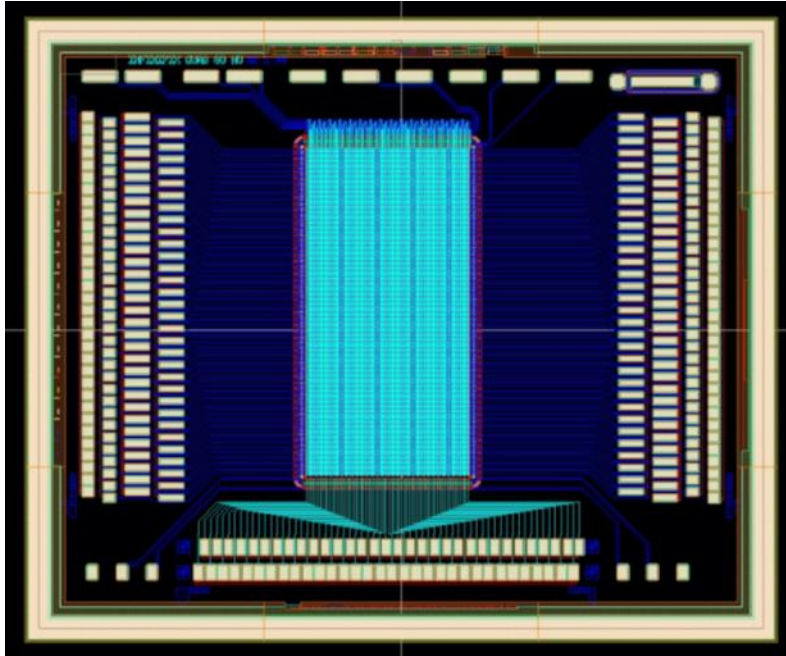
- Interlaced connection of subframes
- Contiguous large drain areas, area efficient approach
- Rotating sensitivity allows for sampling of 4 phases of polarimetry measurement
- Test layouts done and in fabrication



# Device layout



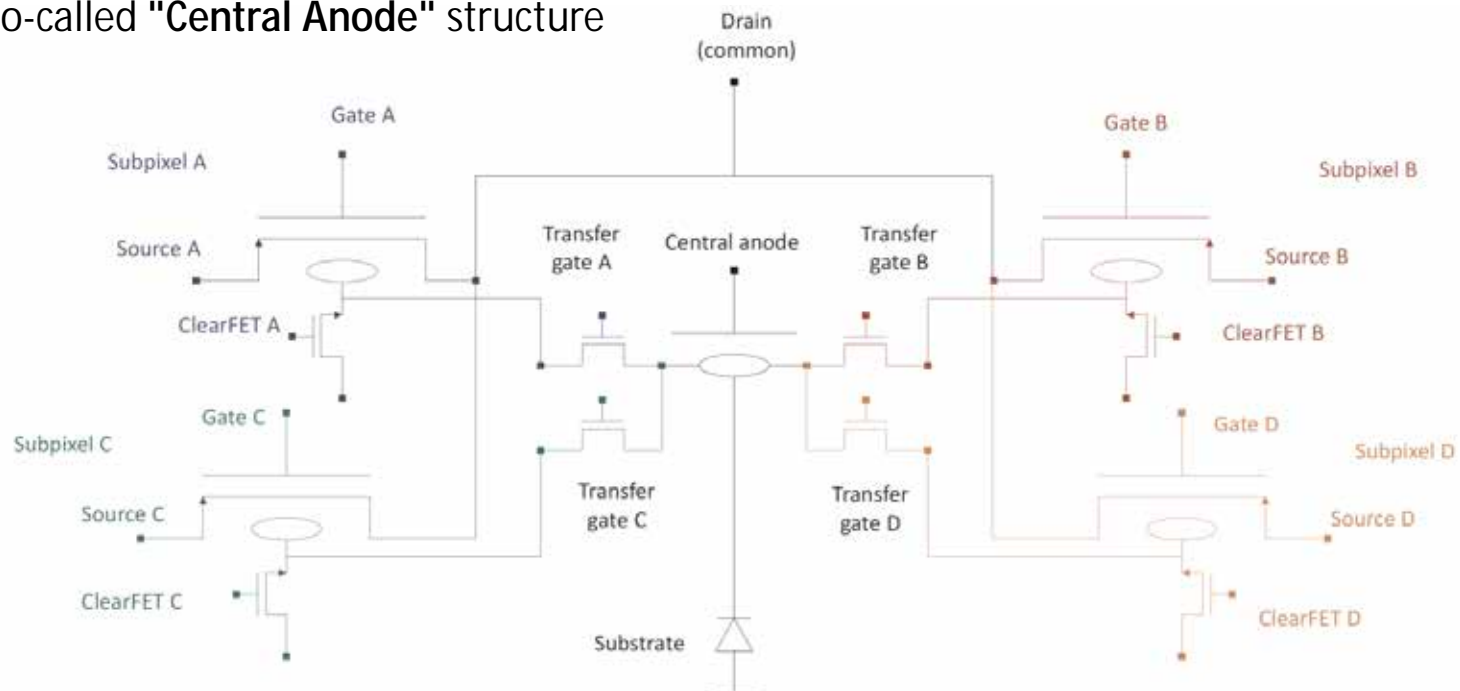
# IQ Structures



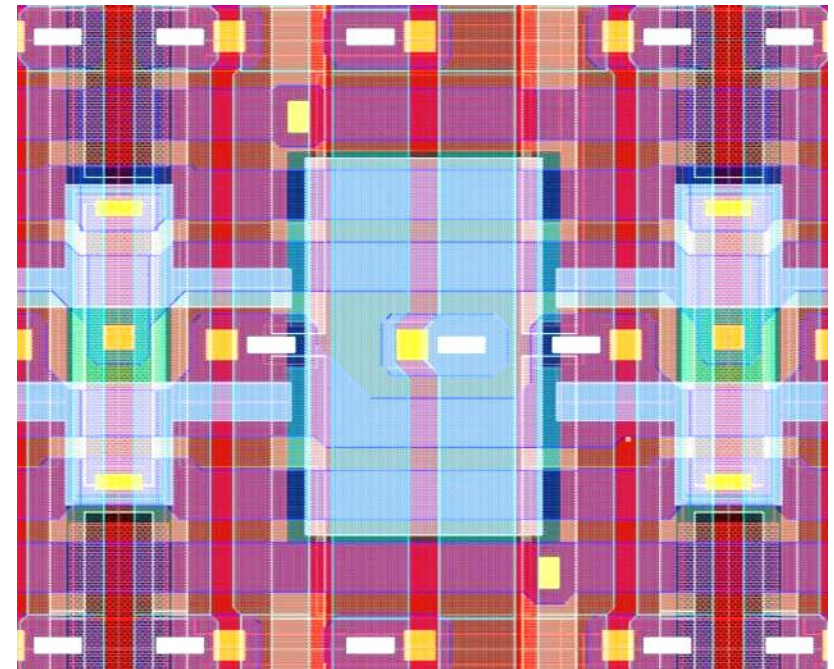
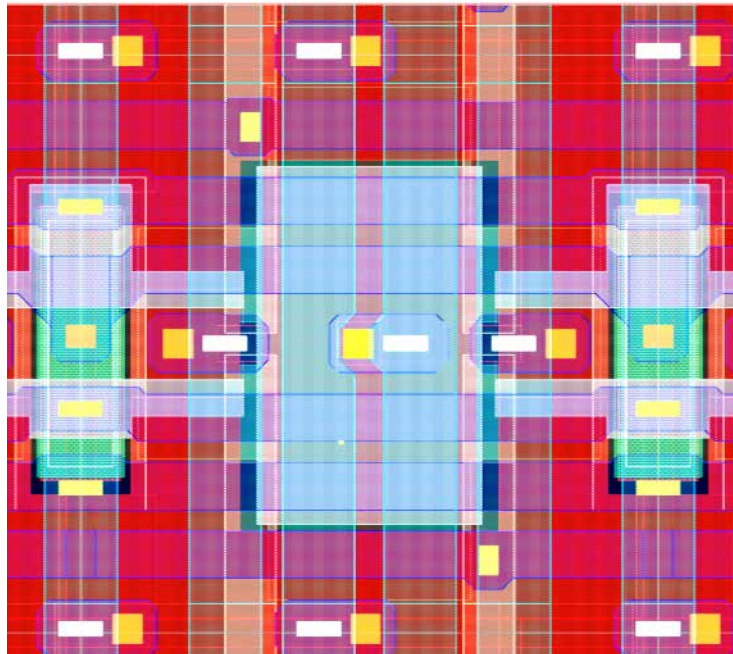
- 60 x 60 mm<sup>2</sup> and 80 x 80 mm<sup>2</sup> pixel prototypes
- Single clear
- Clocked Cleargate
- Source follower readout
- Prototype matrices of 32 x 64 ( 60 x 60 mm<sup>2</sup>) and 32 x 48 (80 x 80 mm<sup>2</sup>) pixels on standard matrix scaffold

# IQCA Structures

- In case very high polarimetric efficiencies are to be achieved, spatial shift of images due to the varying control potentials ("switch") could interfere with the measurements and affect the
- Effect can be eliminated in sensor, if pixel structure robust against this effect
- Have structure with **common central storage node** and transfer the charge collected during integration on-demand to respective storage DEPFET
- So-called "**Central Anode**" structure



# IQCA Structures

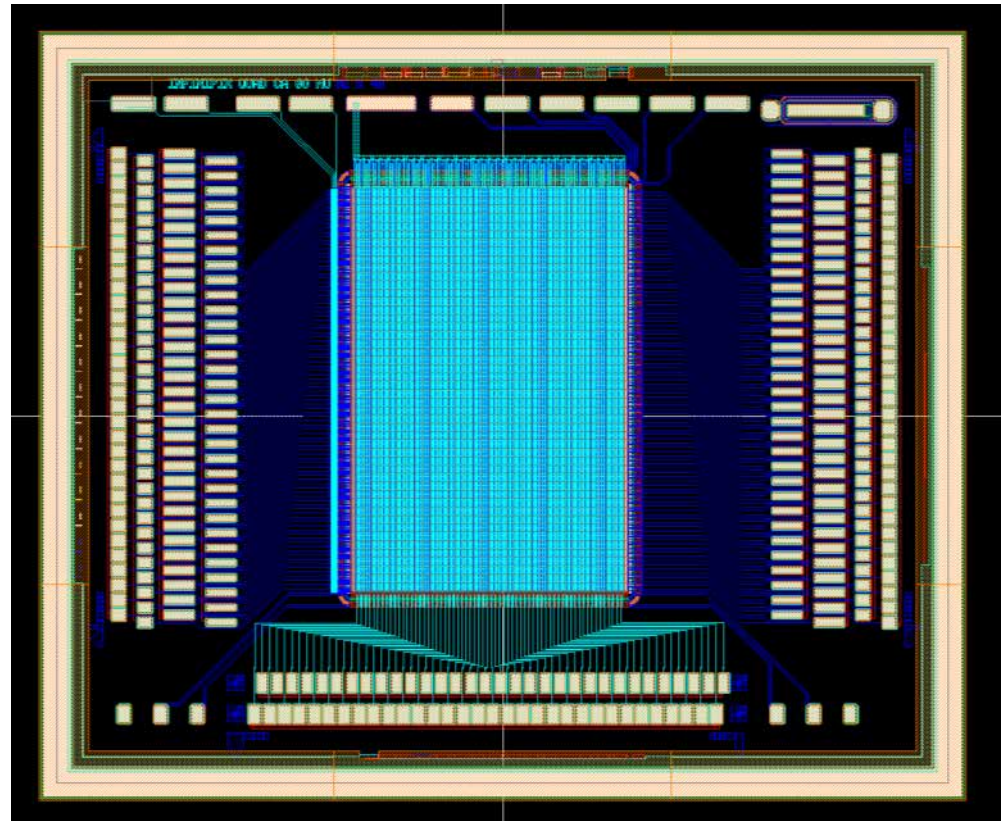


- Clocking of Drain not required
- Transfagate and Anode potential are clocked globally
- Sequential readout of two transistors per row

- 80 x 80 mm<sup>2</sup> pixel prototypes
- Single clear
- Clocked and Static cleargate
- Source follower and drain readout

# IQCA Structures

- 32 x 48 pixel prototypes
- Integrated on standard matrix scaffold
  
- **Critical parameters:**
  - Charge retention (similar to CHC)
  - Charge selectivity
  - Switch speed < 100 ns
  - **New: Spatial conformity!**
  - **New: Charge transfer efficiency!**



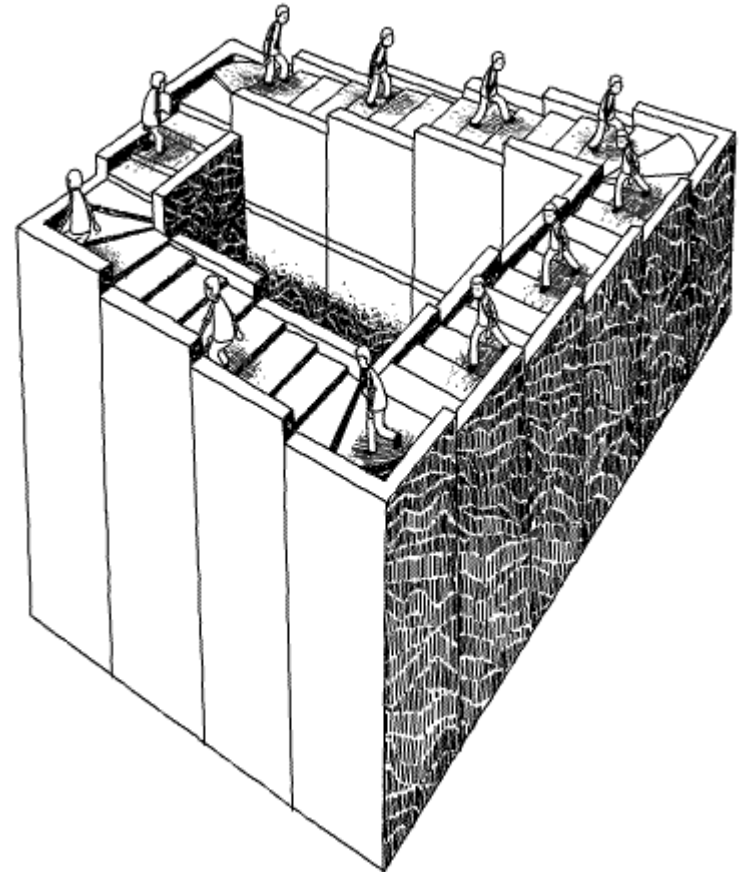


# Repetitive-non-destructive readout

**Beat noise limit using  
the central limit  
theorem!**

**Lower initial noise!**

**Achieve single  
electron photon  
sensitivity!**

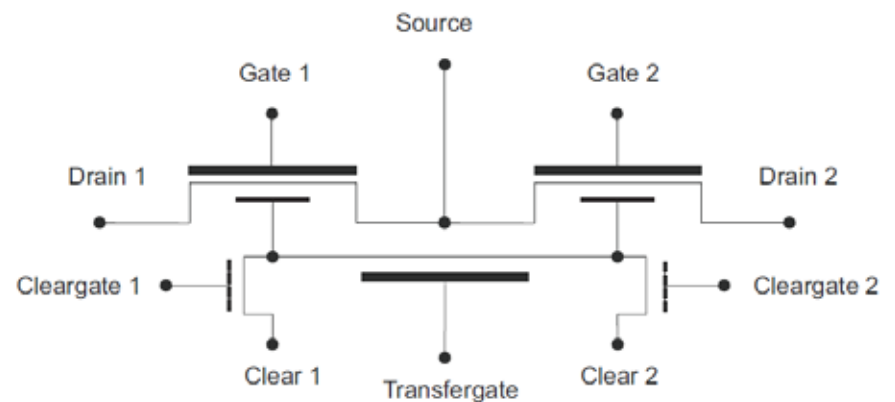
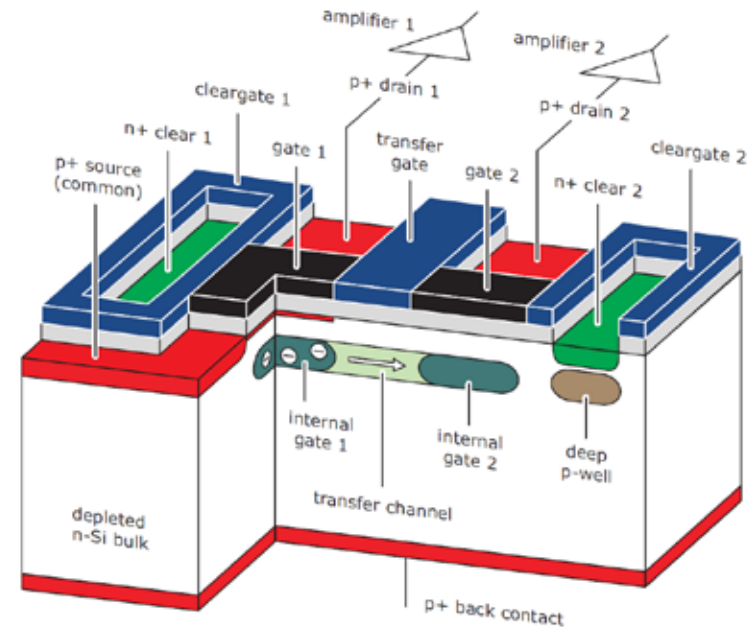




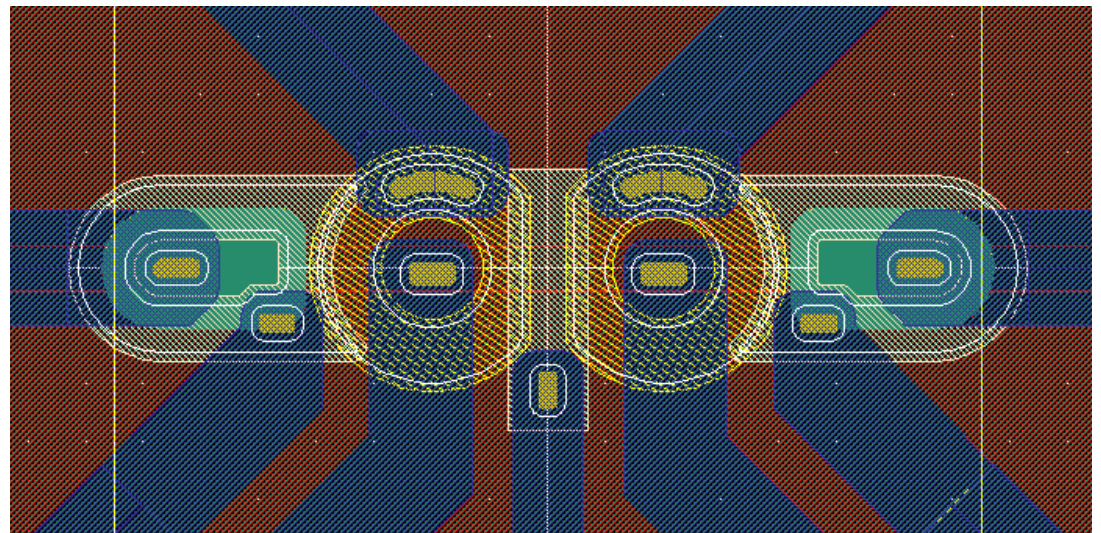
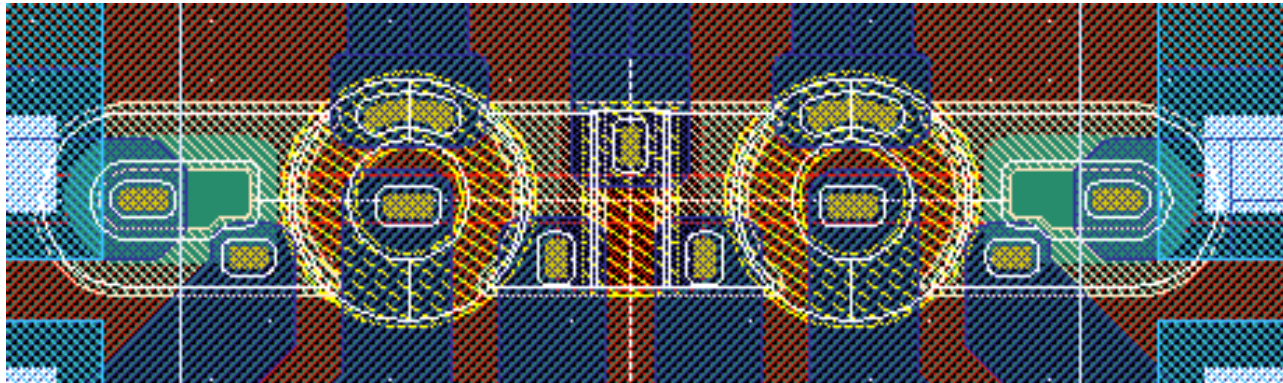
# RNDR devices

## † DEPFET repetitive non-destructive readout (RNDR)

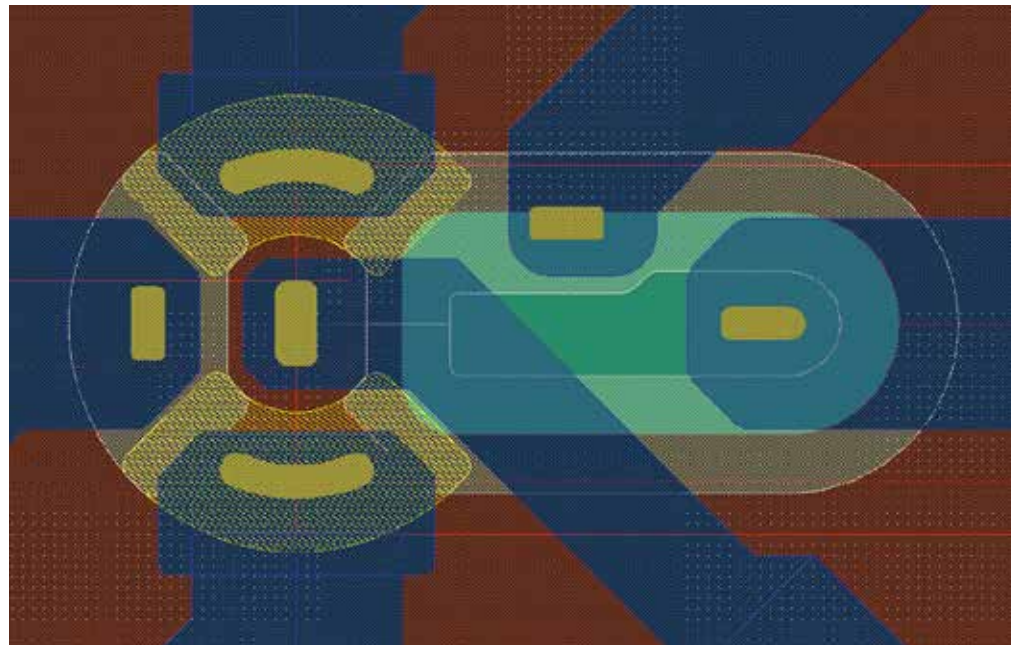
- practical application of the central limit theorem
- 2 DEPFET "sub"pixels in "super"1 pixel
- intra-pixel charge transfer via transfer gate
- allows for statistically independent measurements
- elimination of 1/f-noise limit
- noise reduction by  $N^{1/2}$  @ N readings
- sub-electron noise: 0.18 el. ENC
- single electron distinction



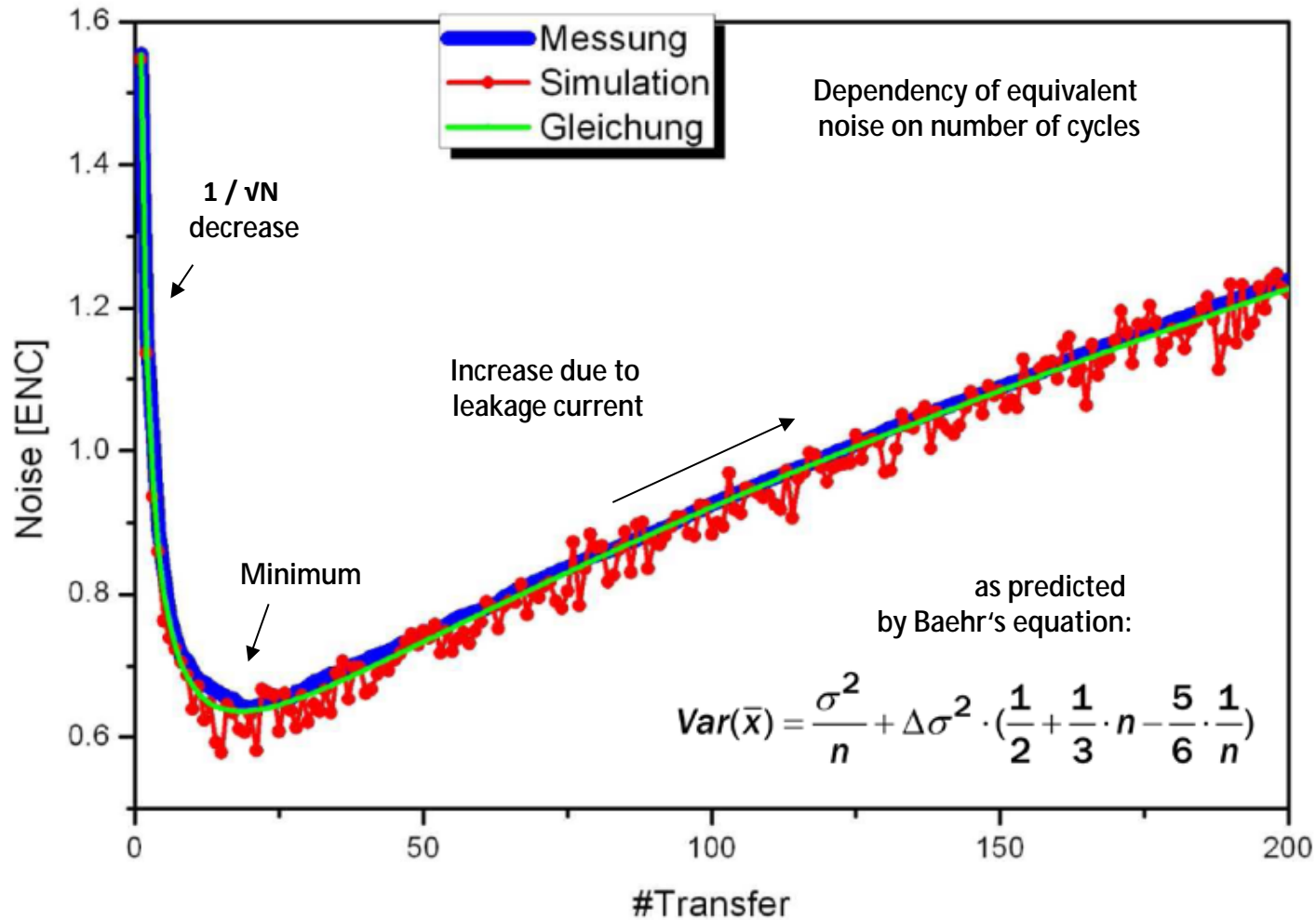
# RNDR devices



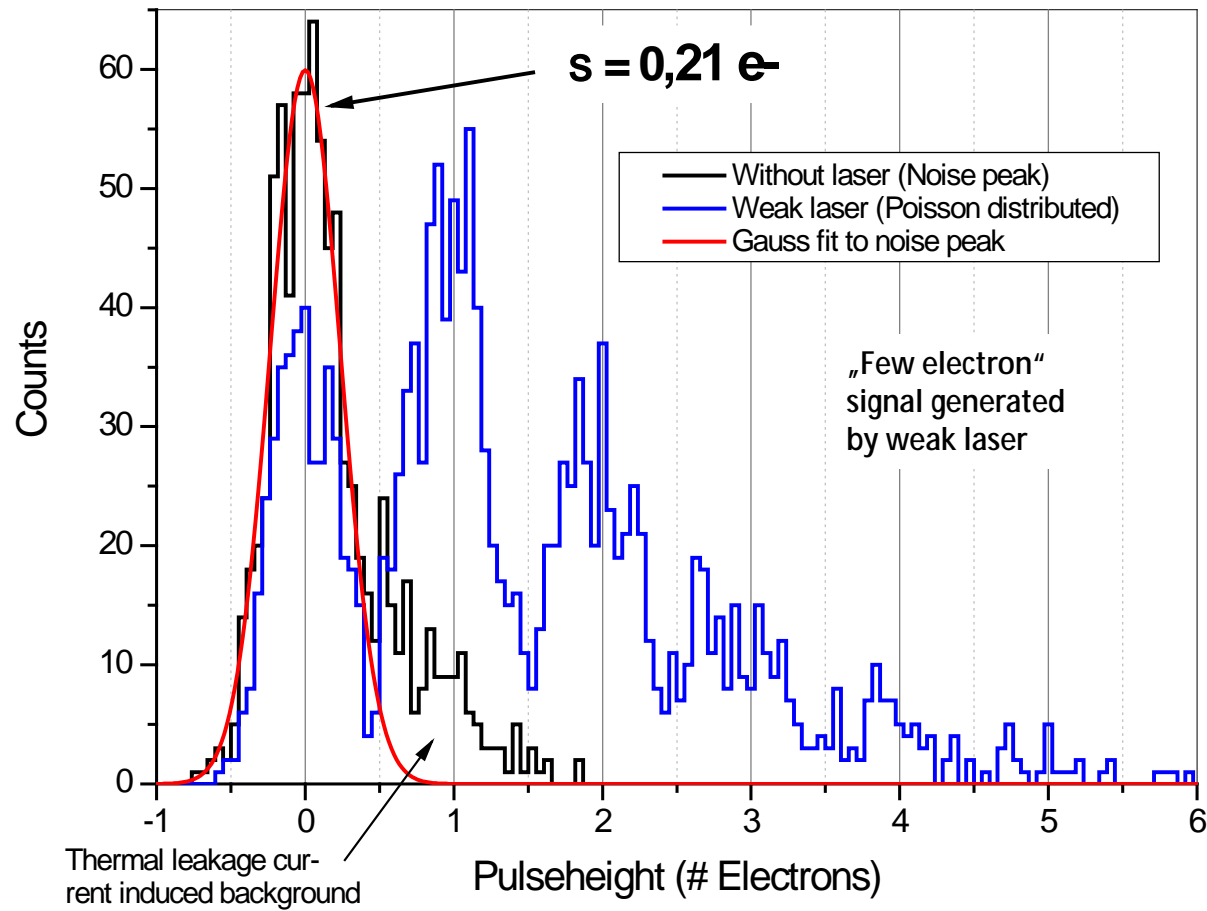
# RNDR devices



# RNDR

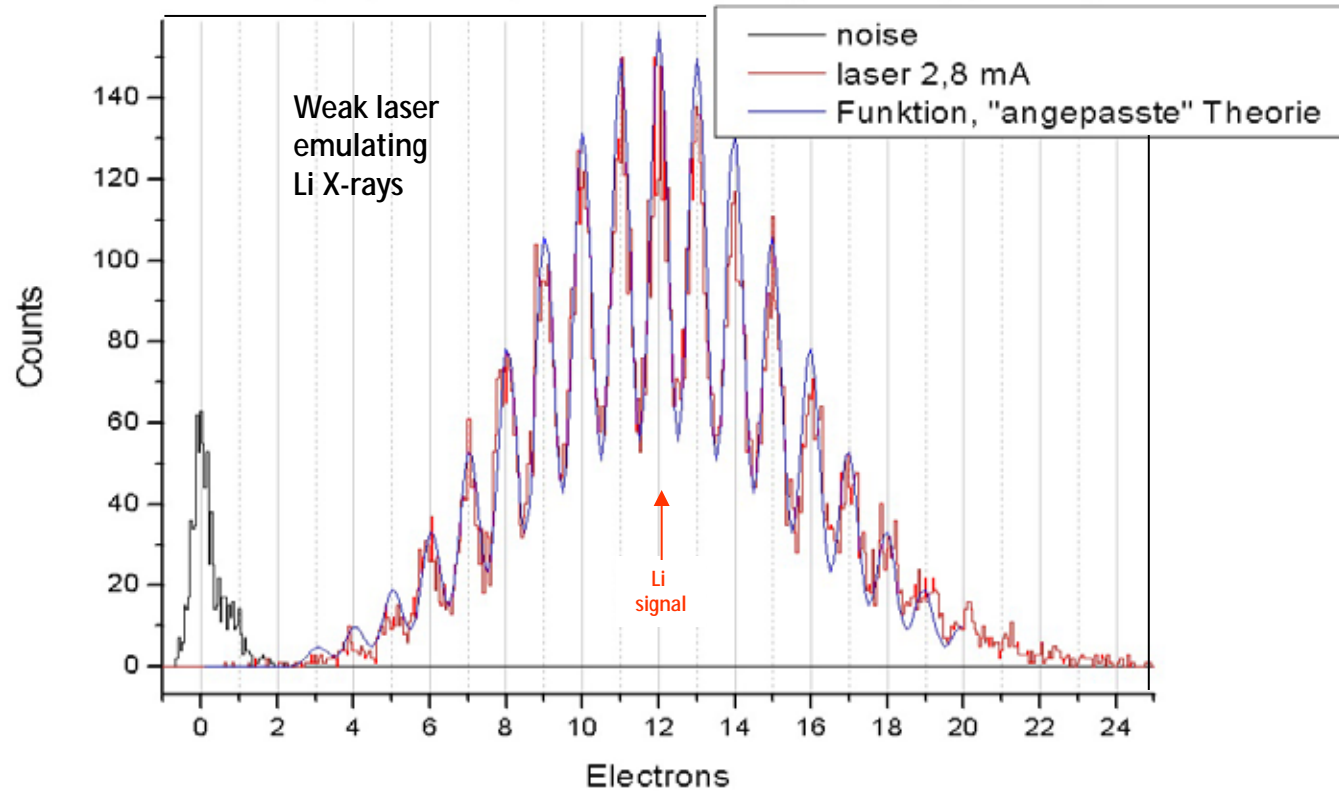


# RNDR

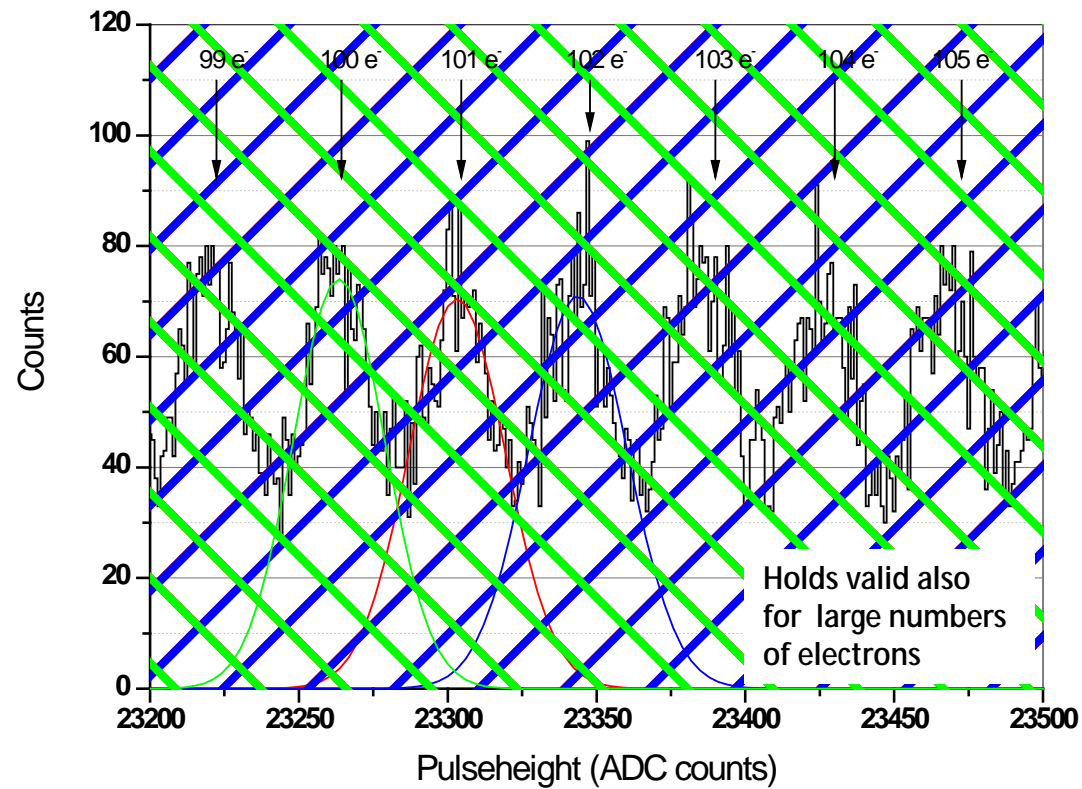


# RNDR

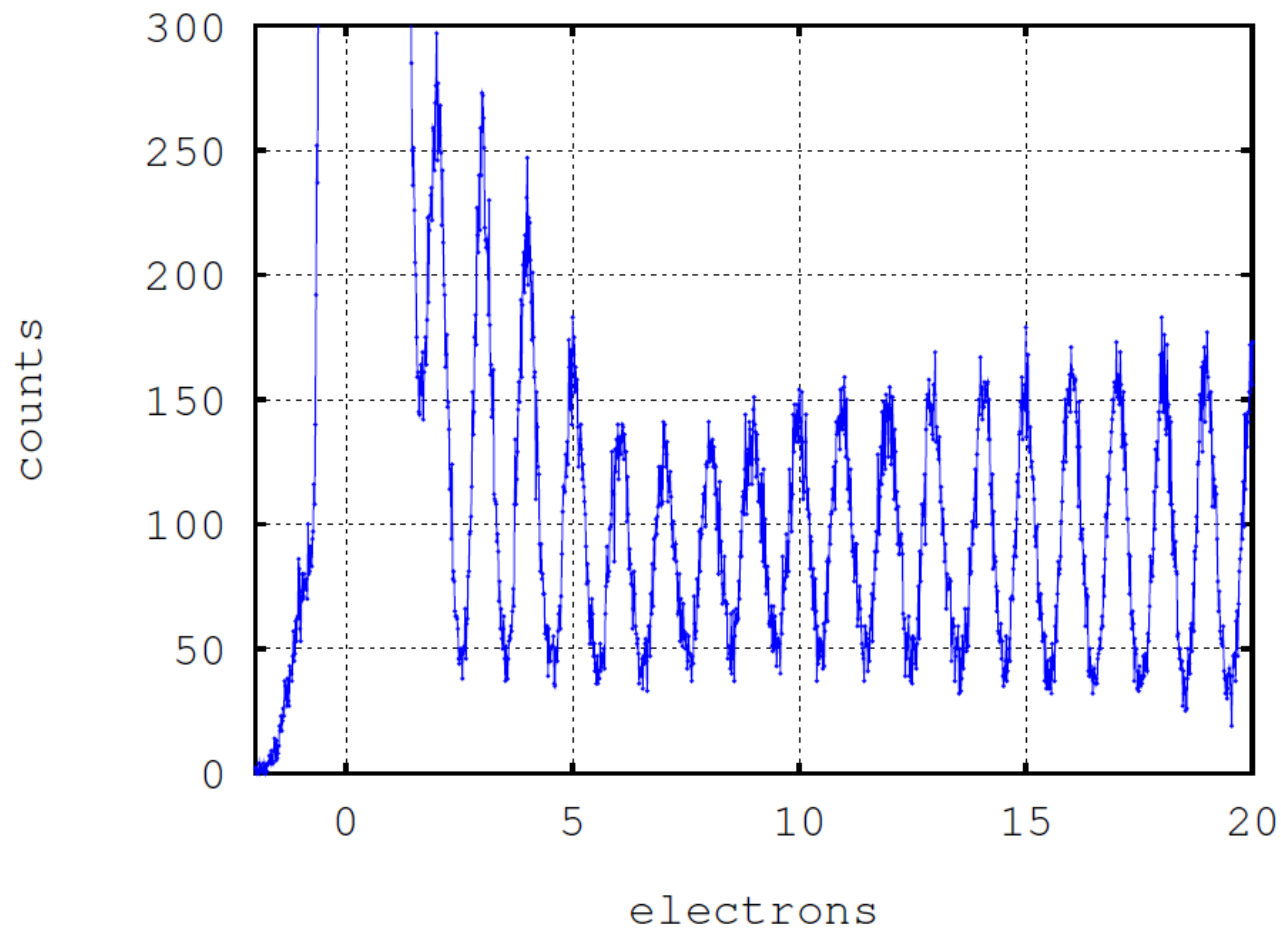
180 Loops, -45°C, weak laser injection (2,9 mA)



# RNDR devices

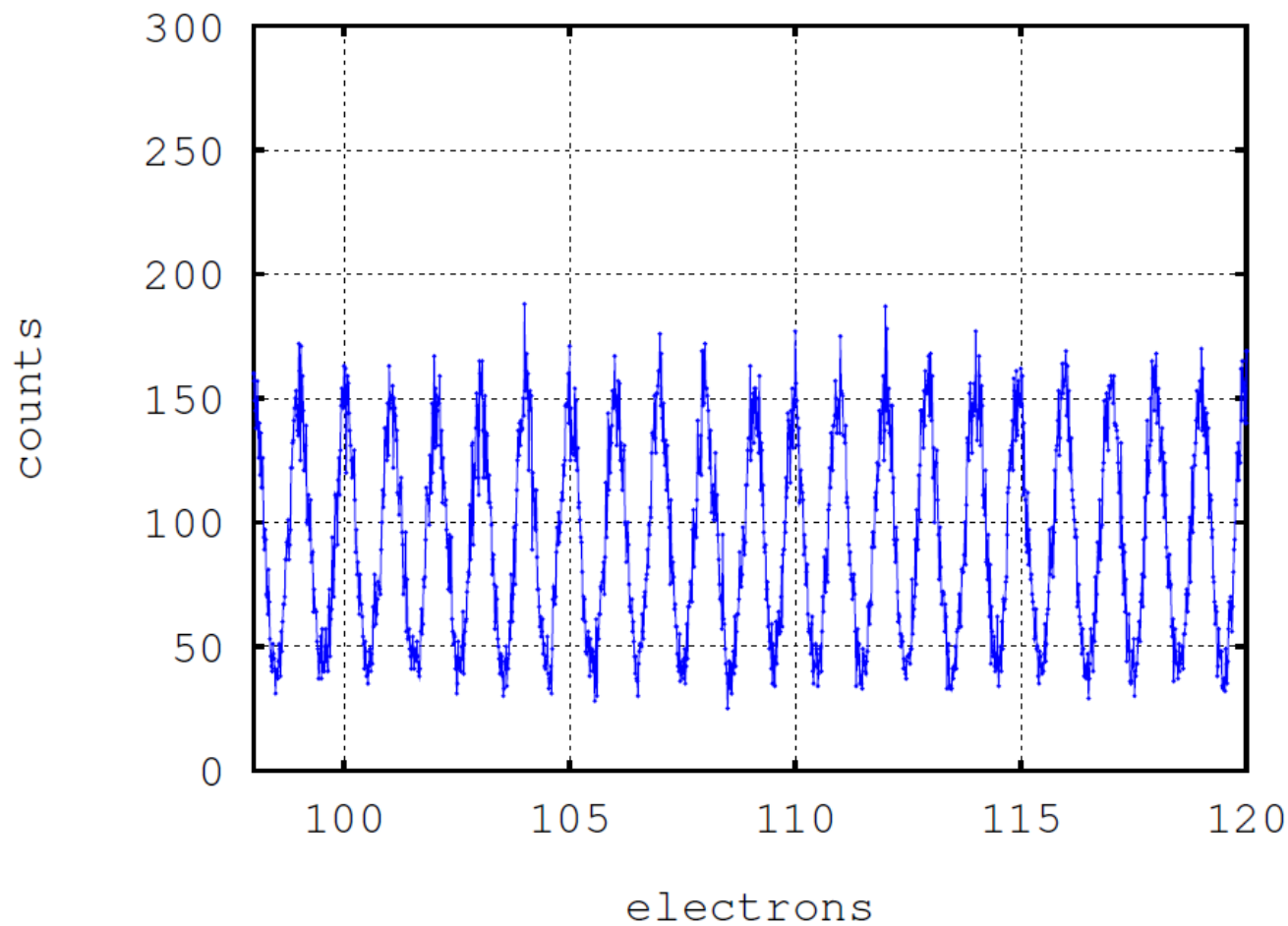


# Series: 0 to 20 e<sup>-</sup>

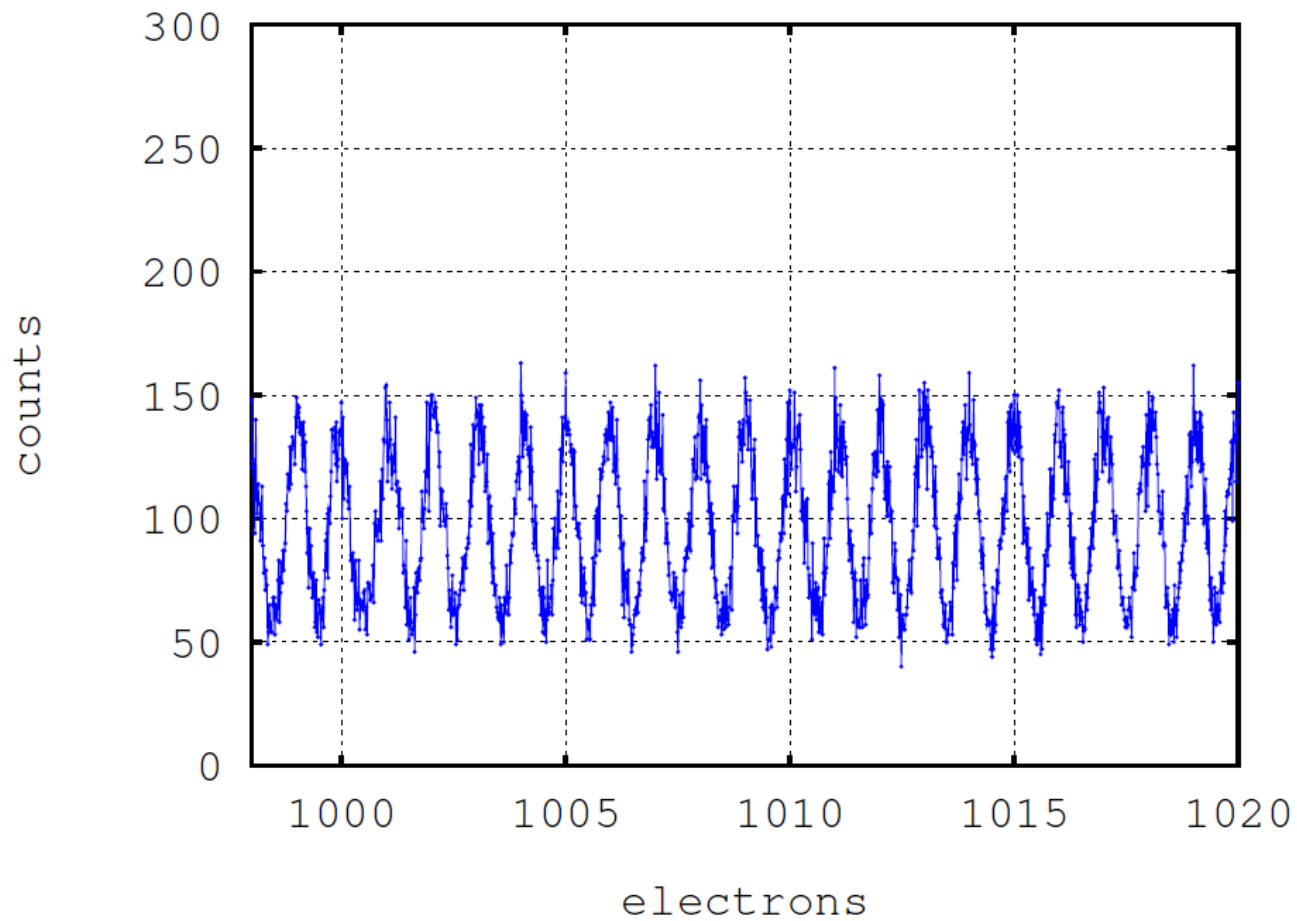




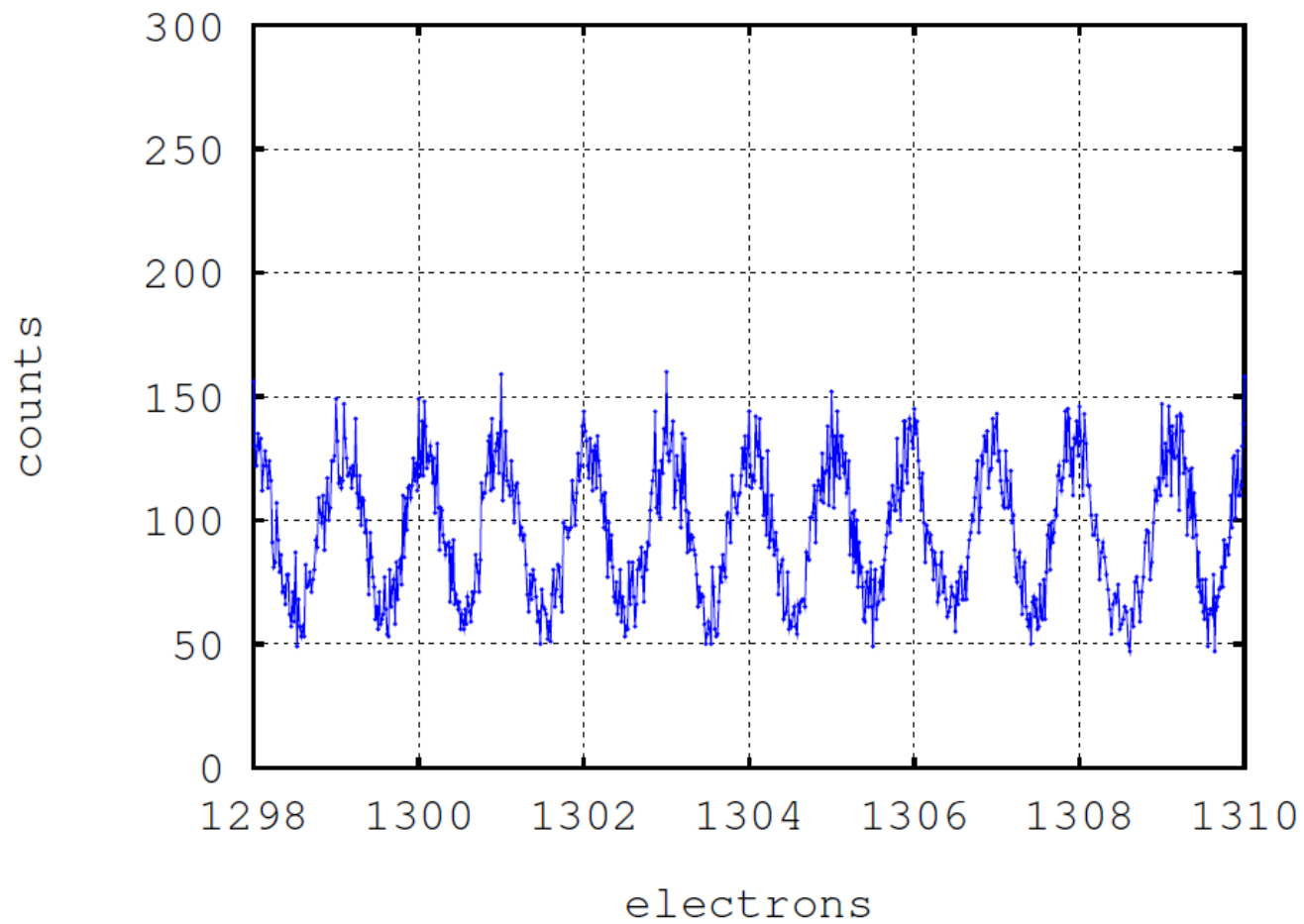
# Series: 98 to 120 e<sup>-</sup>



# Series: 998 to 1020 e<sup>-</sup>

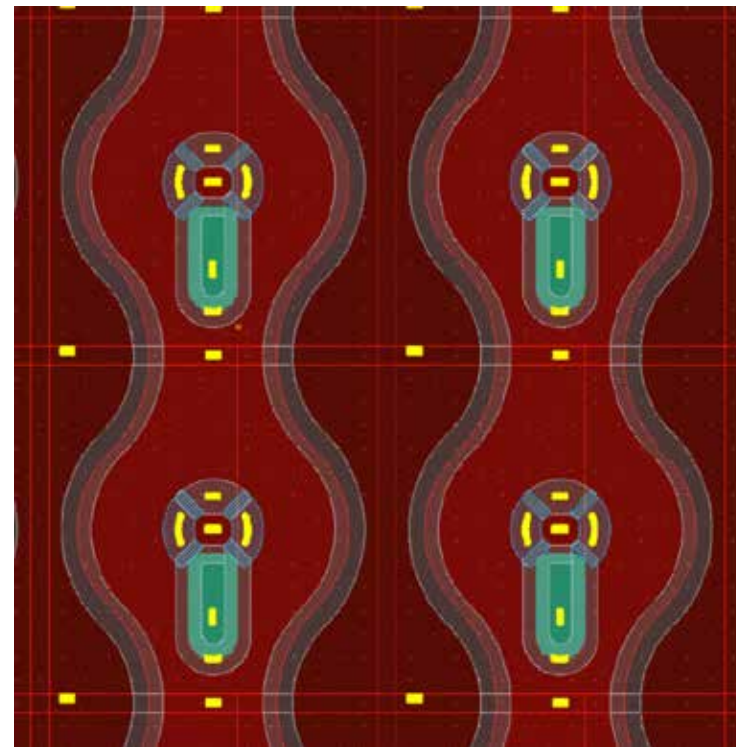


# Series: 1298 to 1310 e<sup>-</sup>



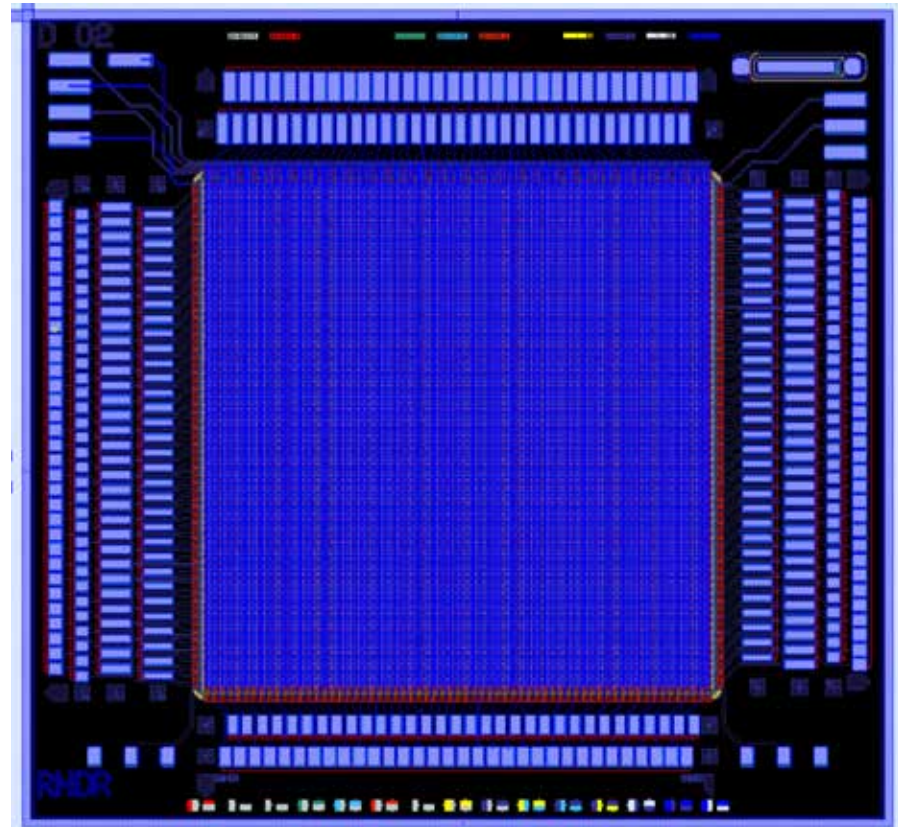
# Matrix devices

- 64 x 64 pixel prototypes
- compact pixel topology
- source follower readout
- row-individual transfergate



# Matrix devices

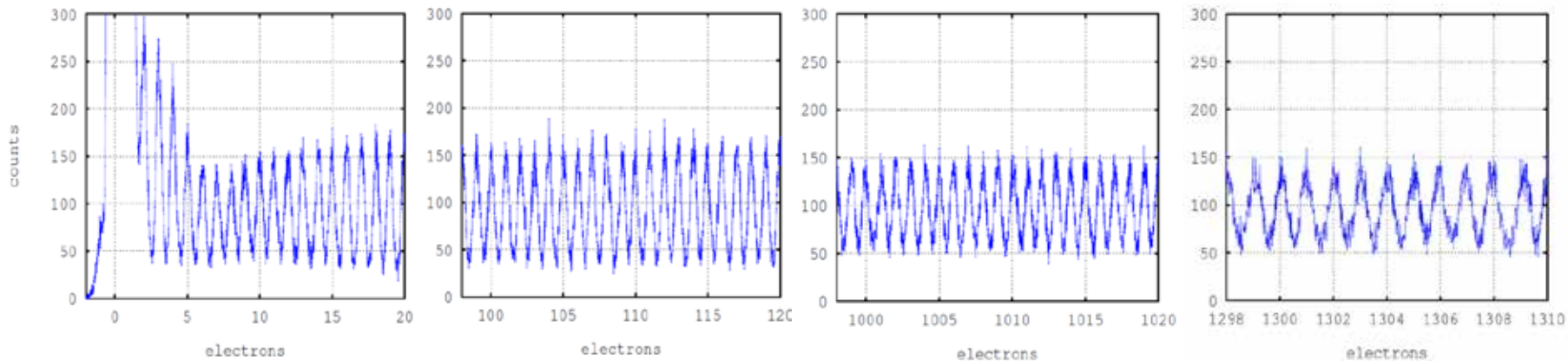
- 64 x 64 pixel prototypes
  - Integrated on standard matrix scaffold
  - third switcher device required (for transfergate clocking)
  - Devices available for evaluation
- 
- **Critical parameters:**
    - Charge transfer efficiency
    - Transfer speed  $< 100$  ns
    - Initial noise
    - Leakage current



# RNDR

RNDR principle works in reality, but totally impractical for use in experiment (except for shuttered solutions)

But what if...?



# Composite multigate DEPFETs

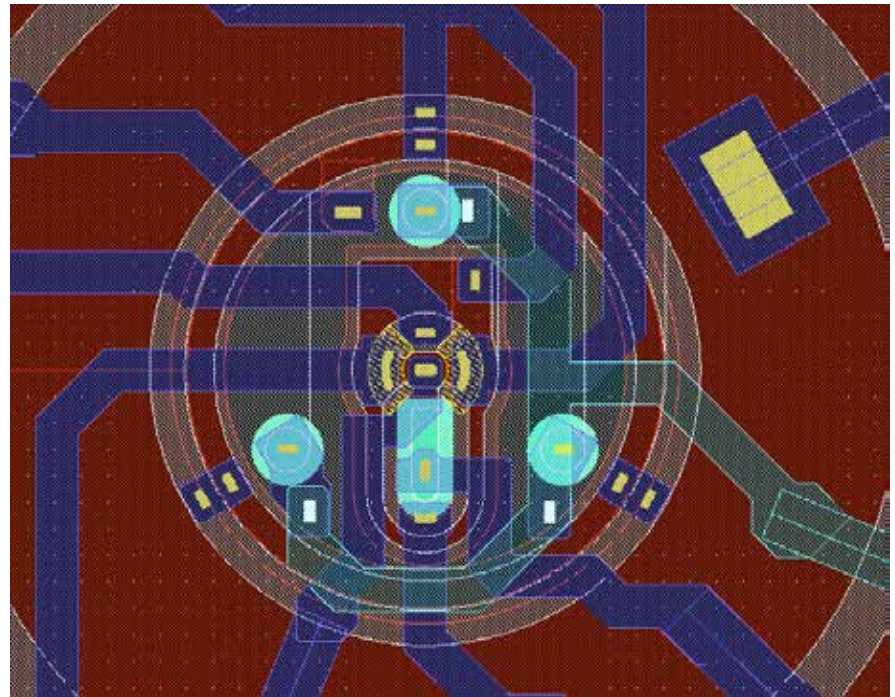
Combine different  
conceptual features

Create devices with  
multiple capabilities



# GPIX RNDR

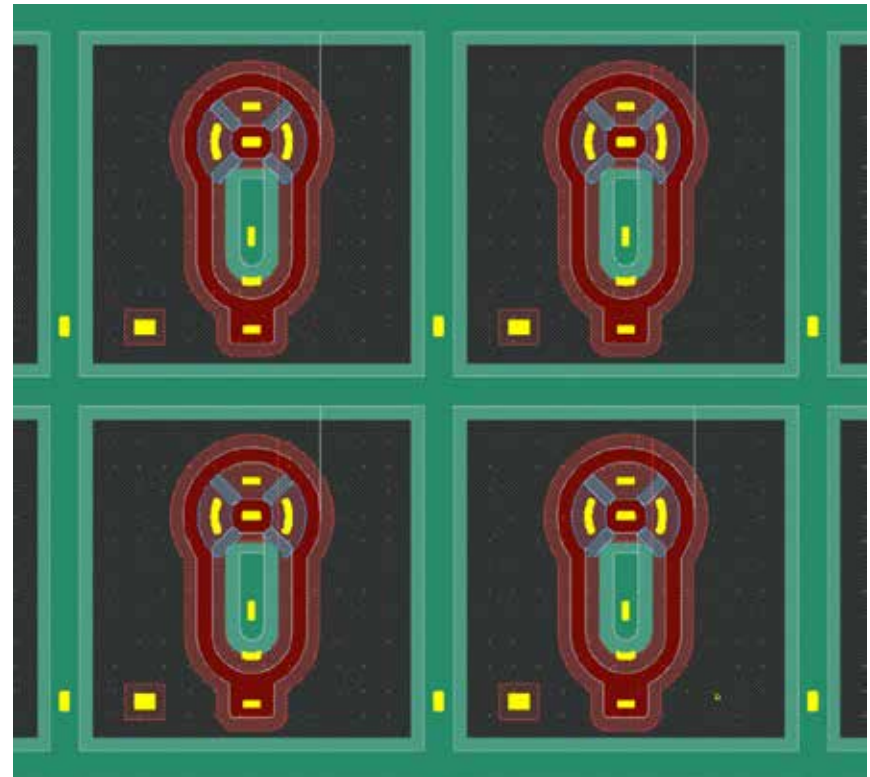
- RNDR pixel embedded in blindgate structure
- Global shutter
- Suppression of bulk leakage current
- RNDR process can take arbitrary time
  
- **Critical parameters:**
  - Charge transfer efficiency
  - Charge retention (also during transfer)
  - Charge selectivity
  - Transfer speed
  - Initial noise





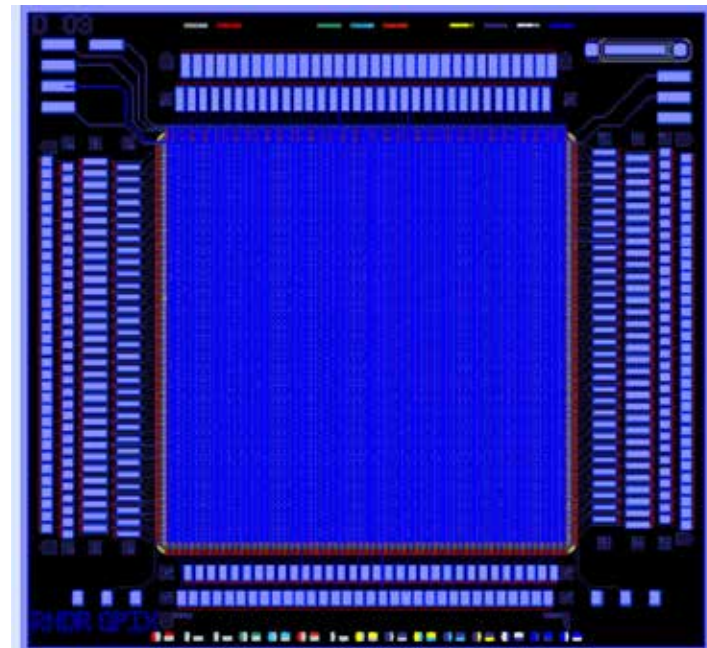
# Matrix device

- Matrix variant available
- 75 x 75 mm<sup>2</sup> size
- Row-individual transfergate
- Global blind and blindgate
- Sourec follower readout



# Matrix device

- 64 x 64 pixel prototypes
- Integrated on standard matrix scaffold
- third switcher device required (for transfergate clocking)
- Devices available for evaluation



**Does it also work with Infinipix?**

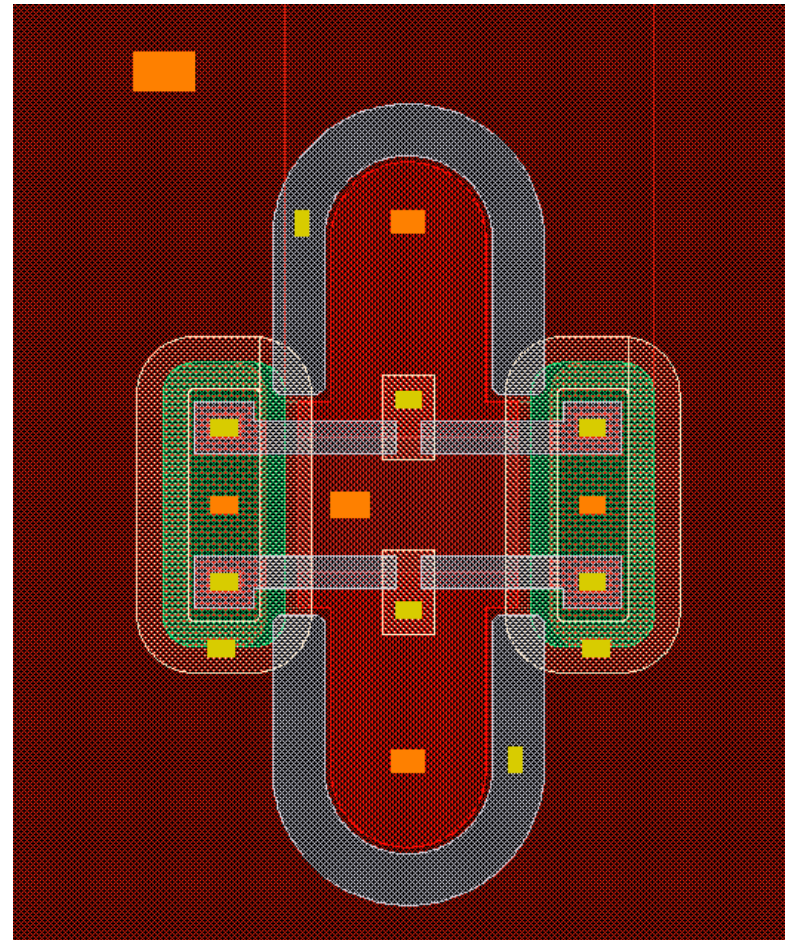
**In theory, yes.**

**We'll see.**

# Infinipix RNDR

## Prototype structure:

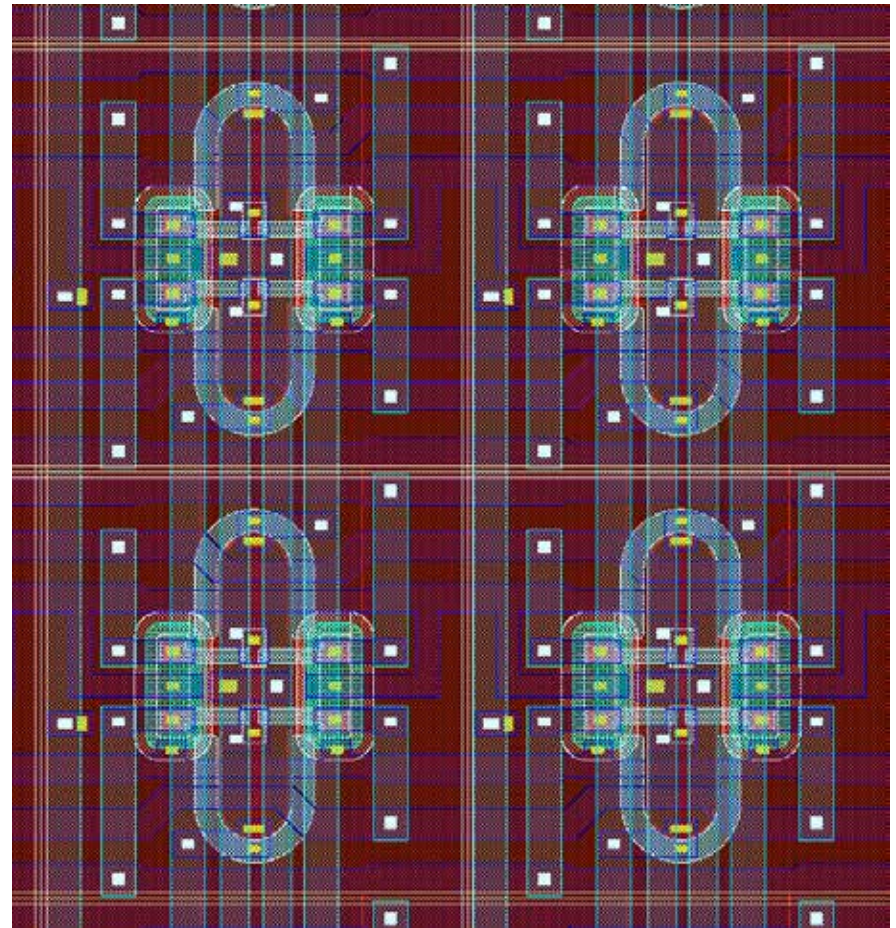
- RNDR feature can easily be implemented
- Global transfergate
- Common clear
  
- **Critical parameters:**
  - Charge transfer efficiency
  - Charge retention (also during transfer)
  - Charge selectivity
  - Transfer speed
  - Initial noise



# Matrix device

## Prototype matrix:

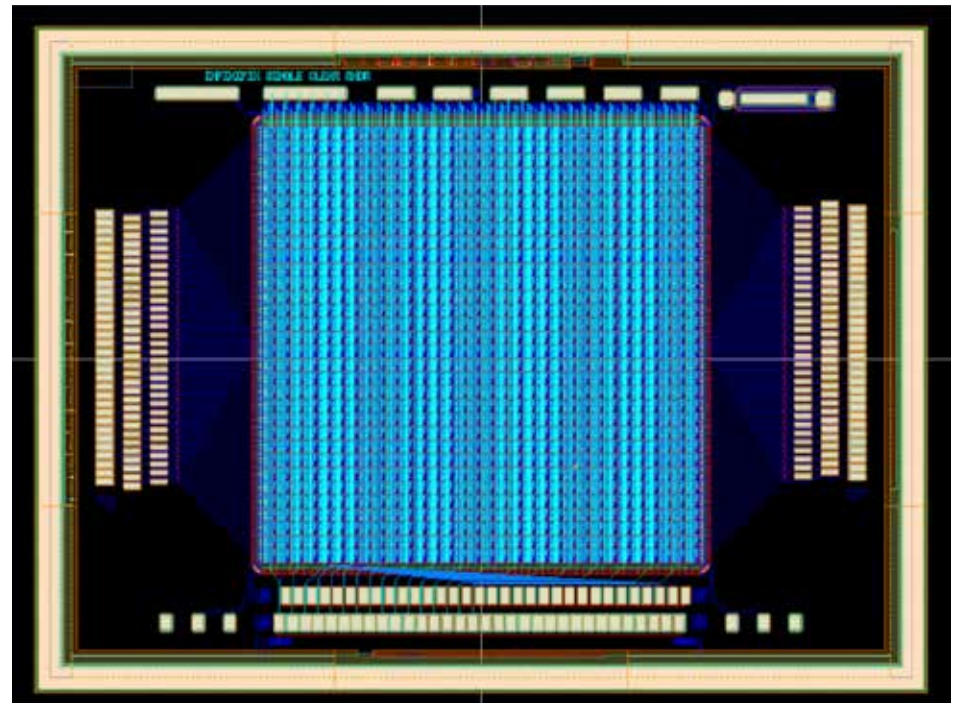
- 150 x 150 mm<sup>2</sup> size
- Two Subpixels per Superpixel
- Common source
- Source follower readout



# Matrix device

## Prototype matrix:

- 32 x 32 pixels
- 150 x 150 mm<sup>2</sup> size
- Sensitive area: 4.8 x 4.8 mm<sup>2</sup>
- Backside illuminated
- "Optical" entrance window
- Chip size: 9.5 x 7 mm<sup>2</sup>
- PXD 11 technology (spectroscopy grade)
- PXD 11 devices in fabrication
- Soon: New production dedicated to Infinipix devices



# Overview

Device	# Gates / pixel	Single pixels	Drift detectors	Matrices
Standard DEPFET	3	available	available	available
GPIX	4	available	available	available
Infinipix	6 (5) <sup>a)</sup>	available	available	available <sup>b)</sup>
IQ	12 (10) <sup>a)</sup>	in production	not available	in production
IQCA	17 (15) <sup>a)</sup>	in production	not available	in production
RNDR	7 (6) <sup>a)</sup>	available	available	available
GPIX RNDR	8 (7) <sup>a)</sup>	available	available <sup>c)</sup>	available
Infinipix RNDR	12 (10) <sup>a)</sup>	in production	in production	in production

<sup>a)</sup> number in brackets is for devices w/ shared clear

<sup>b)</sup> evaluation by MPE

<sup>c)</sup> few devices left

# Summary

DEPFET devices are an ideal platform for the implementation of functional concepts manipulating directly the signal charge

Many different concepts have been tested and verified

We need to find better problems for our solutions!

