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Design Changes for DHPT 1.1

H. Krüger, Bonn University

DEPFET Workshop, Seeon, May 10-13, 2015

Outline

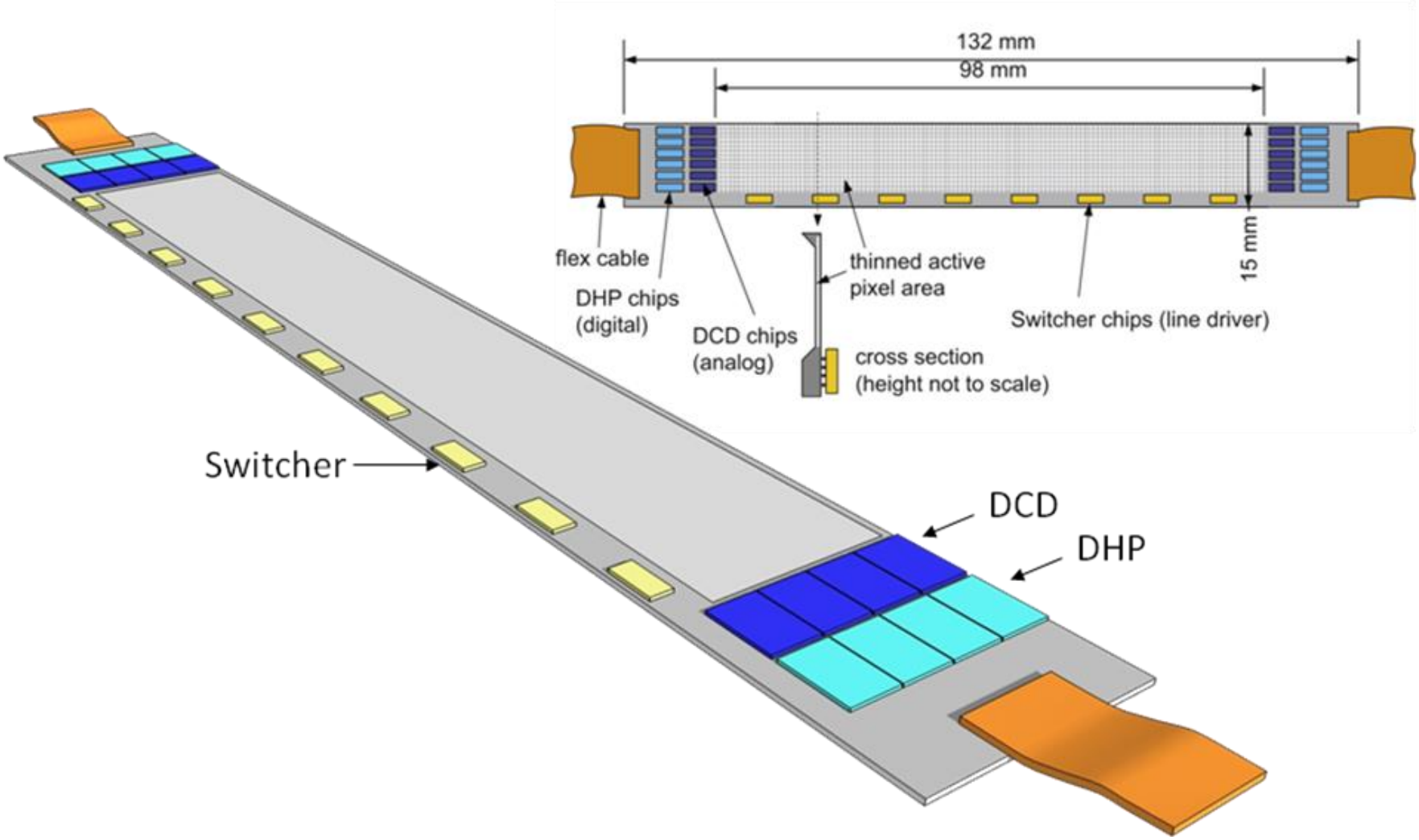
Slides from

DHPT 1.1 - Internal Design Review, HLL, Munich, April 16-17, 2015

Known DHPT 1.0 issues that shall be improved (or are still open):

- Serializer: timing bug
- CML driver enhancement : reduce parasitic resistance
- Prog. delay elements issue: duty cycle distortion
- Data receiver robustness: duty cycle distortion with non-symmetric input edges
- Data processing enhancements (?)

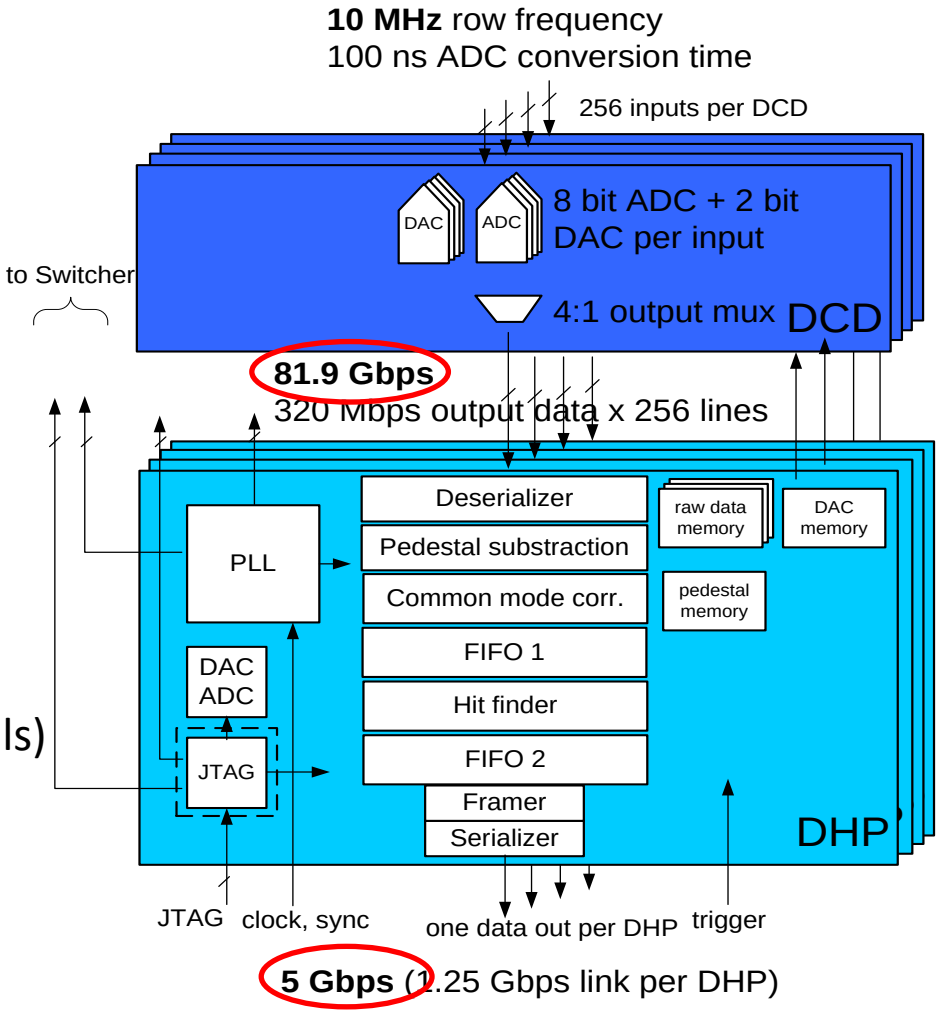
ASICs for the DEPFET PXD



Data Handling Processor - DHP

- Functionality
  - Module controller
    - JTAG bus to DCDB and SWITCHER chips
    - Clock & timing generation & distribution
  - Data reduction (1/20): 0-suppression, triggered r/o

- Data processing details
  - Raw data buffer (two frames, 40µs)
  - Common mode (two pass)
  - Fixed pattern noise correction (static pedestals)
  - Hit finder (FIFO1 + FIFO2)
  - Framing (AURORA)
  - Serializer + Gbit link driver



Data Handling Processor Development

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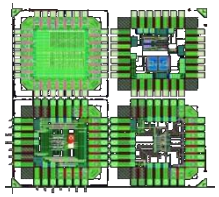
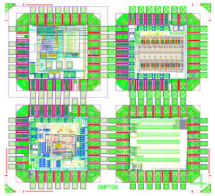


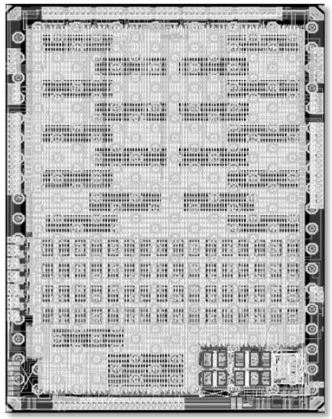
DHPT 0.1 (**65nm**)
Test structures



DHPT 0.2 (**65nm**)
Test structures

DHPT 1.0 (**65nm**)
Full size chip

Current phase



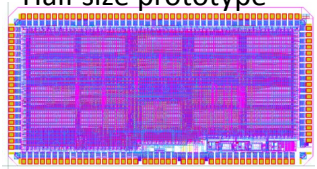
DHPT 1.1 (**65nm**)
Production version

Change from 90nm to 65nm technology

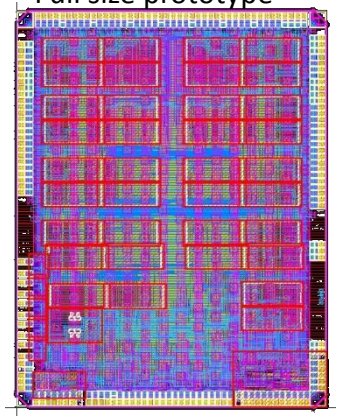
2010	2011	2012	2013	2014	2015	2016

submission dates

DHP 0.1 (**90nm**)
Half size prototype



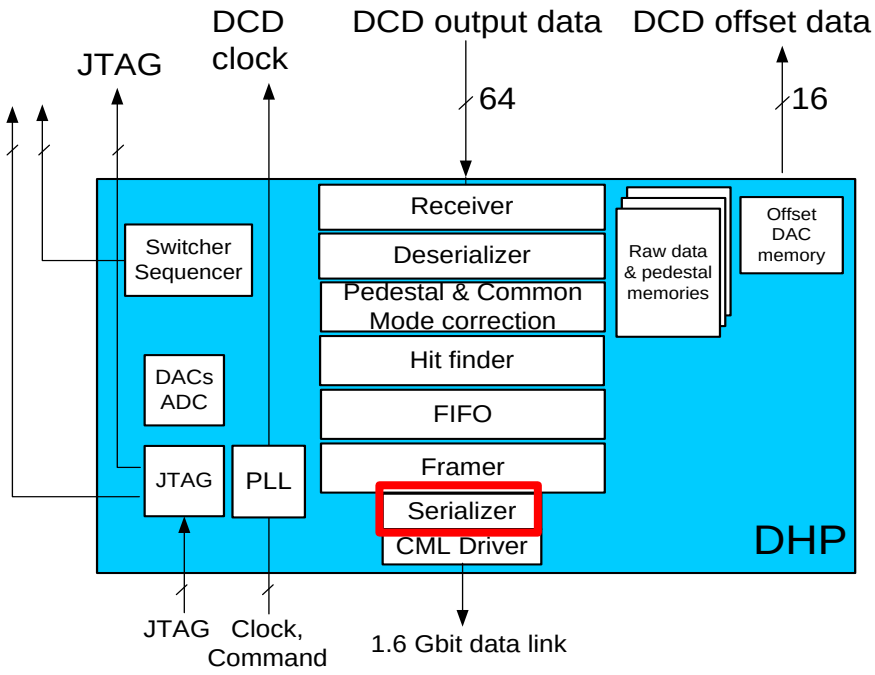
DHP 0.2 (**90nm**)
Full size prototype



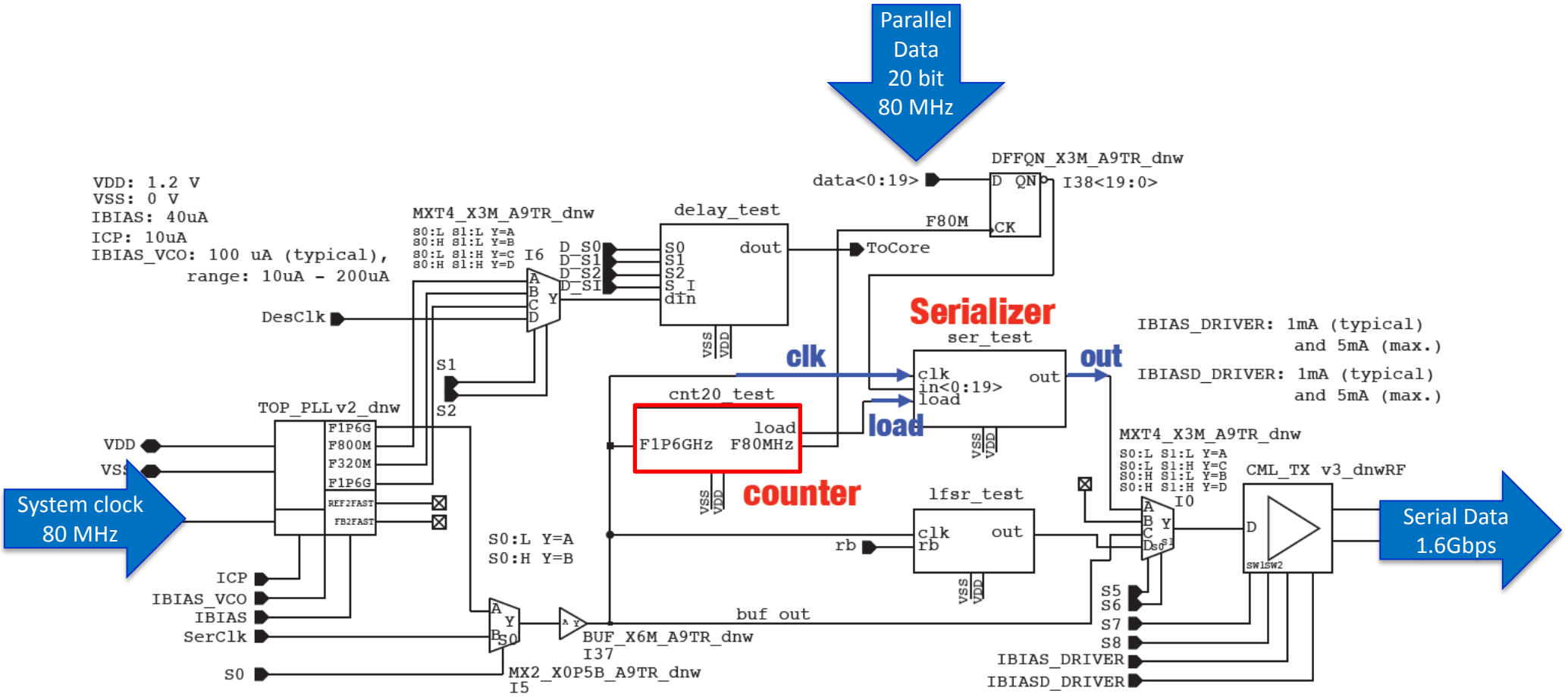
Design reviews

DHPT 1.0 Known Issues

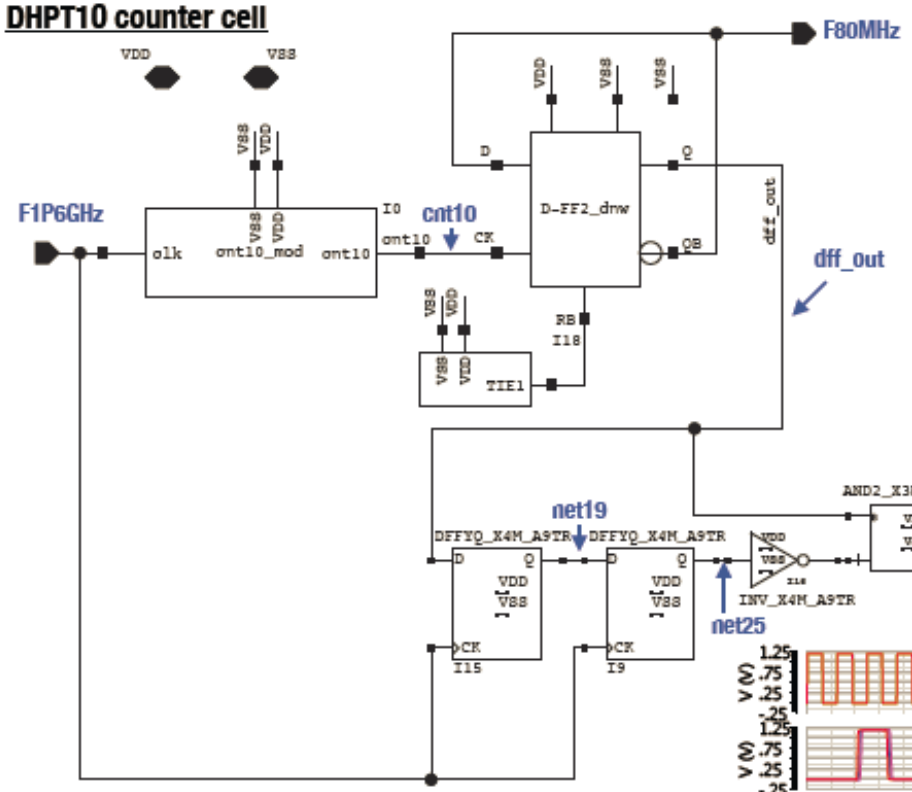
SERIALIZER



PLL + SER Block Diagram



DHPT10 counter cell



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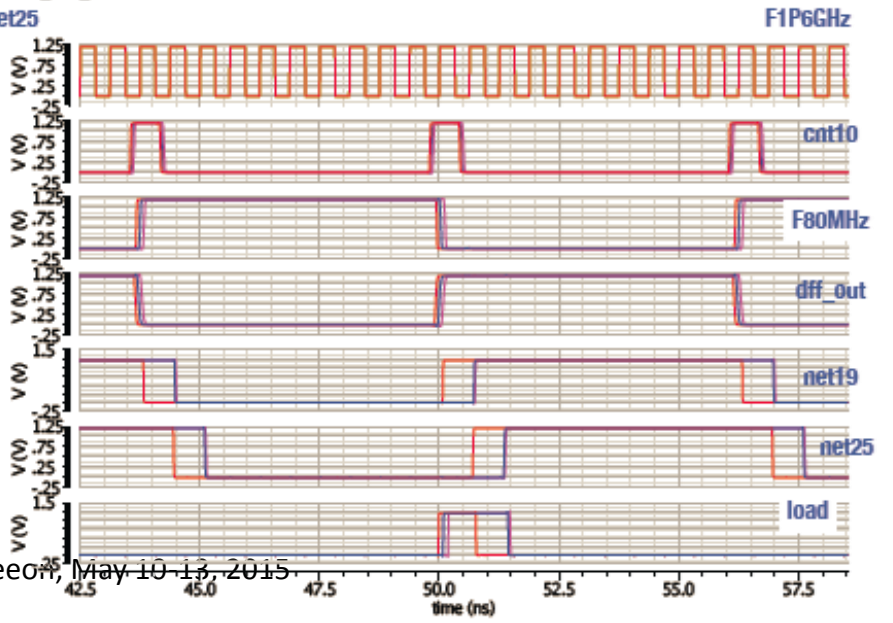
RC-extracted with corners(tt ss ff)



Serializer Bug

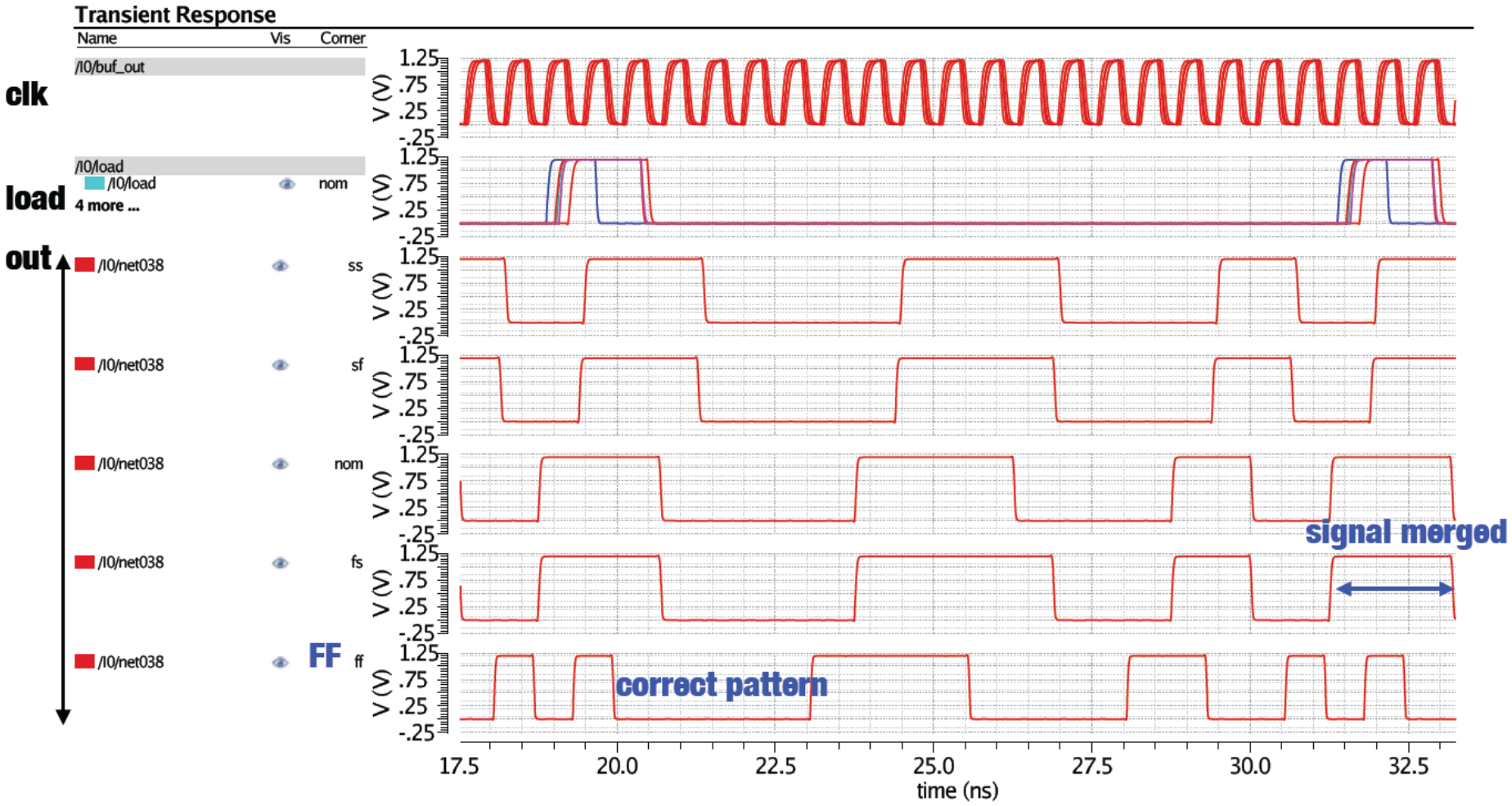
- Mistake made during simulation of the extracted layout with all process corners

- Serializer works, but VCC and/or GCK have to be adjusted:
  - GCK= 80 MHz → VCC = 1.6V (works but should not be applied for a long time)
  - GCK= 60 MHz → VCC = 1.4V (ok)

- Manufacturer test data ➔ wafer batch has „slow NMOS“ (too high threshold)

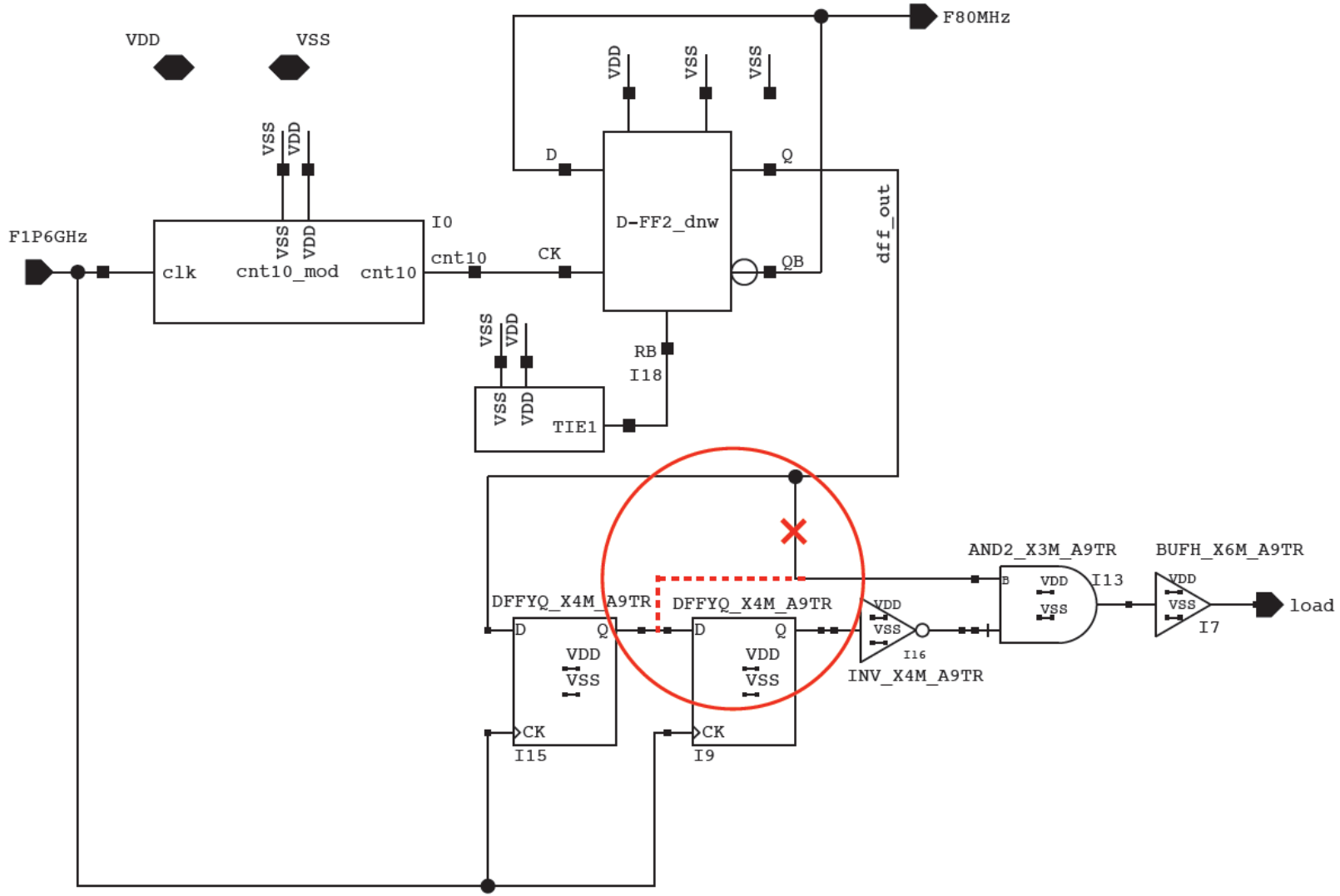
PARAMETER BY LOT:		SPEC LO	SPEC HI	MIN	MAX	MEAN	STD DEV
VTl_N4	(N/.3/.06/1)	0.300	0.490	0.368	0.490	0.423	0.029
Isof_N4	(N/.3/.06/1)	-1.400E-07	0.000	-8.958E-10	-3.833E-11	-2.339E-10	2.063E-10
Isat_N4	(N/.3/.06/1)	0.491	0.735	0.547	0.673	0.593	0.031

DHPT 1.0 Serializer Simulation

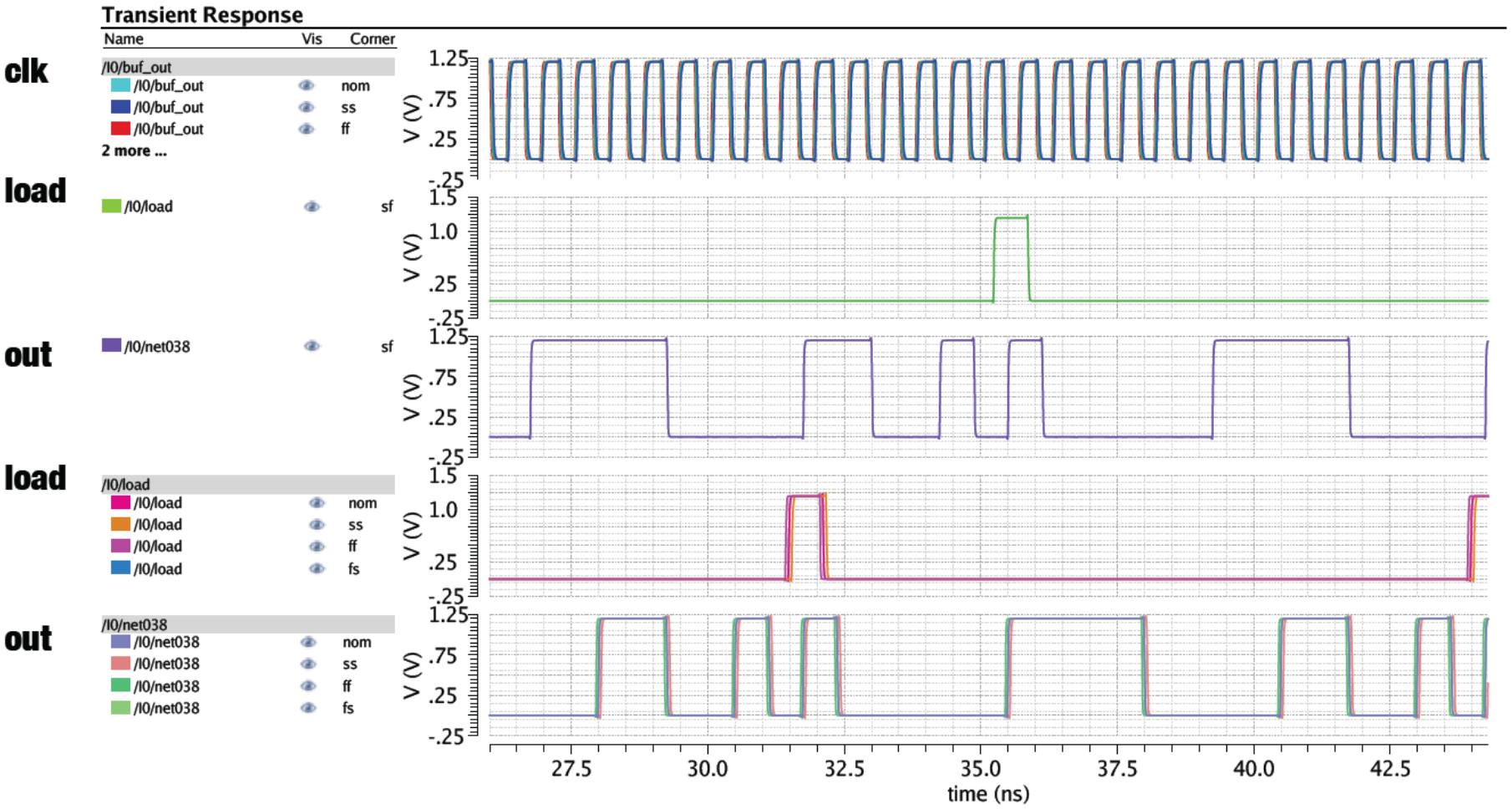


Timing of "load" is not provided correctly, except fast-fast corner.

Design Fix in the Counter Circuit



Serializer Simulation with Modification (DHPT 1.1)



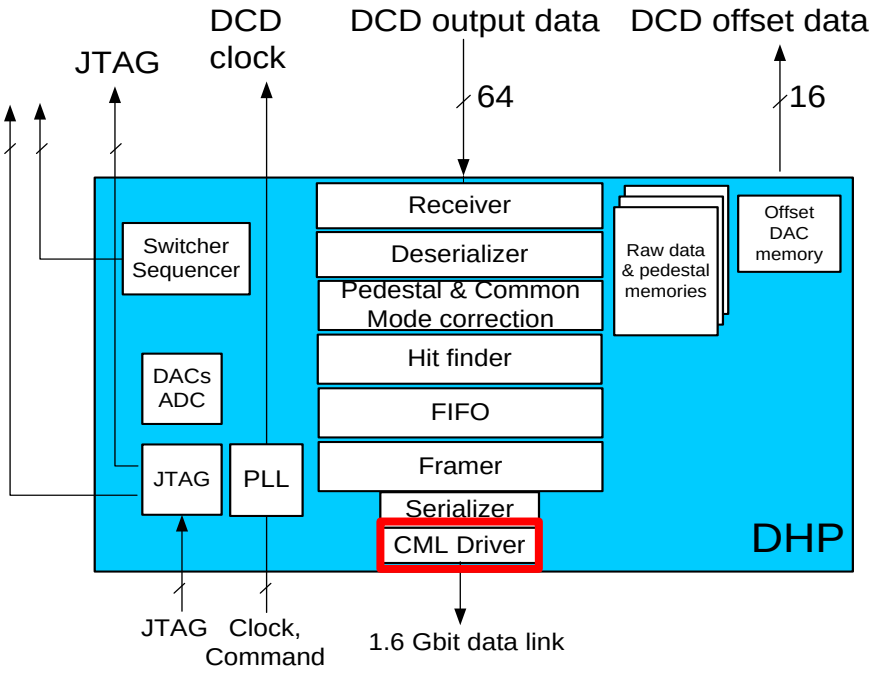
Correct pattern can be obtained with all corners.

Serializer Re-design Status

- Origin of the bug: **understood, reproducible**
- Design modification: **identified**
- Re-design on schematic level: **done**
- Re-design on layout: **done** (homeopathic change)
- Simulation of extracted netlist (all corners): **done**

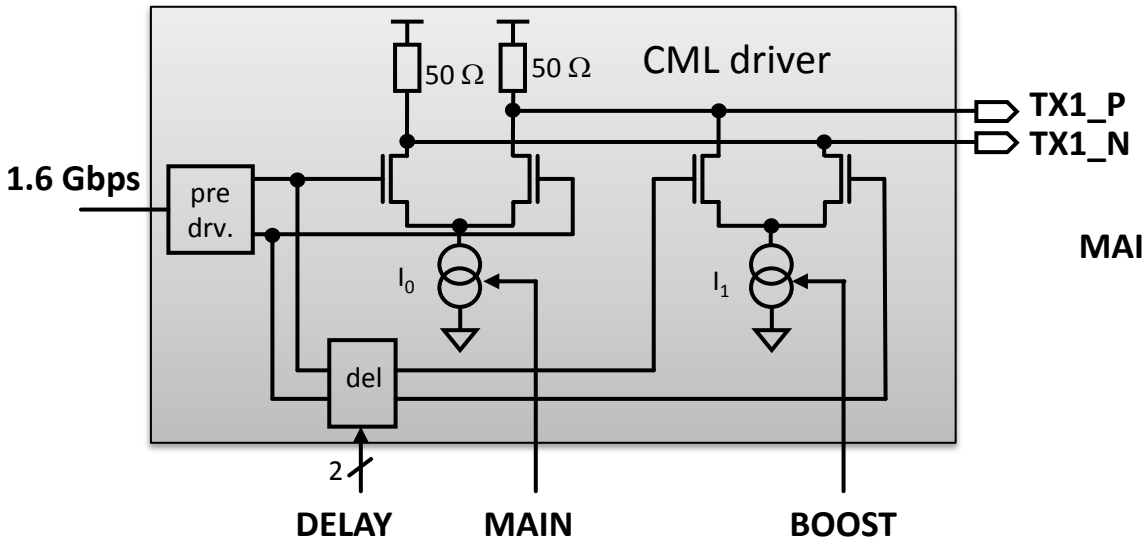
DHPT 1.0 Known Issues

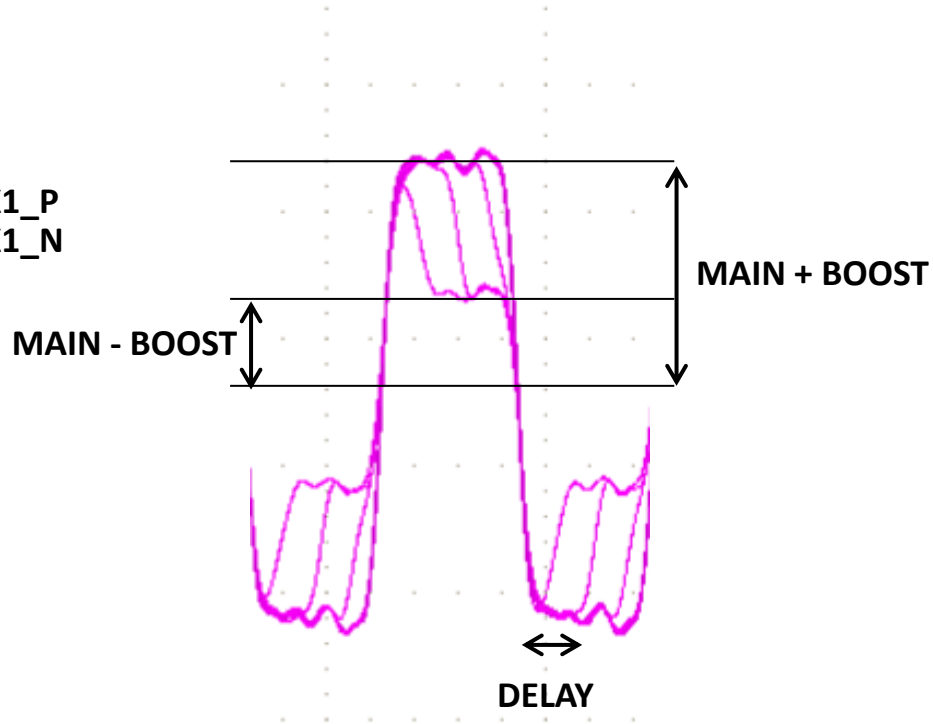
CML DRIVER



CML Driver

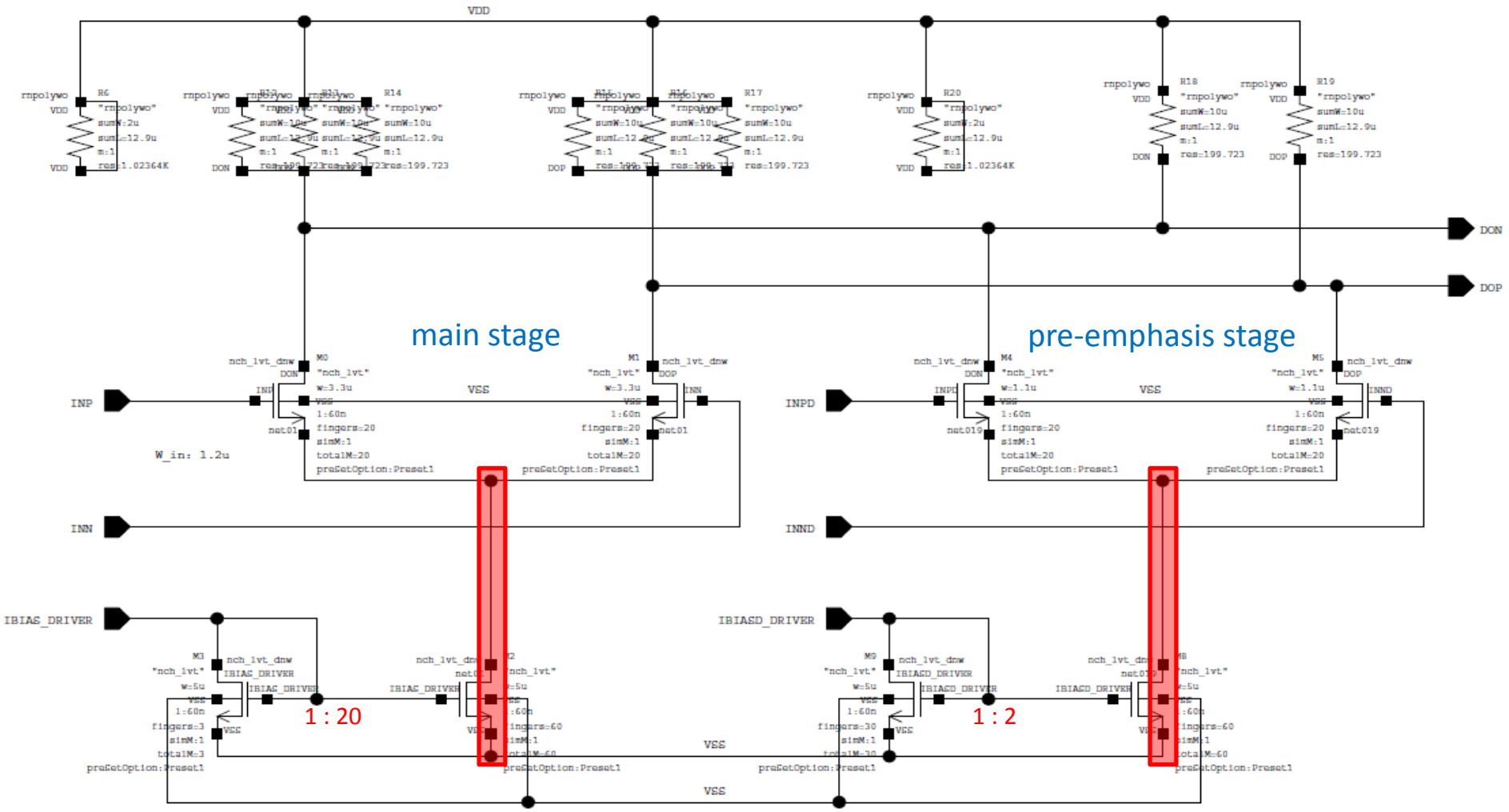
- Works fine
- Try to **enhance the performance** (output swing) to have a bit more safety margin



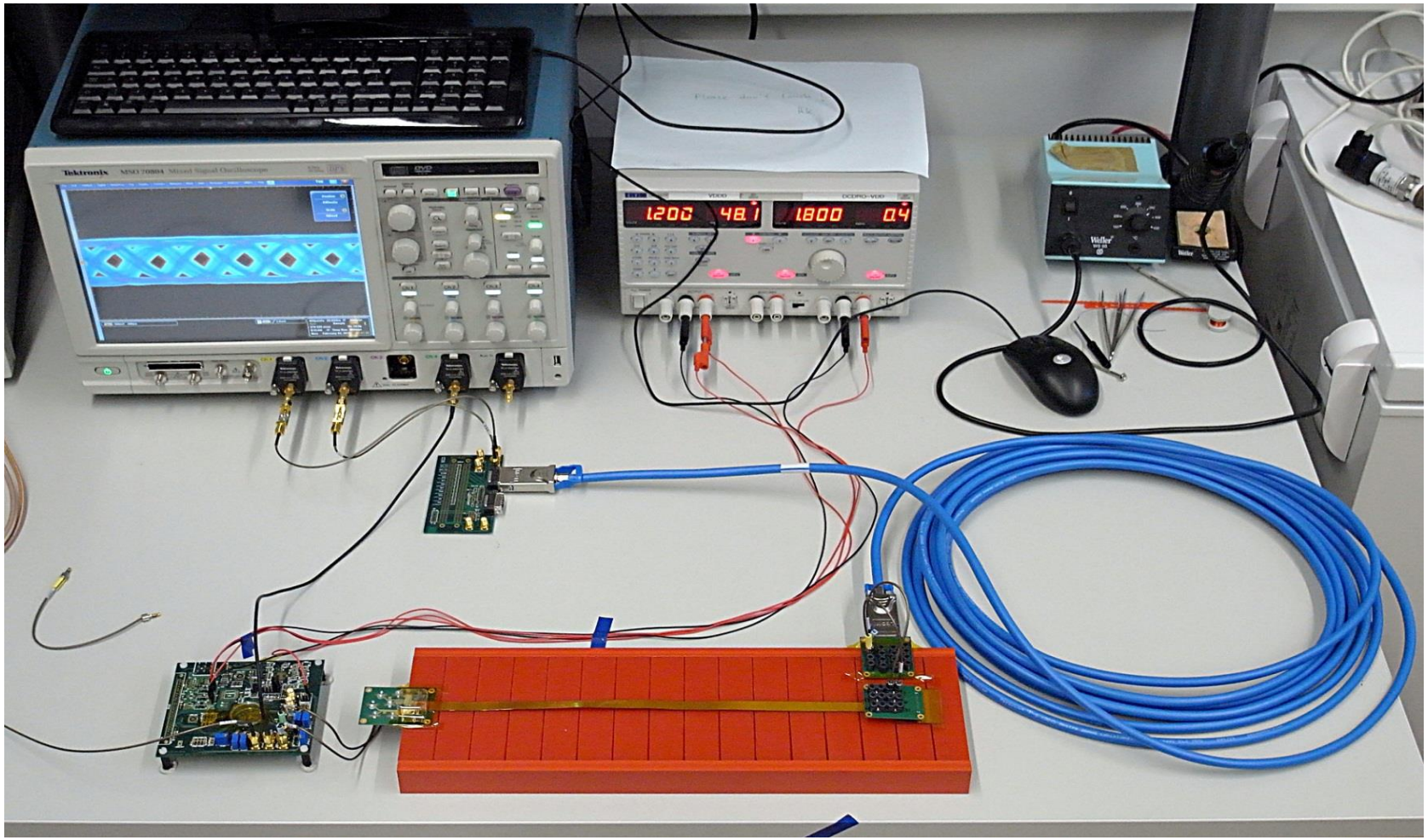


T. Kishishita

Driver Schematic



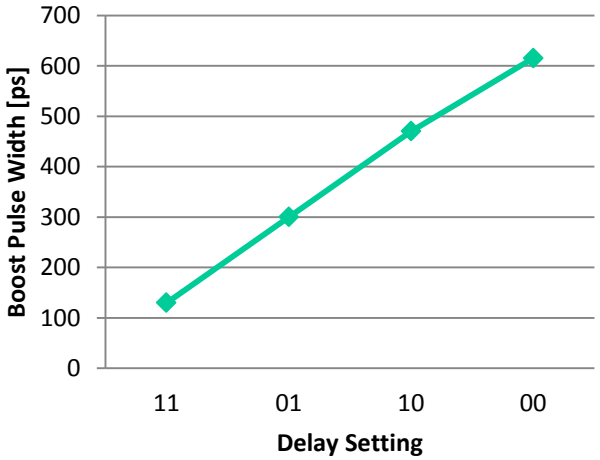
DHPT 0.1 – Test setup

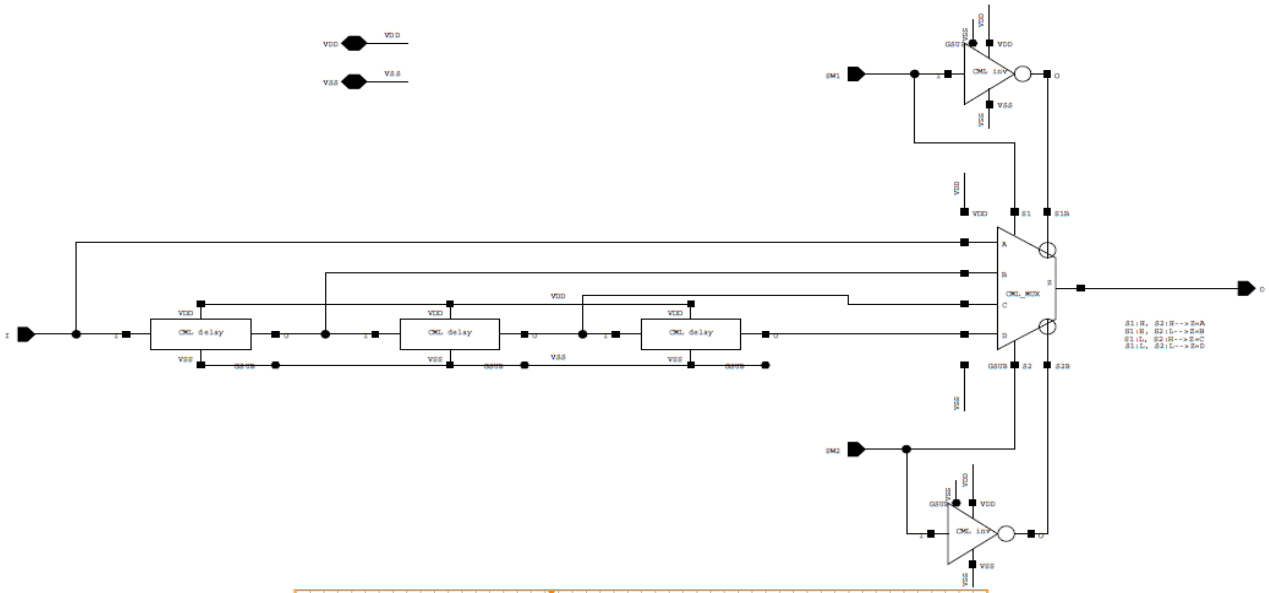


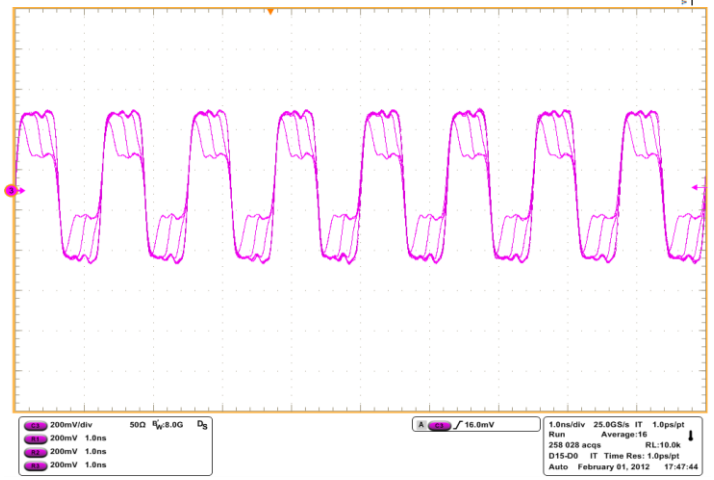
Delay Settings

Setting SW[1:0]	Pulse Width [ps]
11	130
01	300
10	470
00	615

➔ ~170 ps per delay buffer



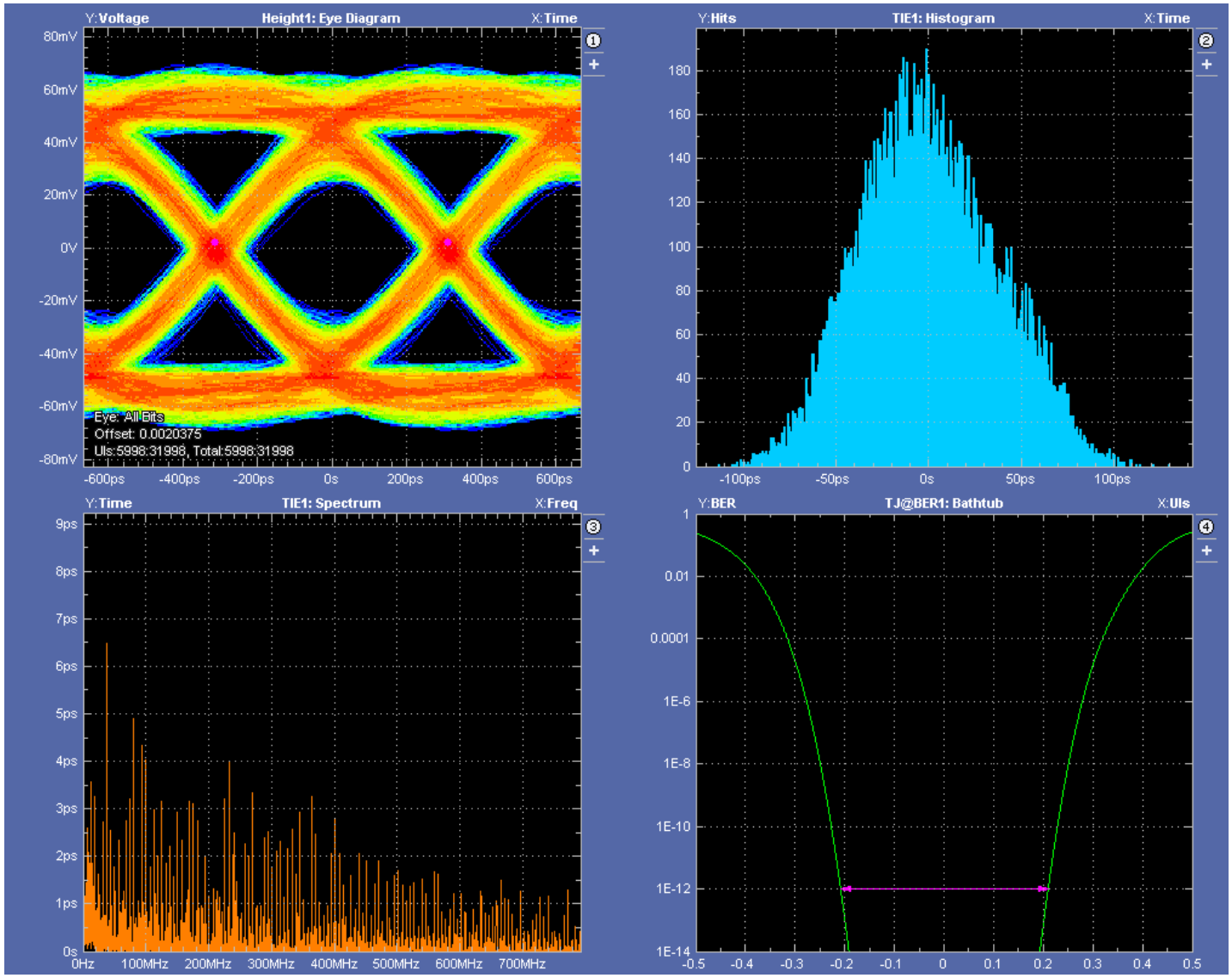




800 MHz clock, different delay settings

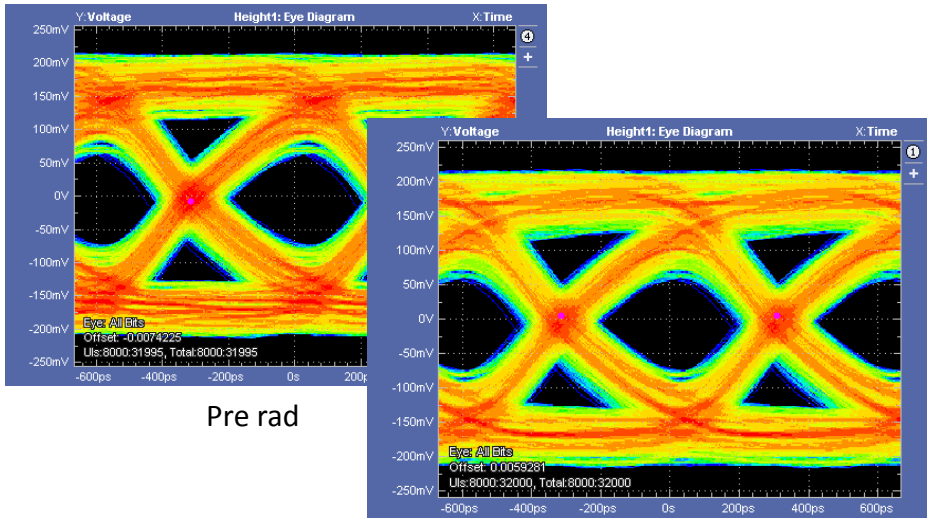
Signal Integrity Characterization

- 1.6 Gbps LFSR-8
- 30 cm kapton cable + 20m AWG26 twisted pair cable



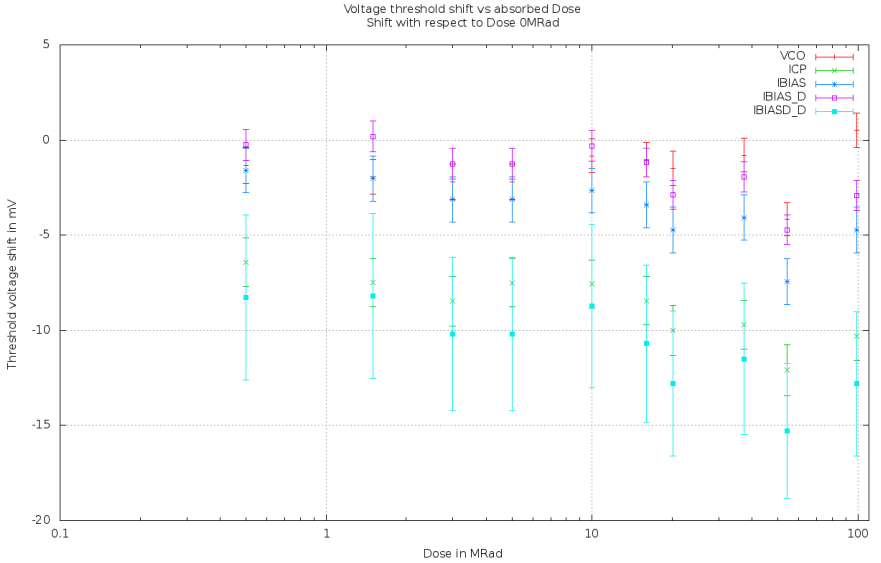
X-ray Irradiation

- TSMC 65nm TID tolerance:
  - V_{THR} shift (wide pMOS and nMOS only)
  - PLL + Gbit link performance
- Up to 100 Mrad (60keV X-ray tube, Karlsruhe)
- Dose rates: ~300 kRad/h (initial) → ~2Mrad/h (end)
- Annealing after each step: 80°C for 100 mir



Pre rad

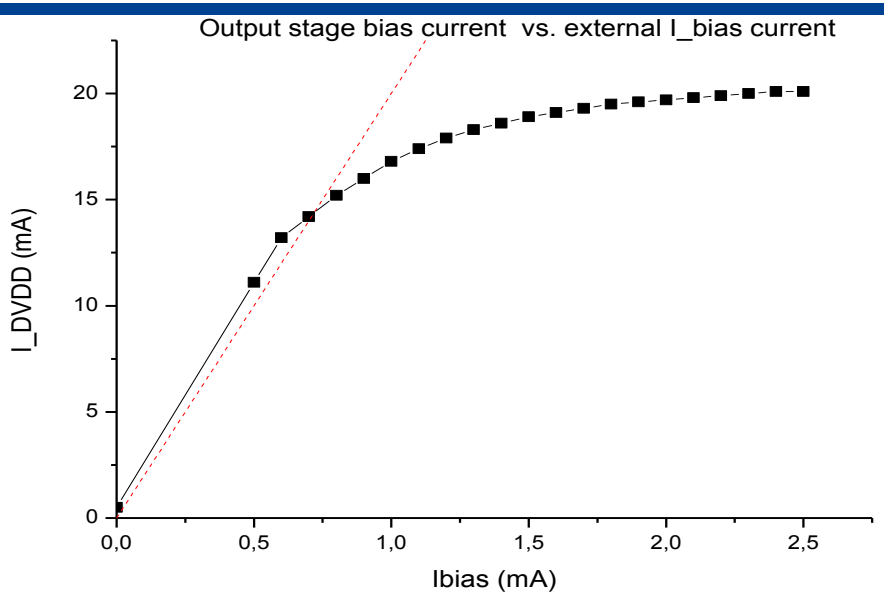
100 Mrad



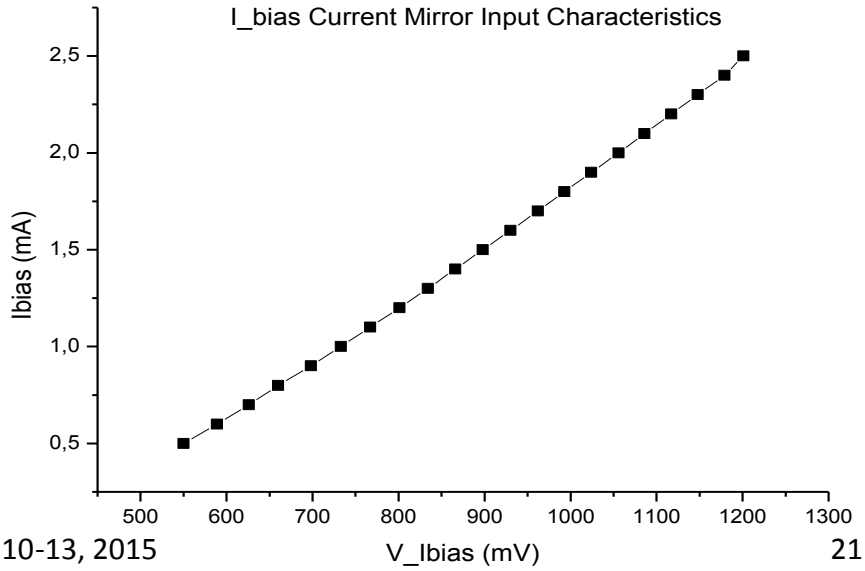
No TID induced degradiation observed up to 100 Mrad

Main Output Current Mirror

- IBIAS_DRIVER current mirror
- Design value
  IBIAS_DRIVER/Ibias = 20
- Non-linear for Ibias > 0.7mA
  ➔ M2 not saturated?
- Drive current limited to 20 mA
  → $Vout_{max}$ = 957 mV



➔ Limited by current sink (M2) or switches M0/M1 (too high on resistance or parasitic wiring resistance)



DHPT 1.0 CML Driver

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DHPT10 CML_TX
Main driver

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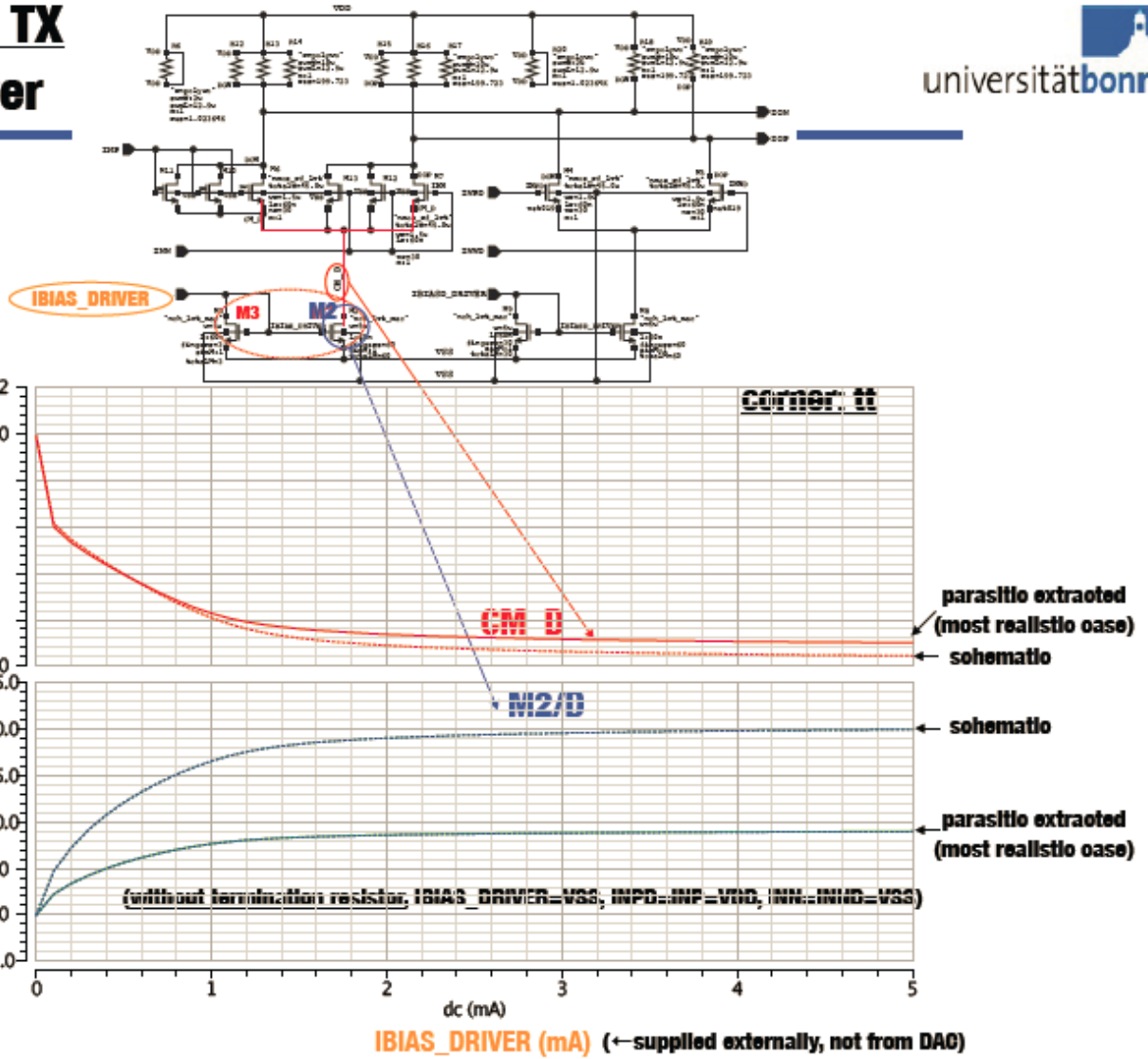

06.05.2015, T.Kishishita

Improved CML Driver for DHPT 1.1

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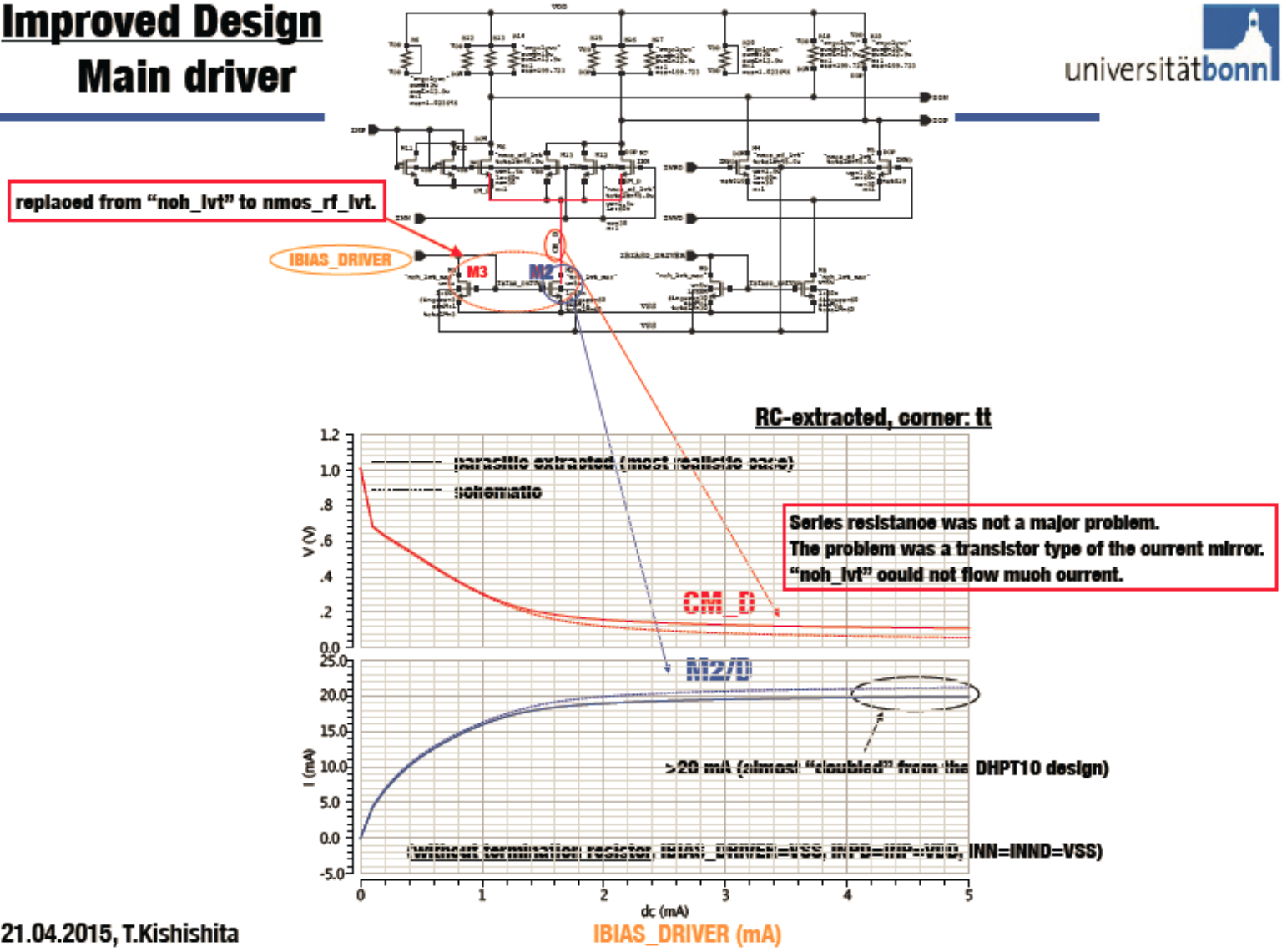
Improved Design
Main driver



21.04.2015, T.Kishishita

CML Driver Enhancements

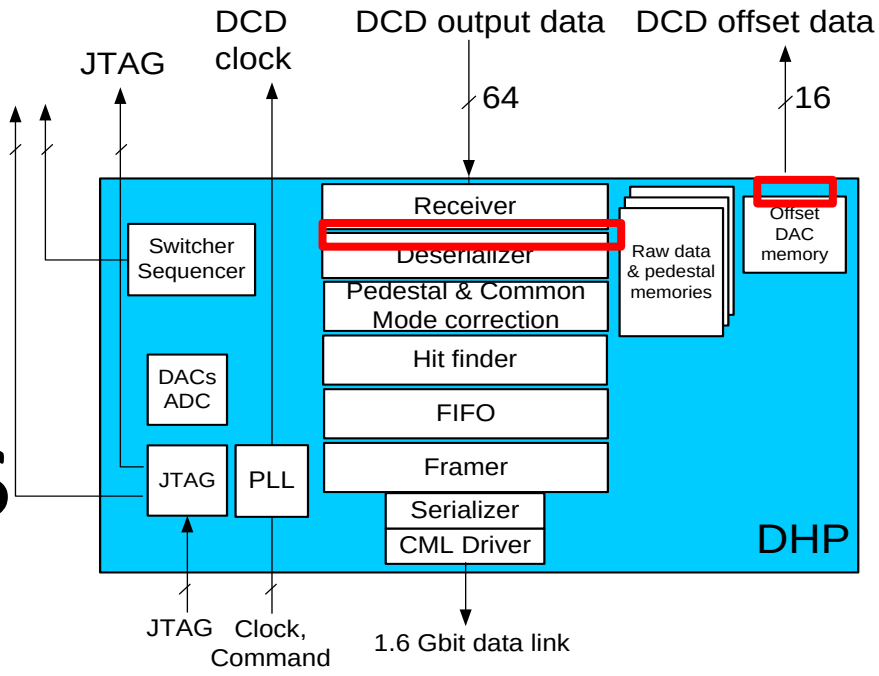
- Delay settings → Ok
  - minimum delay setting (SW[1:0]=11 → 130 ps) shows best eye diagram for long cables
  - Possible optimization: make delay steps a bit smaller (170 ps → 120 ps, 7 → 5 inverter per delay)

- Bias setting improvement
  - **Reduce parasitic resistance (wiring & vias) → done (use of RF transistor layouts)**

- **Note: there is no substantial increase of output swing to be expected due to the 1.2V supply limit**

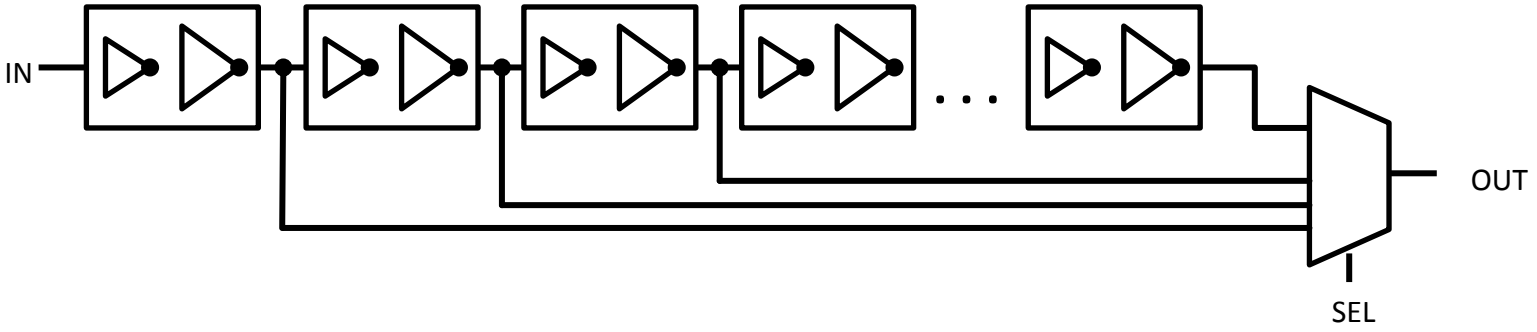
DHPT 1.0 Known Issues

DELAY ELEMENTS



Delay Element Issues

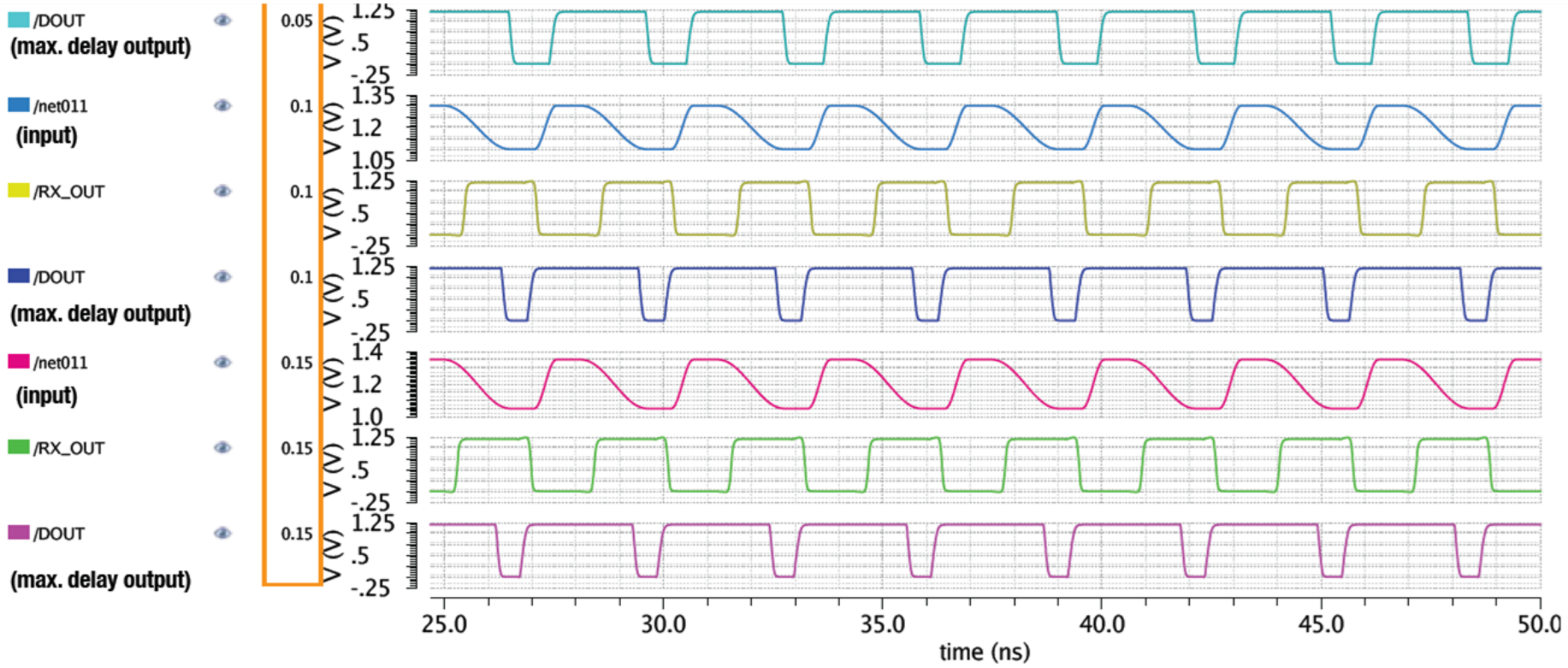
- Programmable delay lines made from std. cell delay elements (inverters)
- Inverter have usually unequal propagation delays for rising and falling edges (Asymmetry of PMOS-NMOS drive strength, process corners, W/L…)
- If all **inverters in the delay chain would be equal**, no duty cycle distortion would occur (differences in rising and falling edge delay would cancel out)
- However the **std. cell delay** elements consist of **alternating no-equal sized inverters**



➔ Duty cycle distortion increases with the number of delay elements used, i.e. the programmed delay time

Data Synchronization Issues

- Duty cycle distortion was overlooked during DHPT 1.0 sign-off
- See also measurements and scans done by Leo, Florian and Felix



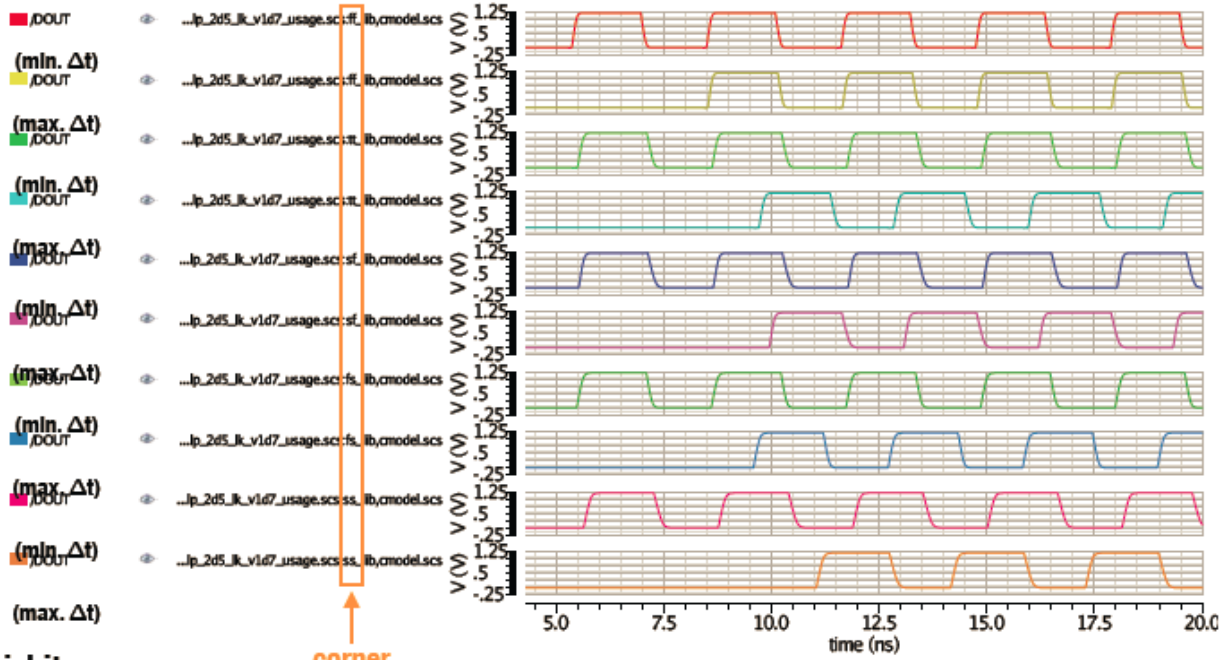
Delay Element Modification

- Custom delay elements made out of identical inverters

All corners covers 3.125 ns (←320 MHz).

Max. delay time with extracted model

	Δt	duty cycle (min. Δt)	duty cycle (max. Δt)
tt	4.20 ns	52.0%	53.3%
ff	3.15 ns	51.4%	52.2%
fs	4.10 ns	51.6%	51.8%
sf	4.43 ns	52.2%	54.9%
ss	5.42 ns	52.8%	54.9%



07.04.2015, T.Kishishita

Duty cycle degrades at most a few percent after max. delay.

Delay Element Re-design Status

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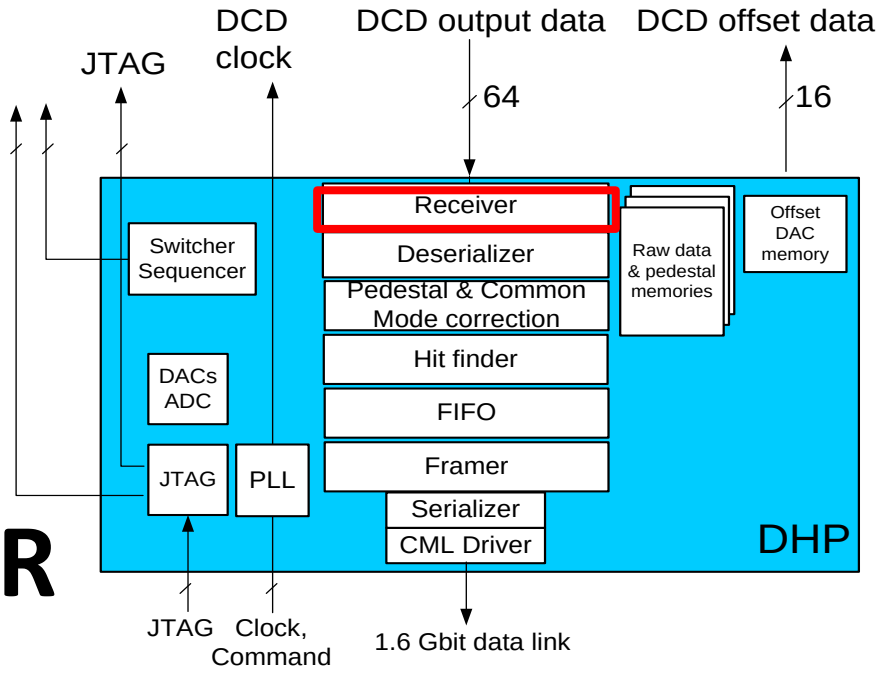
- Origin of the bug: **understood**, reproducible
- Design modification: **identified**
- Re-design on schematic level: **done**
- Re-design on layout level: work in progress
- Simulation of extracted layout (all corners): tbd

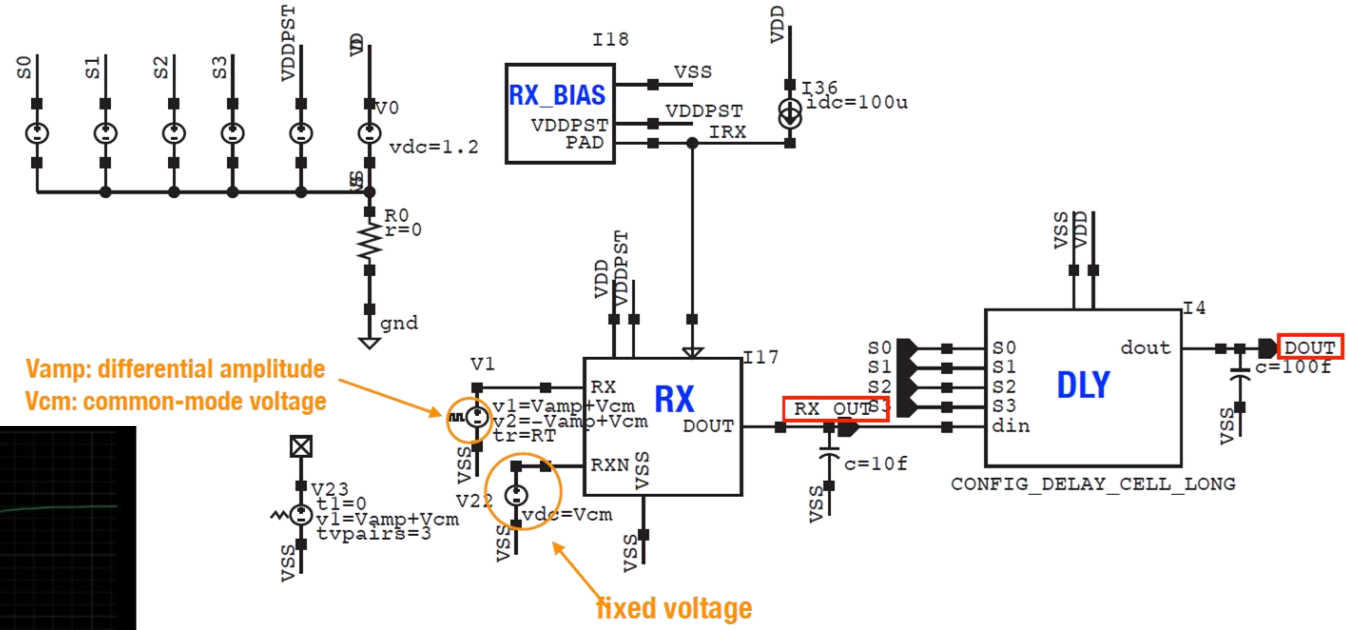
DHPT 1.0 Known Issues

DCD DATA RECEIVER

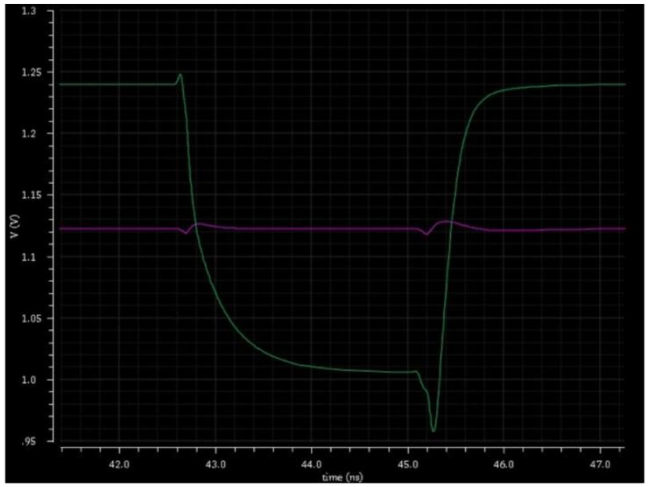


DCD Data Receiver

- Single ended DCD data receivers based on LVDS receivers → low voltage single ended signaling (LVSE)



DCD LVDS output (from Ivan)

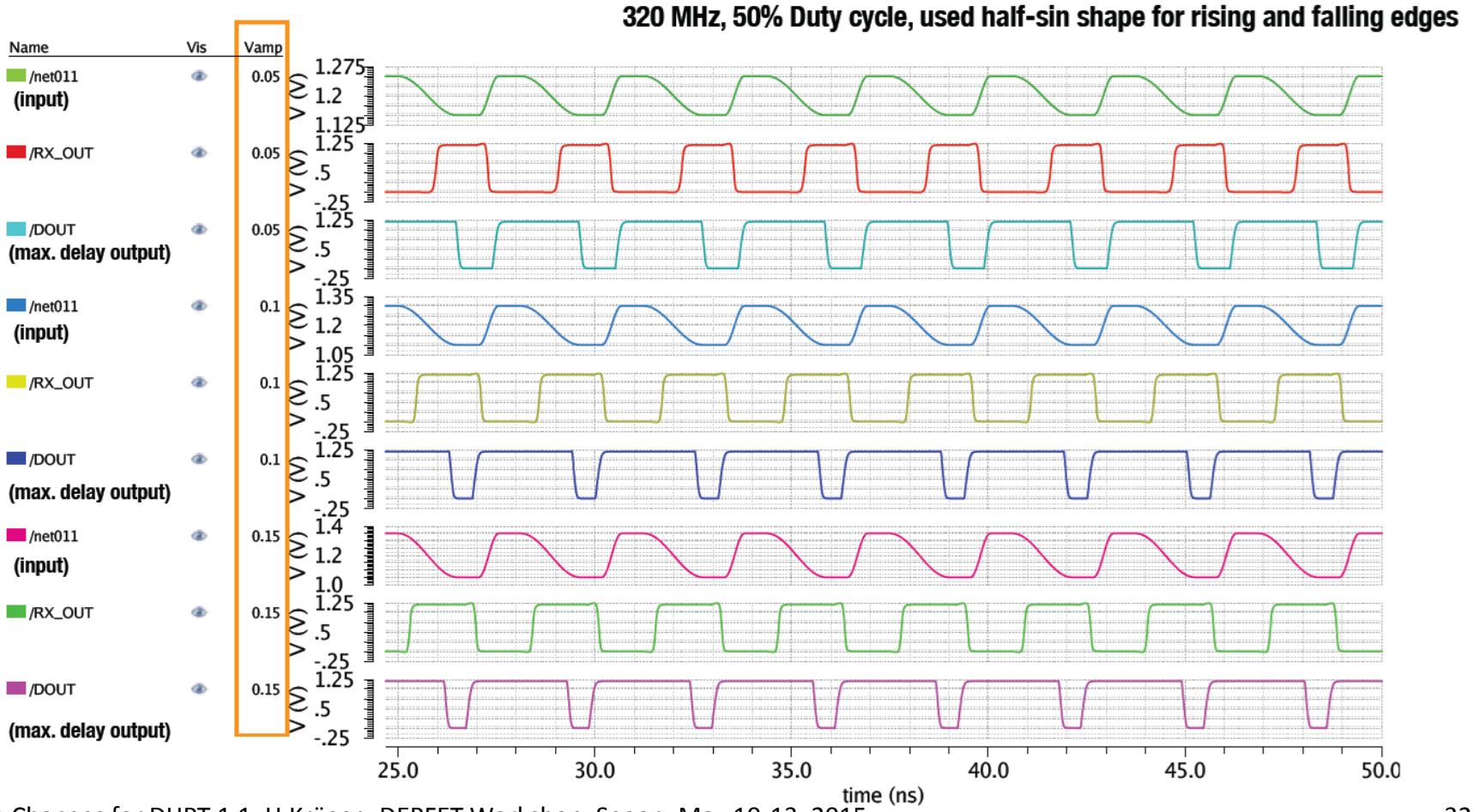


- the falling and rising edges with non-symmetrical shape
- differential amplitude of 120 mV

Duty cycle distortion

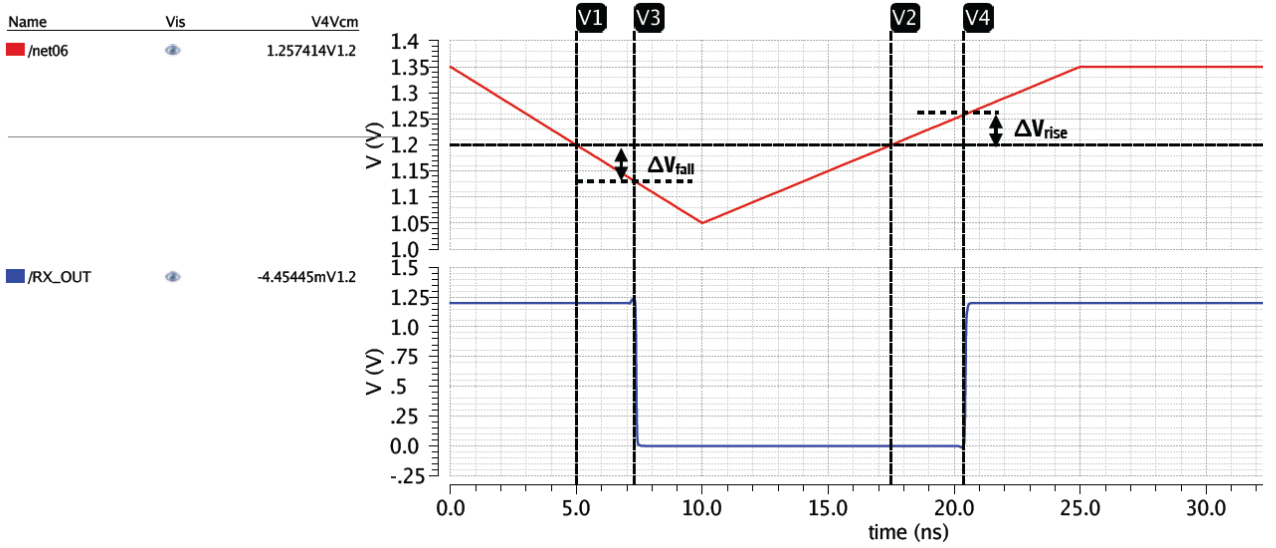
- Asymmetric rise- and fall time of the input signal (+ effect of hysteresis)
- Delay elements (see later slides)

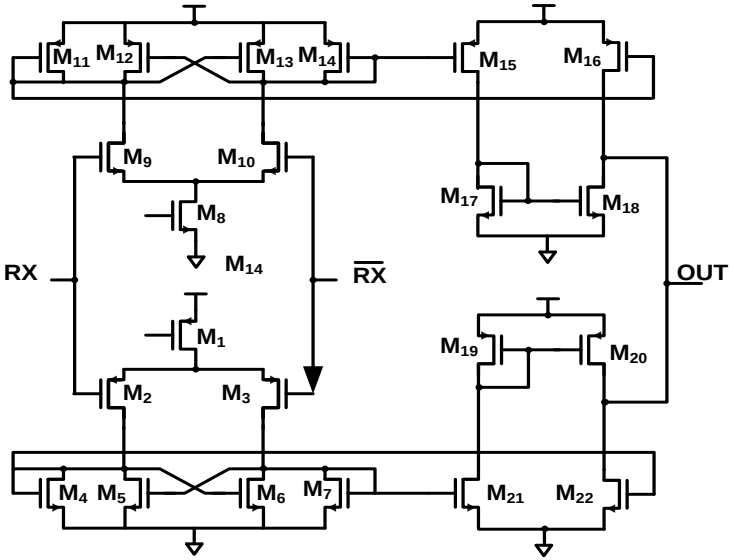
Dependence of the differential amplitude (Vamp, nominal corner)



LVDS Receiver (DHPT 1.0)

- LVDS RX with build-in hysteresis





Markers

	Vcm	V1	V2	V3	V4
x		5.0ns	17.4689ns	7.31256ns	20.3707ns
/net06					
/net06	1.2	1.2V	1.199378V	1.130623V	1.257414V
/RX_OUT					
/RX_OUT	1.2	1.2V	37.1315nV	1.22718V	-4.45445mV

	ΔVfall	ΔVrise
ff	55 mV	46 mV
fs	71 mV	57 mV
sf	68 mV	57 mV
ss	85 mV	68 mV

ΔV_{rise}=57 mV
ΔV_{fall}=70 mV (for nominal corner)

LVDS Receiver Design Modification

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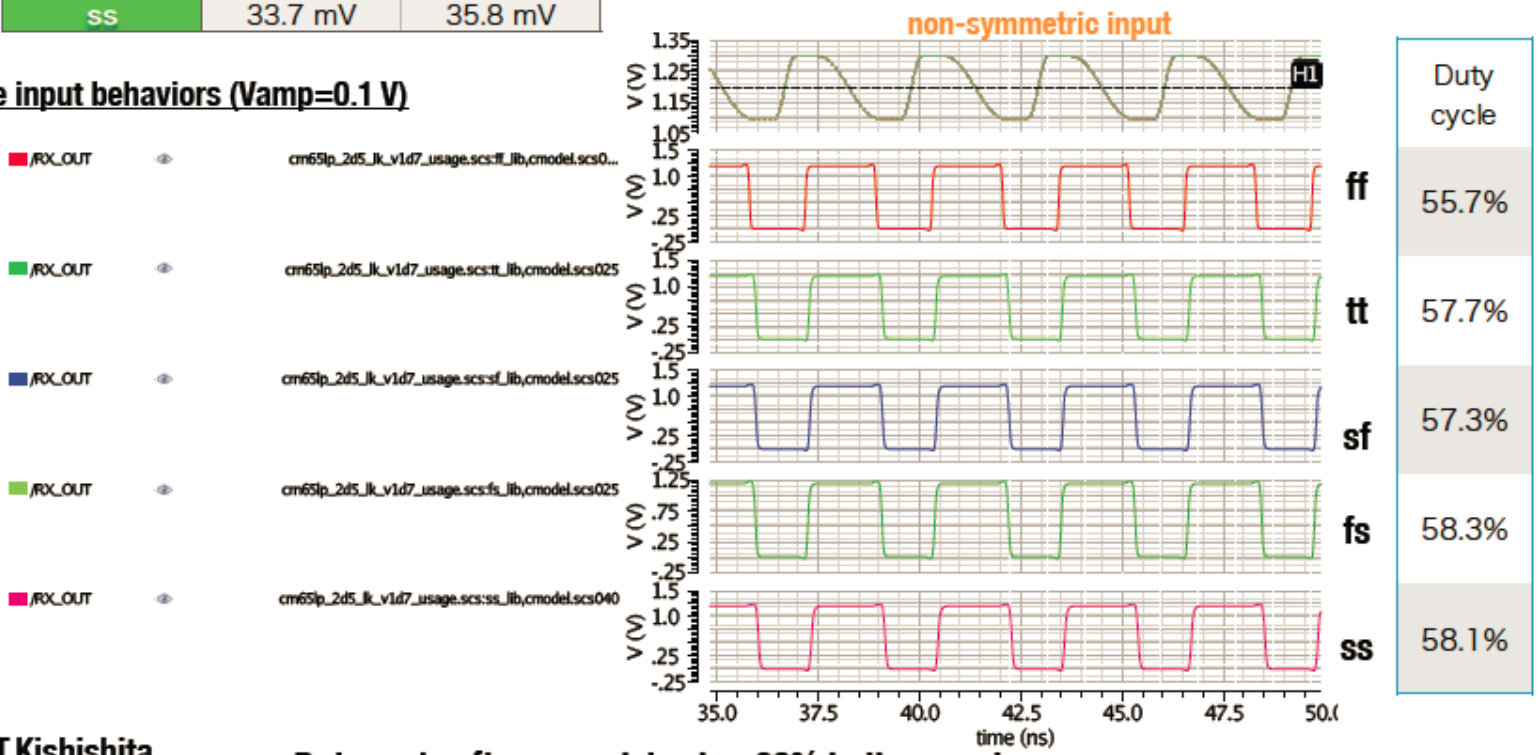
FET sizes and layout modified to reduce hysteresis (~50% of the current DHPT1.0 design).

Hysteresis values with extracted model

	ΔVfall	ΔVrise
tt	27.5 mV	34.4 mV
ff	19.8 mV	30.0 mV
fs	29.1 mV	33.4 mV
sf	26.3 mV	34.1 mV
ss	33.7 mV	35.8 mV

DCD-like input behaviors (Vamp=0.1 V)



07.04.2015, T.Kishishita

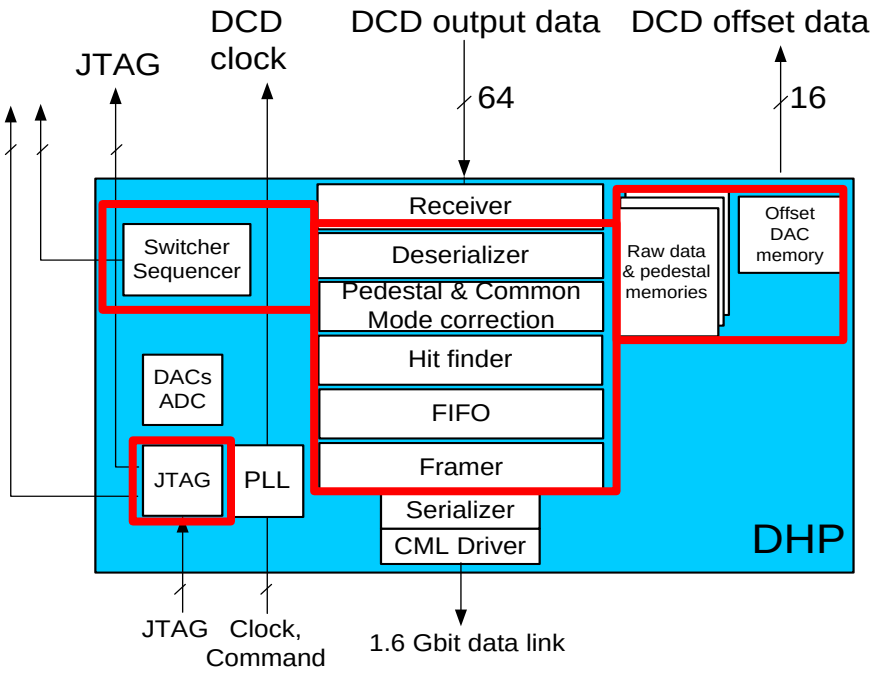
Duty cycle after max. delay is ~60% in the worst corner.

Data Receiver Re-Design Status

- Enhancement: Reduced the input hysteresis to be less sensitive to duty cycle distortion due to asymmetric rise- and fall time of the input signal → **done**

➔ **Suggested improvements of the DCD output signal**

  - Symmetric rise- and fall times
  - Higher signal amplitude



DHPT 1.0

DATA PROCESSING FUNCTIONAL VERIFICATION

Data Processing

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- So far no issues seen
- Things to look into in more detail:
  - Processing of high occupancy data
  - Gated mode
  - Power on configuration

➔ Need more system tests to assess the need of design changes

Data processing enhancements

➔ If not absolutely needed we would like to avoid the process of re-synthesizing the design (lot of work!!!)

What is really needed (no “nice to have” features)?

- Include Chip ID (JTAG programmable) in data header (needed?)
- Modifications for Gated Mode ?
- What else?

DHPT (System) Tests to be done

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- DHPT offsets → DCD
- DCD/DHPT (data, offset and JTAG) communication after TID damage
- High occupancy data processing
- Gated mode
- Triggering
- Raw data transfer
- JTAG timing (next DCD should follow the industrial standard wrt clock edges)
- SEU x-section for realistic neutron energy spectrum (calculate from 24 GeV proton data or re-measure)
- Power-up configuration Ok?
- …

Summary & Outlook

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- Bugs / Enhancements of the full custom blocks
  - Serializer bug → fixed ✓
  - CML driver enhancement -> done ✓
  - Delay element issue → fixed, layout work in progress (✓)
  - Data reciever robustness → fixed, layout work in progress (✓)
- Digital data processing enhancements
  - Not foreseen (yet)
- Sytem test, system test, system tests!
- Final Design Review (including DCDB and Switcher): 15/16.7.2015
- DHPT 1.1 submission in August 2015 ➔ chips available for tests around Dec. 2015

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BACKUP

DHPT 1.1 Production

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- Submission:
  - ~August 2015
  - Two slots per month, 12 weeks turn-around
  - Chips available by Dec 2015

- TSMC 65nm MPW submissions costs
  - 12 mm^2, one wafer (100 chips) included: 59 TUSD + 12 TUSD for bumping
  - Extra 12“ wafer (100 chips): 9 TUSD
  - Two MPW runs per month, turn-around ~12 weeks

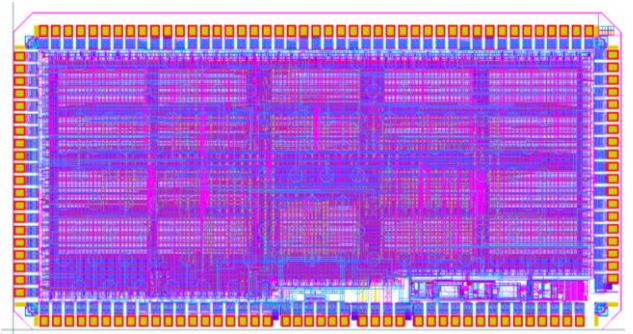
- DHPT 1.1 production
  - MPW + 9 extra wafers (1000 chips)
  - Extra wafers to be ordered after successful verification

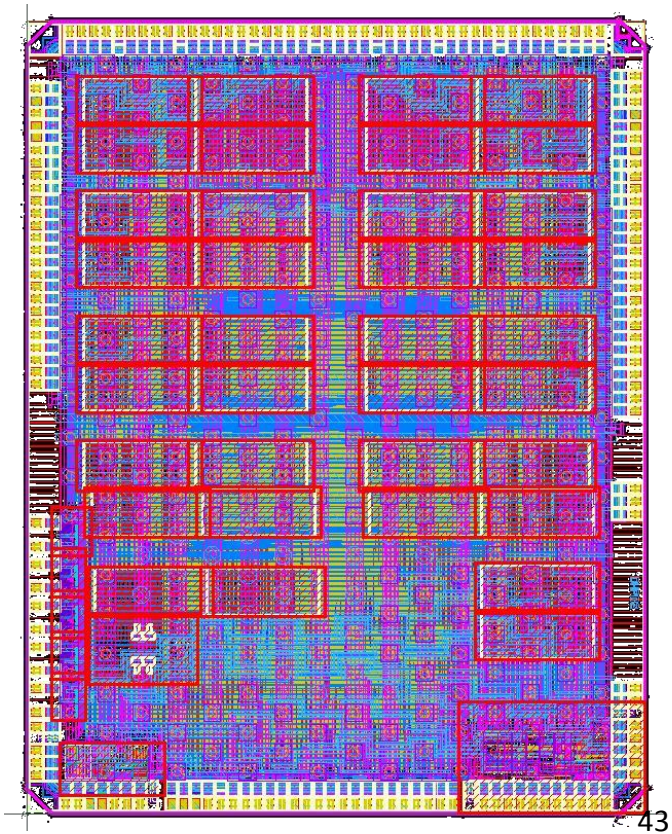
Data Handling Processor – Design History

Started with **IBM 90nm technology** in 2010

- DHP 0.1
  - Half size prototype, 2 x 4 mm^2, C4 bumps
  - Basic digital data processing
  - PLL (1.6 GHz) + High speed serial link
  - ➔ Successful verification

- DHP 0.2 (sub. mid of 2011)
  - Full size chip, 3.2 x 4.3 mm^2
  - Full data processing, added switcher sequencer and bias generators
  - Improvements in link performance (pre-emphasis), buffer size, and data format
  - ➔ Successful tests & system operation (some issues with max. speed of CMOS clock output)

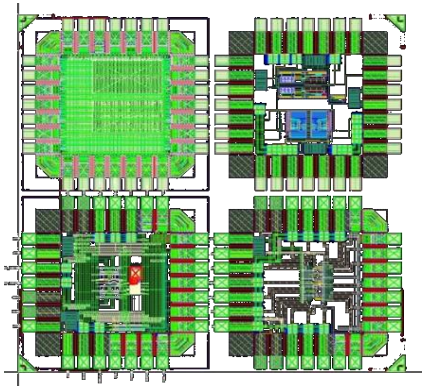




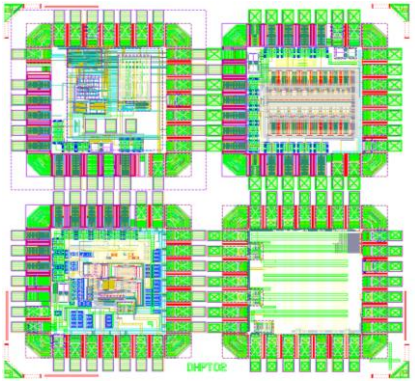
Data Handling Processor – Design History

Forced to abandon 90nm IBM process ➔ chosen **65nm TSMC**, started with small **prototype chips to verify full custom blocks** and rad. hardness performance

- DHPT 0.1 (Oct. 2011)
  - PLL (1.6 GHz)
  - High speed TX (CML driver)
  - Bias generators (U Barcelona)
  - Memory SEU test structures



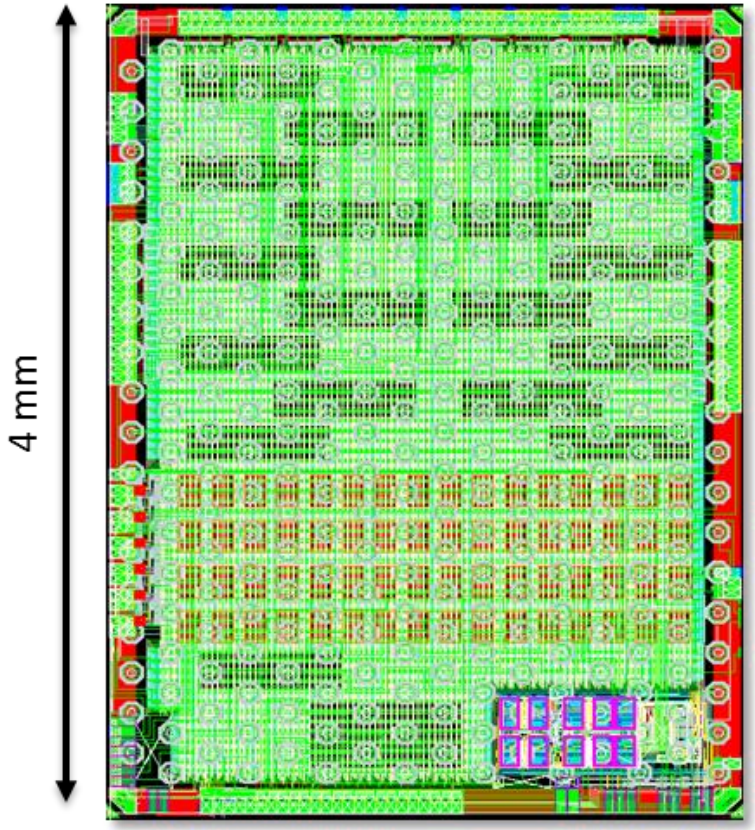
- DHPT 0.2 (June 2012)
  - LVDS RX & TX
  - Temperature sensor (U Barcelona)



Data Handling Processor – Design History

First **full size 65nm chip** submission (DHPT 1.0) after internal design review

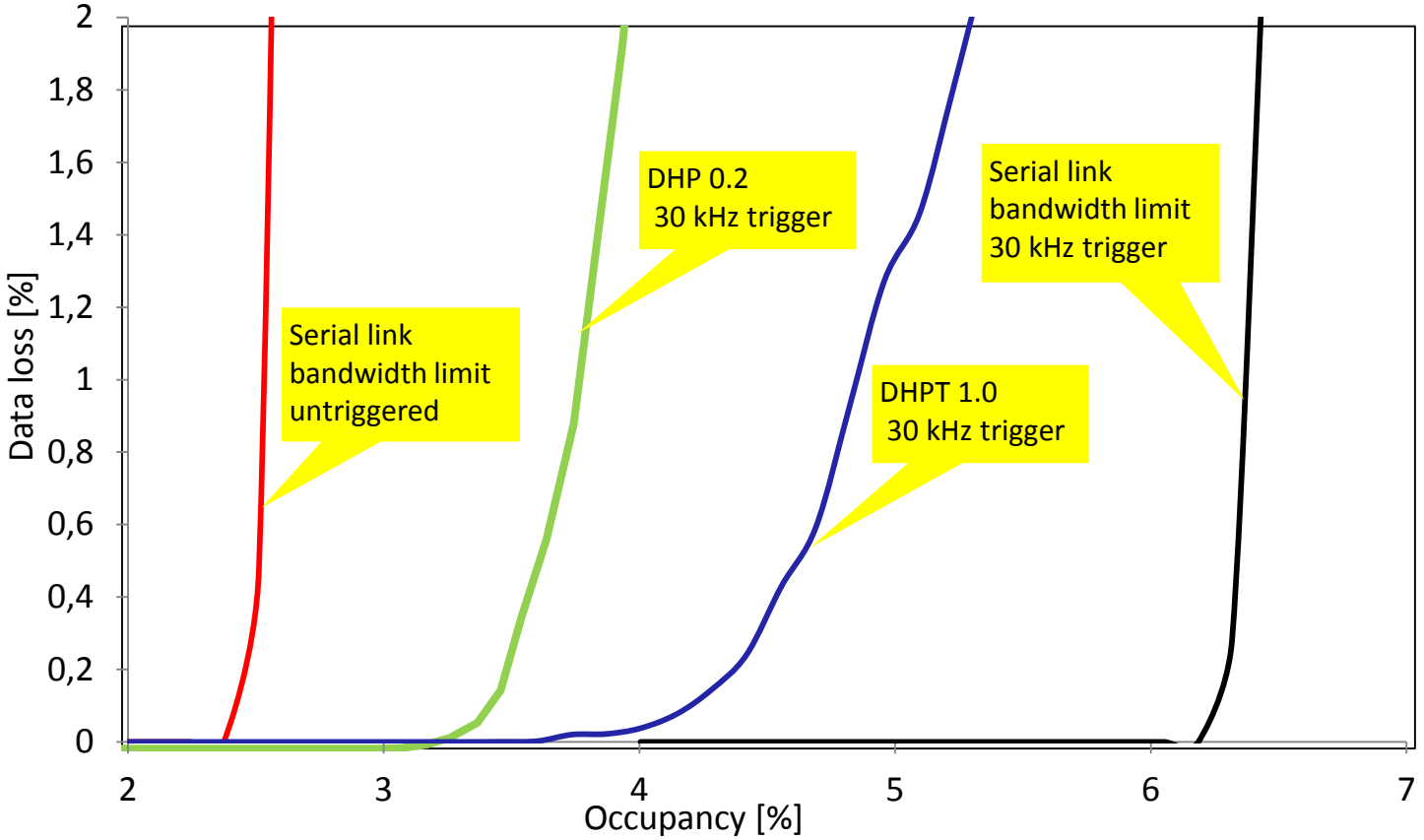
- DHPT 1.0 (Aug. 2013)
  - Full size chip
  - Includes all pre-verified full custom blocks
  - Footprint & electrical compatible to DHP 0.2
  - Improved memory & processing resources wrt. DHP 0.2



Data handling processor DHPT 1.0

Expected DHPT 1.0 Data Losses

- FIFO 1: 64 FIFOs in front of the hit finder ➔ 256 words deep (DHP 0.2 → 16)
- FIFO 2: between hit finder and serializer ➔ 4096 word deep (DHP 0.2 → 512)



DHPT 1.0

COMMAND TIMING

Notes on DHP Command Timing and Format

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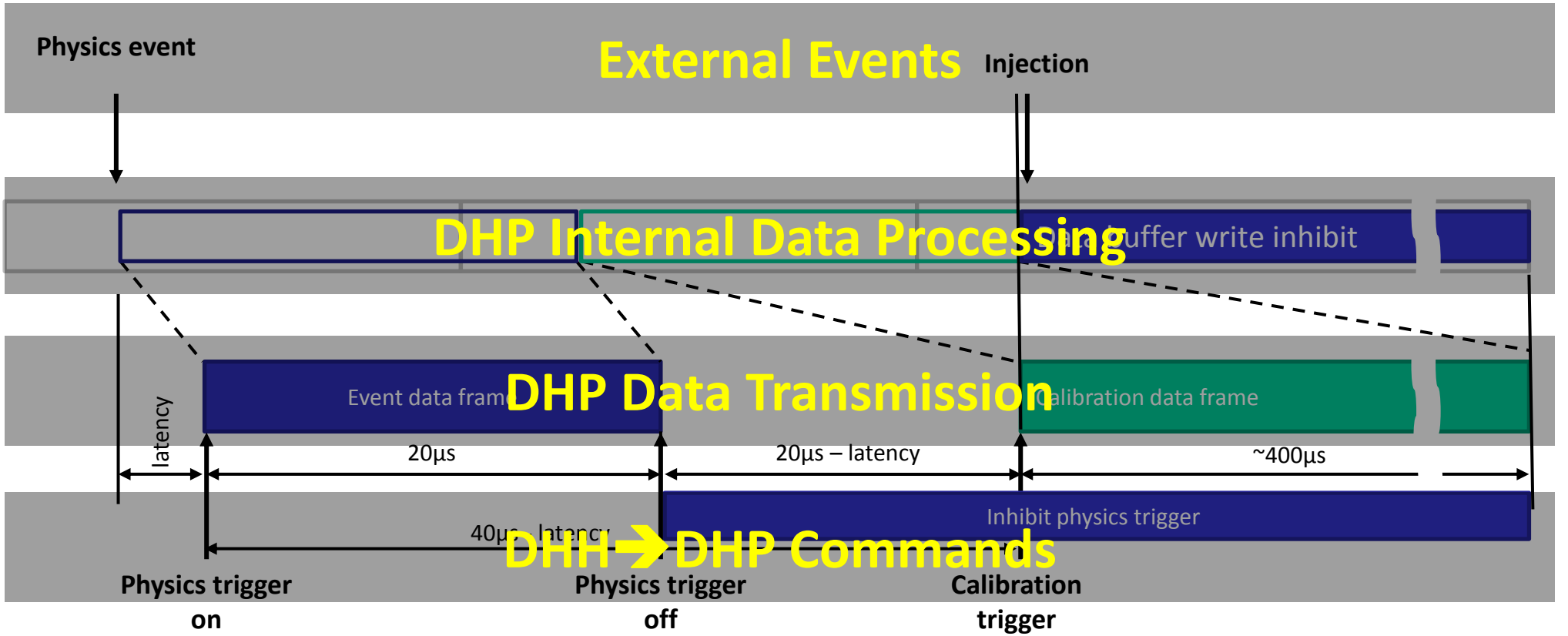
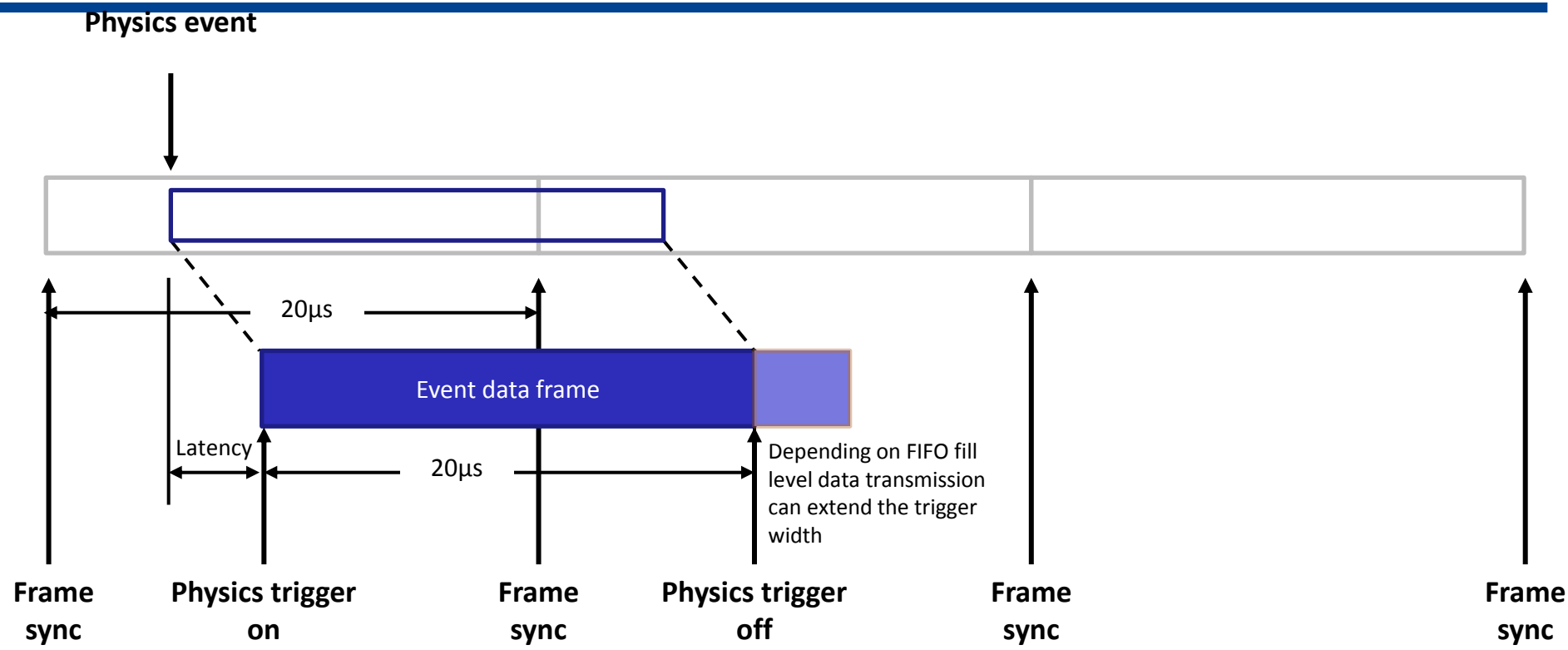
- **One control word per row period** is send synchronized to the DHP clock GCK (76.35 MHz)
- The control word (8 bits) transmits **four independent commands**: <RST|TRG|VTO|FSYNC>
  - RST: Reset, level sensitive, pulse width selects different reset modes
  - TRG: Physics trigger, level sensitive, pulse width selects raw data frame size
  - VTO: Veto (gated mode), level sensitive, selects veto sequence while on
  - FSYNC: Frame sync, edge sensitive
- The state of every command is encoded in two bits (Manchester code)
  - <10> = on
  - <01> = off
- Two additional control words are accepted (broken Manchester code)
  - <00 01 11 01> synchronization sequence, **should be used as IDLE**
  - <11 10 00 FSYNC> CALTRG (mem_dump): calibration data trigger, edge sensitive, allows simultaneous FSYNC command transmission
- The command latency in the DHP core is in the order of a few GCK cycles

Explanation of the Timing Diagrams

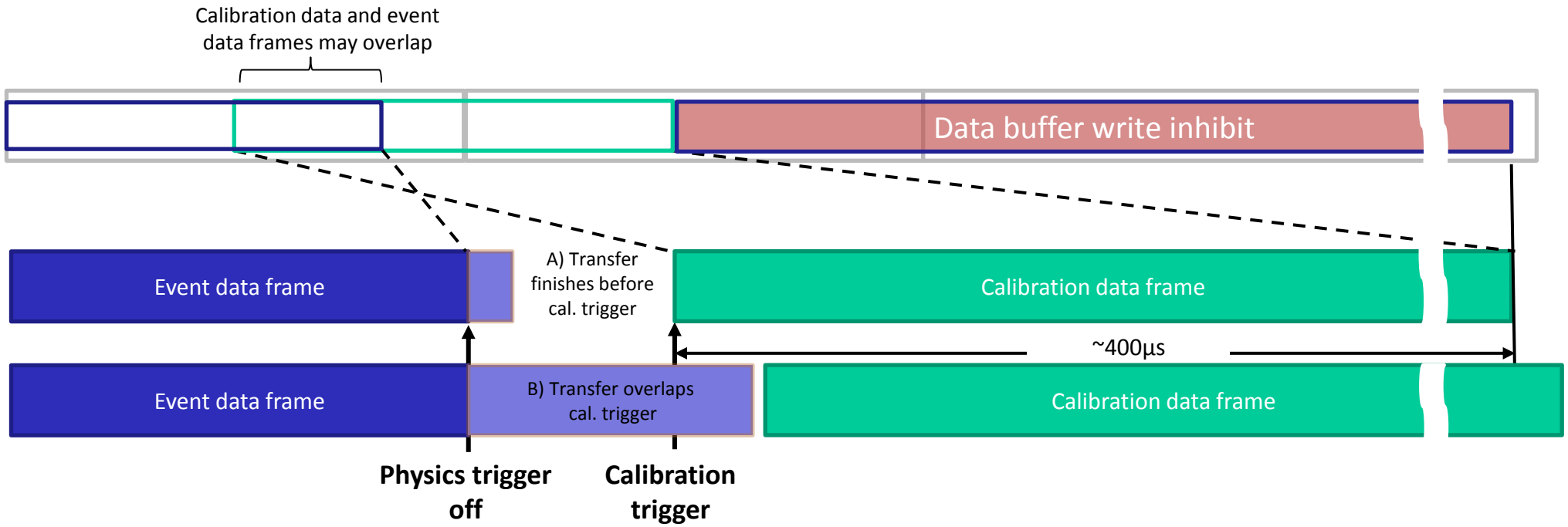


DHP timing for triggered data taking



- The transmitted *Event data frame* starts with hits from [row_m, raw data $frame_n$] and ends with [row_{m-1}, raw data $frame_{n+1}$]
- The row index m is a function of the phase between *trigger* and *frame sync*
- The trigger command is level sensitive and its width selects the size of the raw data frame to be processed
- The default width is 1536 GCK cycles (8 GCK cycles/row · 192 rows/frame)

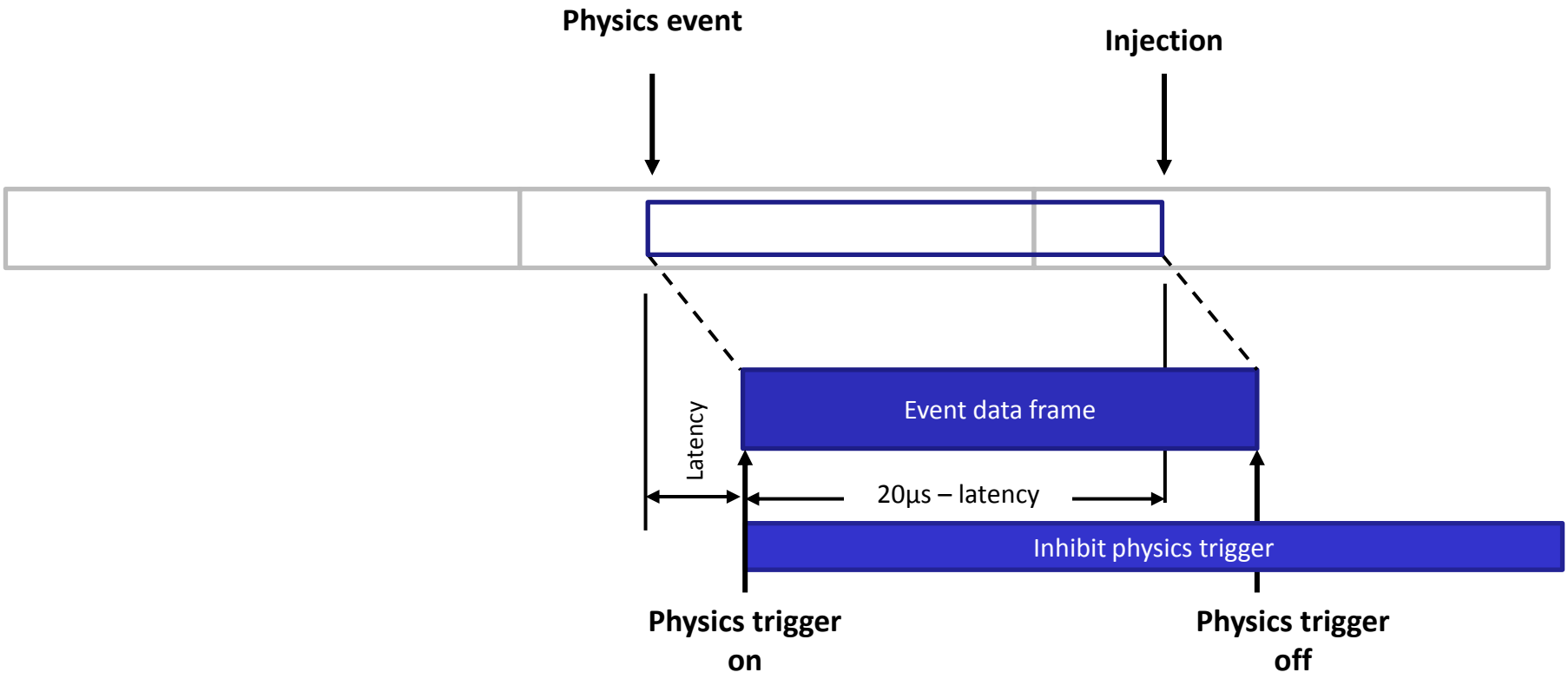
DHP timing for calibration data taking



- The calibration trigger can be send any time within a frame period
- If the previous event data transmission is not yet finished (case B), the calibration data transmission will be put on hold until the FIFOs are flushed. In some cases remaining event data still might be send after the calibration data frame (**not recommended**).
- The transmitted *Calibration Data Frame* is re-sorted and always starts with [row_0, raw data $frame_{n+1}$] and ends with [row_{max}, raw data $frame_n$]
- Programmable row_{max} and defines the raw data buffer size to transmit (default m= 191)

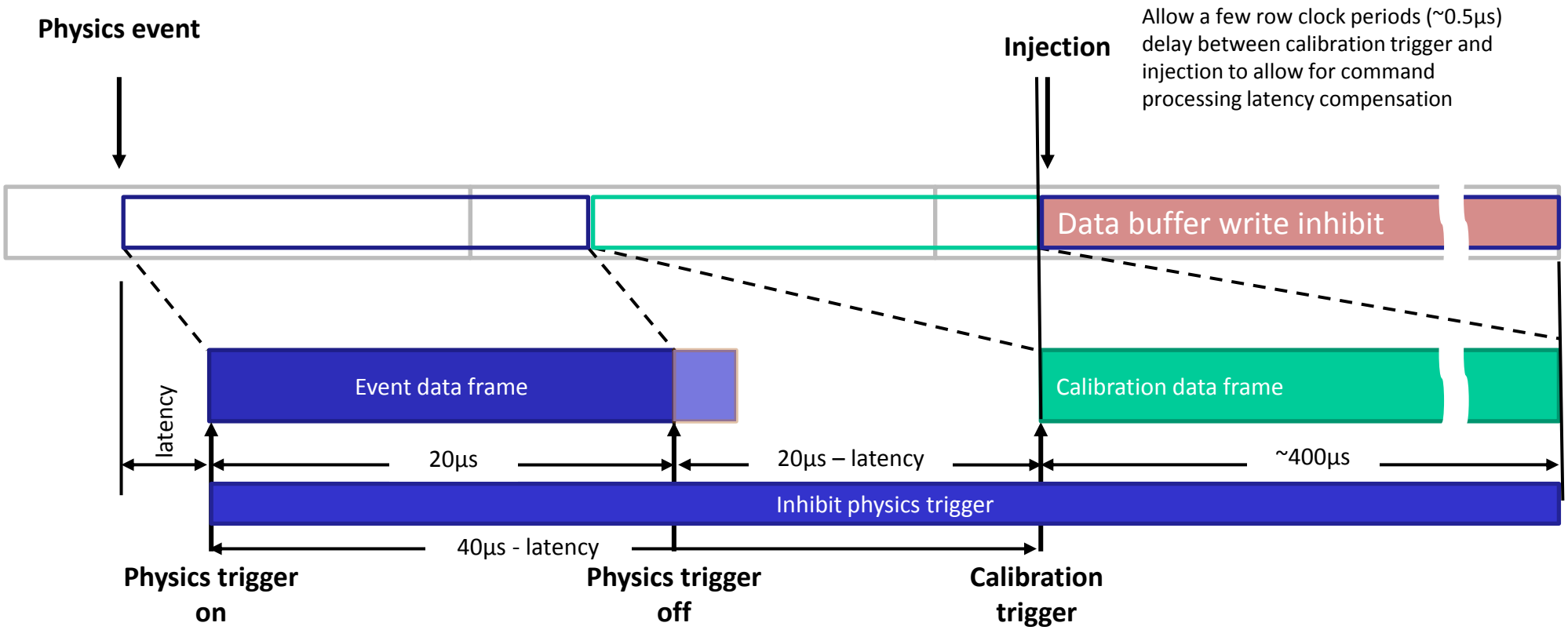
For better readability periodic *frame sync* commands are omitted in this and the following drawing s

DHP timing for injection sequence w/o calibration data taking



The suppression of physics triggers should start **20µs – latency** before the injection starts.

DHP timing for injection sequence with calibration data taking



- The suppression of physics triggers should start **40µs – latency** before the injection starts.
- Calibration trigger should only be send if the previous event data transmission has finished