

Testing of the DHE Modules

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Tests at CAD-UL

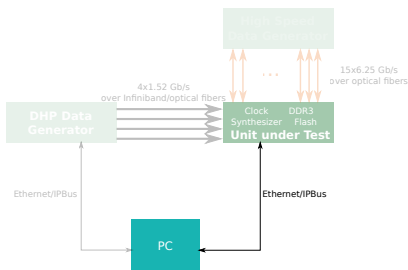
Tests at TUM

High Speed Links

Current Source



52 (Belle II) and 18 (Photon Factory) DHE/DHC modules v.3.2 are produced and are tested by the board manufacturer (CAD-UL GmbH).
Tests started on the January 28th.



Hardware Setup

- Carrier board
- Hameg 4040 four channel power supply
- A nettop PC with test software

Commissioning Problem

- Low FPGA core voltage (0.5 V instead of 1 V)
 - wrong feedback resistance for DC/DC converter



- Test environment based on python scripts and standard DHH programs
 - mostly automated, power supplies controlled by the script
 - results stored in log files and paper check lists
 - implemented return values in clock synthesizer and flash programmer:
 - **return != 0** - fail
 - should be used in PXD slow control state machines
- Time for test: 5 min / module
- Tested items:
 - **IPBus Ethernet link**: used for configuration and reading test results. **OK.**
 - **Flash programming**: return value of the program, revision check. **OK.**
 - **Clock synthesizer**: return value of the program. **OK.**
 - **DDR3 memory**: test core with error counter. **0 errors.**
 - **Power consumption**: **OK.**

Tests at CAD-UL

Tests at TUM

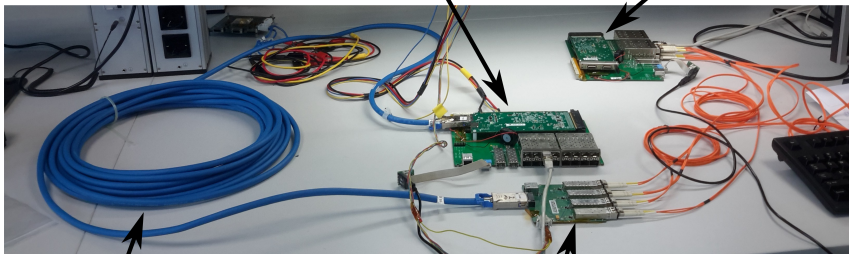
High Speed Links

Current Source



**Unit under Test
DHE v.3**

Source DHE v.1



**15 m Infiniband
Cable**

**SFP-to-Infiniband
Adapter**



- **4 DHP high speed links:**
1.52 Gb/s aurora with error counter and signal eye amplitude, BER up to $6.8 \cdot 10^{-13}$
- **Current source:** coarse test with resistive load (10.1 kOhm) installed on adapter board

Results

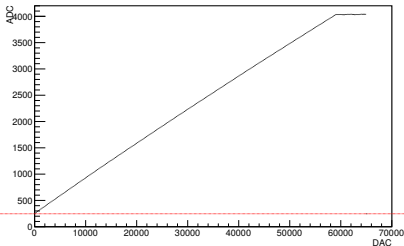
- One module has link established, while eye amplitude stays at 0
 - DFEEYEAMPLITUDE is not a good parameter to monitor
- Unstable aurora channels on some cards
 - Test repeated with IBERT (Internal Bit-Error Rate) core
- Current source problems: offset current varies between cards



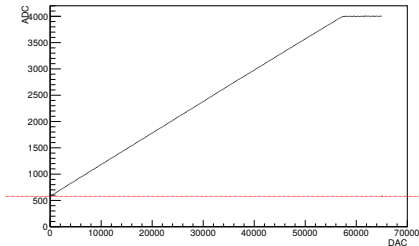
- 10 minutes test with IBERT, same parameters as with aurora links
- Worst case link: 500 errors
- Problem identified:
 - automatic calibration of the decision feedback equalizer (DFE)
 - Xilinx recommends to switch DFE calibration to the manual mode for 8b/10b signal (Answer Record #45483)
- New tests without automatic DFE calibration: all channels OK
 - previous link with 500 errors: 0 errors over 4 days ($\text{BER} < 2 \cdot 10^{-15}$)



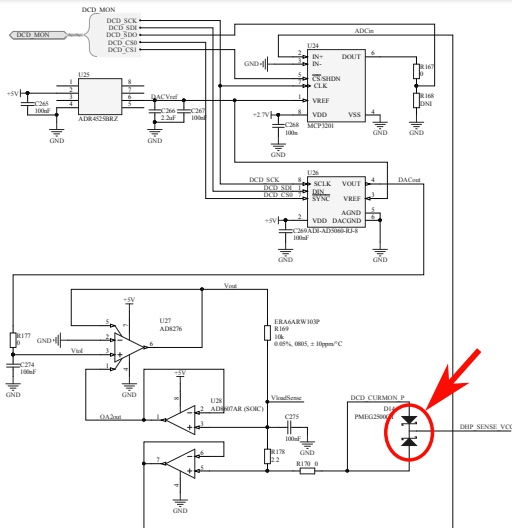
ADC DAC, Module 0021



ADC DAC, Module 0022



- Offset current differs from module to module



- High reverse current at protection diode
- Problem fixed by replacing the component with the diode with lower reverse current

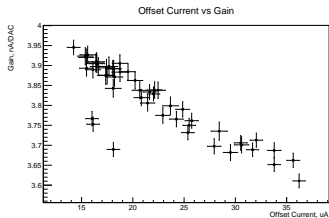


Figure : Gain fit with old diodes

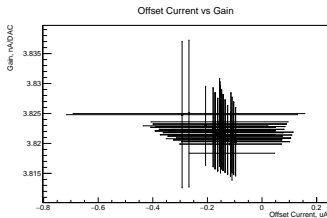


Figure : Gain fit with new diodes

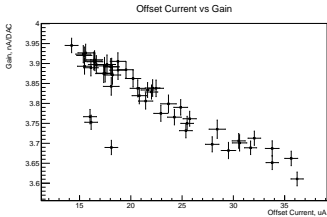


Figure : Gain fit with old diodes

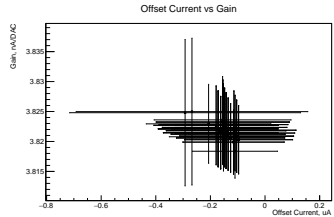
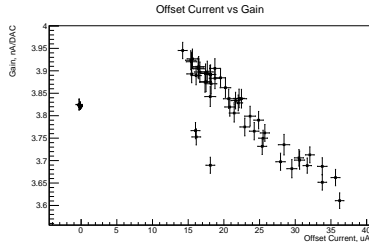


Figure : Gain fit with new diodes





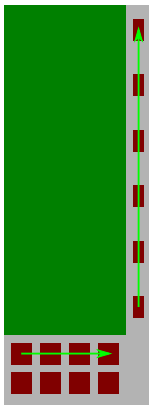
- Full test and characterization of the 52 DHE modules (Belle 2): all **good**
- Basic test of the 18 DHE modules(Photon Factory) at CAD-UL: all **good**
- Variable offset current on current sources solved by replacing protection diode with lower reverse current
- Problem with DFE on the DHPT high speed links found. No problems caused by hardware.
 - Next firmware update will address this issue.



Thank you for your attention!
Questions?

Back up slides

Outer Backward



DCD1 DCD2 DCD3 DCD4
DHP1 DHP2 DHP3 DHP4

Outer Forward

