Pilot run production: yield outcome after 2nd metal

19th International Workshop on DEPFET Detectors and Applications

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Outline

- Yield info from preliminary tests on common contacts
- Yield info from tests on 1st gate row
- System issues
- Conclusions and further developments

Preliminary tests [I]

These tests were performed on all the wafers of the pilot run production, i.e. W30, W35 and W36, for a total of 18 half ladders (12 outer and 6 inner).

What do we test and what do we learn?

- All common contacts, but the drain lines, are tested
- Detection of shorts among the sensor layers
- Estimate of ESD, bus and capacitive coupling resistors and of number of shorts in the poly lines
- First skimming of healthy modules

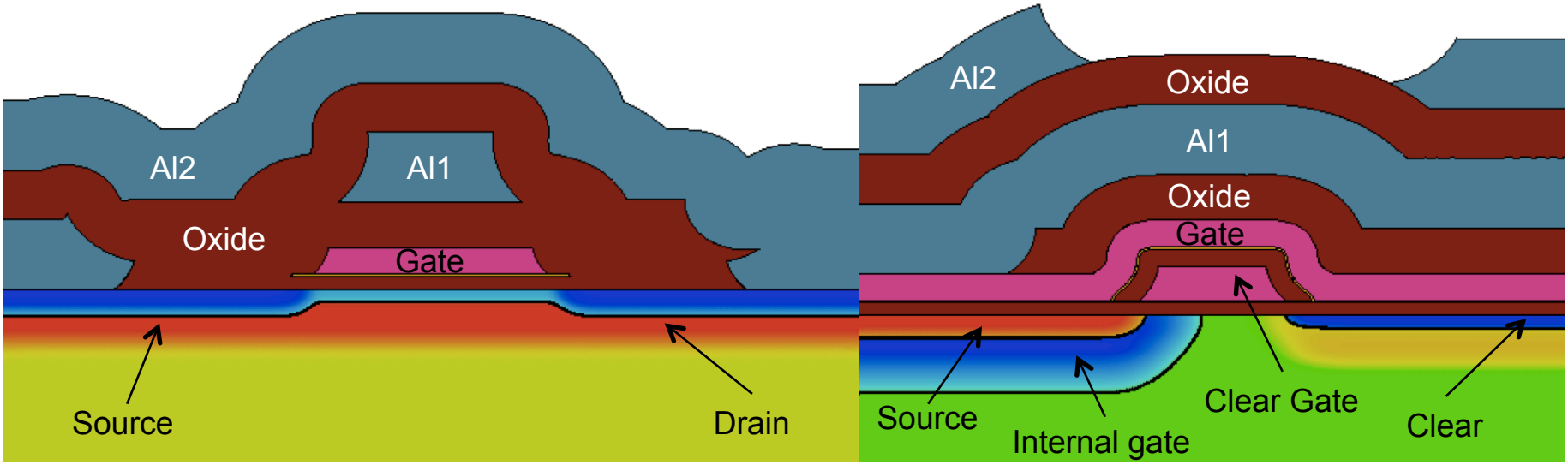
Preliminary tests [II]

Detection of shorts between n^+ (AC) and p^+ regions (S, Drains):

1. All Clear VS Source

Detection of shorts between poly1 (CG) and poly2 (AG):

1. All Gate VS Clear Gate
2. All Gates VS Source
3. Clear Gate VS Source

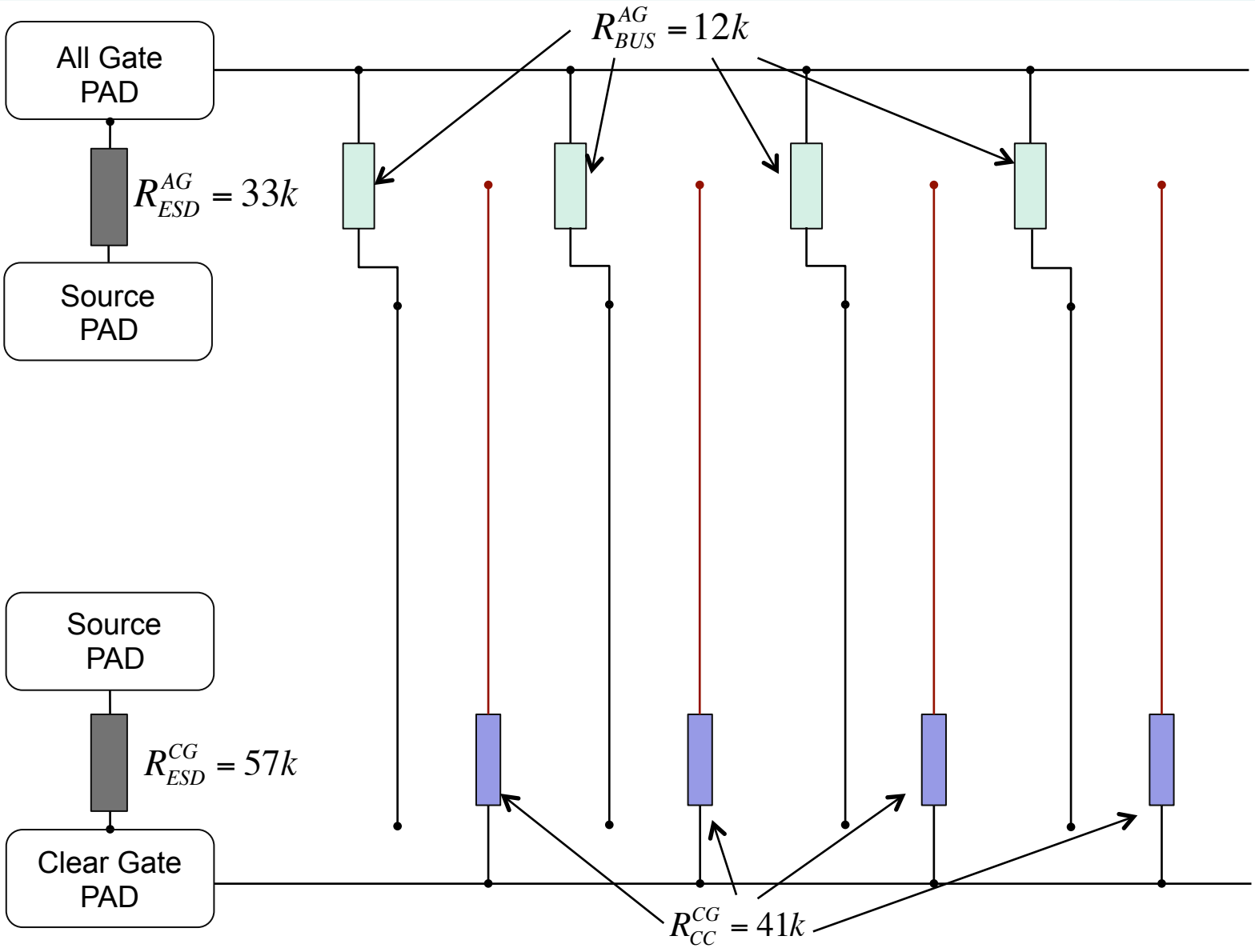


All Clear VS Source

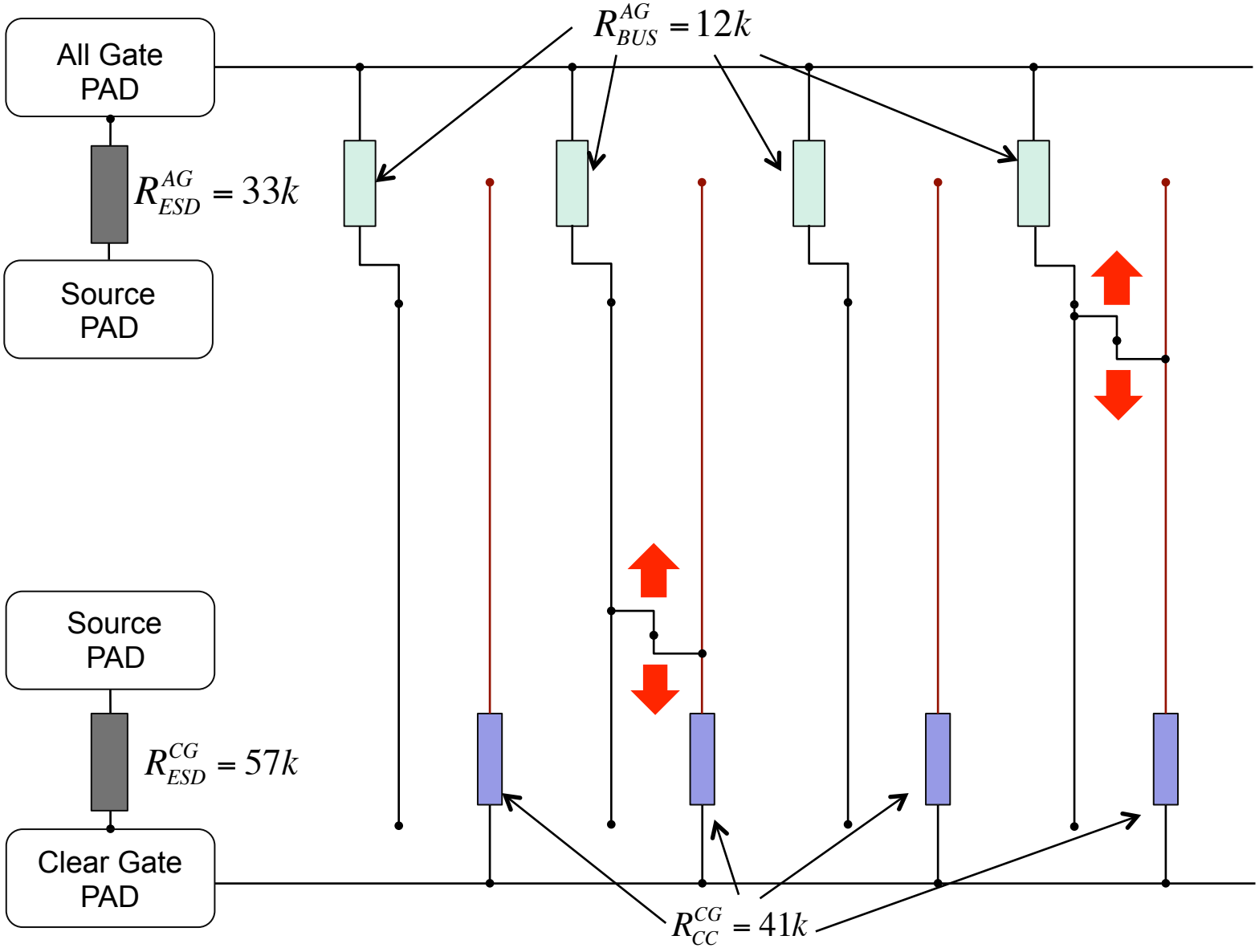
	W30	W35	W36
IF	- 40.4	- 45.7	- 42.7
OF1	- 46.7	- 47.2	- 40.2
OF2	- 43.2	- 277.0	- 40.1
OB1	- 50.4	- 46.5	$> -10^6$
OB2	-61.9	$> -10^6$	- 62.8
IB	- 53.3	$> -10^6$	- 60.5

- All Clear and Source regions tested in reverse bias.
- The entries in the table refer to the current at 10 V, in nA.
- Cells marked in red refer to not usable chips, cells in orange to chips that are not optimal, but currently working.

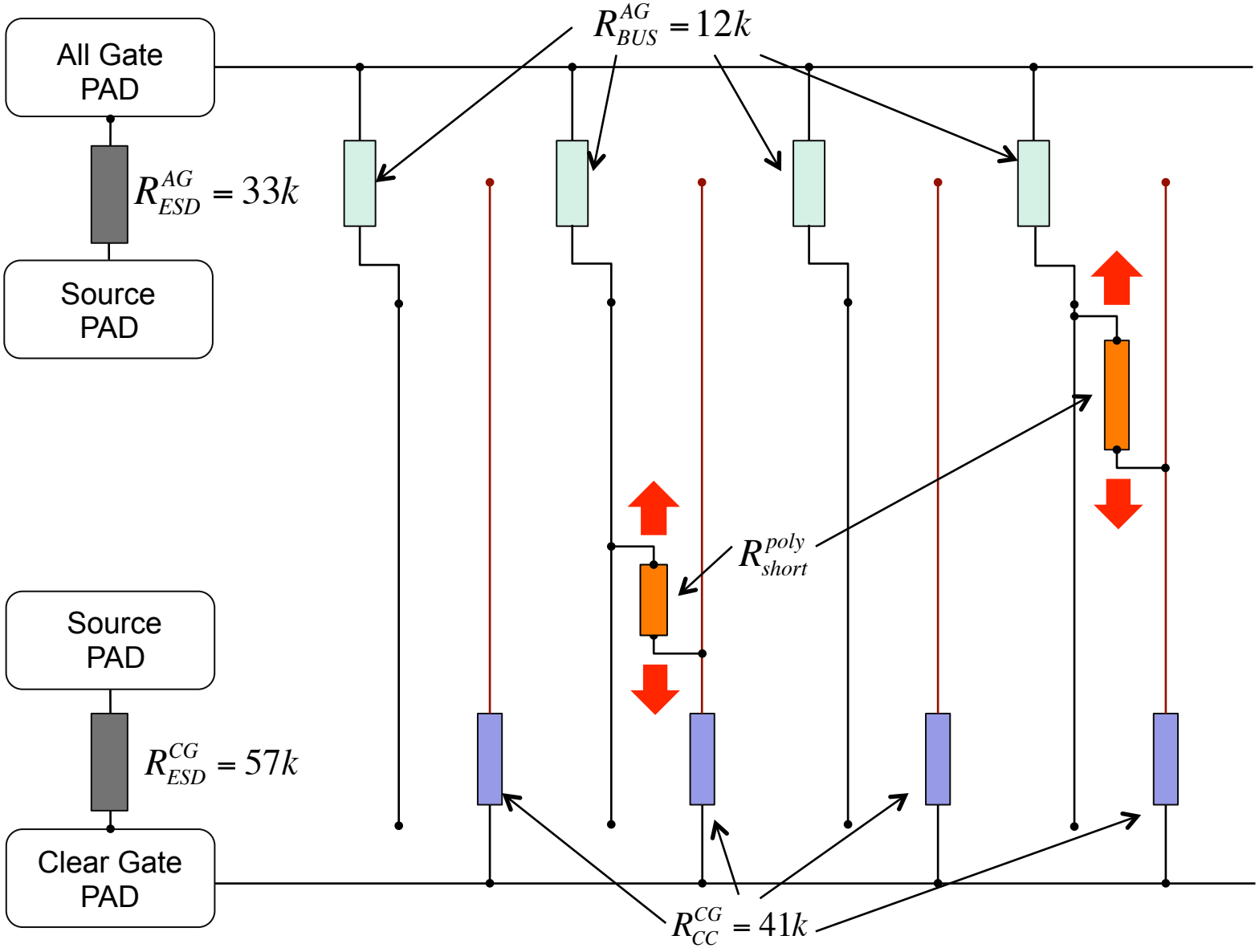
The poly1/poly2 electrical net



The poly1/poly2 electrical net



The poly1/poly2 electrical net



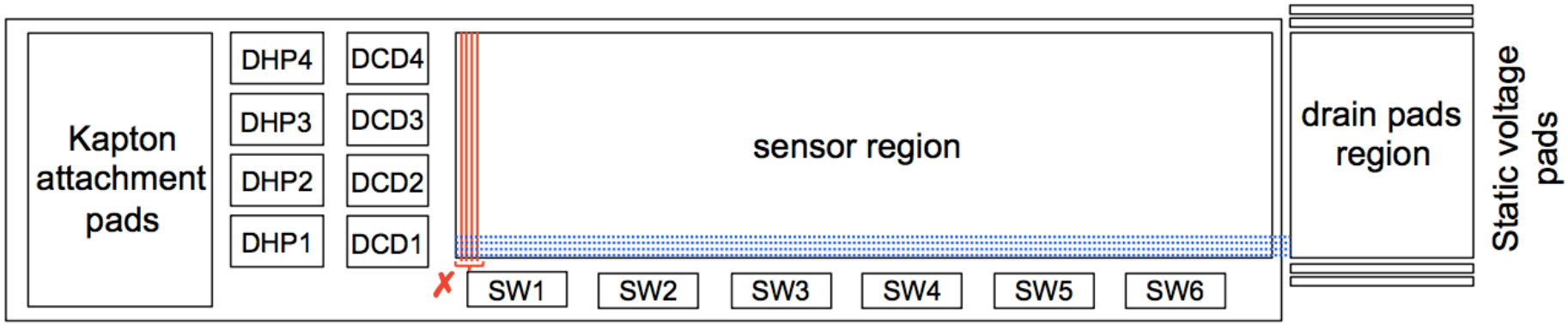
All Gate VS Clear Gate

Chip	W30		W35		W36	
	R_{net} (kΩ)	#shorts	R_{net} (kΩ)	#shorts	R_{net} (kΩ)	#shorts
IF	18.6	≥ 2	19.1	≥ 2	25.2	1/3
OF1	44.2	0	21.4	≥ 2	28.4	1/2
OF2	34.8	1	30.1	1/2	30.9	1
OB1	14.4	≥ 2	57.4	0	38.2	1
OB2	35.2	1	26.5	1/2	30.0	1/2
IB	17.1	≥ 2	56.2	0	35.1	1

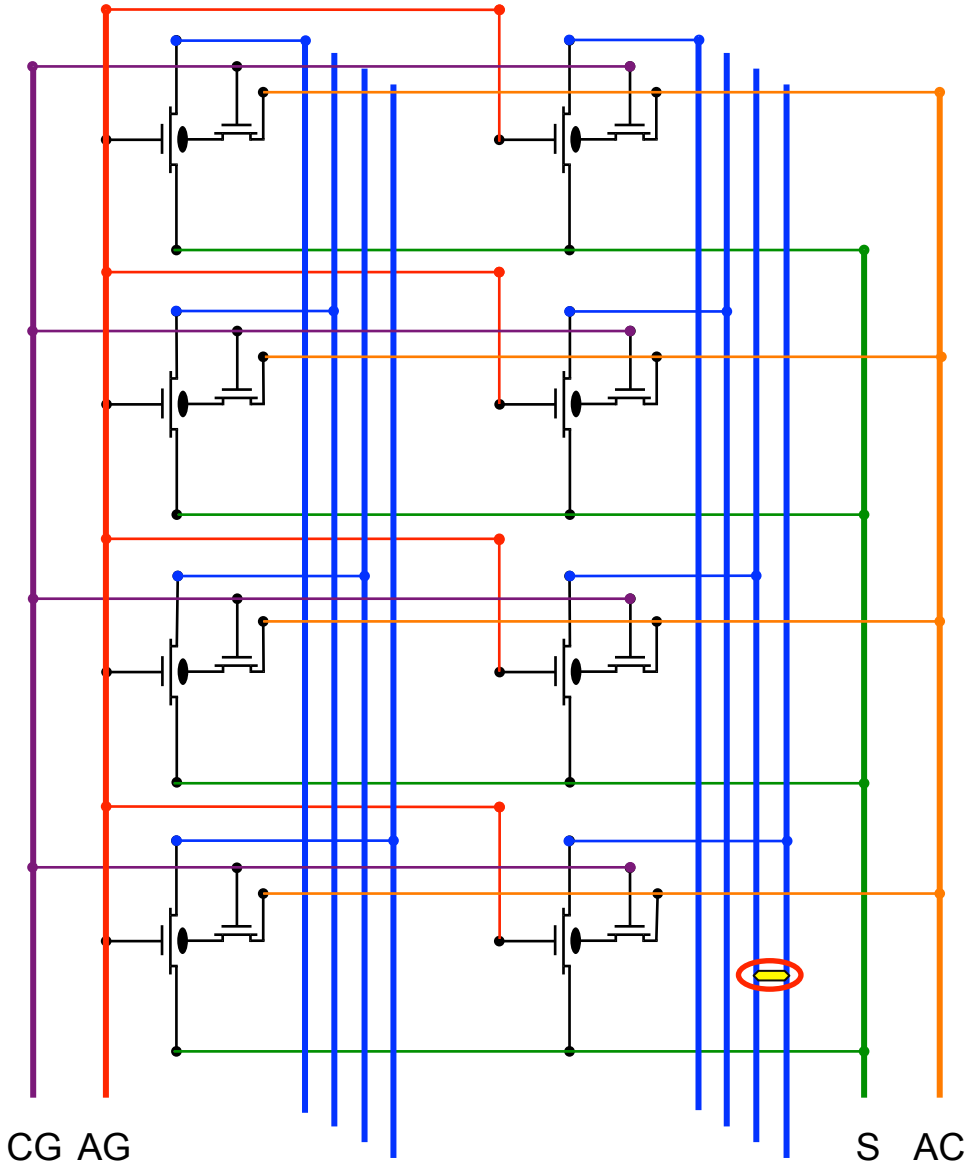
- The calculation of the number of shorts between AG and CG lines gives a precise number only in case of zero or one short.
- Two or more shorts cannot be resolved. For example, two shorts in two different pairs or one short located at the end of one CG line will give values comparable within the uncertainties.

Shorts/Opens detection on full chip [I]

- Pre-tests give a selection of healthy chips that need further characterization.
- Test of each pixel (via e.g. a transfer characteristic) not feasible due to time constraint.
- Possible to verify status of drain lines (Al2) from transfer characteristics of the transistors in the first gate.
- The test on the first 1000 DEPFET of the matrix (or the most distant from the fan out) is performed using a probe card and the switch system build into the PA200 probe station.



Shorts/Opens detection on full chip [II]



- Static voltages:
  - Clear Gate (CG) = +5 V
  - All Gates (AG) = +2 V
  - Source (S) = 0 V
  - All Clear (AC) = +15 V
- Transfer characteristics:
  - Drains = -5 V
  - Ext. Gate = 2 V ↘ -3 V
  - Measurement of I_{ds}
- The external needle allows a voltage sweep on one electric gate row (4 physical rows)
  - → Interruptions in neighbour drain lines appear like $I_{ds} \approx 0$ A.
  - → Stringers among drain lines appear like a current multiple of the single DEPFET current:

$$I_{DS}^{short} = N_{short} I_{DS}^{1}$$

Combined* yield outcome after AI2

Yield (%)			
	W30	**W35**	**W36**
IF	75.0	100.0	100.0
OF1	100.0	100.0	100.0
OF2	100.0	100.0	100.0
OB1	99.8	99.4	**0**
OB2	99.6	**0**	99.8
IB	100.0	**0**	100.0
TOT	**95.7**	**66.6**	**83.3**

Yield calculated taking into account the following equation:

$$Yield(\%) = \frac{1}{10} \cdot \left(D - D_S \right)$$

With D the total number of drain lines (1000) and D_s the number of drain lines involved in the short.

Total number of

- perfect half ladders: **10** [6 outer (all OF) and 4 inner (2 IF + 2 IB)]
- not usable chips: 3 (1 IB + 2 OB)
- chips with faults in drain lines (as from production): 4 (all OB)
- chips damaged during testing: 2 (1 IF + 1 OB)

* After merging results from pre-tests on AC and Source and transfer characteristics

Grading of the half ladders

Rainer's Yield Criteria			
	W30	**W35**	**W36**
IF	3[a]	2a[b]	2a[b]
OF1	0	2a[b]	2a[b]
OF2	2a[b]	2a[b]	2a[b]
OB1	2[c]	2b[e]	**4**[f]
OB2	2[d]	**4**[f]	2[c]
IB	2a[b]	**4**[f]	2a[b]

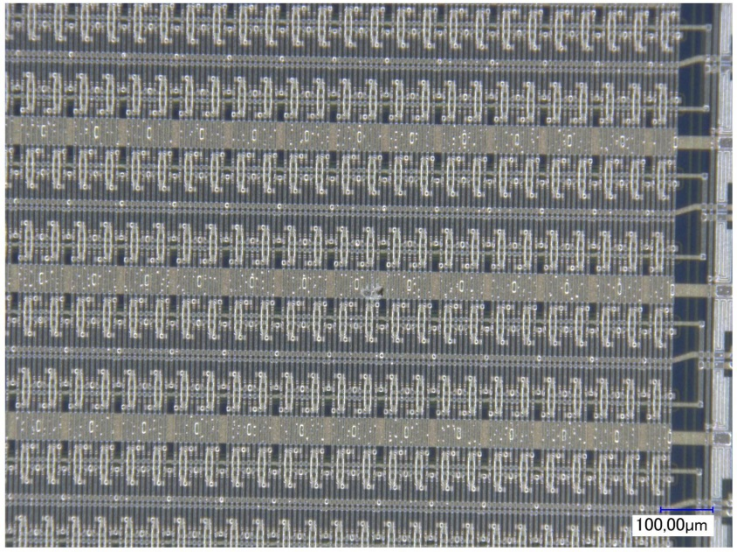
Rainer's criteria for yield calculation:

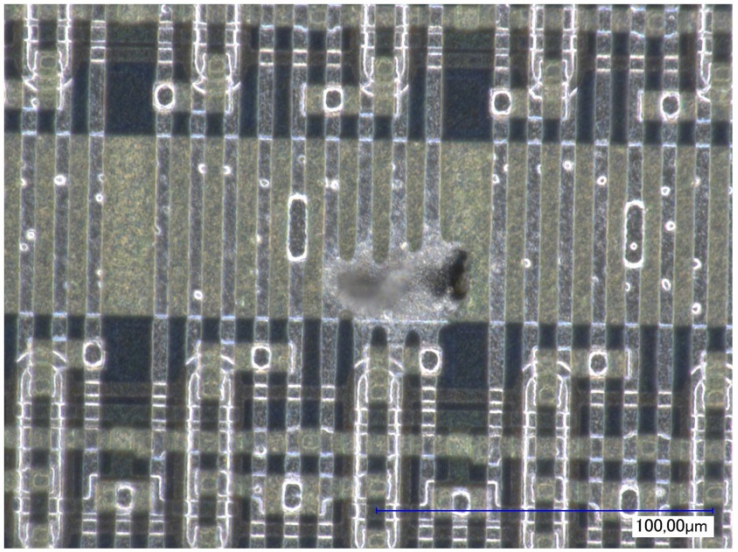
0: no faults
1: pixel level faults
2a: row level faults
2b: column* level fault
3: high impact faults
4: lethal faults
5: to be clarified

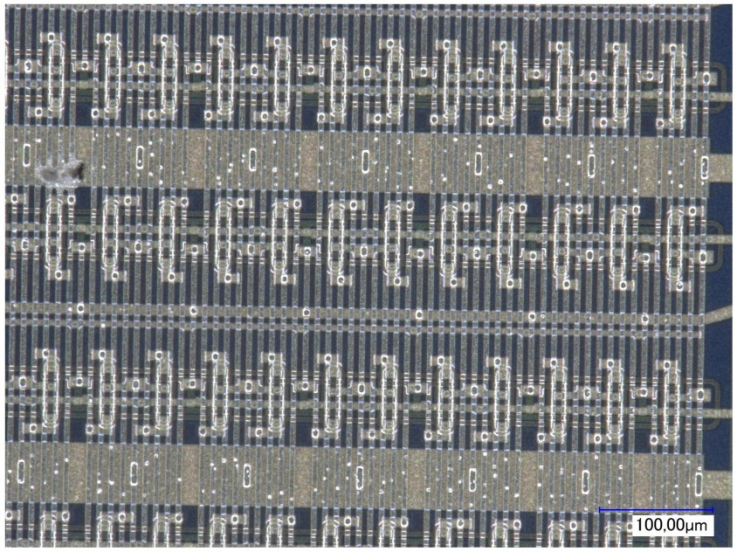
* Column level faults in Al2 can be repaired by rework (grade 2b → 0).

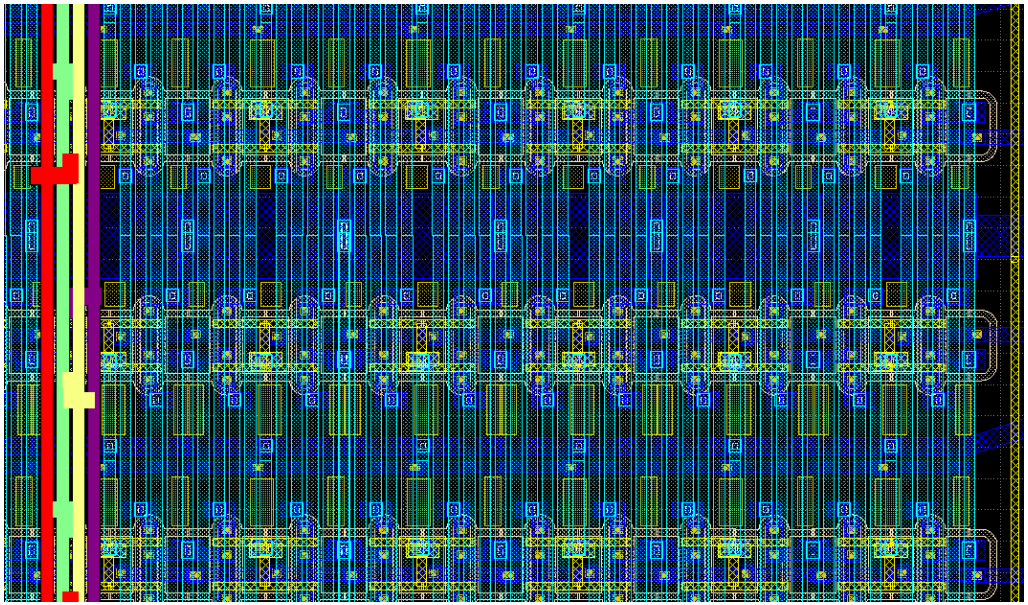
[a] Damaged by operator: DCD4 region is compromised
[b] Shorts between poly layers
[c] Non identified fault in drain lines (rework)
[d] Short in drain lines due to a production defect/dirt particle (rework)
[e] Scratched by operator: 6 drain lines in DCD1 region compromised (no rework)
[f] Short between n+/p+ regions

W30 – short in OB2

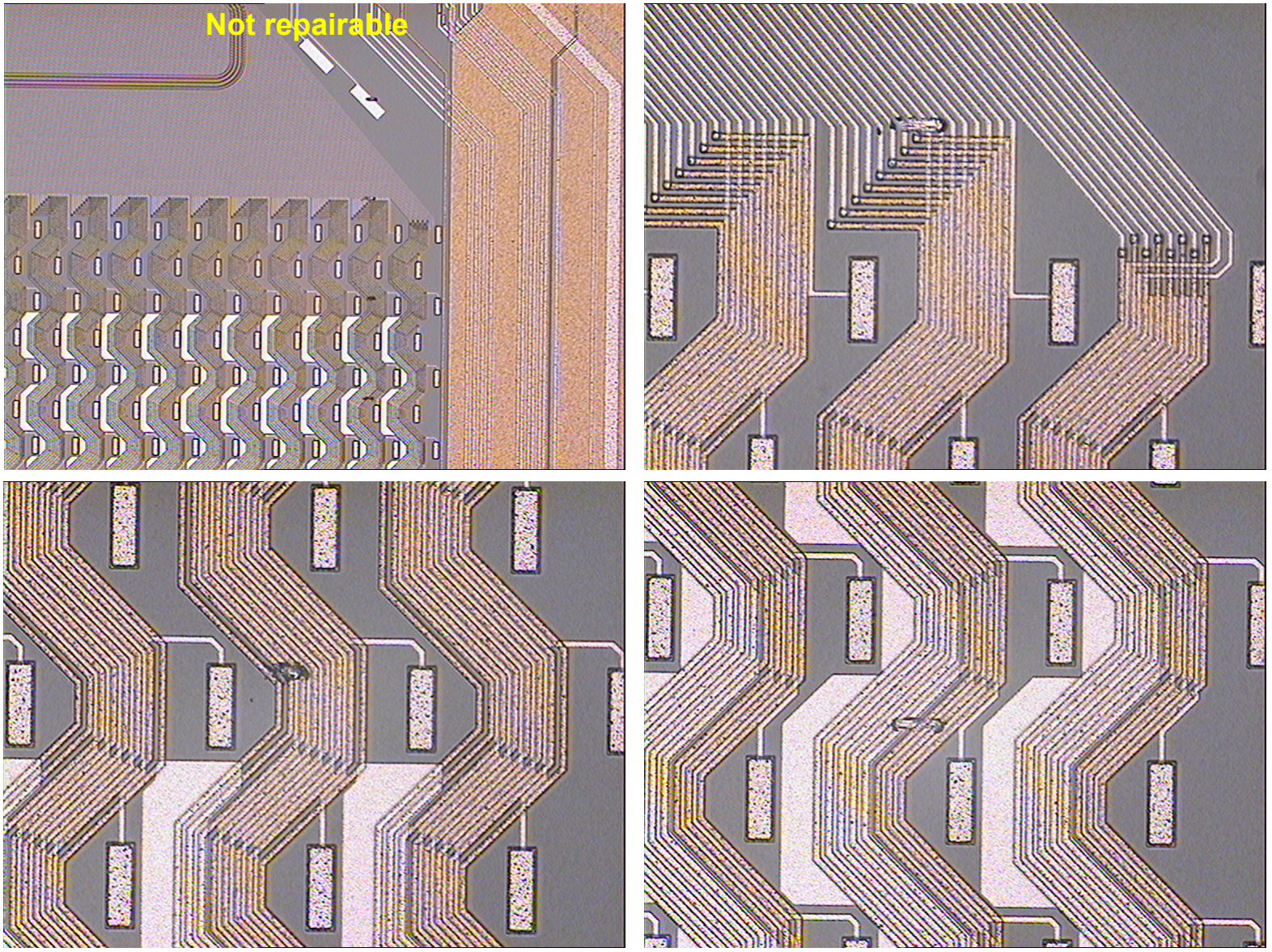








W35 – shorts (due to scratches) in OB1



System issues/failures
(from last SeeVogh meeting – 31.03.15)

1. Chuck not planar →
   - Bad probing in the right hand side of the fan-out (source in conf #2) – (E/W tilt)
   - Bad contacts (higher contact resistance ➔ smaller I_{ds}) for higher chuck steps (N/S tilt)

   → **NOW SOLVED:**
   - Chuck planarized
   - Use of sense line at source contact (currently possible only for conf #2)

2. Electrical failures (due to contact problem in SMU2 preamp of Keithley 4200) →
   - System freeze
   - Bad characteristics due to wrong applied voltage (AC/conf #1 or S/conf #2 – critical)

   → Need investigation – currently on hold (temporary solution: SMU2 and SMU3 swapped and measurement of voltages for all static needles)

3. Electrical failures (in Keithley 2612) →
   - System freeze

   → Possibly due to a timeout error in the communication between KITE (Keithley GUI) and the instruments:
   - Software upgrade seems to solve the problem via the introduction of settling time and keeping the SMUs in the ON state for the whole duration of the measurement

4. Software failures (**fully understood**) →
   - KITE (DAQ software) crash
   - System freeze if data folder remotely accessed

Conclusions and future developments

- Preliminary tests on all common contacts were performed on all the three wafers of the pilot run production.
- The outcome of these tests is a total of three faulty chips (due to shorts between n+ and p+ implantations) and presence of some shorts (not always identifiable) between the two polys.
- A complete overview of the yield after Al2 is given by tests on the (1000) transistors in the first gate row, which give info on the presence of shorts among drain lines or interruption in each single line.
- The final (combined) yield outcome shows the presence of 10 chips of grade 2a (shorts in poly lines), 5 chips usable, but with faulty drain lines (either due to fabrication defects or operator mishandling), and 3 not usable chips.
- Final yield outcome (on wafer level) will be given after tests on the periphery (i.e. End Of Stave and balcony), which will be performed using the atg prober.

Thank you for your attention!

Backup Slides

Switch system