PXD9 Pilot Testing - Discussion

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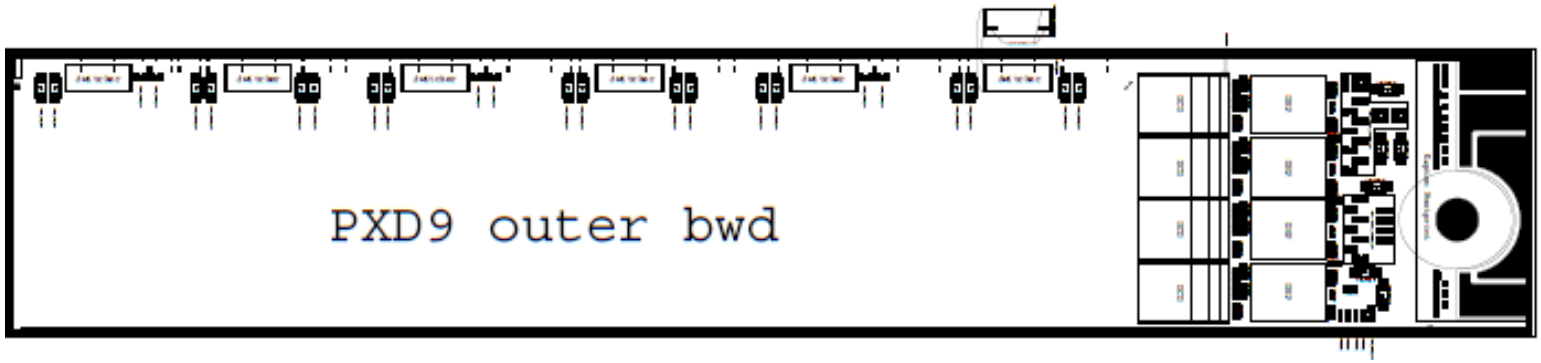
PXD9 Modules - Components

- Two wafers will be ready within ~6 weeks
- We agreed to assemble 5 outer backward modules on the kapton and 2 outer forward modules on the hybrid7 board
- ASICs needed:
  - 28 x DHPT1.0
  - 28 x DCDPP
  - 42 x SwticherB18v2 (gated)
- SMD components

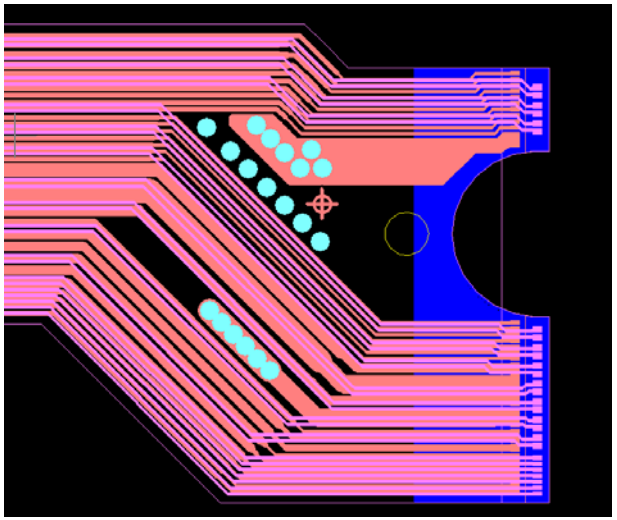


Kapton for PXD9 Pilot Testing

280mm

430mm

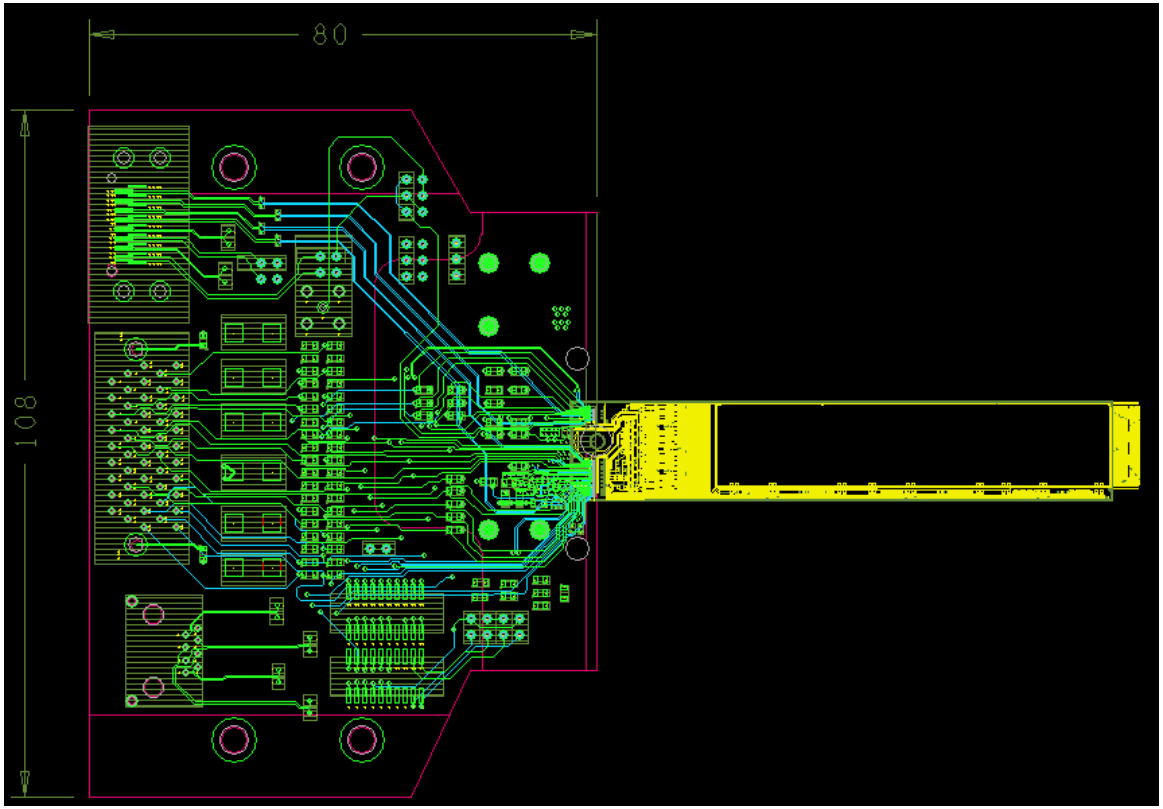
Wirebond fanout for outer backward module (OB) and inner forward



Number of kaptons: 1 (+ 9 expected end of May)

- test full signal path (kapton + data patch panel + cable)
- Combined data patch panel + power patch panel available (by Stefan Rummel)

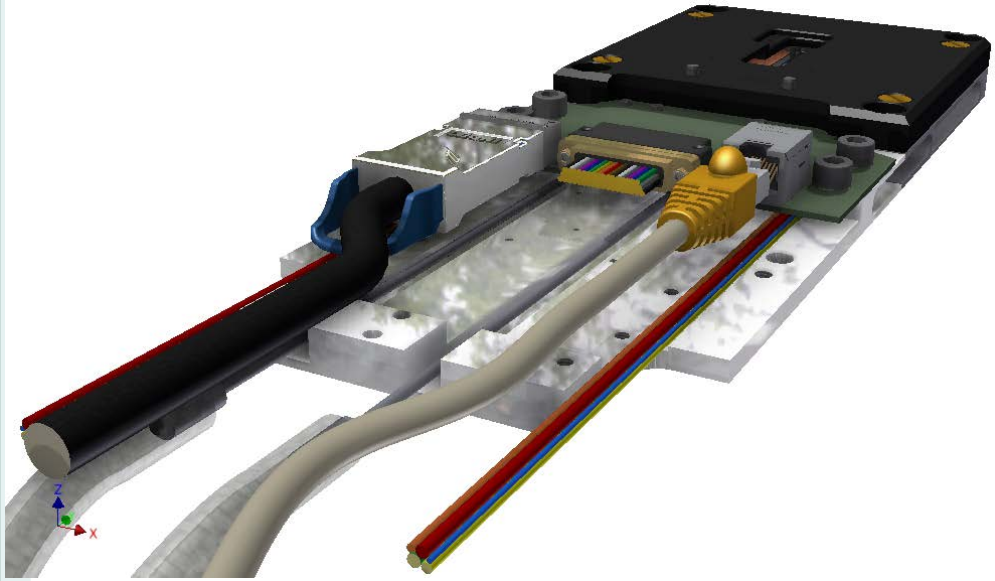
Hybrid 7 for PXD9 Testing

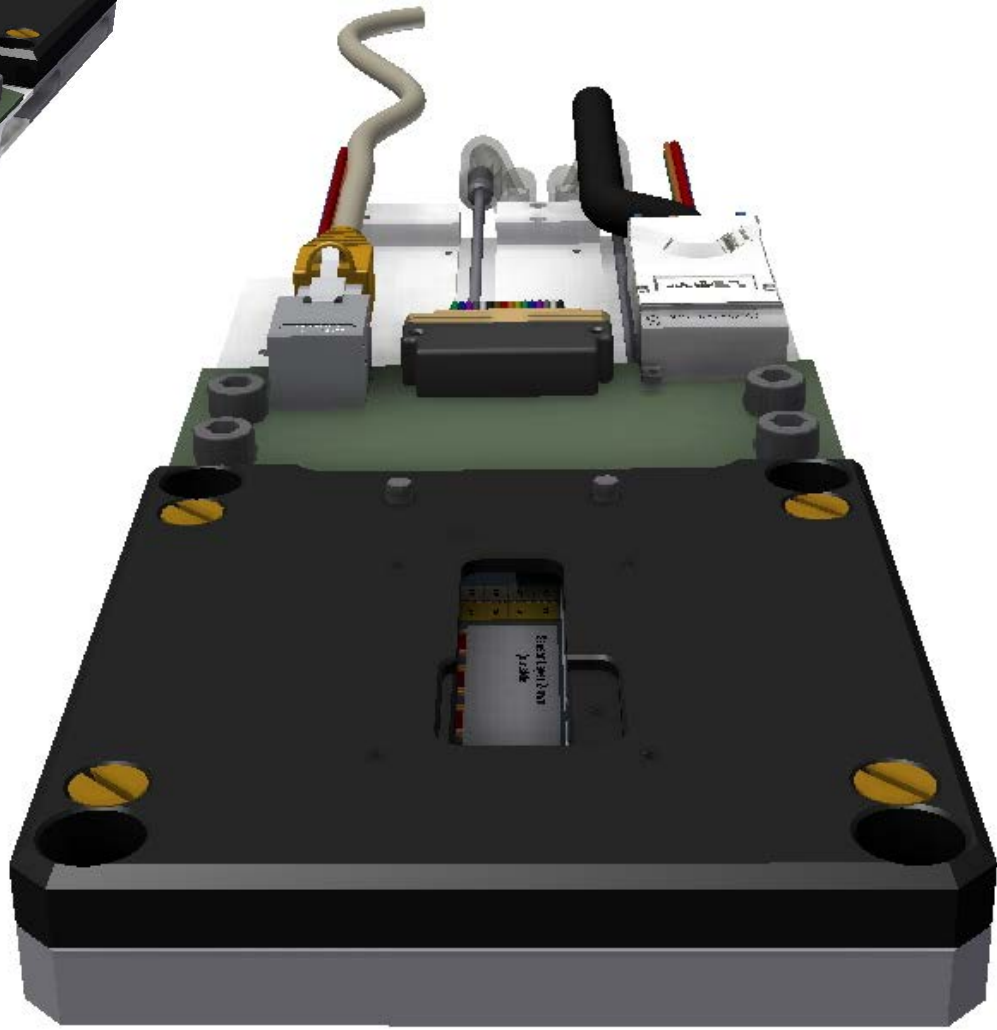


Hybird7 (for Outer Backward and Outer Forward – 2 different layouts) are in preparation:

- Layout can be finalized after the workshop
- Lead time for PCBs 6 weeks
- Mechanical holder in preparation (lead time 10 weeks in MPP wokshop)
- Focused on PXD test rather system test (much shorter traces, more decoupling)

Housing of PXD9 on modified EMCM box

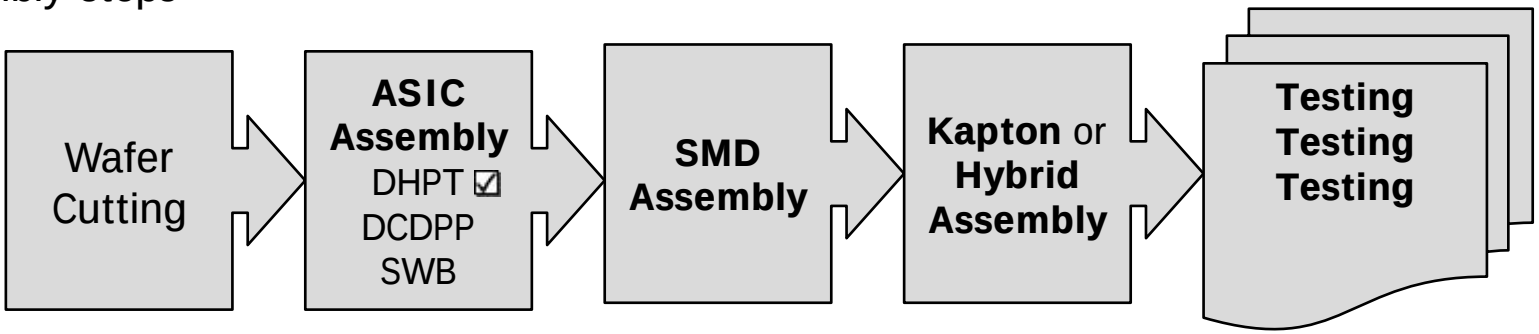




- re-use of EMCM boxes (still long lead time)
- Opening in the box (top and bottom) for laser and beam test

PXD9 Modules – Time line

Assembly steps



What is the time line for the various assembly steps and are the components ready?

- PXD9 processing takes ~6weeks, then two wafers are ready for cutting (one week)
- Jig/tool for ASIC assembly @ IZM needed?
- DHPTs tested, 30 pcs. ready for assembly
- SwitcherB18v2 (gated): bumps are placed @ PacTech; Testing with Probe card still necessary
- DCDPP: Testing with probe card delayed until reason of high contact resistance is identified
  - Main suspect is the probe card mother board
  - Dummy mother board currently under test
  - New mother board will take two weeks (optimistic scenario)
  - How many DCDPP can be tested per day? What man power is available?
  - Does DCDPP testing collide with SWB testing?
- SMD components (processes @ NTC and HLL in preparation): decision end of June 2015

What is ready/missing for PXD9 testing?

What is ready?

- Switcher sequence for 192 channels ready
- Automatic JTAG configuration of DHPT1.0, DCDPP and SWB
- Procedure to automatically power up/down the DEPFET pixels and ASICs
- Fast display of raw data (python based)

What is missing?

- More experience with the various components like DHE and Power Supply (we found stability issues with both devices)
- Move from DHE carrier board and custom housing of the power supply to proper grades (with well defined supply voltage and cooling)
- Gated-Mode support by the DHE (how do we discharge information in the DHP?)
- Test analog common mode correction on the EMCM
- Documentation: test plan for PXD9, allowed voltages (including limits if the sense line connection is lost), DHE board and FPGA firmware