Advanced JTAG for Future Impementations

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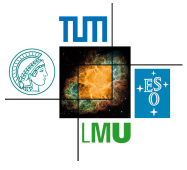


Outline

Outline

IEEE 1149.1, Daisy Chain

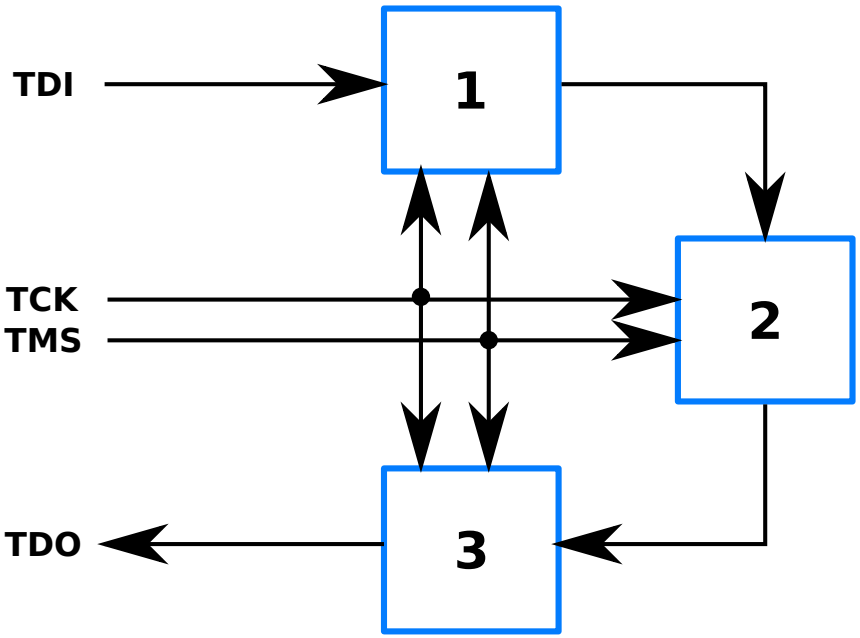


Figure : Daisy chain topology

- TCK and TMS connected in parallel
- TDI and TDO connected in daisy chain
- ASIC **3** accessible only if **2** and **1** are not broken
- In PXD: up to 14 ASICs in the chain

Complications with Daisy Chain

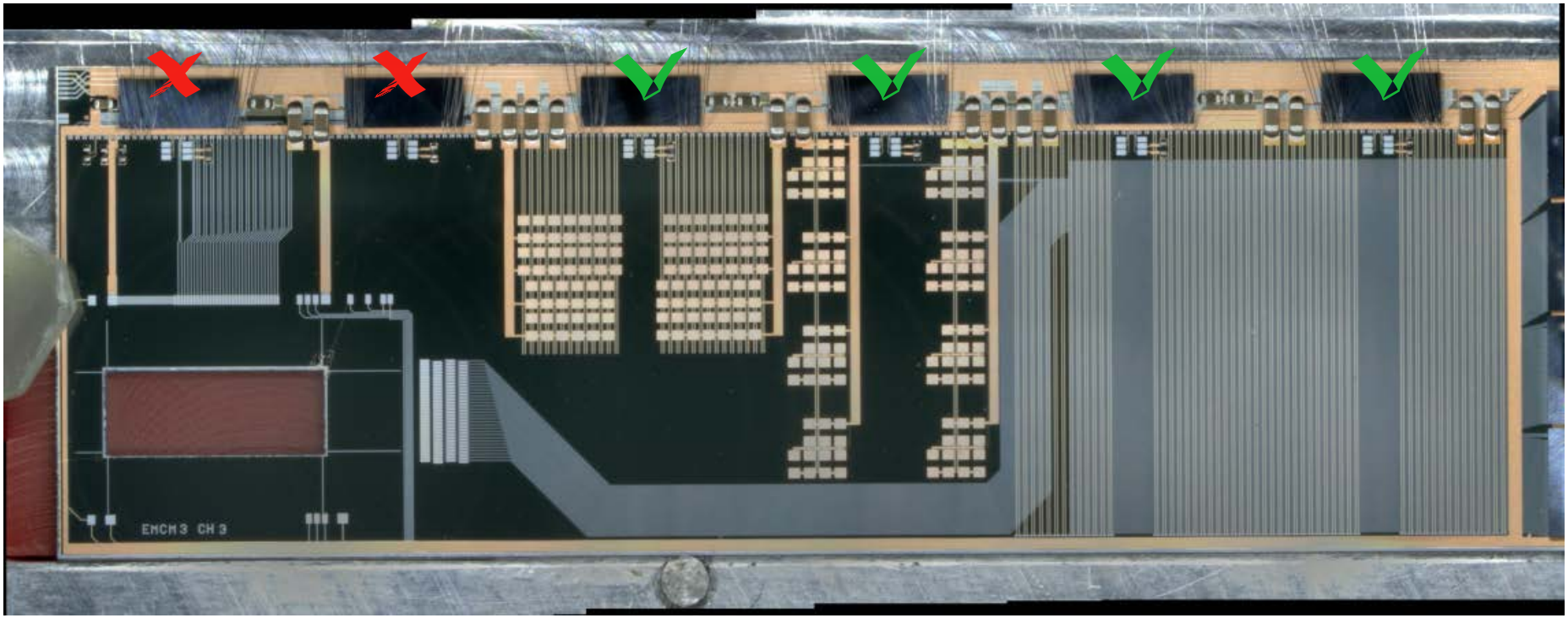


Figure : EMCM3 W17-3 with Switcher 5 broken

- Switcher 5 broken
  - switcher 6 cannot be accessed
  - no readback from any switcher possible

Outline

IEEE 1149.7 Architecture

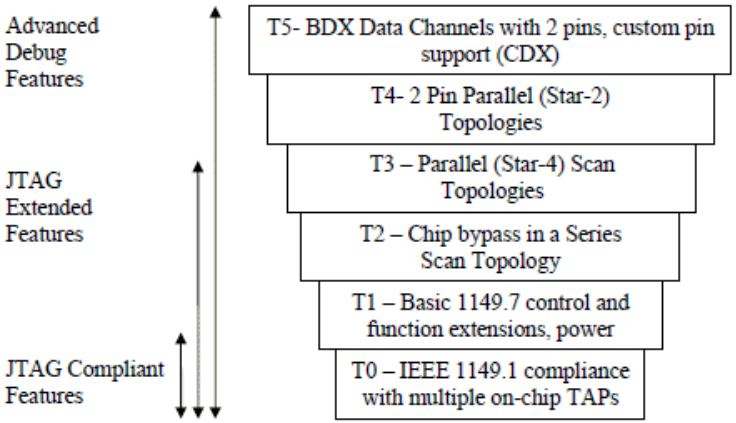


Figure : IEEE 1149.7 architecture

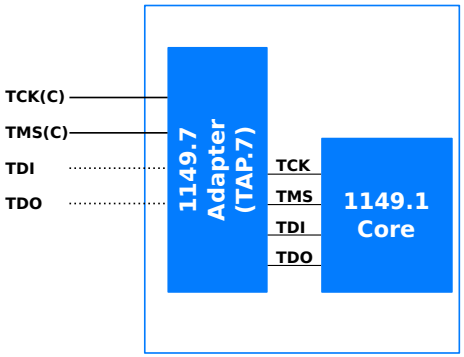


Figure : IEEE 1149.7 integration with older designs

- Backwards compatible with IEEE 1149.1 standard
- Implements 6 additional classes for advanced features
- TAP.7 cores commercially available
- Valid IEEE 1149.1 control sequence (Zero-Bit-Scan) as escape sequence

IEEE 1149.7 Architecture

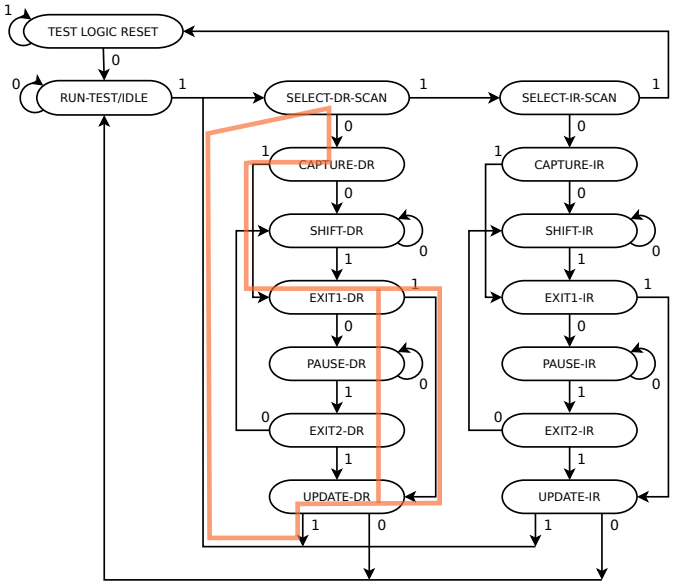


Figure : Zero-Bit-Scan as escape sequence

- Valid IEEE 1149.1 sequence
- Does not change status of the JTAG registers
- Gives access to registers of the IEEE 1149.7 controller

IEEE 1149.7 Star Topology

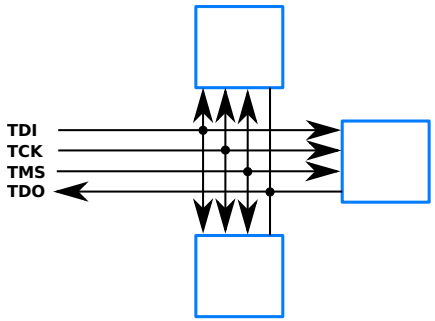


Figure : Star-4 topology, TAP3

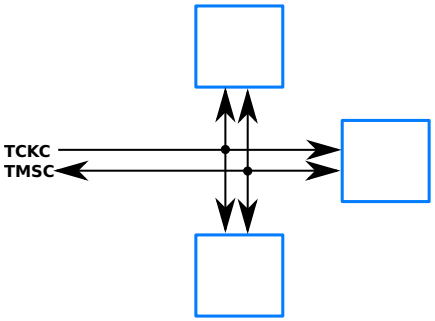


Figure : Star-2 topology, TAP4

- TAP3: parallel **TCK**, **TMS**, **TDI**, **TDO** uni-directional signals
- TAP4: parallel **TCKC**: uni-directional, **TMSC**: bi-directional
- Direct addressability with mandatory TAP.7 Controller Address (TCA)

Node ID[7:0]	**Device ID[27:12]** Part Number	**Device ID[11:0]** Manufacturer
34 27	26 11	10 0

- 4 bit Controller ID allocated by master based on the TCA

TAP4 Serialization

- Time division multiplexing

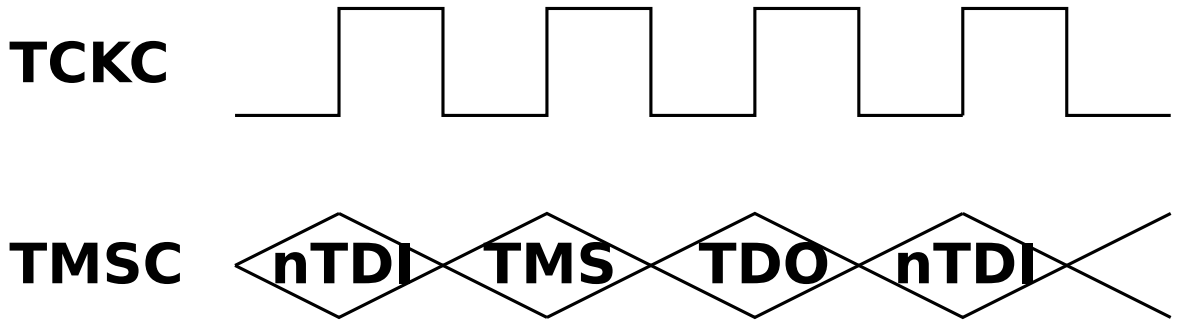


Figure : TAP4 OScan1 format

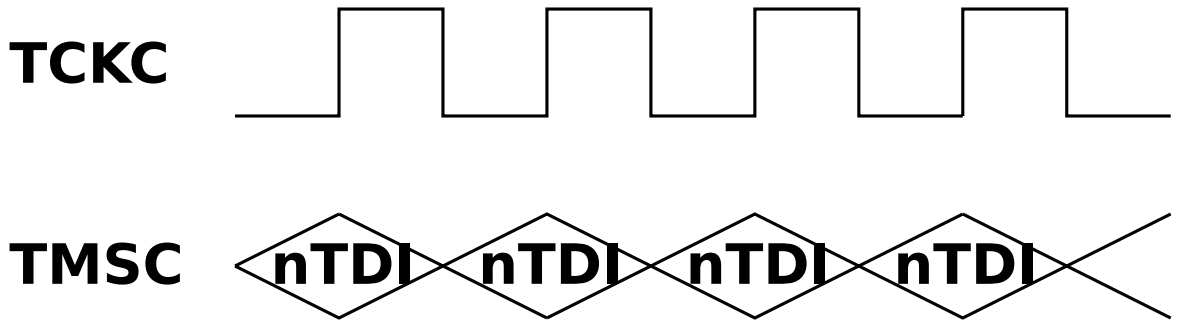
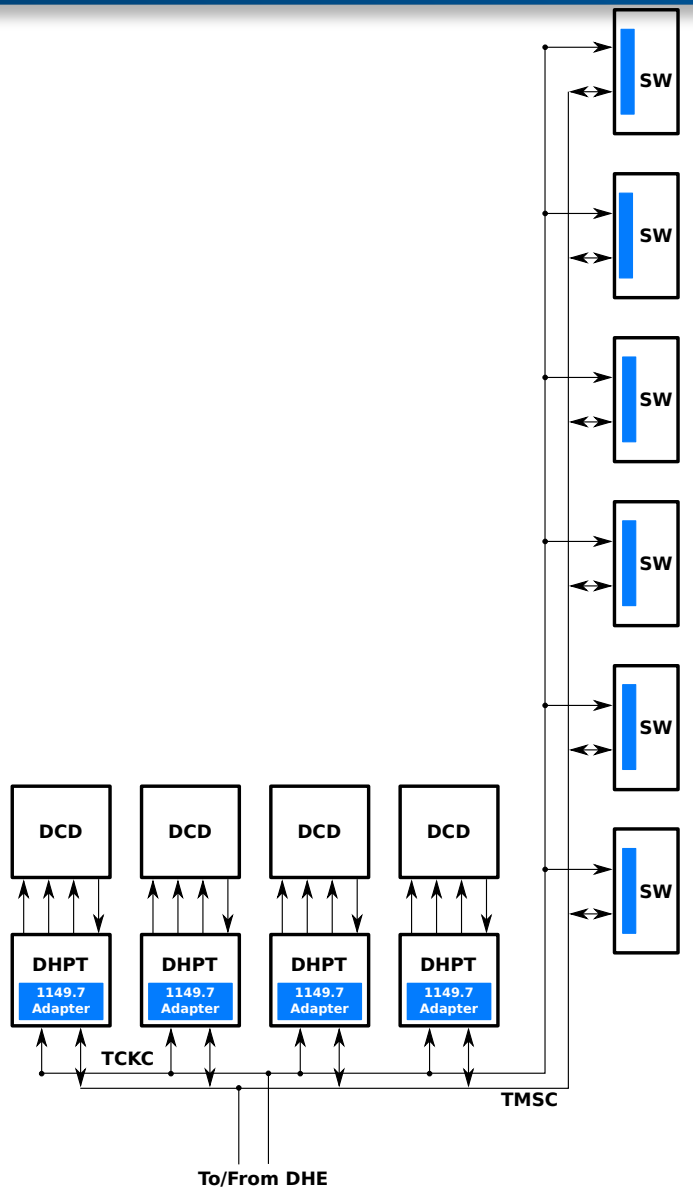


Figure : TAP4 Oscan7 format

IEEE 1149.7 Design Requirements

Work packages:

- Implementation in ASICs
  - DHPT/Switcher mandatory
  - DCD optionally
- FPGA support / **Software support**
- Changes in module layout
  - Star topology
  - Node ID encoding



Outline

Conclusions

- Long daisy chain fails if a chip in the chain fails
- Solved by the IEEE 1149.7 with the star topology
  - resistance against ASIC failure
  - reduced pin count
- JTAG is not a slow control friendly standard:
  - standard does not define length of the registers
  - functionality often encoded in the bit fields of long JTAG registers
  - this makes hard to implements synchronous logic and fast scan functionality
  - different protocol with star topology (I2C) may solve this problem

Literature

- Doing more with less - An IEEE 1149.7 embedded tutorial : Standard for reduced-pin and enhanced-functionality test access port and boundary-scan architecture
  http://dx.doi.org/10.1109/TEST.2009.5355572
  - Talk: http://btw.tttc-events.org/material/BTW10/Presentations/Session%203.2.pptx
- Neal Stollon, On-Chip Instrumentation: Design and Debug for Systems on Chip (Springer US, 2011),
  http://www.myilibrary.com?ID=308357
- 1149.7-2009 - IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture,
  http://dx.doi.org/10.1109/IEEESTD.2010.5412866

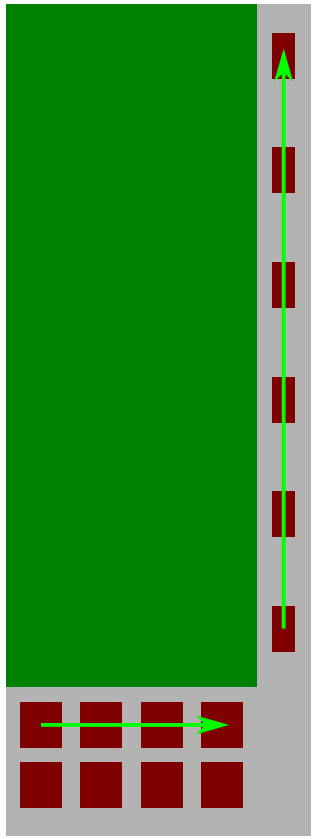
Thank you for your attention!
Questions?

Back Up

Back up slides

Back Up

Outer Backward



Outer Forward