Status of ONSEN

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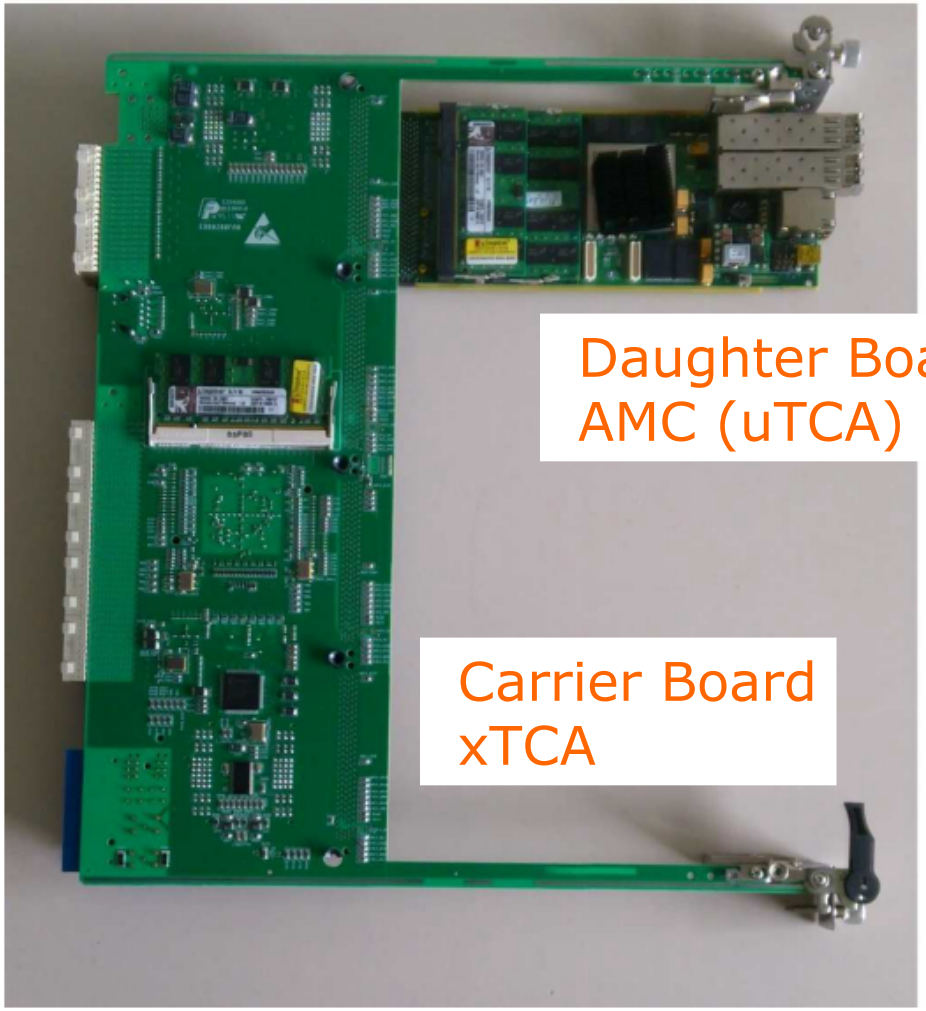
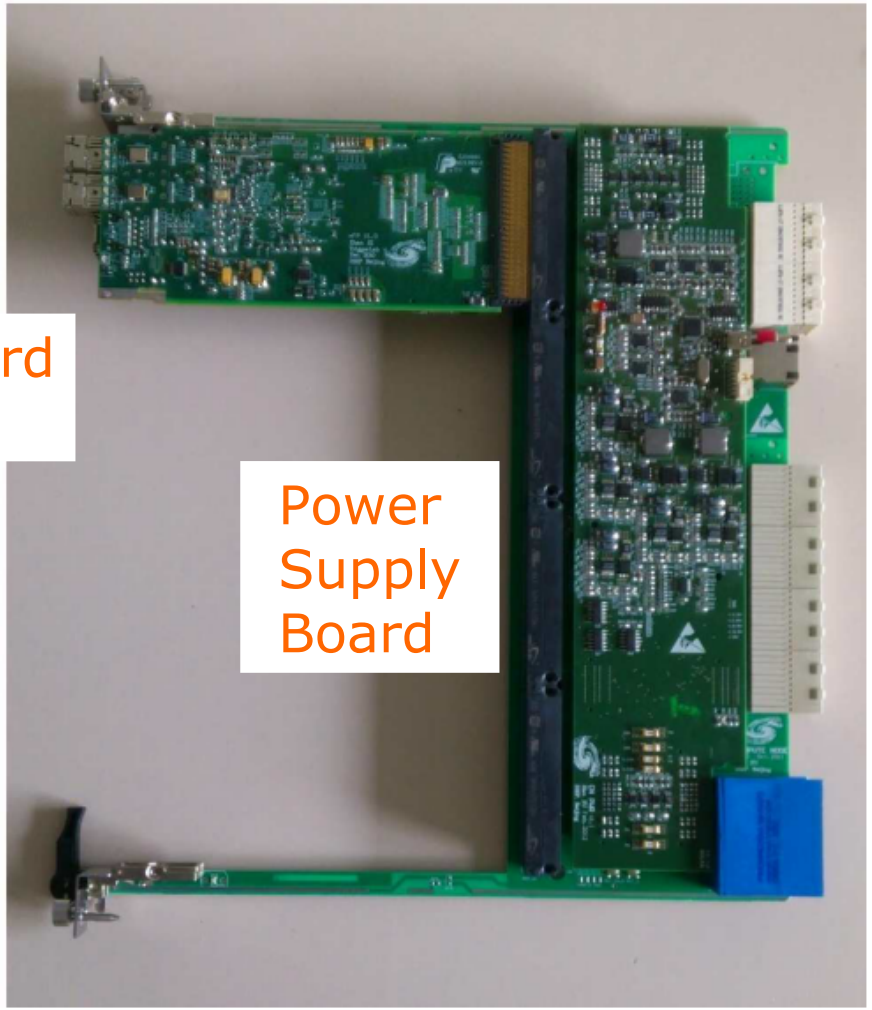
OUTLINE

1. Status of xFP/AMC board
   hardware testing procedure
   (preparation of QA for mass production)
2. Status of xTCA carrier board
   (see also talk by Jingzhou Zhao)
4. discussion:
   test at KEK in October?
5. discussion:
   firmware development for next DESY test
6. discussion:
   event builder interface
   (preparation for discussion at B2GM)

Reminder: Compute Node → xTCA carrier board and xFP/AMC board
AMC is uTCA formfactor (but partially different pin assignment)
Reminder: only xFP/AMC used at DESY tests





Status of xFP/AMC board

- v4.0 was brought by Jingzhou Zhao from IHEP to Giessen in 01/2015
- now two different designs/layouts
  - ONSEN board
    larger FPGA (FX70T)
    2 x 6.5 Gbps optical links
    → 1 board remained in Giessen
    → tested
    → GREEN LIGHT
  - DATCON board
    smaller FPGA (LX50T, same as Belle2Link)
    4 x 3.25 Gbps optical links
    → 1 board shipped to Bonn
    → GREEN LIGHT (as of today, see talk by Bruno Deschamps)
- FPGAs are pin-compatible

Hardware testing procedures @ Giessen
(also for QA of Mass Production)

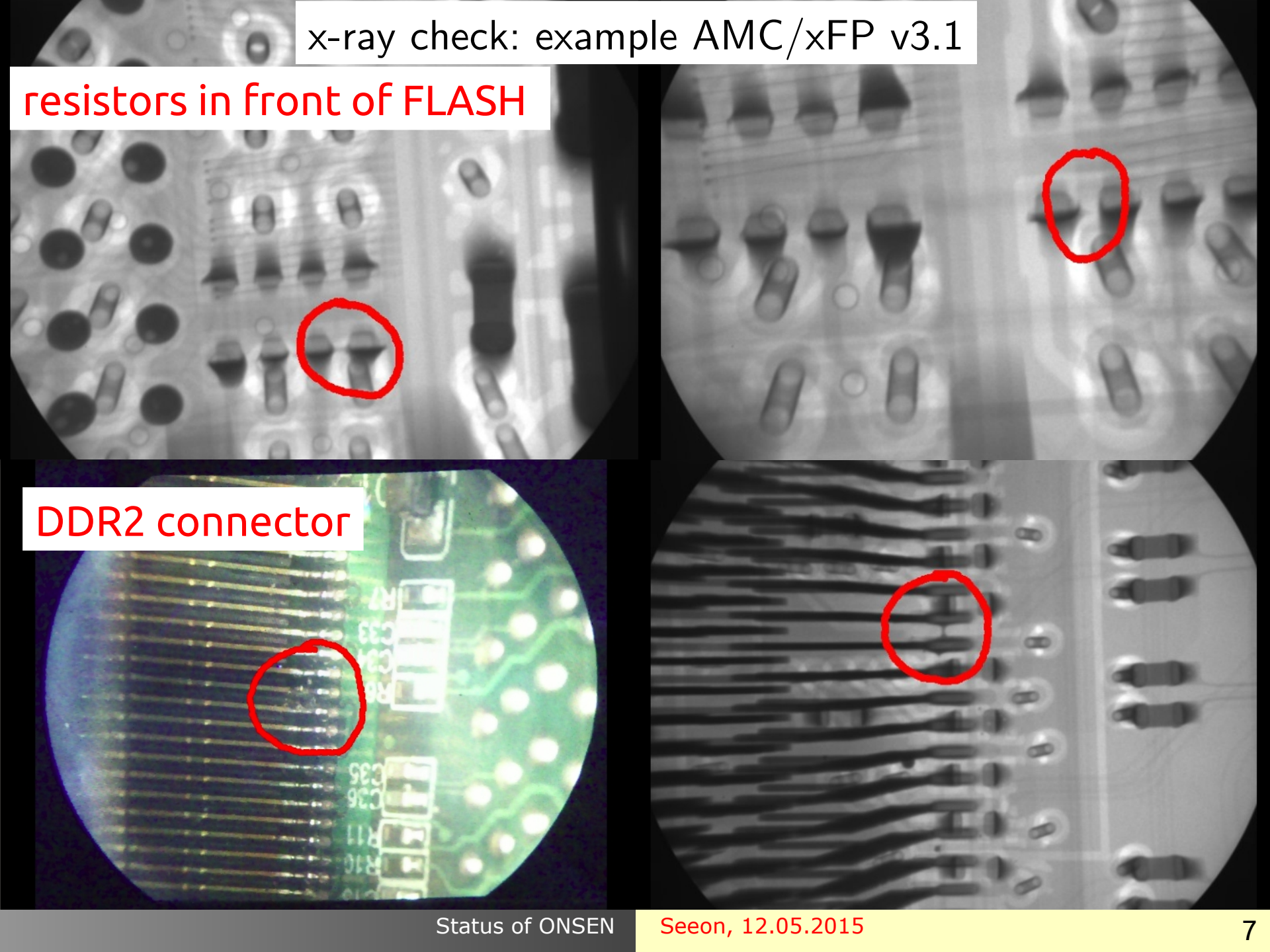
1. dedicated FPGA cores
2. x-ray check
3. thermal check

Example for tests with dedicated FPGA cores
Test of 8 AMC cards v3.2 at Giessen

by Björn Spruck, Thomas Geßler, Milan Wagner, David Münchow, Dennis Getzkow

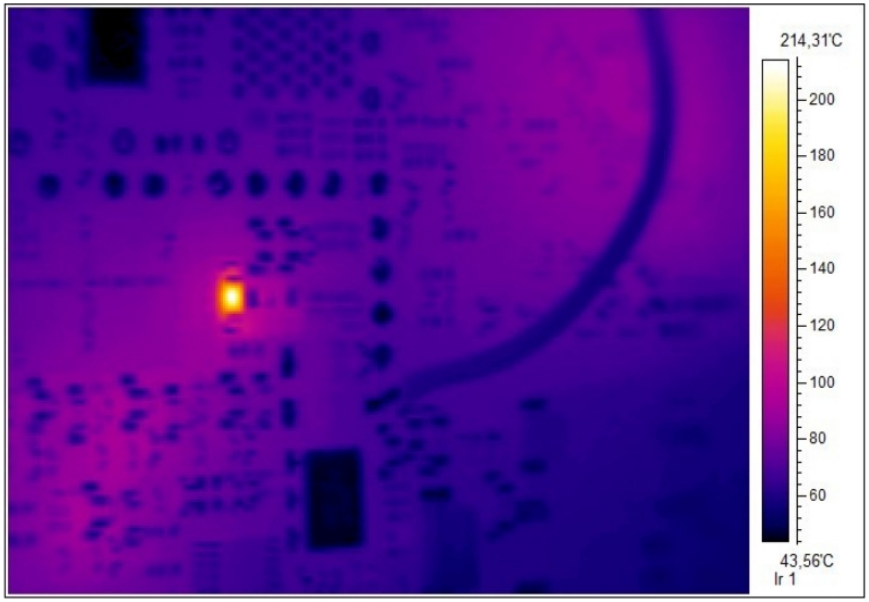
	1	2	3	4	5	6	7	8
Seriell	✓	✓	✓	✓	✓	✓	✓	✓
RAM1	✓	X	✓	✓	✓	✓	✓	✓
RAM2	✓	X	✓	✓	✓	✓	✓	✓
PPC	✓	✓	✓	✓	✓	✓	✓	✓
FLASH	✓	✓	✓	X	X	✓	✓	✓
PROM	✓	✓	✓	✓	✓	✓	✓	✓
OPT 1 (3.125 Gb/s)	-	-	-	-	-	-	✓	✓
OPT 2 (3.125 Gb/s)	✓	✓	✓	✓	✓	✓	✓	✓
OPT 3 (3.125 Gb/s)	-	-	-	-	-	-	✓	✓
OPT 4 (3.125 Gb/s)	✓	✓	✓	✓	✓	✓	✓	✓
Ethernet	✓	✓	✓	✓	✓	✓	✓	✓
Backplane (3.125Gb/s)	✓	✓	✓	✓	✓	✓	✓	✓
Linux (on PPC)	✓	✓	✓	✓	✓	✓	✓	✓

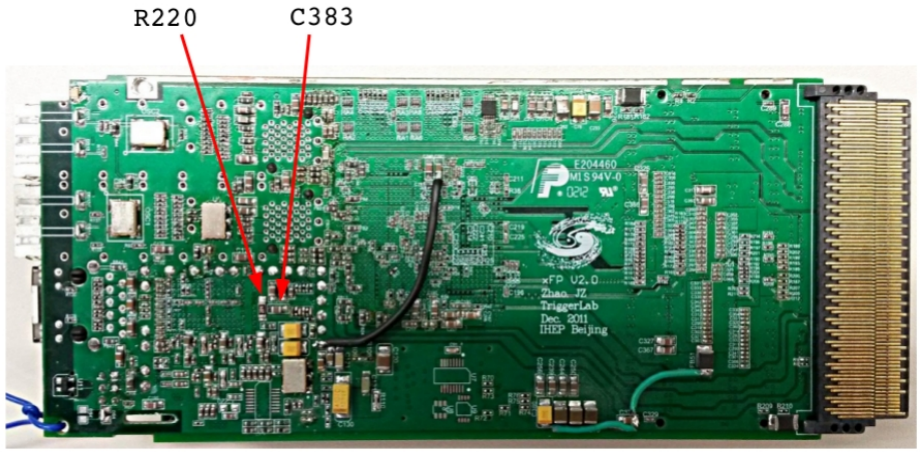
x-ray check: example AMC/xFP v3.1



Thermal check, example:
xFP/AMC v3.3, v2 boards affected, but not v3.1 boards

Capacitor C383 wrong by 10^3 (uF instead of nF)

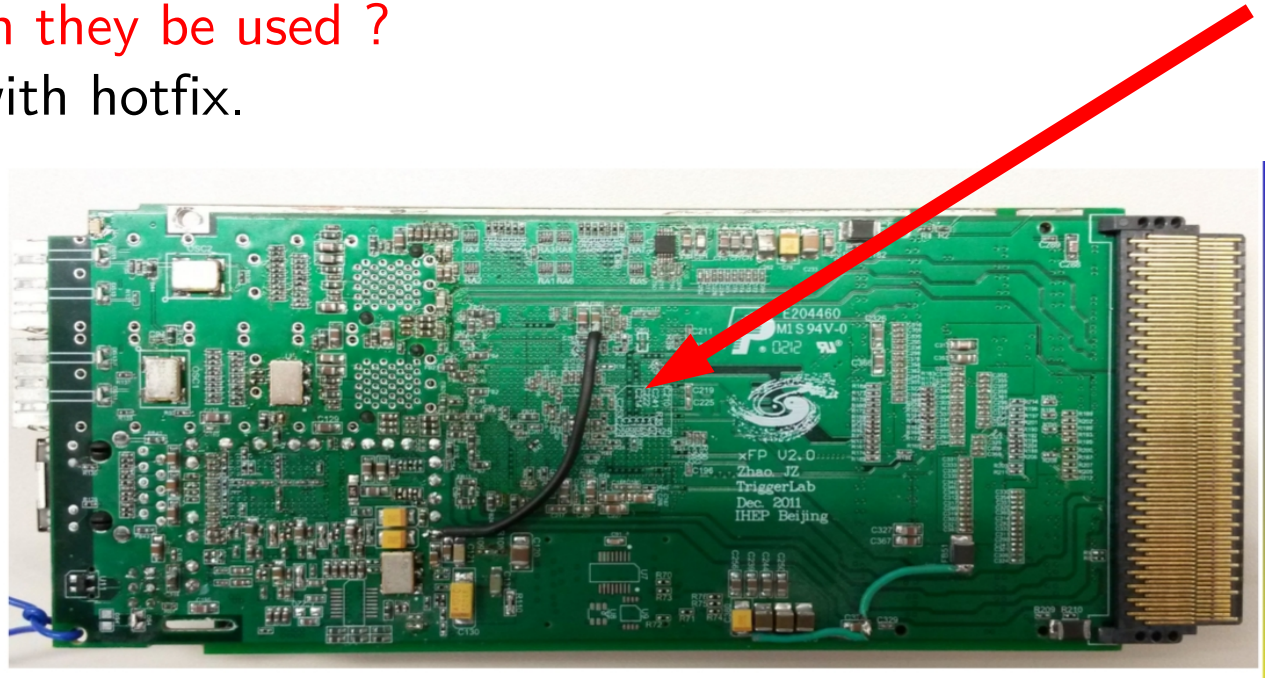




List of xFP/AMC issues found during hardware tests @ Giessen
→ all of them fixed for v4.0

xFP/AMC card hardware testing	
pin 7 and 9 of SFP+ left open → limited bandwidth to 4.25 Gbps	v3.1 (all)
diode, wrong polarity	v3.1 (some)
diode missing	v3.3 (1x)
resistors at FLASH, soldering short circuit (confirmed by x-ray)	v3.2 (1x)
RAM connections, soldering short circuit (confirmed by x-ray)	v3.2 (2x)
Capacitor C383 wrong by factor 10^3 (uF instead of nF) (found by thermal camera)	v3.3 (all), v2 (all) v3.1 not tested
ADC out of range → fixed by adding voltage dividers for 12, 5, 3.3, 2.5 V to ADC	v3.3 (all)
Voltage drop ($\geq$80 mV on V=+1 V line) for large bitstreams	v3.3 (all)

AMC cards in pocket.-ONSEN at KEK are v3.3
w/ V=+1V power supply problem
→ can they be used ?
yes, with hotfix.



before hotfix: measured voltage on +1V directly below FPGA (C235):
917 mV (confirmed by JTAG measurement)

hotfix: thick cable between one of the 1V pins of PSU and C271 (or C248)

after hotfix: V_{int} rising from ~923 to ~976 mV (on same board with same bitstream)
confirmed with one additional board

Status of xTCA carrier board

- v3.2 was brought by Jingzhou Zhao from IHEP to Giessen in 01/2015
- some issues detected
  $\rightarrow$ requires new iteration
  (see details talk by Jingzhou Zhao)

xTCA carrier board, changes for new v3.3 (expected end of may 2015)
serial pins to AMC cards - used I/O pins with wrong bank voltage - used I/O pins w/o LVDS drivers $\rightarrow$ fixed by assignment to different pins
fan-out clock (necessary for the serial links) $\rightarrow$fixed by reassignment and use of LVPECL termination
wrong capacitor values on DDR2 power supply filter (factor 10^3, caused problematic signal) $\rightarrow$ fixed
only 8 of 16 backplane links working at same time (MGT power supply problem $\rightarrow$ fixed)
automatic programming chain of 4 AMC cards on 1 carrier board (wrong power supplied to the bypass chips $\rightarrow$ fixed)
missing PCB trace added, to enable IPMI bitstream loading
inverted LVDS signals $\rightarrow$ fixed
new: changes to rear side of xTCA board USB, JTAG, RJ45, and added design for a rear transistion module

by Jingzhou Zhao and Thomas Geßler

Summary & Conclusion

- presently only 2 xFP/AMC boards of v4.0
  (the final one, but boards have now different layout!)
  - for Giessen xFP/AMC design, green light is given
  - for Bonn xFP/AMC design, green light is given

  $\rightarrow$ next step: mass production
- using existing boards of older versions?

  $\rightarrow$ limited solution

  - requires hotfixes
  - reminder: v3 and v4 are not firmware-compatible
    (different bitstreams)
- temporary use of Panda boards?

  $\rightarrow$ limited solution

  $\rightarrow$ requires soldering of clock (160 MHz vs. 157.25 MHz)

Material for discussion

Discussion:
Test at KEK in autumn? (maybe October, before B2GM)

Proposed plan by Itoh-san (by Email, May 11, 2015):

1) Add "Pocket DHH" to KEK test bench
2) Resume test bench with
   Pocket DHH +Pocket Onsen + Pocket DAQ + mini-HLT,
   connected to the common FTSW trigger
3) Debug the event building scheme at EVB2
   and establish the automatic recovery at run-stop and start,
   which we could not make it during last DESY beam test.
4) High-rate test (30 kHz) will follow
   by applying the dummy trigger from FTSW
   (note: requested by BPAC)
5) Then we will port the debugged system to DESY site,
   and prepare for the 2nd DESY test.

Who can go to KEK for 1-2 weeks? (and: EPICS support included?)

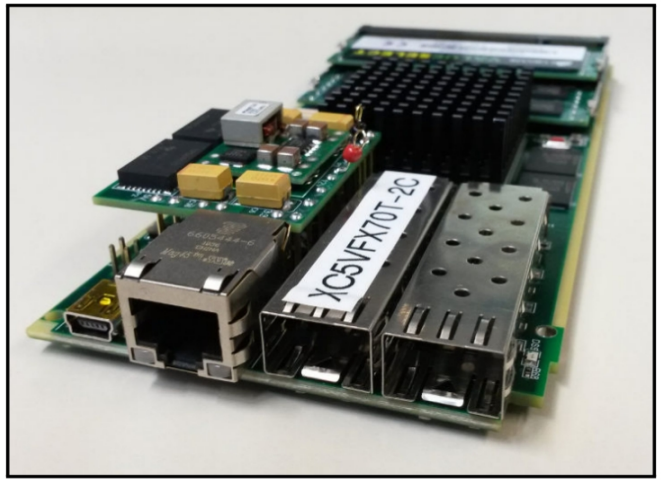
Discussion: firmware development for next DESY test beam?

2 large workpackages

- do we need cluster data format ?
  issues:
  - decoding/unpacking inside ROI-filter
  - basf2 unpacker
  - will cluster rescue be switched on?
    (will Steffen Behr from KIT be there?)

- do we need full frame support (e.g. pedestal monitoring)?
  (or part of full frames)
  issues:
  - interleaving with normal events
  - „chained mode“ in buffer management
  - ROI-filter bypassing
  - basf2 unpacker
  - how does EVB handle them?

Preparation of Discussion for B2GM (proposed by Itoh-san): Interface from PXD to Event Builder (EVB2)



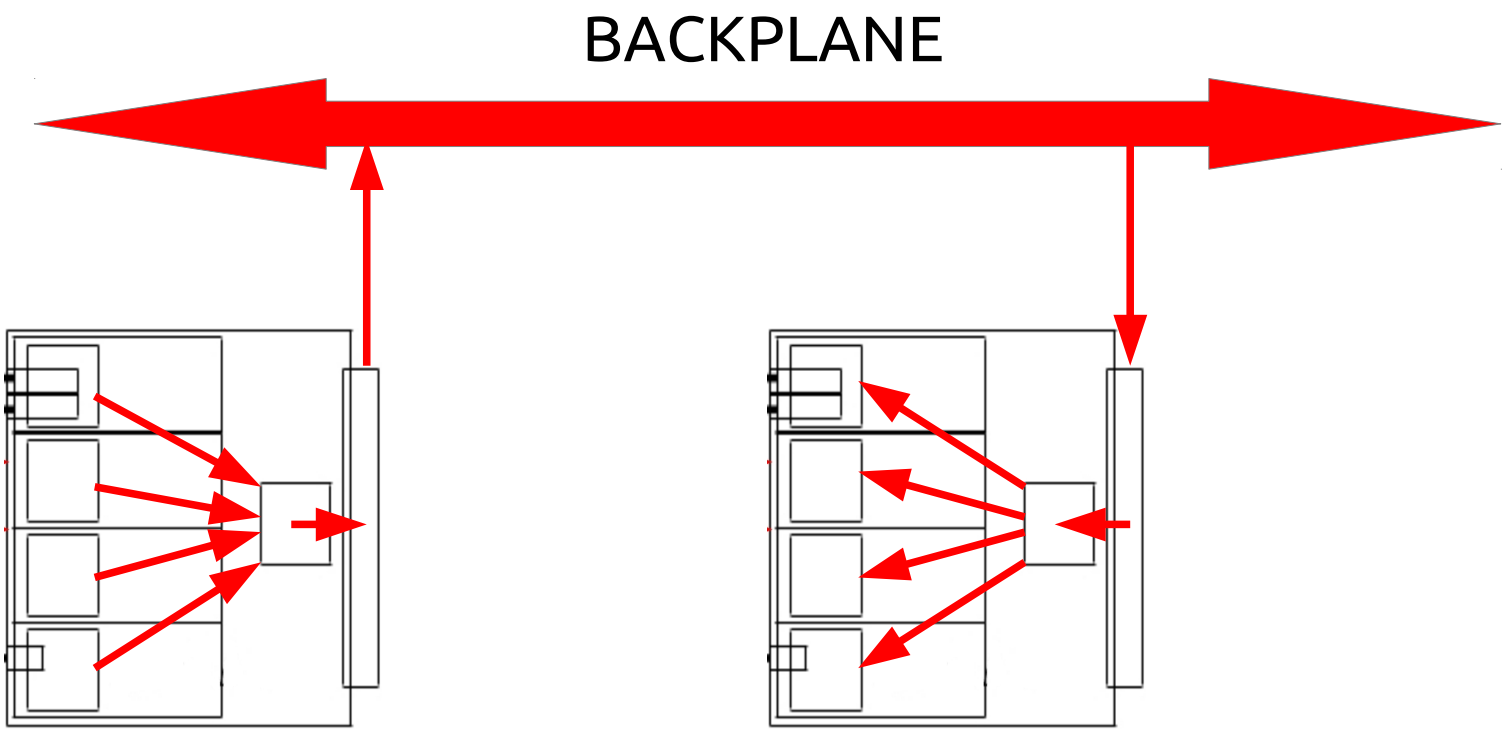
- default concept (the „easy way“)
  - 32 x RJ45, copper cable, TCP
  - FPGA firmware: *siTCP* from BeeBeans Tech.
    already used in DESY test, no problem observed
  - accepted and confirmed by Yamagata-san
    (his only worry:
    buffer of switches with optical inputs)
  - issue:
    RJ45 connectors on xFP/AMC card are used for slow control (PPC)
    solution: use SFP+ converters SFP+ $\rightarrow$ RJ45
    all of them are purchased
  - implication event building on ATCA not required
- why do we need the carrier board ?
  - ROI distribution
  - reason: broadcast of ROIs on GB ethernet backplace at the limit ~100 MB/s
  - solution: matching, send the correct ROI to correct FPGA
    master thesis of Dennis Getzkow, presented in Prague

related to EVB2 discussion at B2GM: xTCA Carrier Board for Event Building?

- main issue of ONSEN: FPGA is too small
  (memory controller requires significant FPGA resources)
  → TCP or UDP needs another AMC card („outsender module“)
  (so, not 32, but 64 cards required)
  → DDR2 RAM is 2 x 2 GB
  but only 2 GB are used so far (reduces possible HLT latency to 2.5 s)

- possible solution?
  send data out to a „ONSEN concentrator“
  by Aurora link-layer protocol (requires less resources)

- significant firmware development required: multi-step data transfer
  (see next slide)
  → 4 „outsender“ AMC cards
  here: no ROI core, less resources required
  in this case: carrier board is needed for partial event building
  problem: reduced BMBF funding (–25%) in next 3 years


BACKPLANE
x8
COLLECTORs
CONCENTRATOR

THANK YOU.