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DEPFET

Active Pixel Detector

Offset Operation on Hybrid 5

-

Test beam lessons learned with Hybrid 6

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On behalf of the Lab and Test Beam Groups

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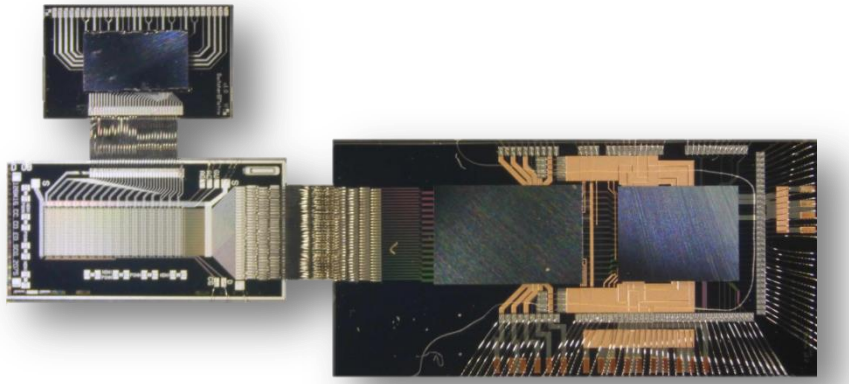
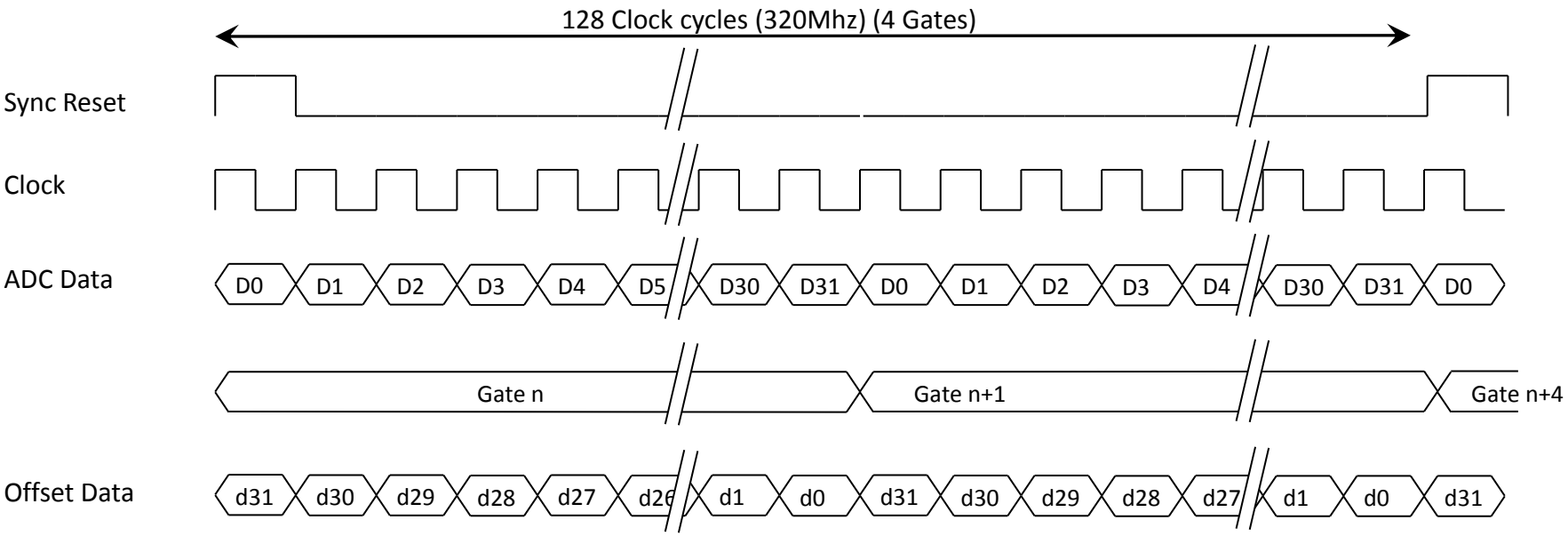
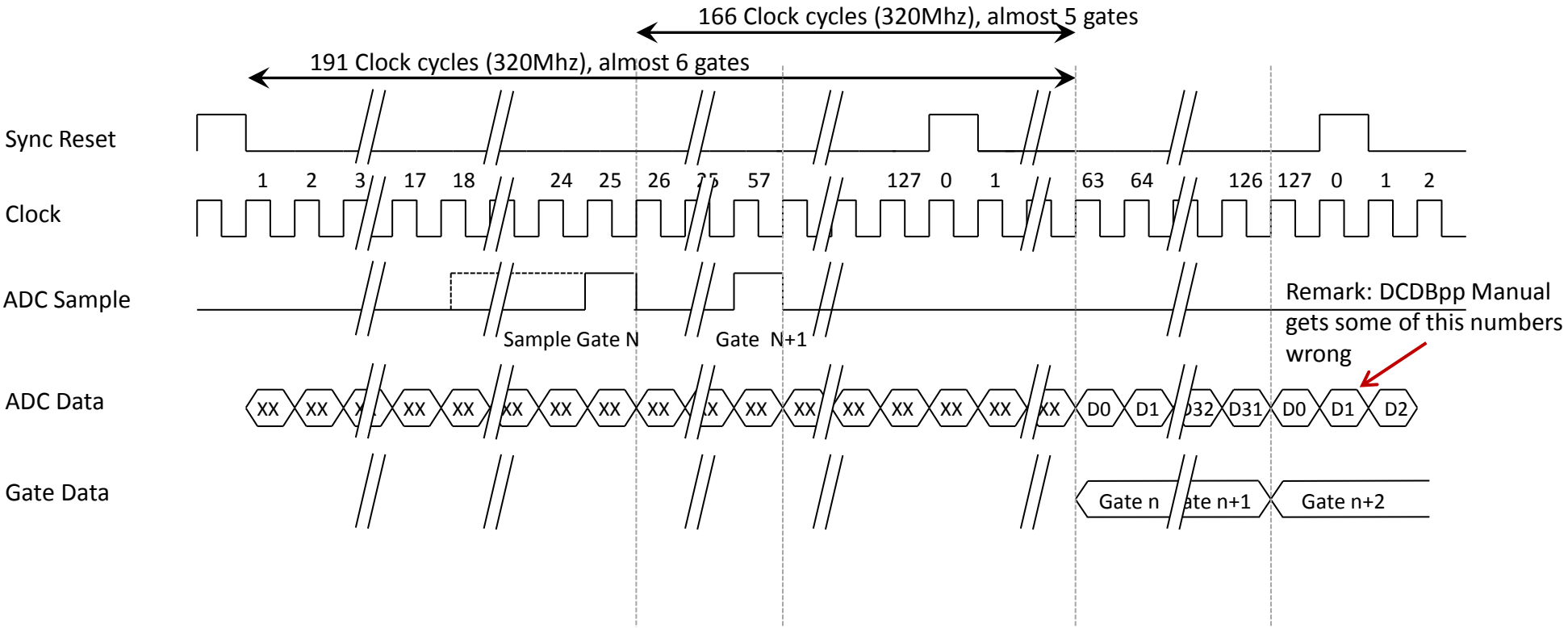
DCD Sampling scheme (easy, wrong)

- Data and control signals between DCD and DHP:
- Sync Reset, clock, Data Out (8*8bit),
  Offset In (8*2bit)



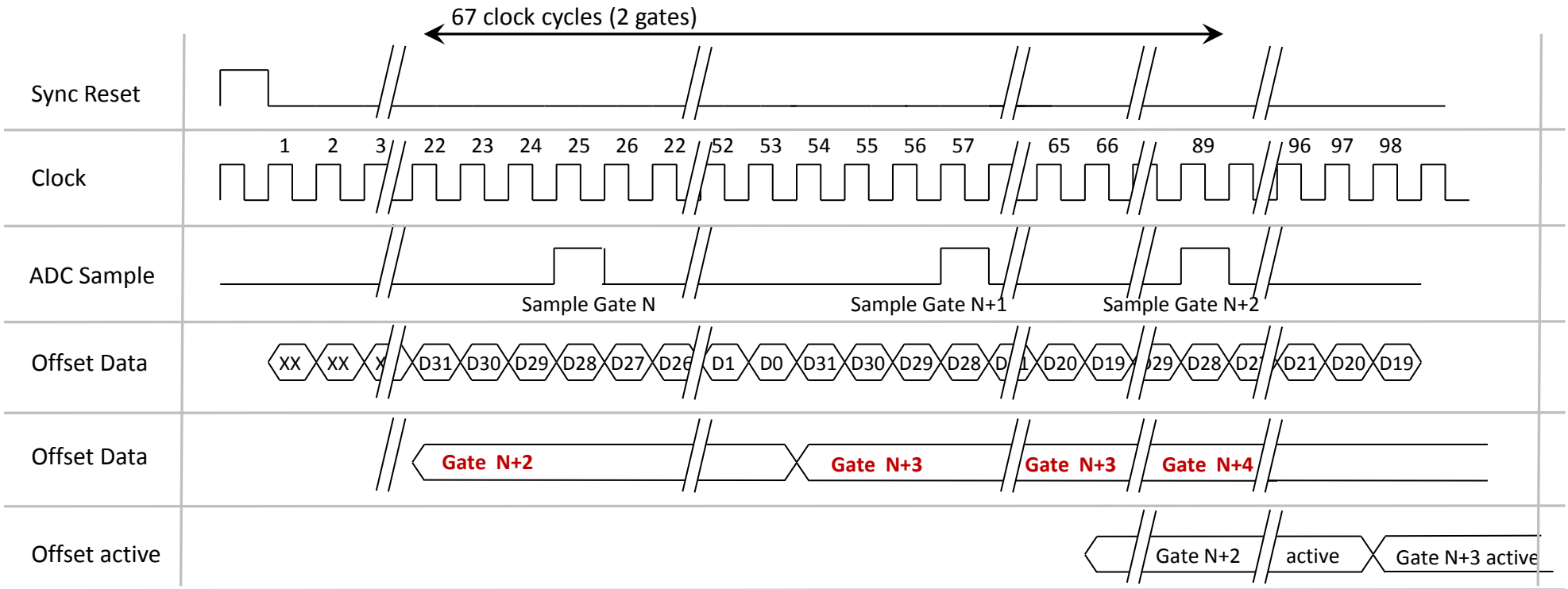


DCD Sampling scheme (Data)



- Data needs to be deserialized into 2 128bit memory words
- In order to be correct: DHP needs correct setting, where D0 of gate n starts
  - Two settings: Sync Reset (row2Sync) can be shifted, Deserializer start can be shifted
- Needs to be right. Bad writing in memory means, that we have one matrix gate is split in two DHPT gates -> Bad CM correction

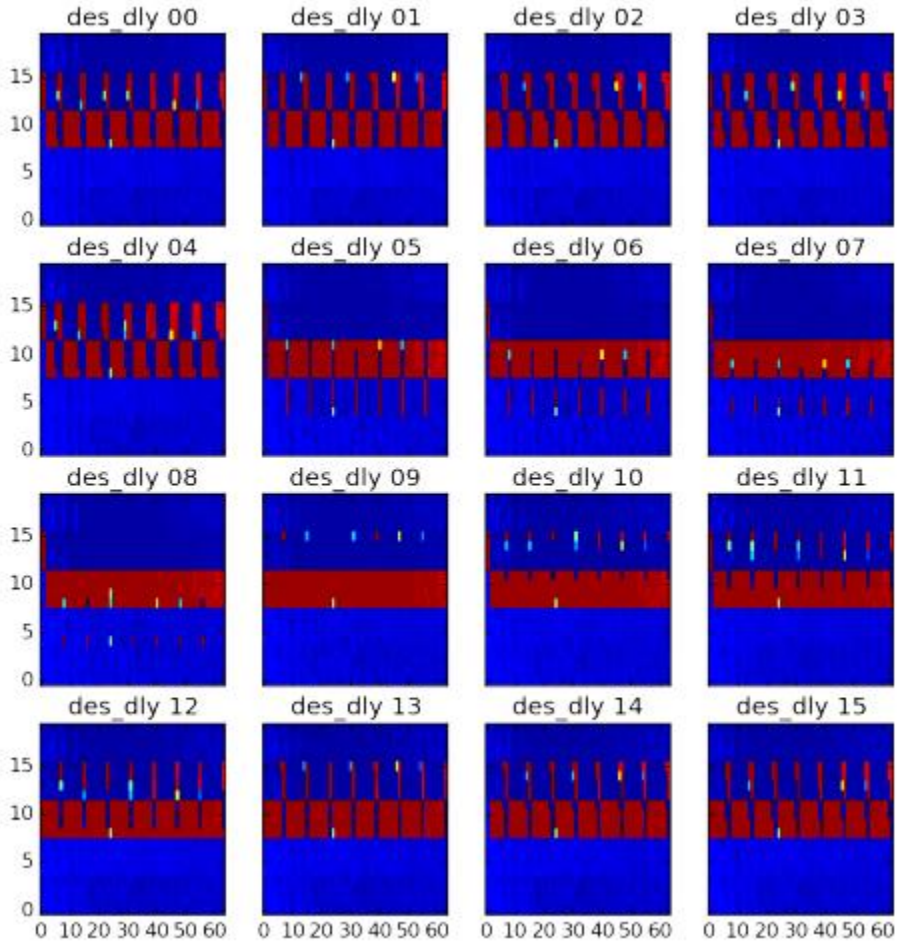
DCD Sampling scheme (Offset)

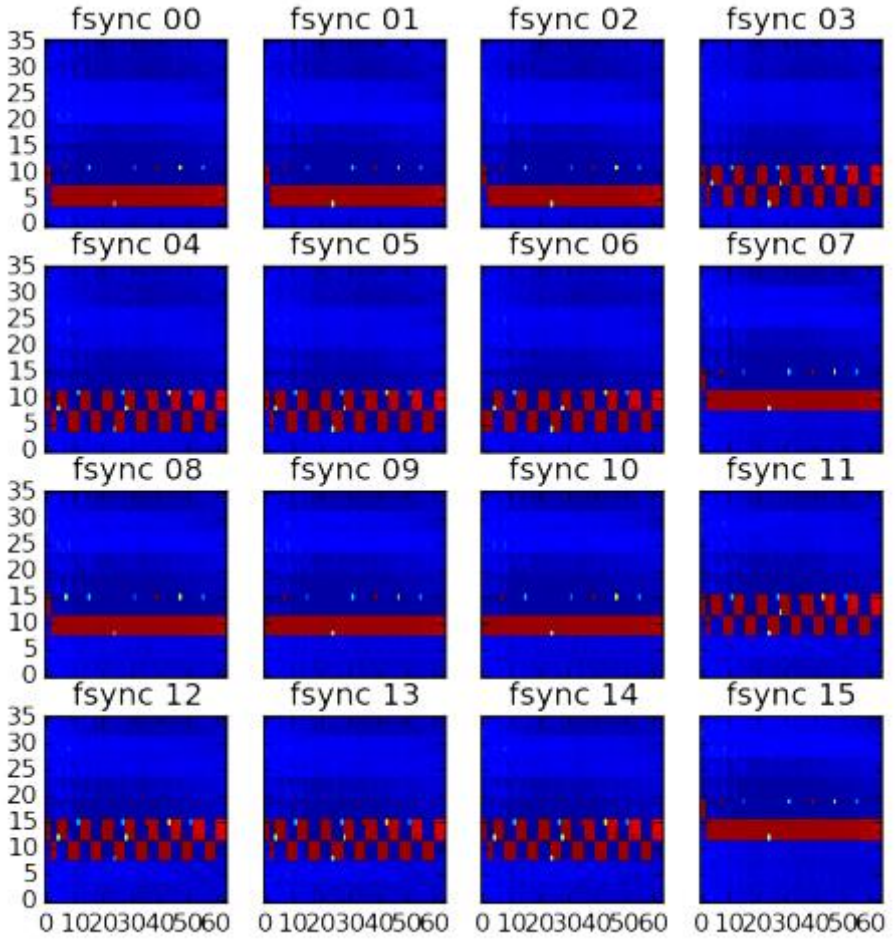


- Data needs to be serialized from 4 16bit words
- In order to be correct: DHP needs correct setting, where D0 of gate n starts
  - Two settings: Serializer start can be shifted in each word, Address offset can shift memory address to be used
- Offset data must be shifted in ~230 clock cycles (7 gates) before corresponding data comes out
- Bad timing solvable by software

Offset Timing

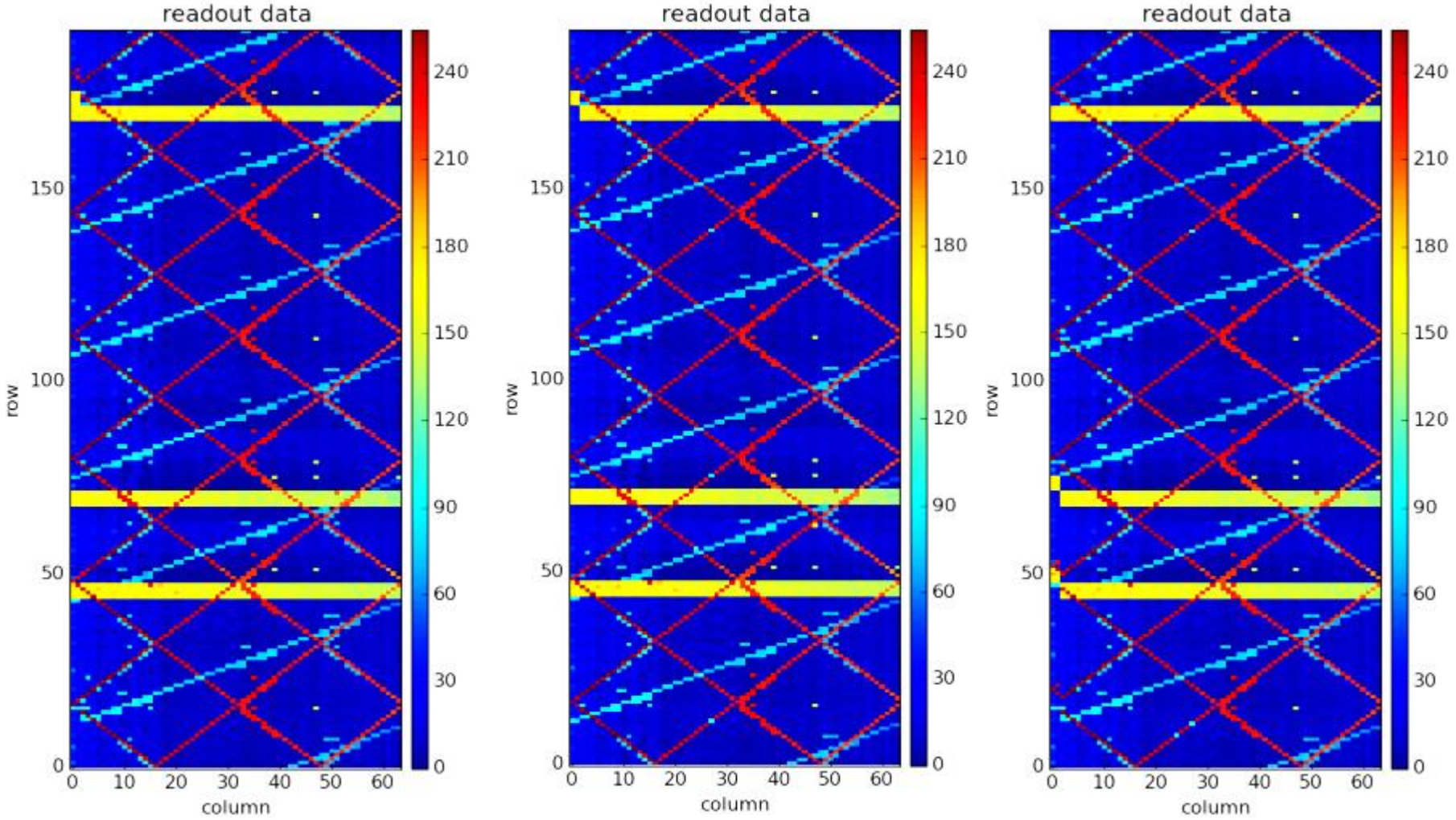
- Switch on offsets in one Gate and sweep settings





Offset Mapping

- Quite complex mapping scheme, solved
- Delays not touched yet

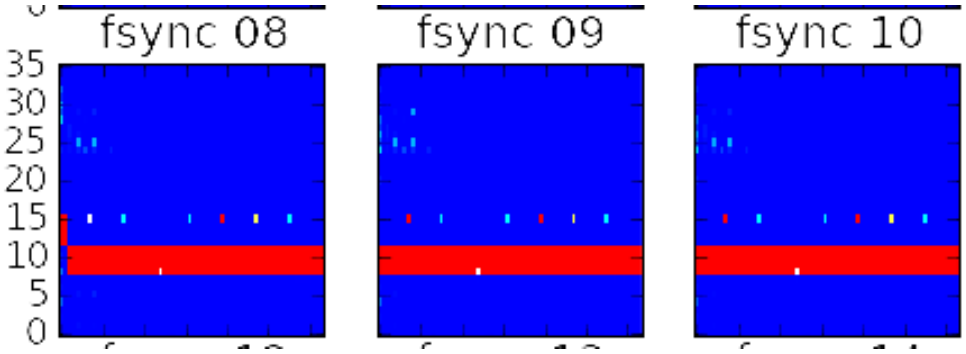


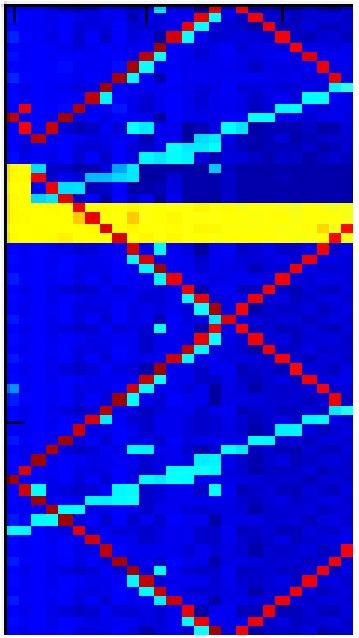
Offset Mapping

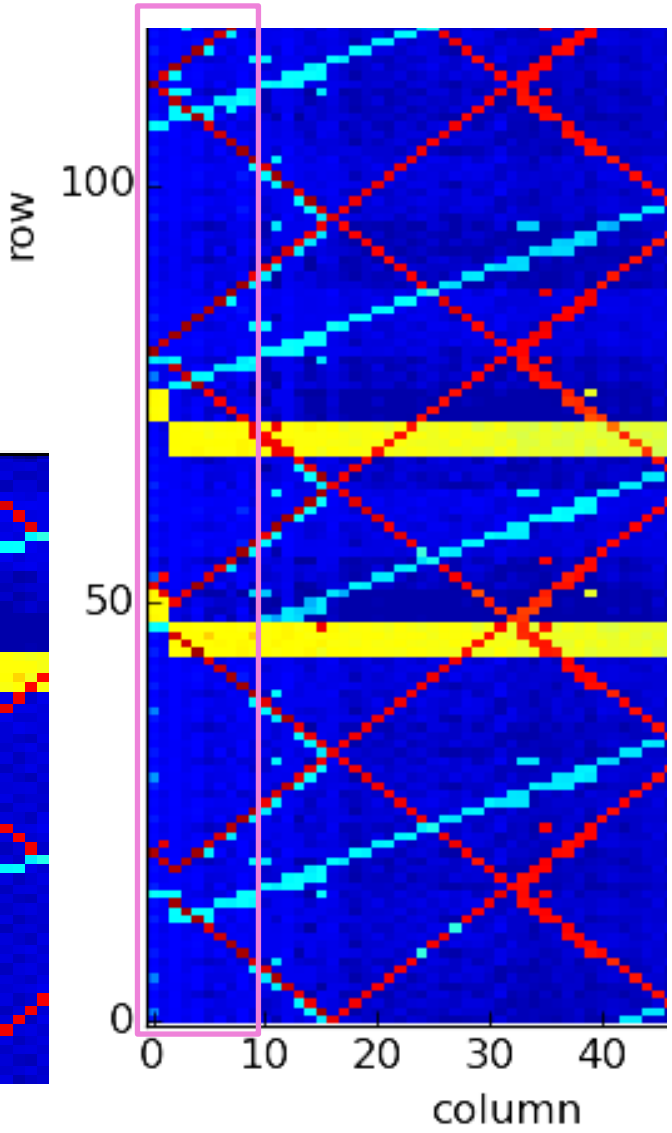
- 8 consecutives values are one gate late
- ADC0 – ADC 7 on link 0

- D0 – D7 is shifted out first by DCD -> Unlikely to be late
- D0 – D7 is shifted out last by DHP -> possible?
- But: Data would need to be 1 gate (32 clock cycles) late
- I can not think of any error mechanism except for DHP serialiser - Open for new Ideas

- How to rule out problems in DHP data taking or DCD
- DCD injection circutry – DHE Support?







Offset Delay scan

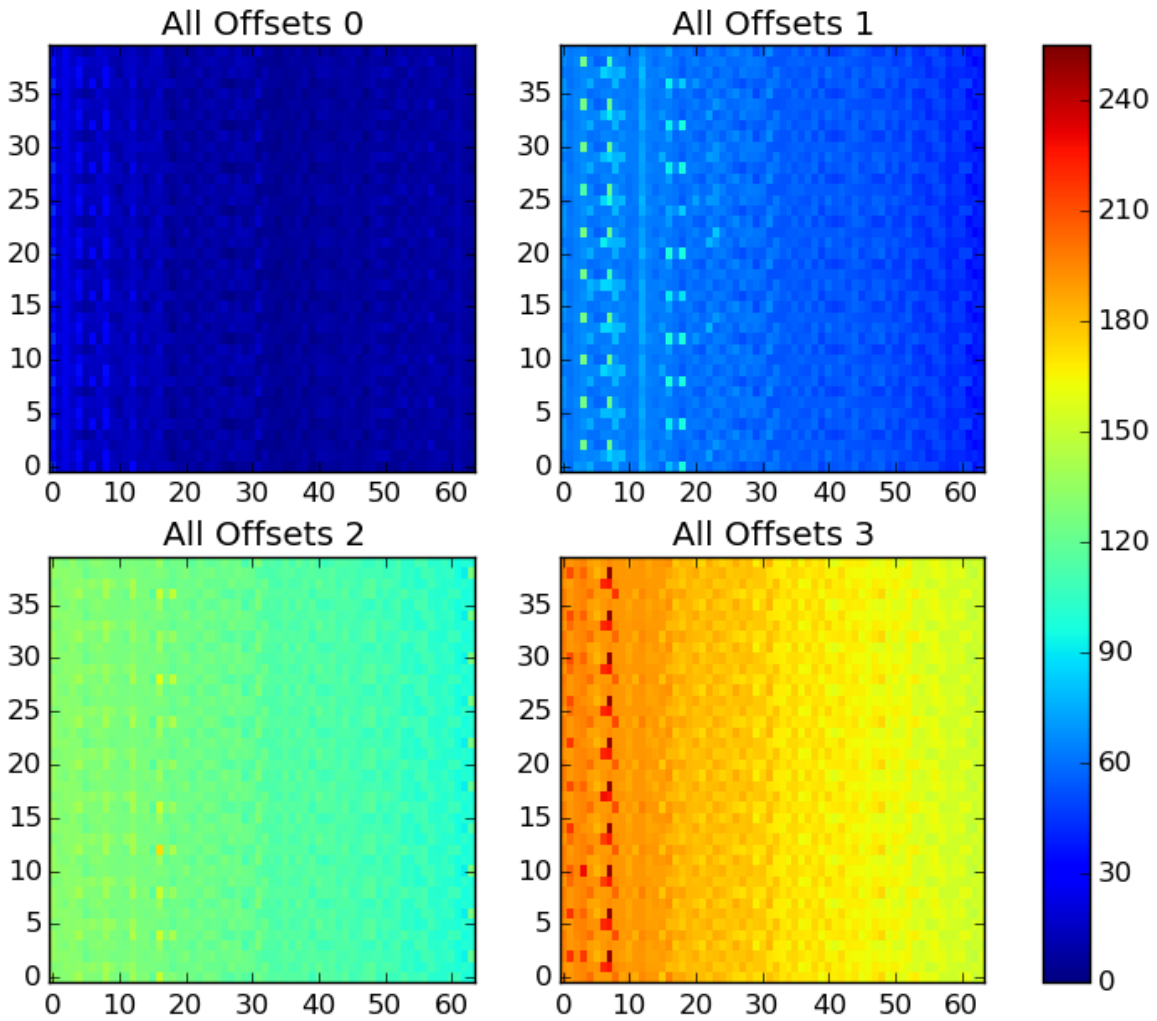
- All data lines have independent delay elements. Task: Find best setting.
- On Data: Scan test pattern with different delay settings.

Offset:

- Data not directly available
- Idea: Use ADC data to reconstruct data

- Calibrate expected value for each channel.

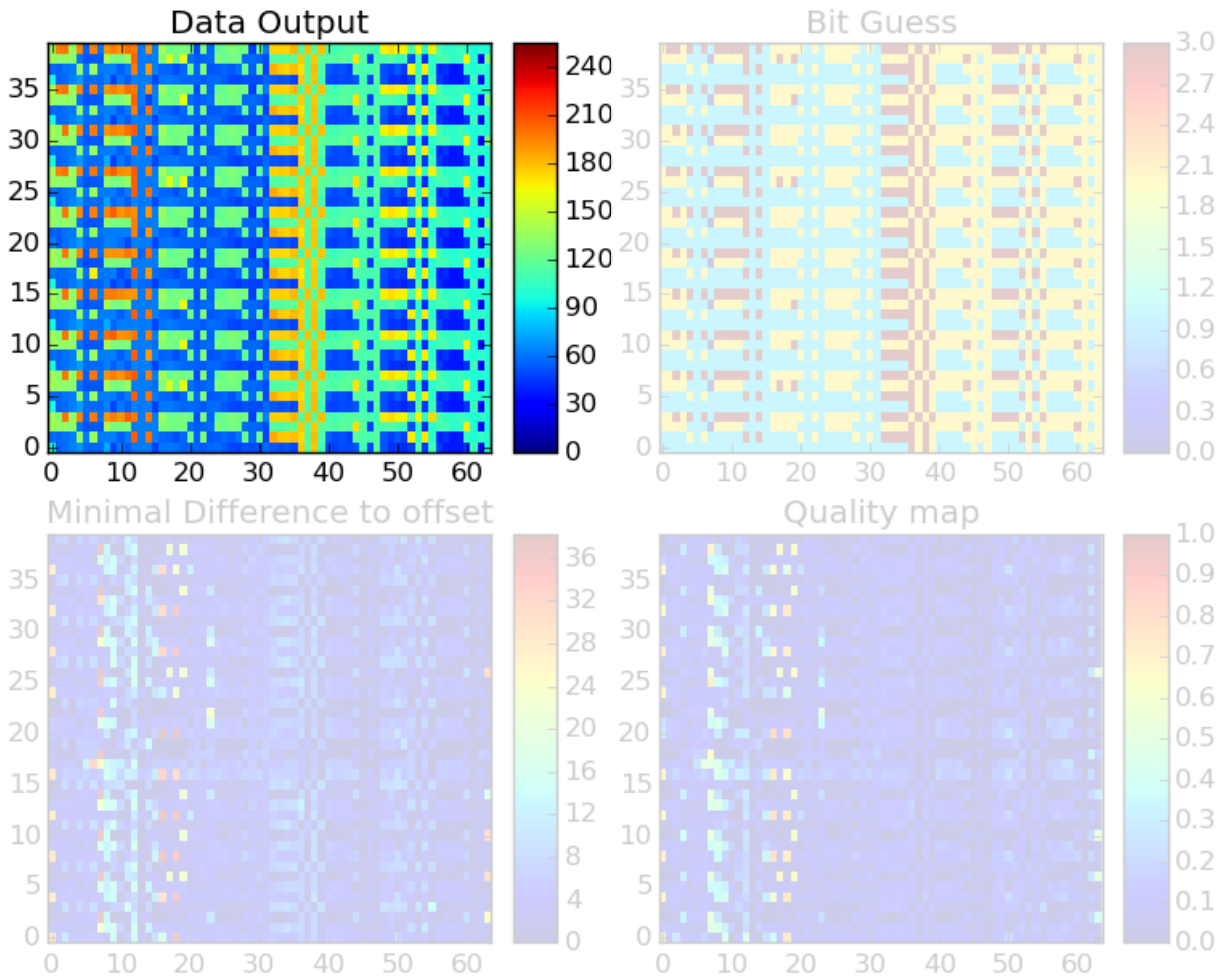
- Off-Topic: There is a gradient, even if offset DACs are switched to quite low values. Need confirmation from EMCM!



Offset Delay scan

- Program pattern and read out
- Check which value it could correspond to
- Get quality of measurement

- To be done:
- Compare bit pattern with programmed testpattern
- Same algorithm as for normal data delay scan



Hybrid 6.0

- PXD6 - J00 on Hybrid 6

Capacitive Coupled ClearGate
50x75 µm2 pitch
768 drain lines (256x3 DCD/DHP)
120 gate/clear lines (4 Switcher)

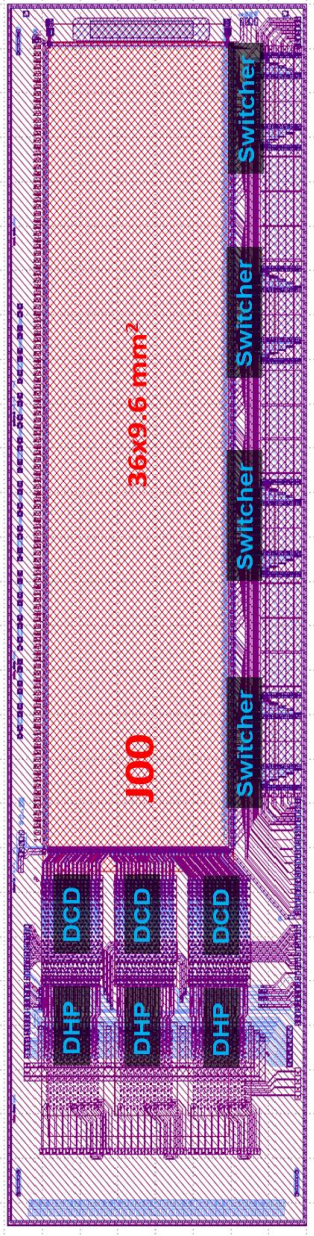
DCDBv2, DHP0.2, SwitcherB1.8G
Speed: 250 MHz
→ Broken during power down

- PXD6 - I00 on Hybrid 6

Capacitive Coupled ClearGate
50x100 µm2 pitch
768 drain lines (256x3 DCD/DHP), only DCD0, DHP0 assembled
120 gate/clear lines (4 Switcher)

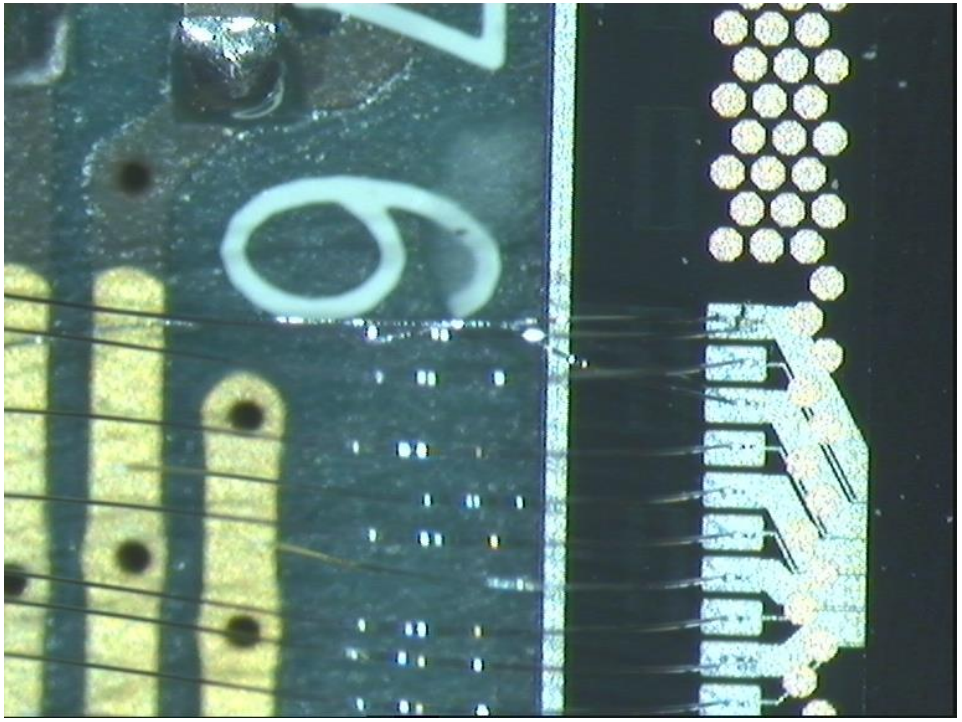
DCDBv2, DHP0.2, SwitcherB1.8G
Speed: 250 MHz

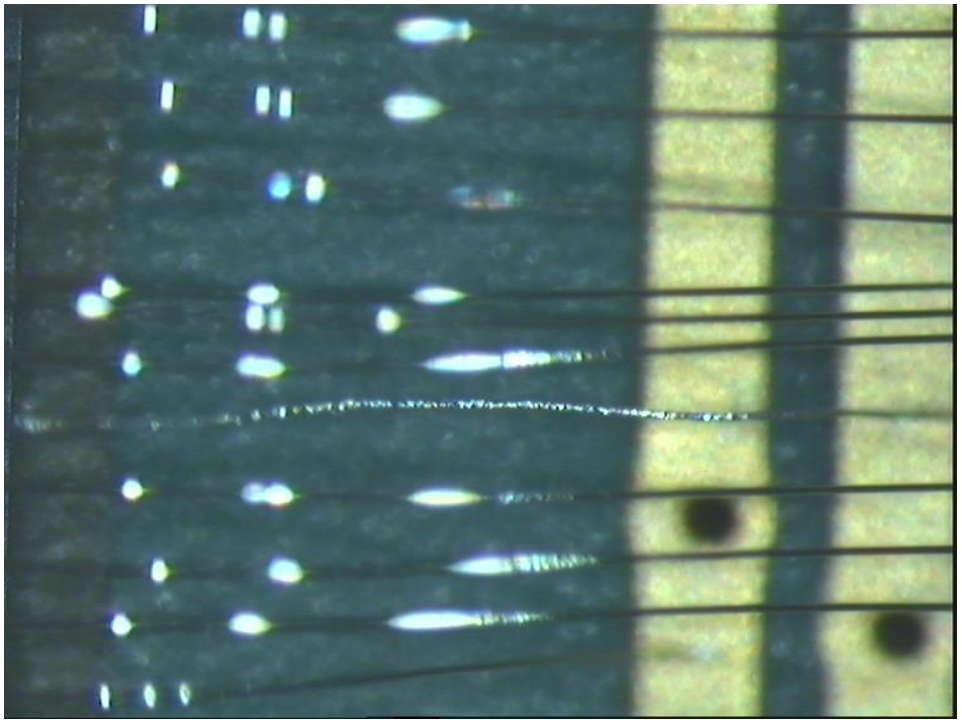
- DHE and Power Supply



Melted Wirebonds

Bug in the power down sequence → Fixed (some wire bonds melted)





Two good options for not melting wirebonds:

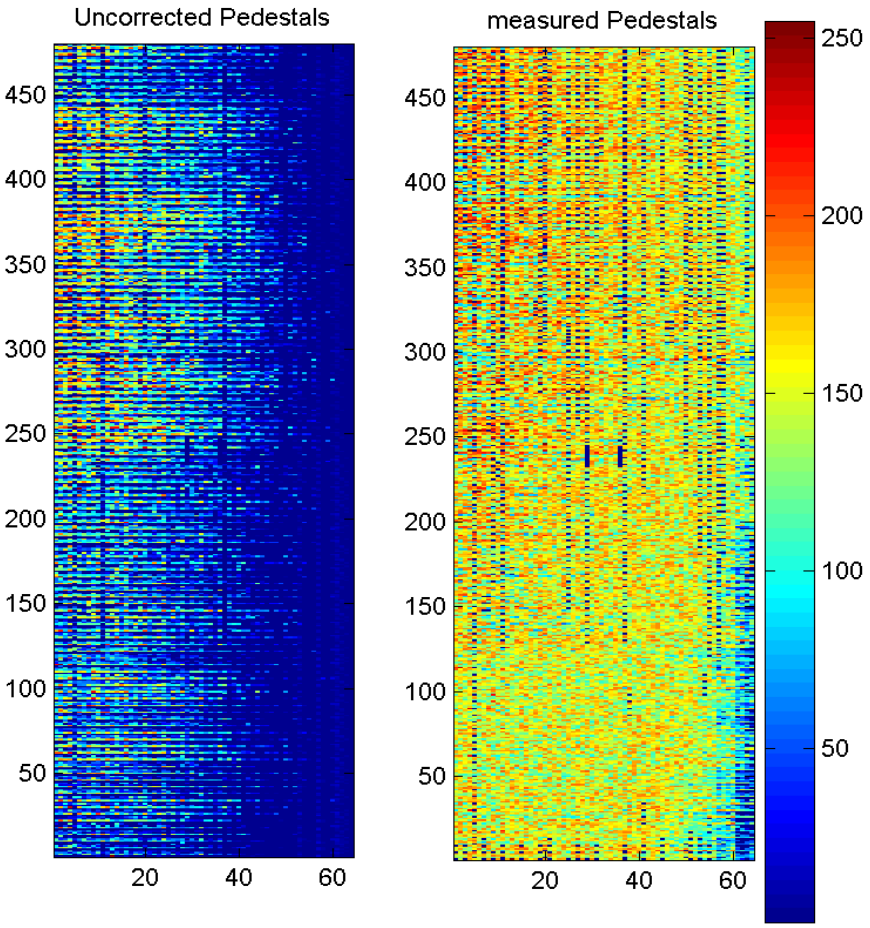
- Instant (emergency) powerdown
- Gracefull (slow) powerdown **with current limits**

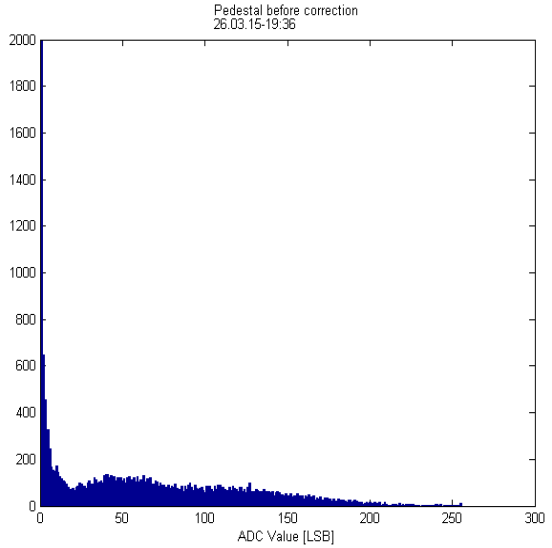
A bad option for not melting wirebonds:

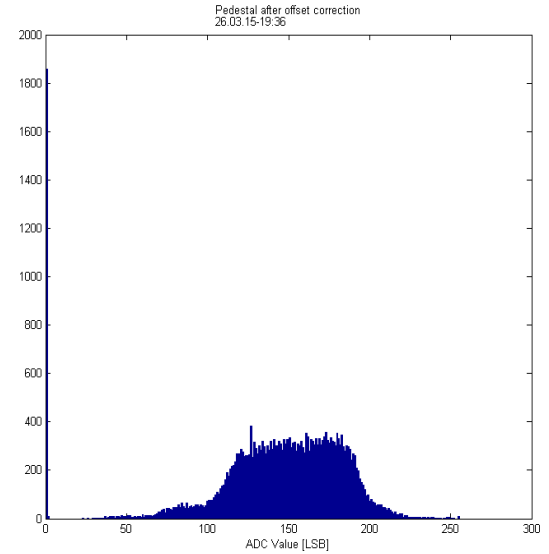
- Rely on the user to not make stupid things

Hybrid 6.0

Pedestal compression I00

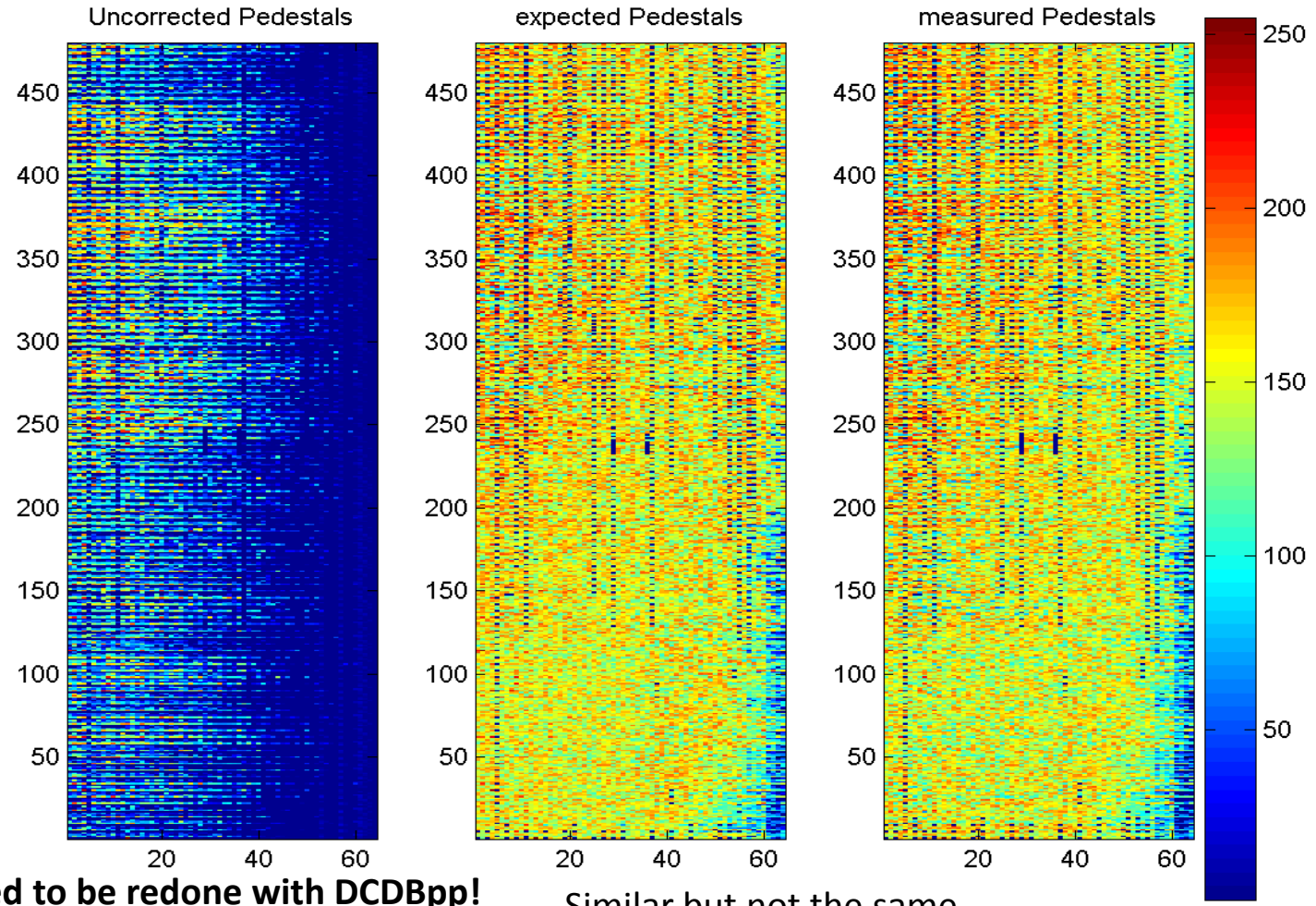






Power routing: the 3 DCDs show different pedestal distribution.
Gradient over columns observed in J00

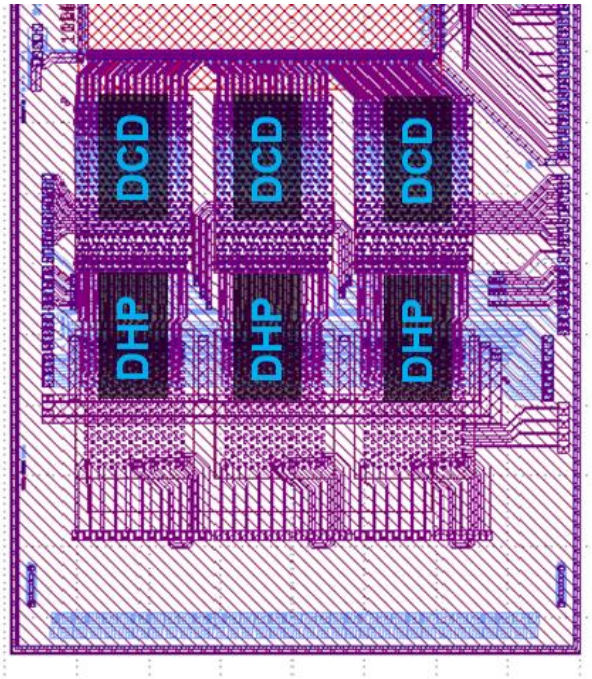
Hybrid 6.0 Offset correction (I00)

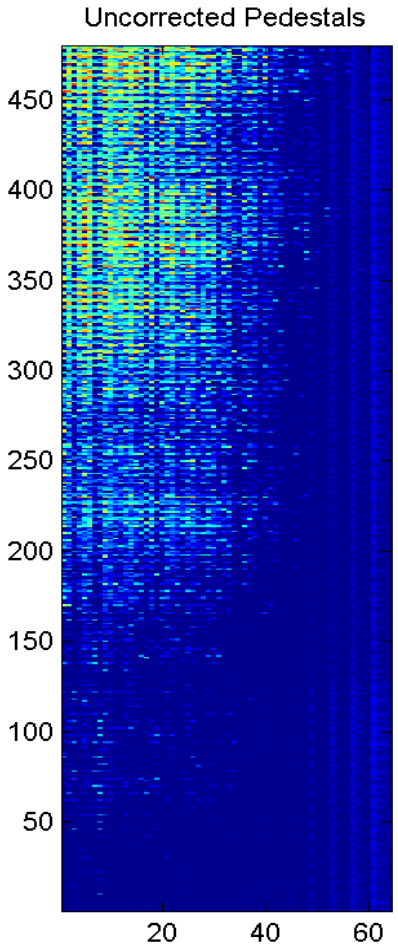


Measurements need to be redone with DCDBpp!
Strength, intersymbol interference etc…

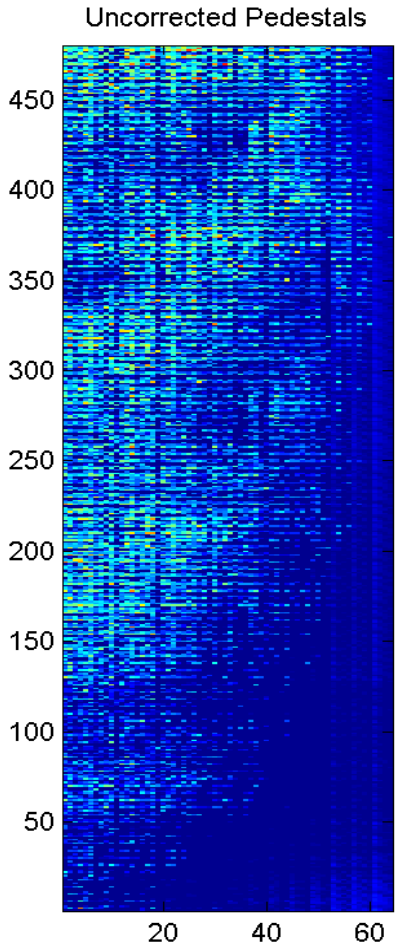
Similar but not the same.
Offset DAC can have crosstalk with other offset DAC values or the value it had before.

Hybrid 6.0 DCD Powering and Gradients (J00)

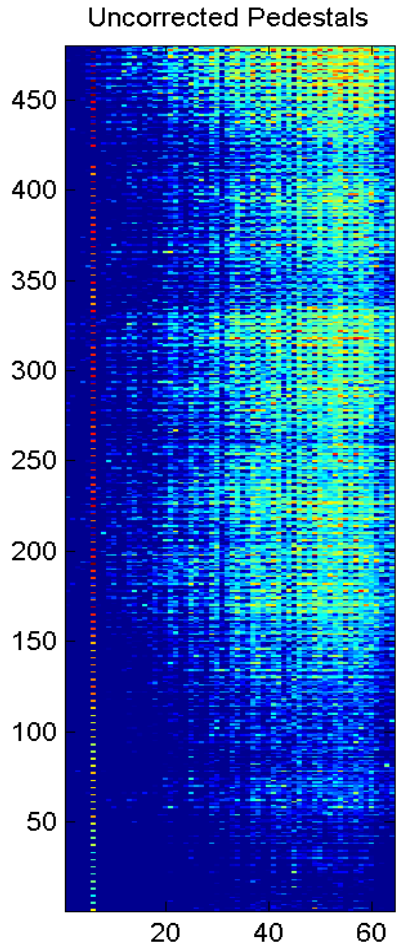




Powered from the left

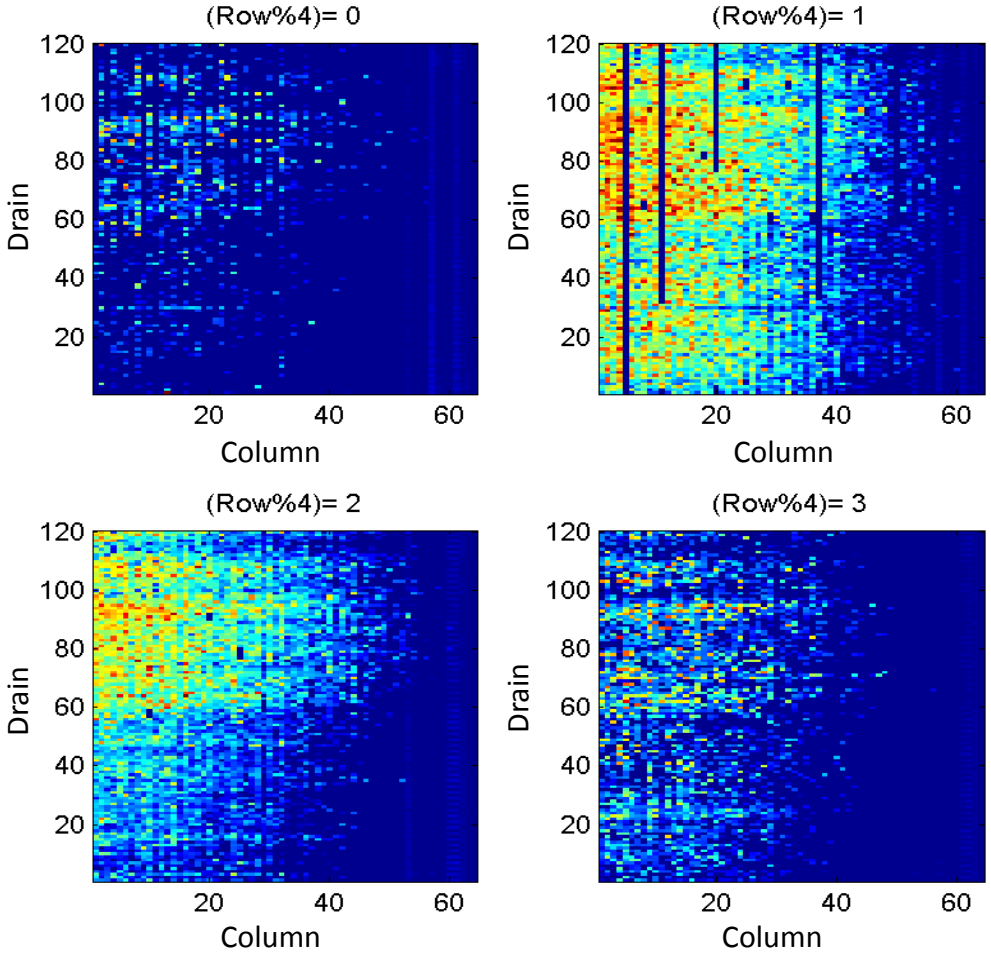


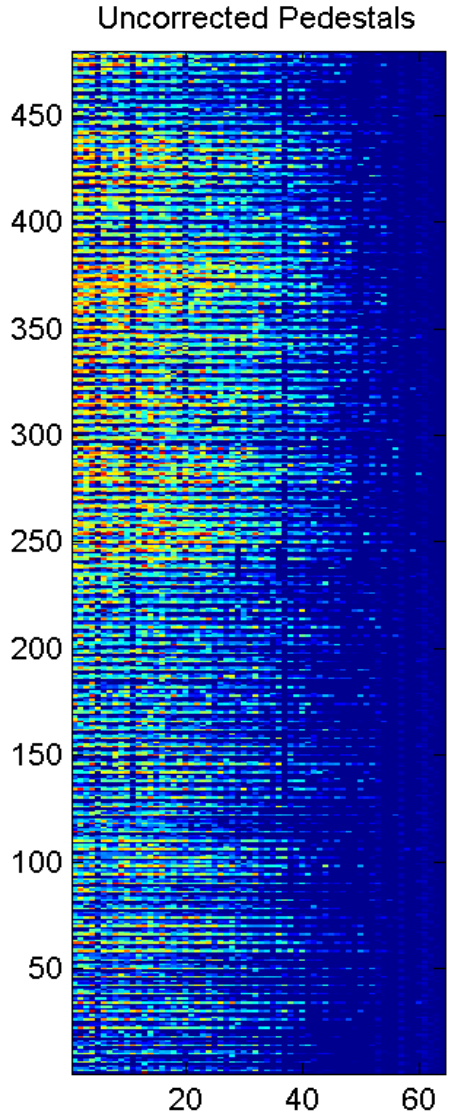
Analog from left
Digital from right



Powered from the right

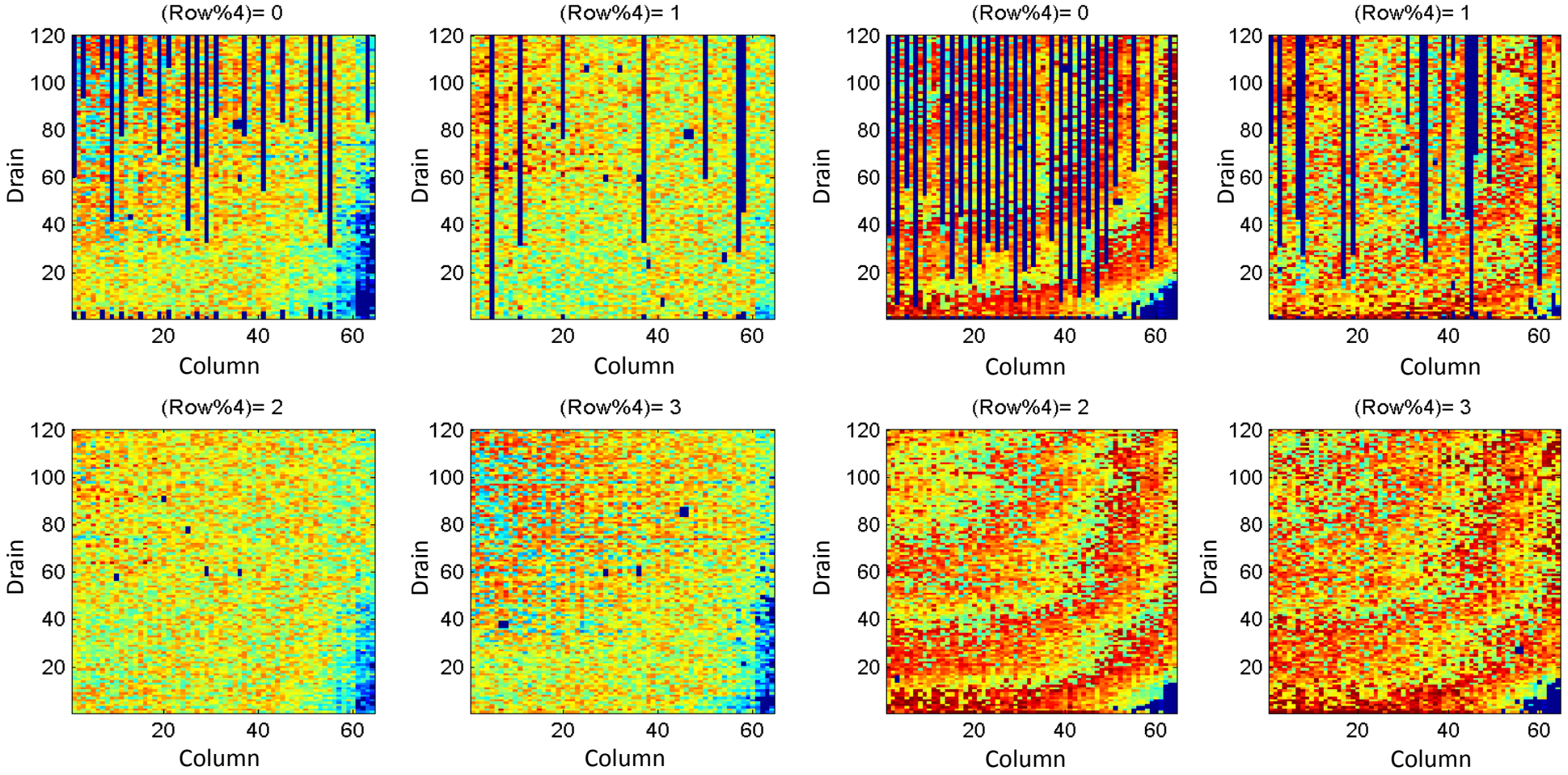
Hybrid 6.0 Rows seperated (I00)





Some pedestal effects are static and could be mitigated by static DAC

Unconnected drains



I00 DCD0 **J00 DCD0**

Conclusions

- Offset:
  - Mapping done
  - Delay scan almost done
  - **Some Values show up in wrong gate -> Unknown reason**

- Powering:
  - Needed to power up one by one?
  - For DHPT not
  - For DCDB not
  - Possible with LMU PS?

- DCDB is not configured after power up
  - Ivan working on this Issue

- Static differences on PXD6 observed, expected for PXD9 (even/odd row)
  - Possibility of having a static offset bit in DCDB?

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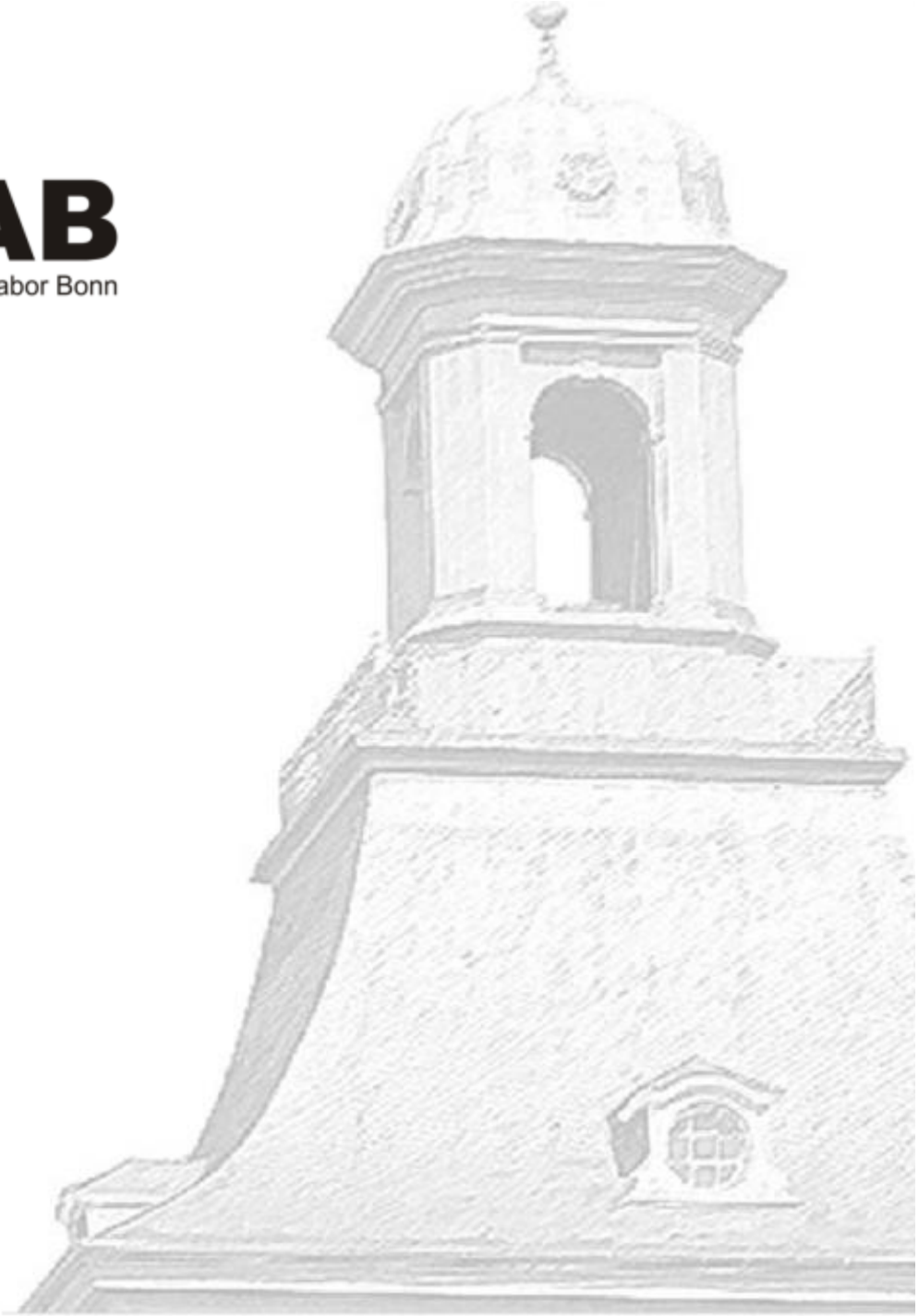

Thank you

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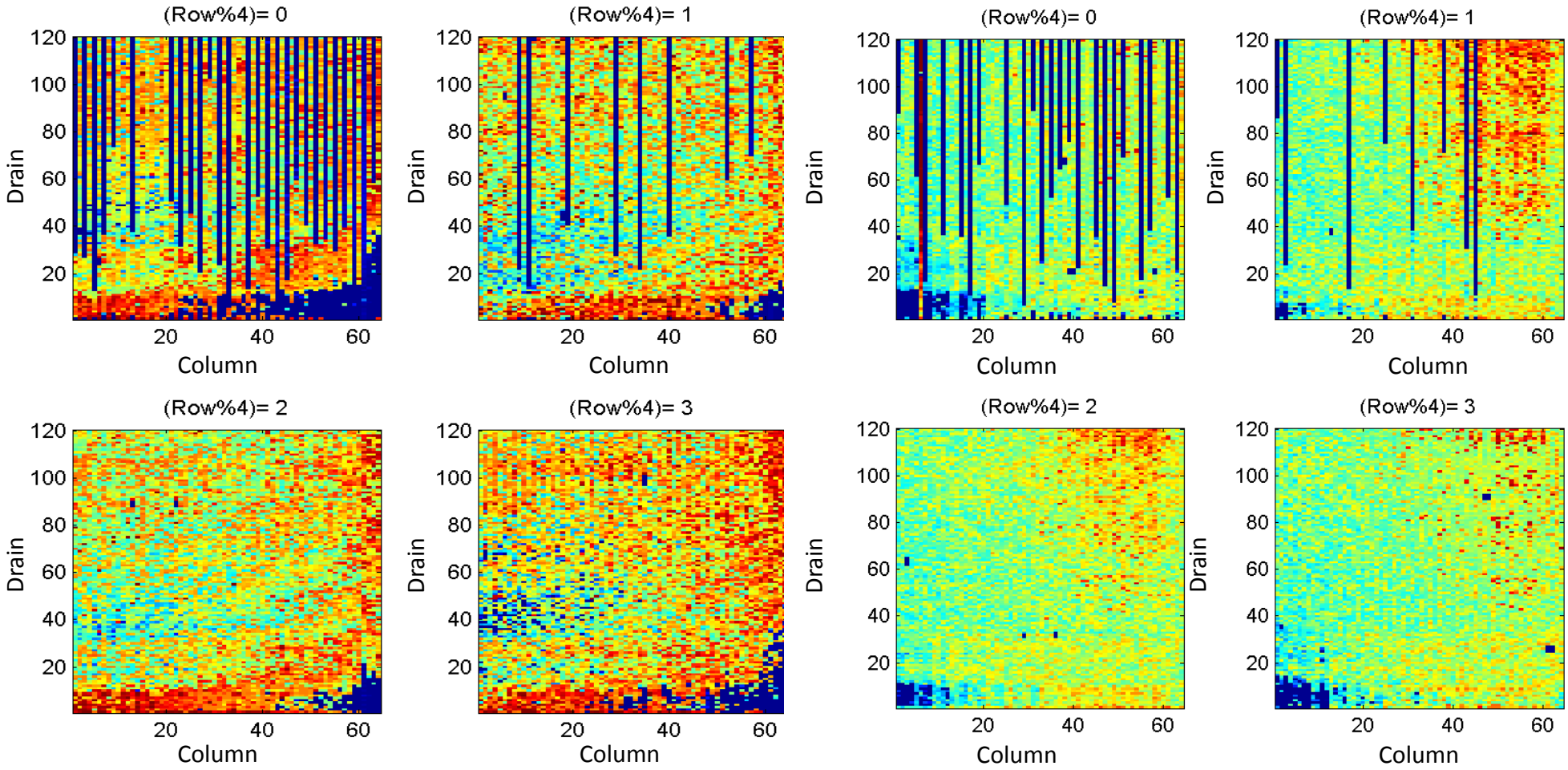
Unconnected drains



J00 DCD1 **J00 DCD2**

Pedestal pattern projected (I00)