

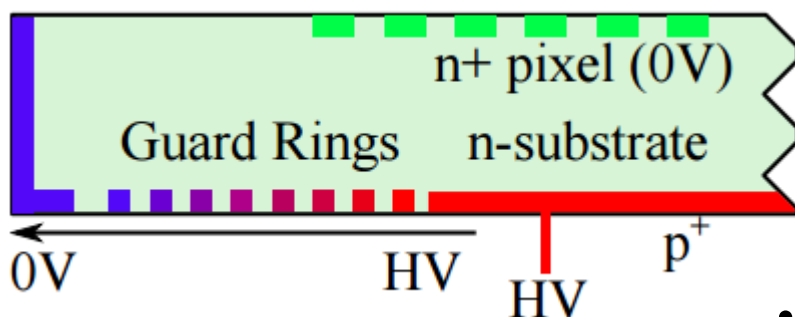
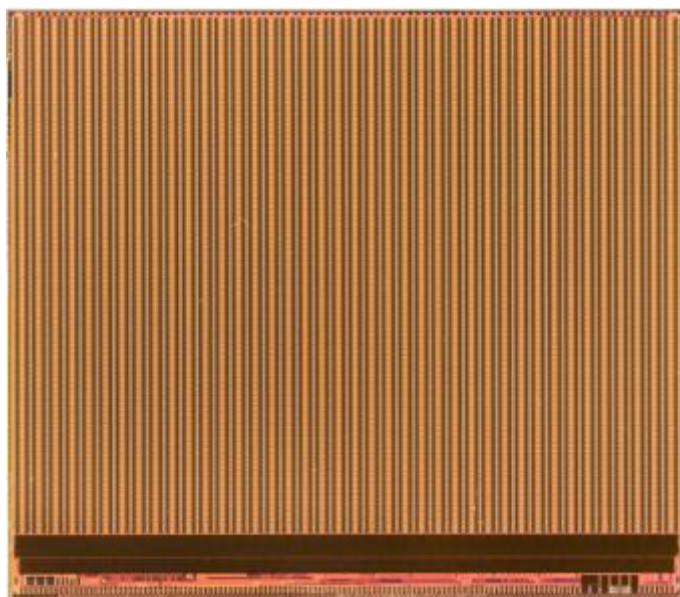


# FANGS for BEAST

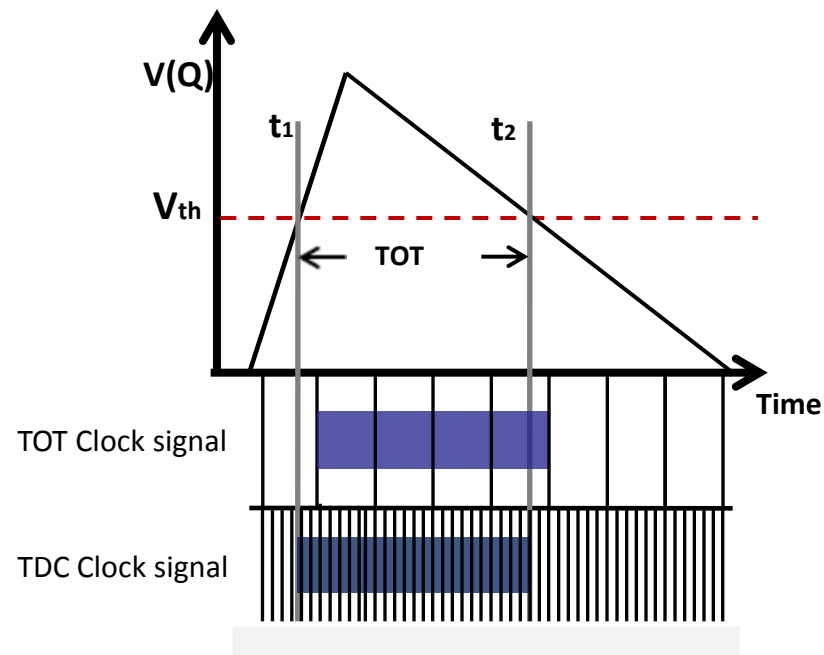
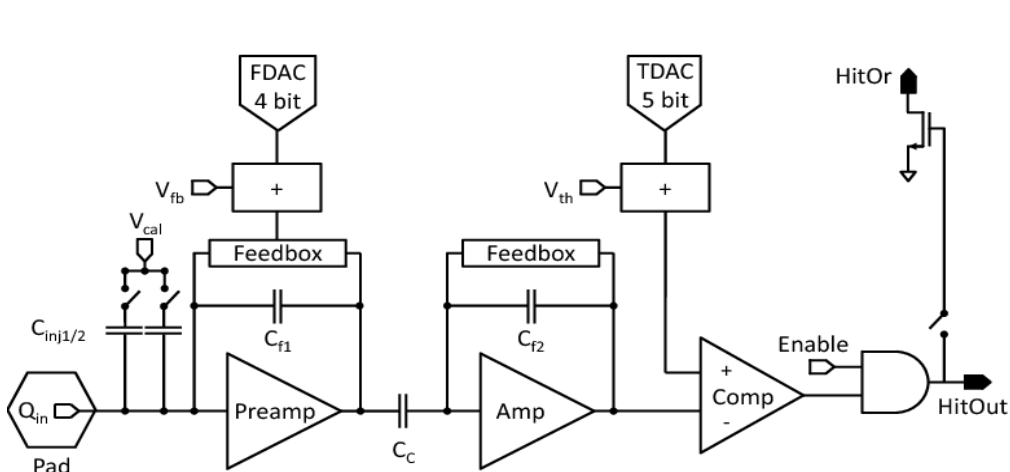
J. Dingfelder, A. Eyring, Laura Mari,  
C. Marinas, D. Pohl

University of Bonn



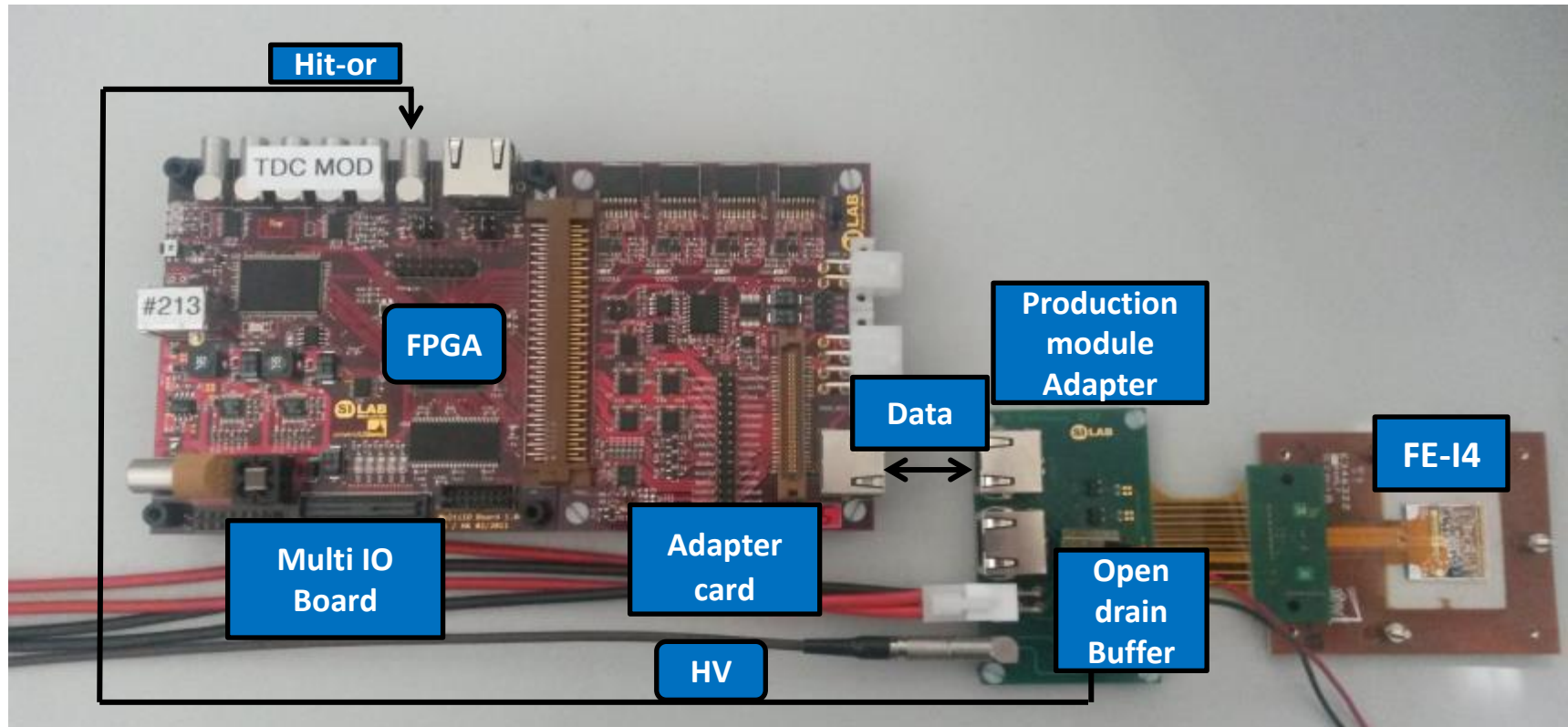


- FE-I4 read out chip
  - **High hit rates and radiation hard**
  - IBM 130 nm CMOS process
  - Provides read out for 80x336 pixels
  - Thickness=150  $\mu\text{m}$
  - Physical size=**21x19 mm<sup>2</sup>**
  - Bump bonded to Si sensor
- Sensor:
  - n-in-n planar
  - Pitch=**50x250  $\mu\text{m}^2$**
  - Thickness=200  $\mu\text{m}$
  - Physical size=19x20 mm<sup>2</sup>
  - HV=60 V
  - Power=1.2 W
- Background radiation measurements in Phase 2:
  - Sensitive to low keV X-rays (6 keV to 60 keV)
  - Particle rates (25 ns)

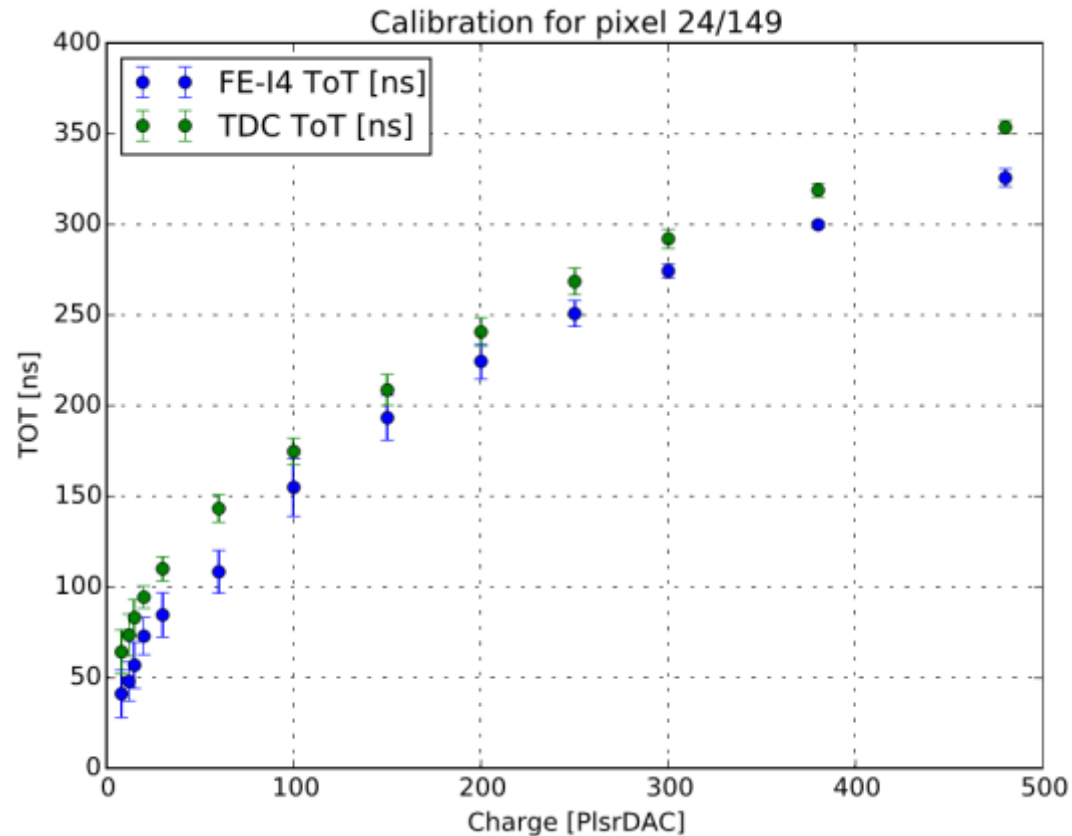


- Two stage amplifier → Discriminator with adjustable threshold.
- Time over threshold (**TOT**) with externally supplied 40 MHz clock.
- Time to digital converter (**TDC**) uses 640 MHz FPGA clock.
- Output of each pixel is ORed.
- Internal charge injection circuit for threshold tuning and calibration

→ Both, high speed and adequate energy resolution achieved at the same time

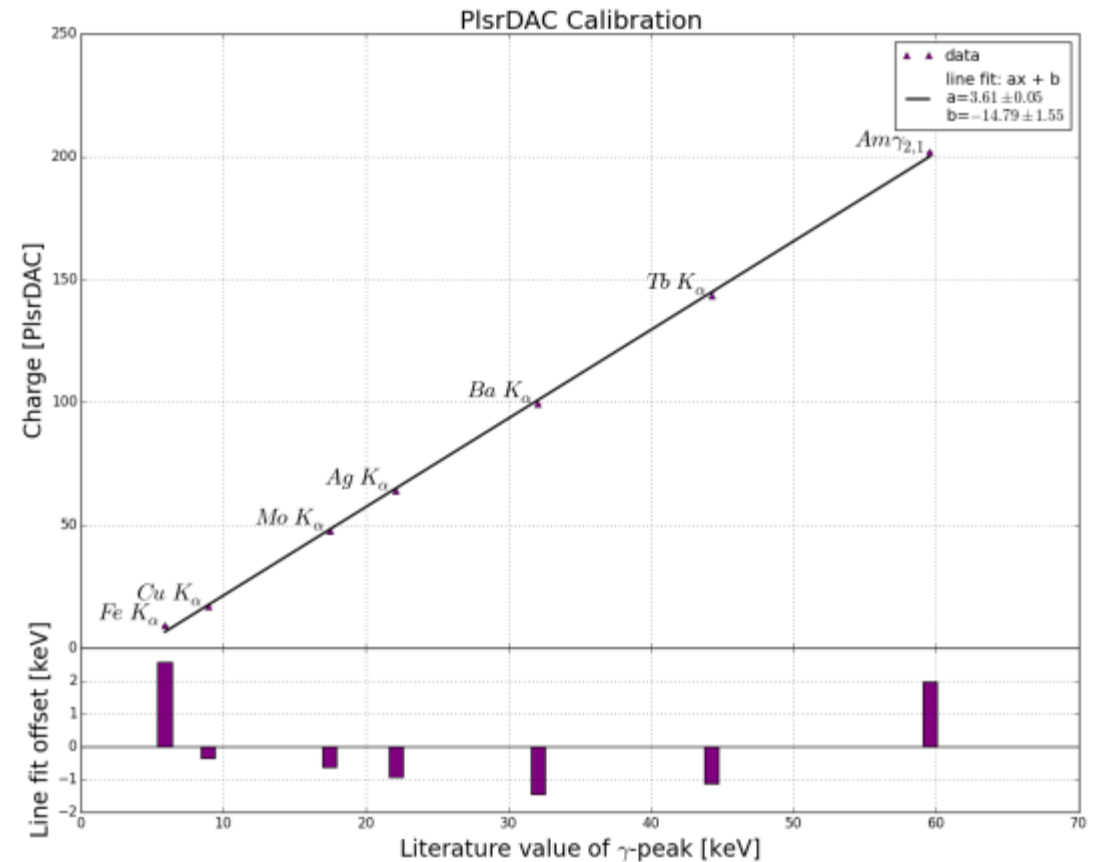
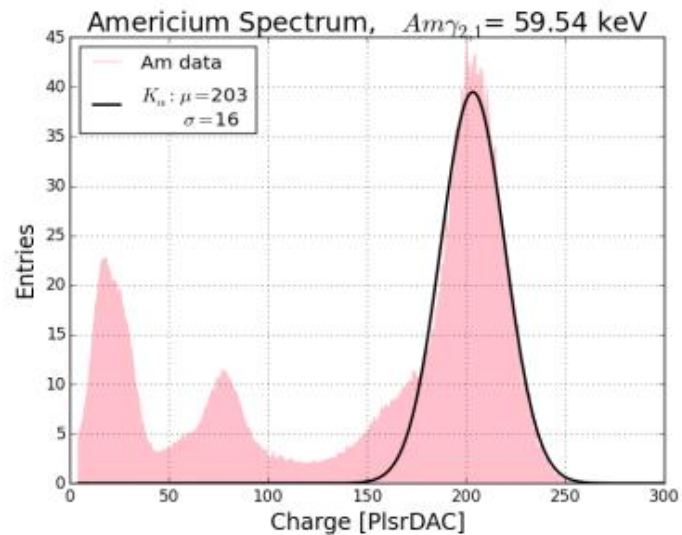
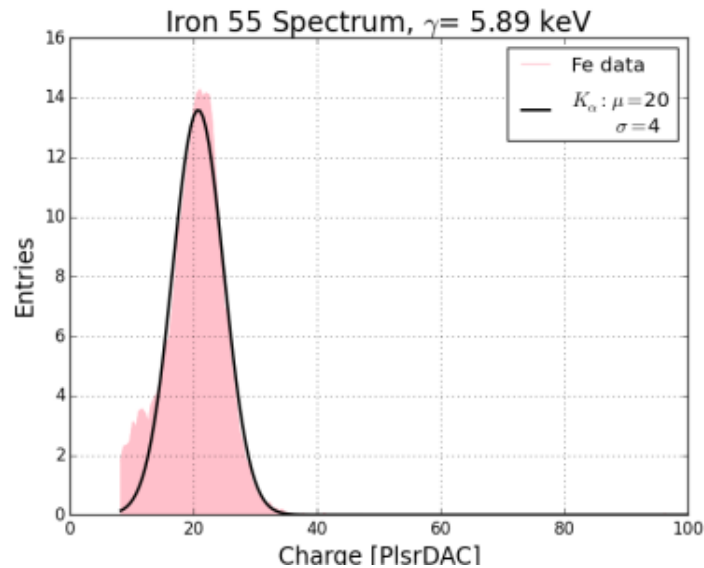


- USBpix used for readout and pyBAR for analysis.
- **Open drain buffer** amplifies HitOr signal on long cables (O(30 m)).
- New USBPix3 readout system being tested at the moment (8 FE at a time).
- Software allows to monitor multiple FE in parallel.

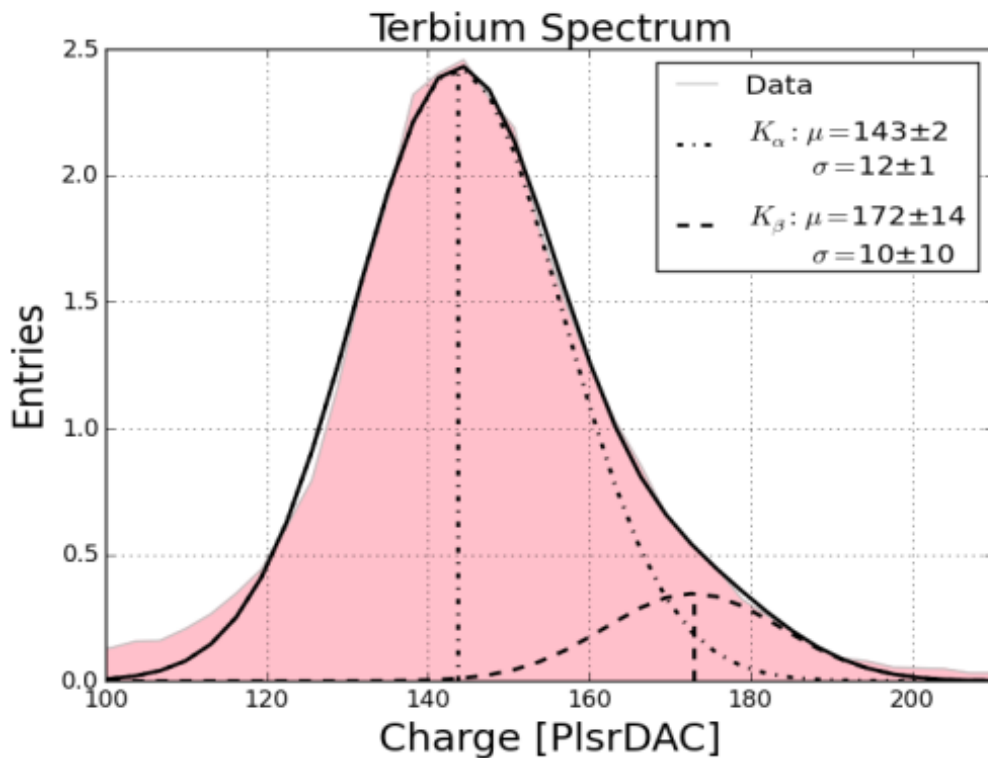


- Threshold tuning noise based
- $V_{th}$  and TDC as a function of charge different for each pixel.
- Per pixel calibration needed.
- Internal charge injection in units of PlsrDAC  $\sim 55$  electrons

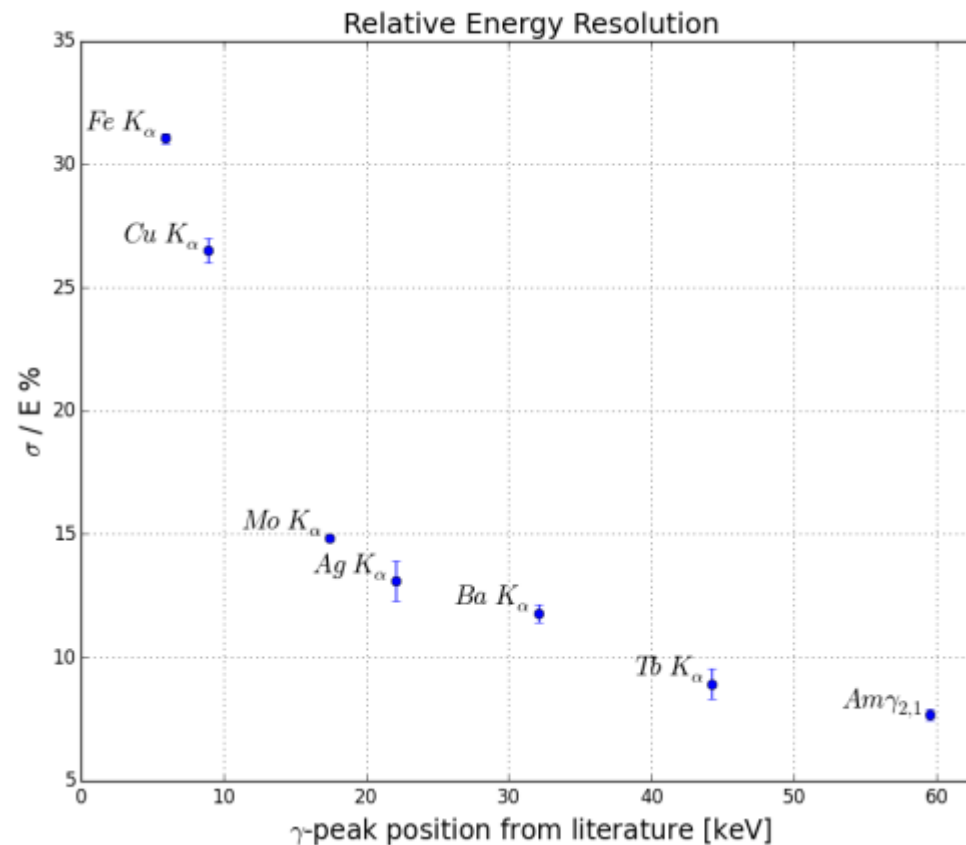
# Calibration and Dynamic Range



- Wide dynamic range covered (wider also possible)
- Lowest measured plsrDAC value  $\sim 7$ 
  - Threshold of  $\sim 1000$  electrons feasible



- Terbium  $K_\alpha = 44.23 \text{ keV}$ ,  $K_\beta = 50.65 \text{ keV}$
- $\Delta E = 6.42 \text{ keV}$



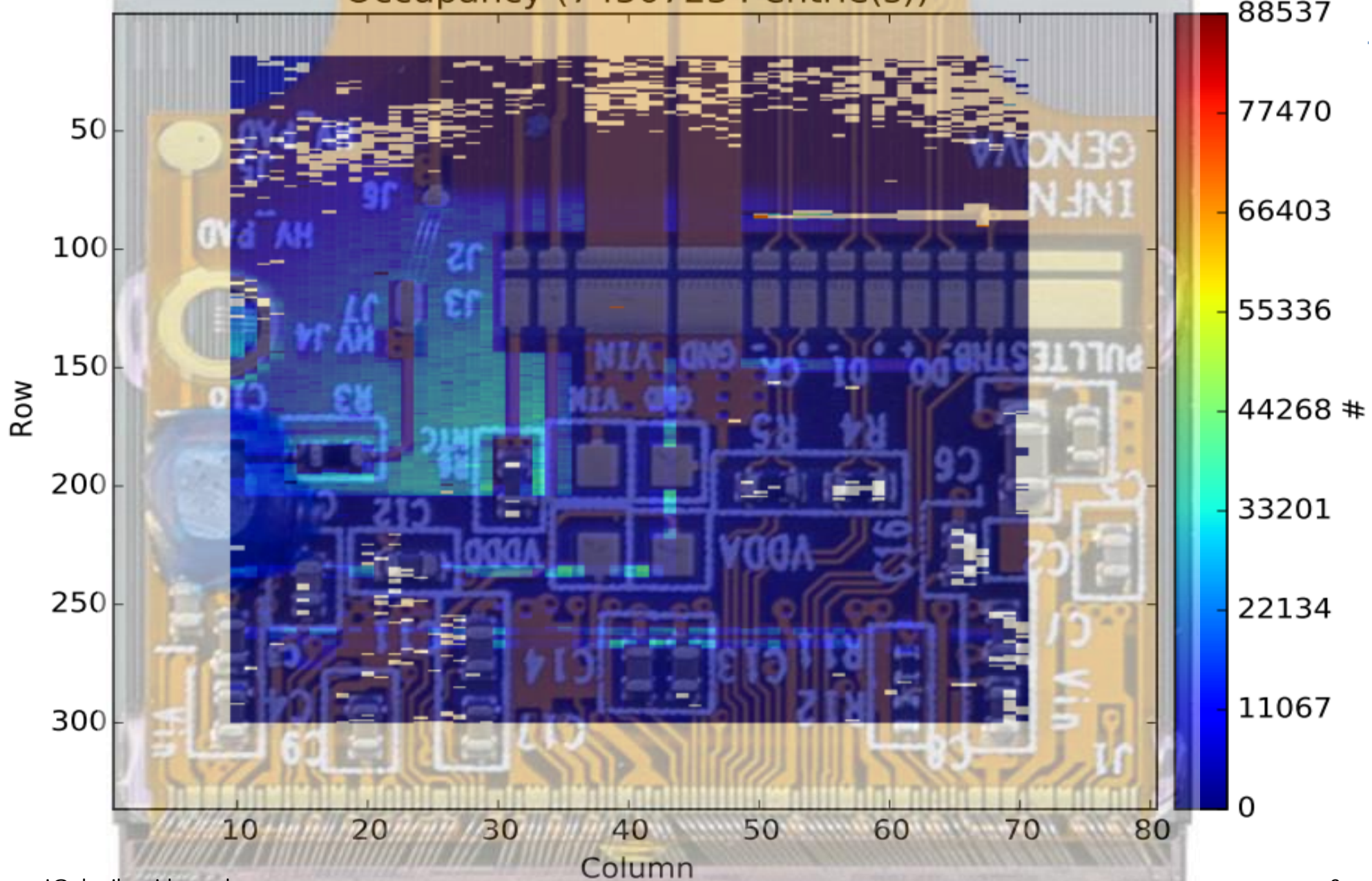
- Adequate energy resolution
- Better than 15 % above 10 keV



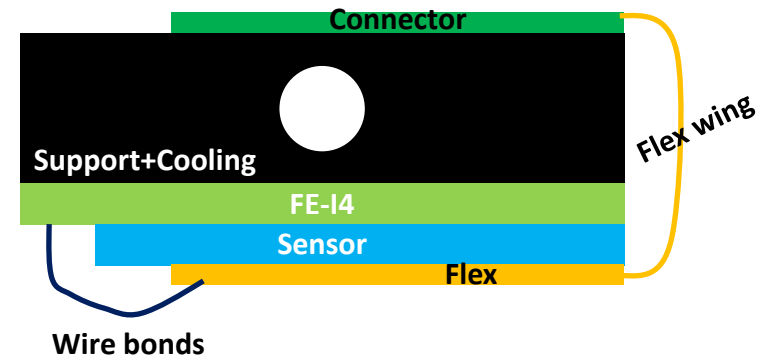




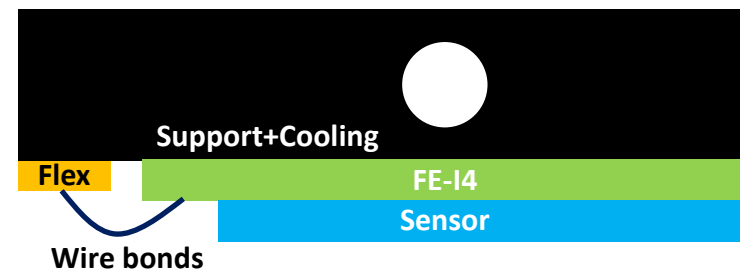
Occupancy (74507234 entrie(s))



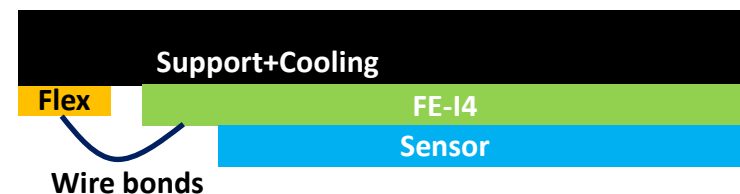
- How to mount few single chips in Phase 2?  
(Reusing existing infrastructure)



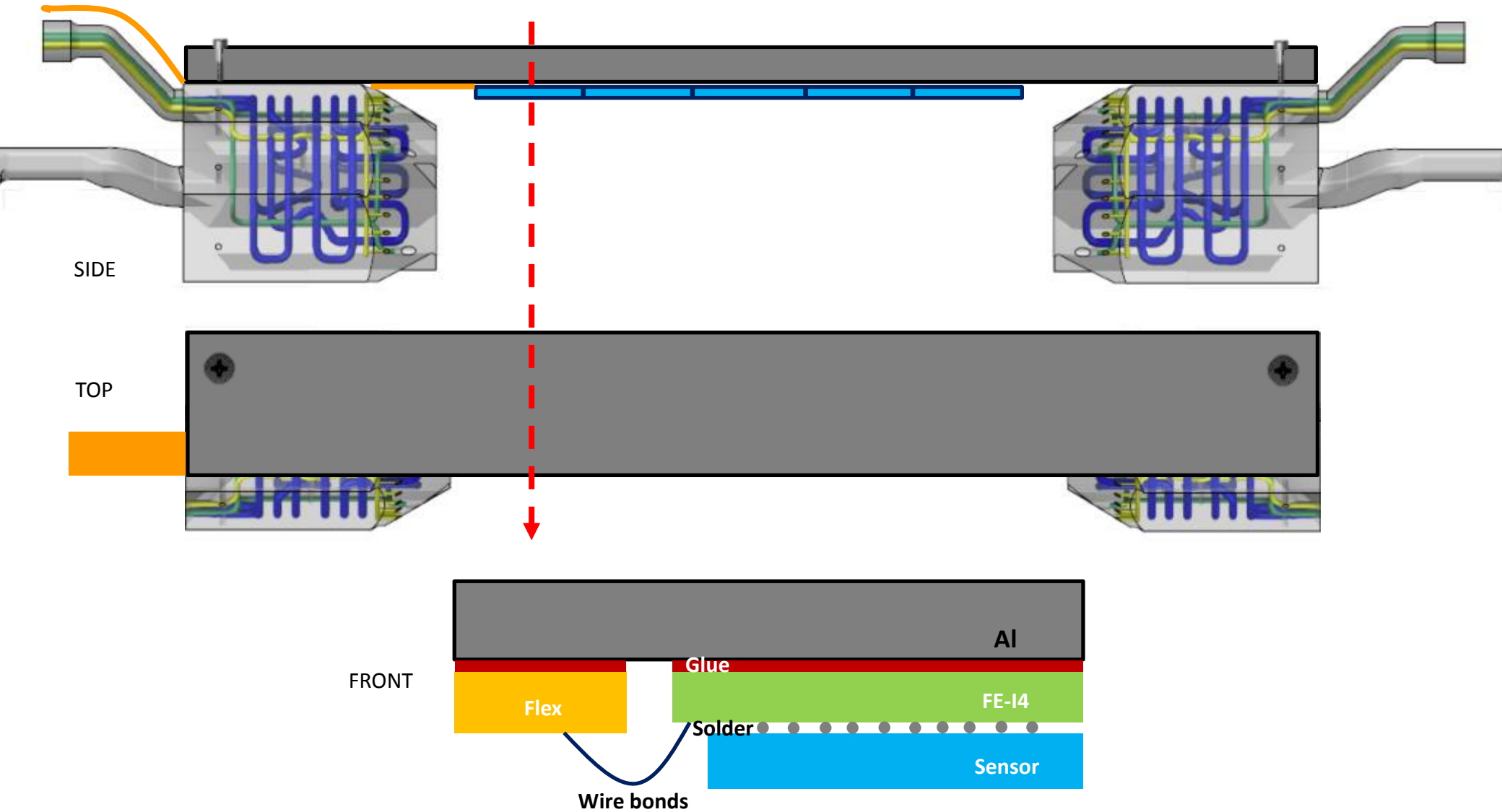
- Move the flex to one side. No material in front!

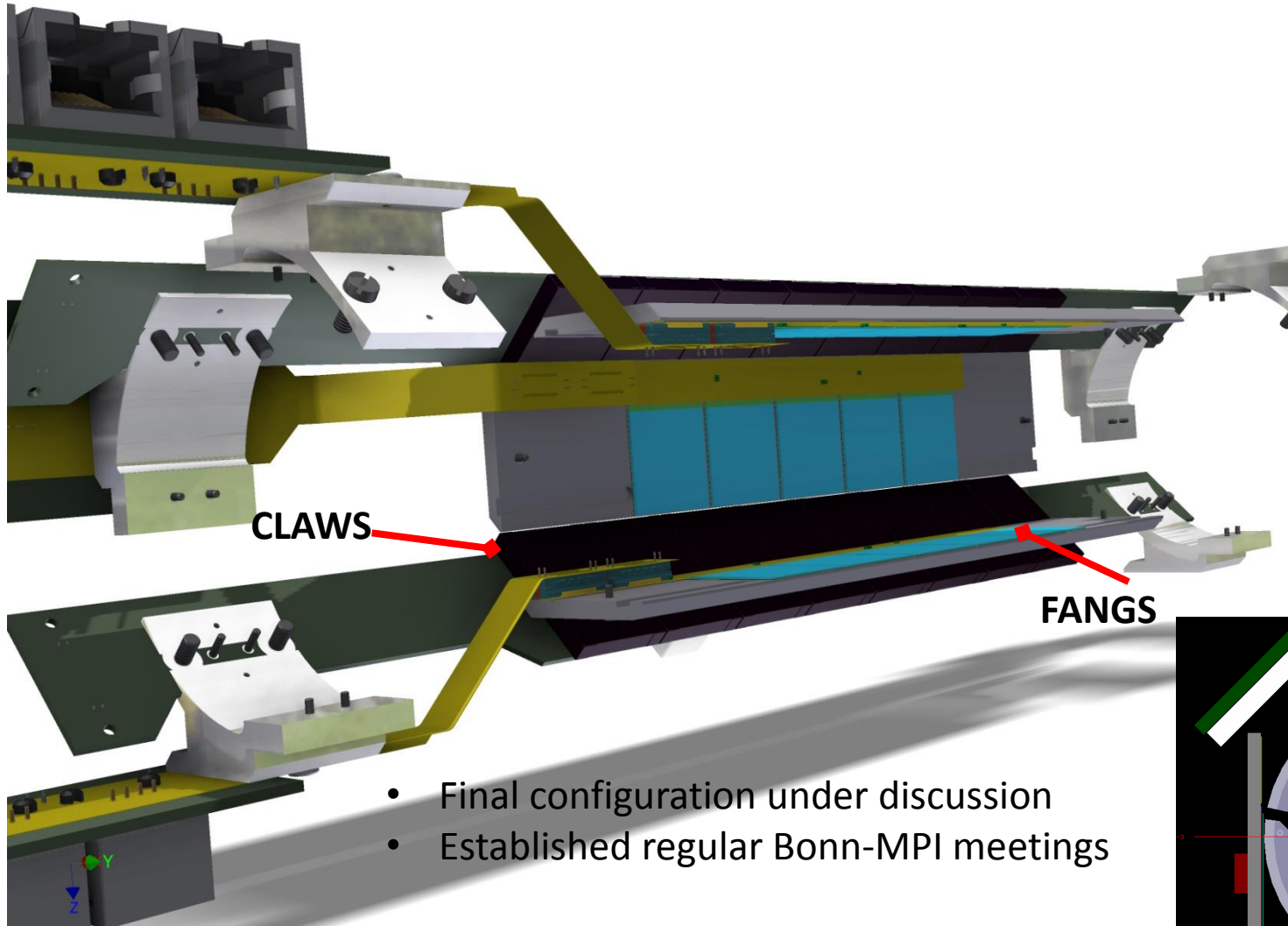


- Thinner support. Make use of PXD cooling



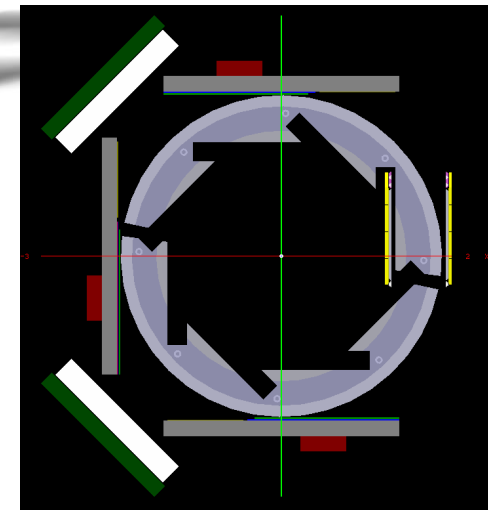
# Mechanical Arrangement

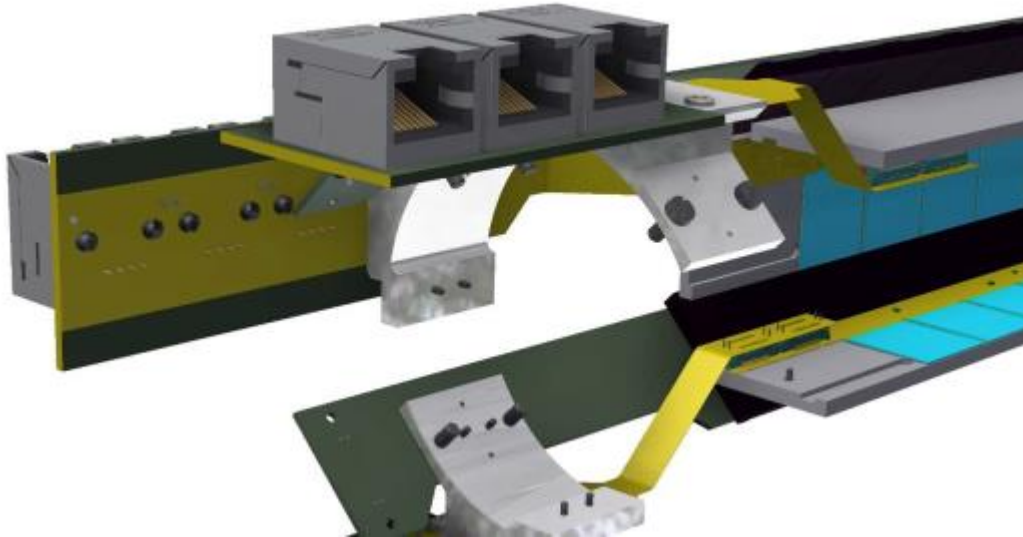




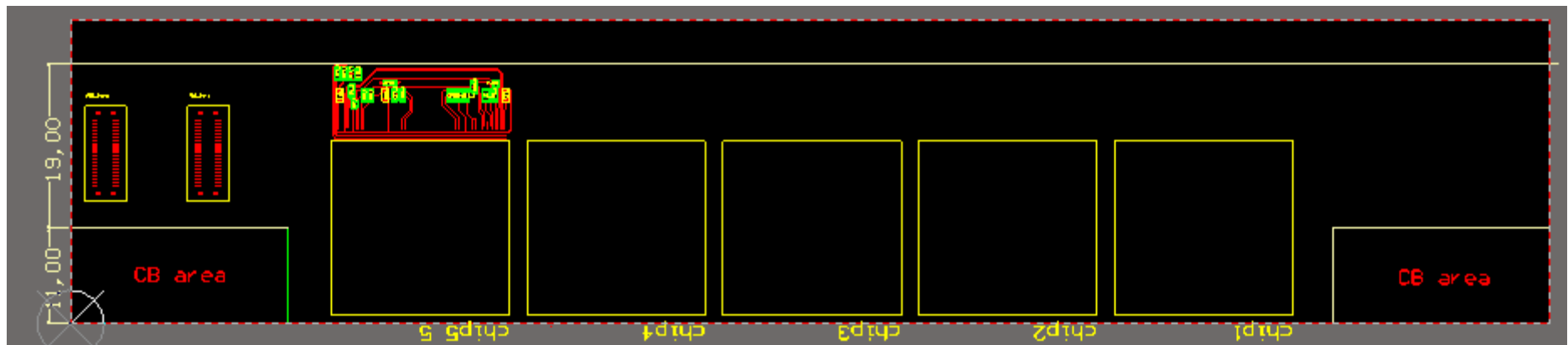
- Final configuration under discussion
- Established regular Bonn-MPI meetings

CAD integration by K. Ackermann (MPI)  
BASF2 implementation M. Ritter (KEK-MPI)

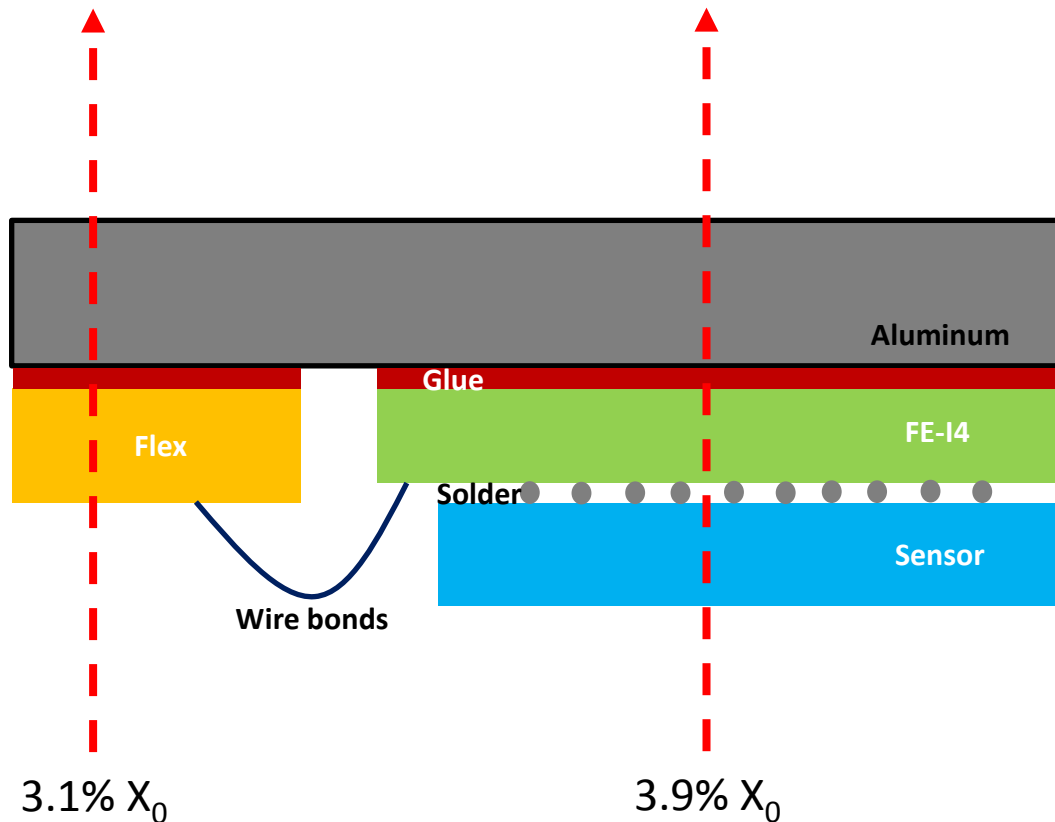




- ❑ Design still evolving:
  - 8 mm wide Kapton
  - 2 x 40 pin connector on backward side
  - Short intermediate Kapton connecting to a PCB attached to SVD ring
  - 4 Ethernet and 1 power connectors on PCB



# Aluminum Stave Material Budget



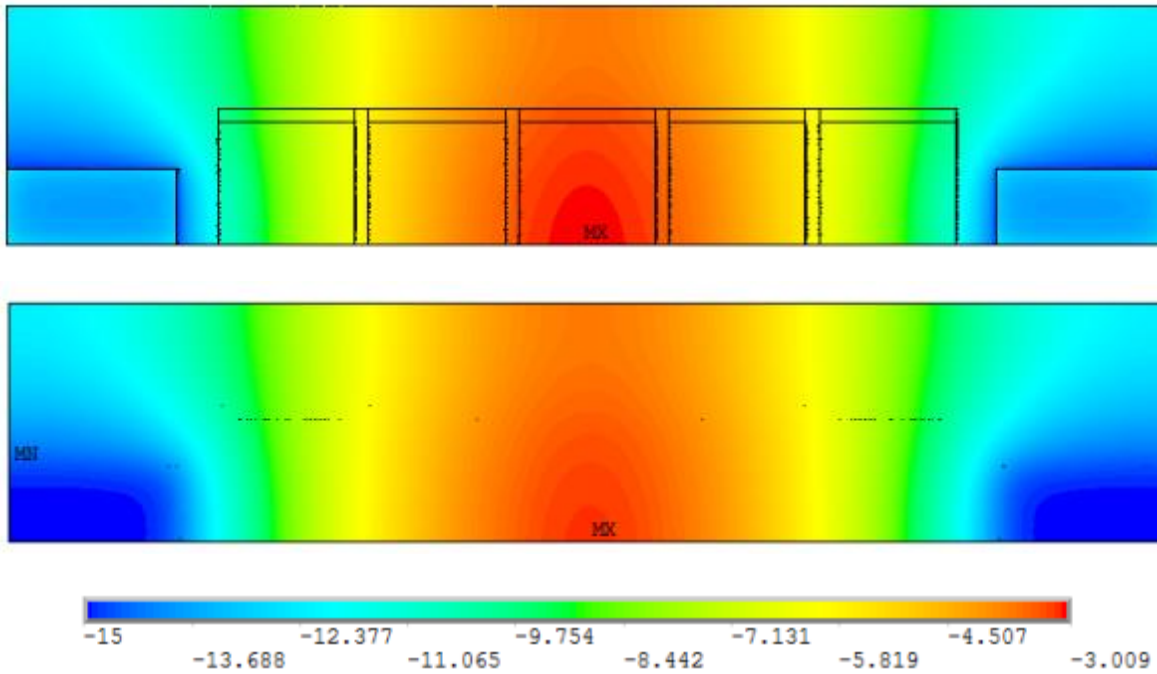
- Low and flat material budget distribution
- No impact in outer detectors

Reminder: PXD+SVD contribute with  $\sim 4.0\% X_0$

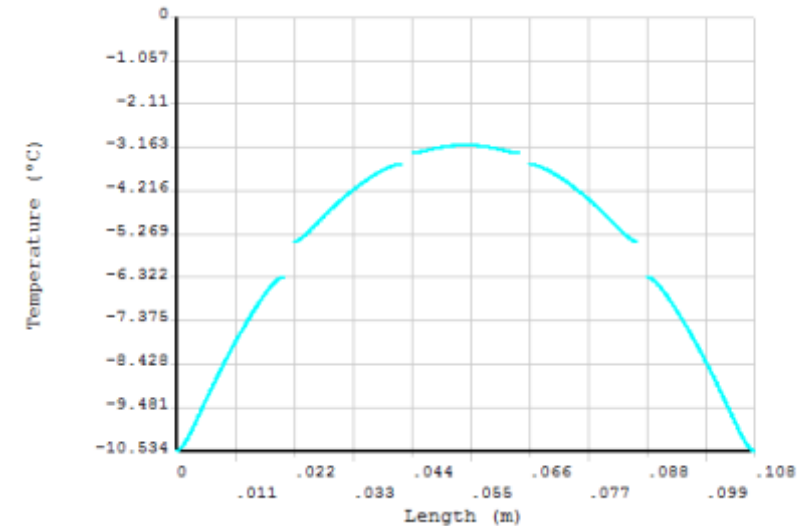
- Support:  
3 mm thick Aluminum  $\rightarrow 3.4\% X_0$
- Epoxy:  
50  $\mu\text{m}$  thick  $\rightarrow 0.014\% X_0$
- FE-I4  
150  $\mu\text{m}$  thick  $\rightarrow 0.16\% X_0$
- Sensor:  
200  $\mu\text{m}$  thick  $\rightarrow 0.21\% X_0$
- Solder balls  
SnAg  $\rightarrow 0.17\% X_0$  (3.3% of the area)
- Flex (or 500  $\mu\text{m}$  PCB)  
66  $\mu\text{m}$  thick polyimide  $\rightarrow 0.023\% X_0$   
24  $\mu\text{m}$  Cu (2 layers)  $\rightarrow 0.17\% X_0$



# FEA of a FANGS (AI-based) Stave



FANGS for BEAST, C. Marinas (University of Bonn)



- Maximum temperature =  $-4\text{ }^{\circ}\text{C}$
- Maximum  $\Delta T$  within one sensor =  $4\text{ }^{\circ}\text{C}$
- Power = 1.2 W each FE
- Cooling block =  $-15\text{ }^{\circ}\text{C}$
- Environment =  $20\text{ }^{\circ}\text{C}$  at 2 m/s

- Proper heat handling
- Low and flat temperature profile

- FANGS is rapidly evolving into a final detector system for background (energy and rates) measurements at BEAST Phase 2
- All the aspects related to the design, characterization, integration are in good progress
- 30 hybrids (FE-I4 and planar sensor) have been prepared (twice what is needed)
- Front end has been **tuned to cover the expected energy range with proper resolution**
- **Multiple-FE DAQ** with long cables is being tested with a new readout system
- Kapton flex and intermediate boards are being designed
- Mechanical concept and cooling management are well in progress

**Thank you**

