PXD9 Pilot run
Metal system characterisation after Al2

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for the MPP/HLL team

DEPFET

Active Pixel Detector

Belle II

Outline

- Motivation
- Description of the measurement system
- Yield information
- System failures
- Conclusion and Future developments

Motivations

1. Test of DEPFET transfer characteristics at the first gate row to get info on:
   - shorts
   - Opens

→ map of the fanout with precise localisation of faults

→ possibility of rework in faulty areas

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1. Test of DEPFET transfer characteristics at the first gate row to get info on:
   - shorts
   - Opens

   → map of the fanout with precise localisation of faults

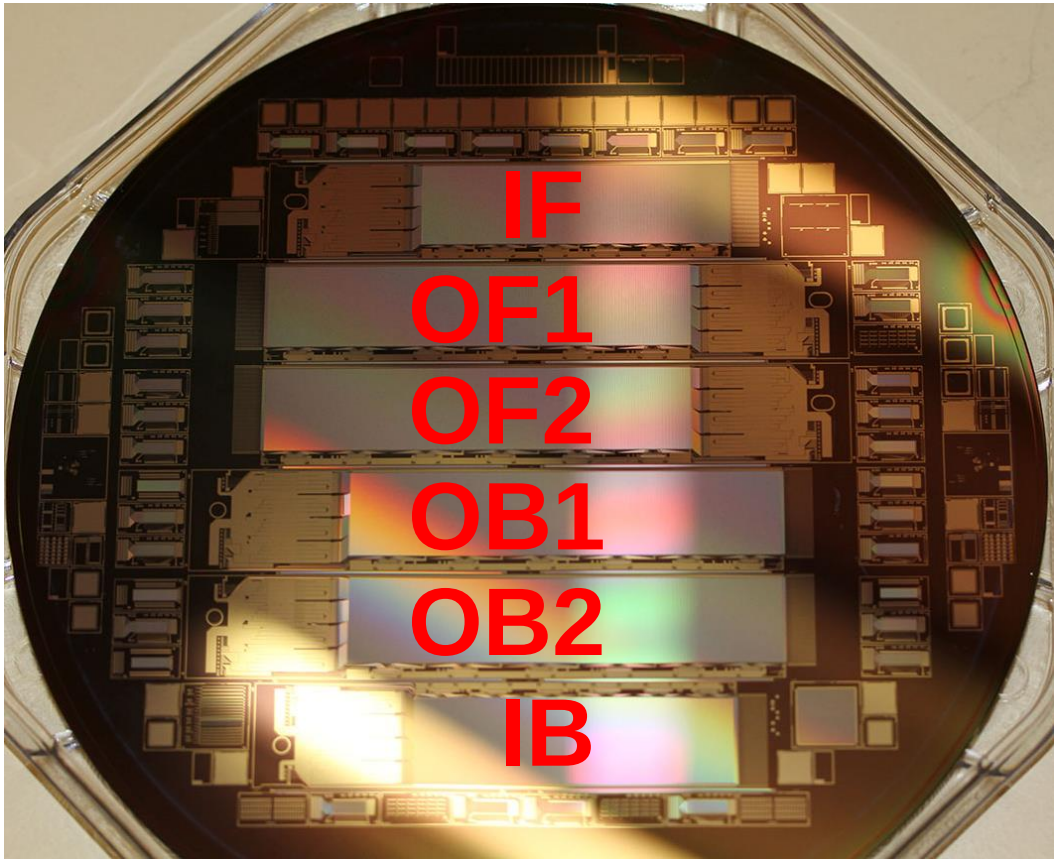
   → possibility of rework in faulty areas

2. Precision measurements at multiple gate rows to get info on:
   - mean current value, pedestal spread
   - threshold voltage and transconductance
   - source contact distance effect

   → Such precision measurements were not foreseen in the first place and are consequently **NOT POSSIBLE WITH THE CURRENT SETUP**

   → The DAQ system needs **substantial improvements** (foreseen for the first half of April)!

Wafer and chip layout

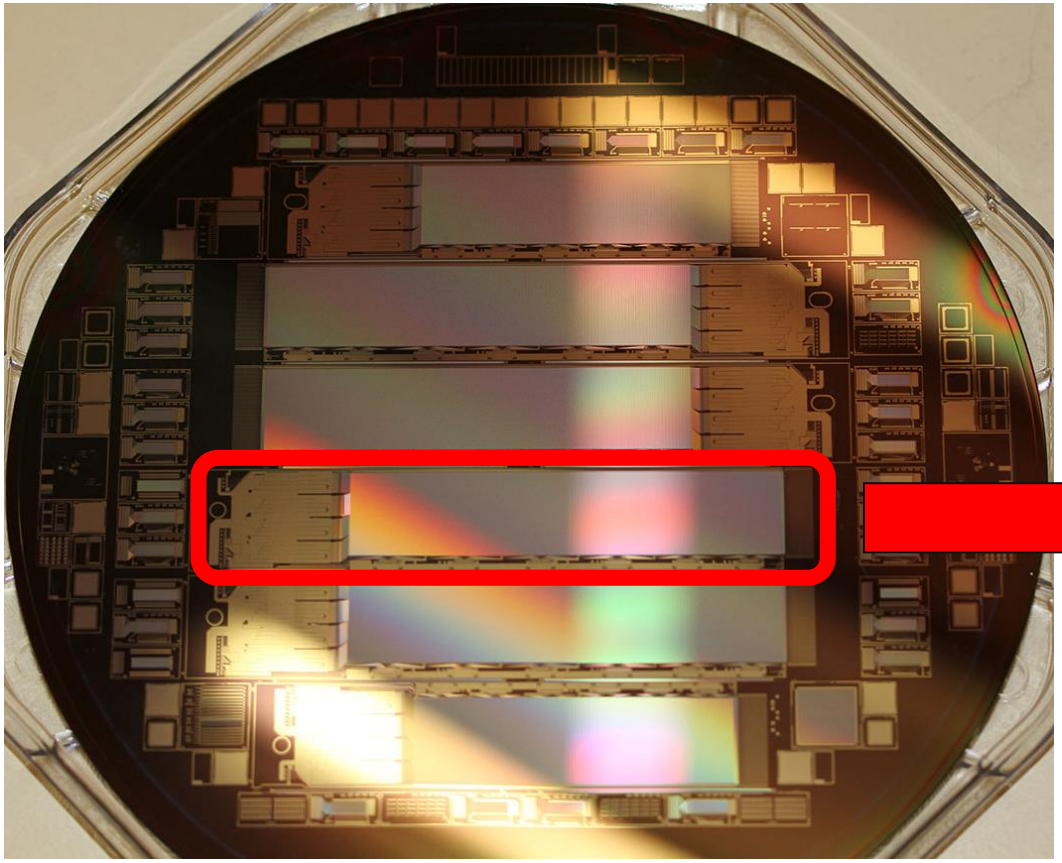


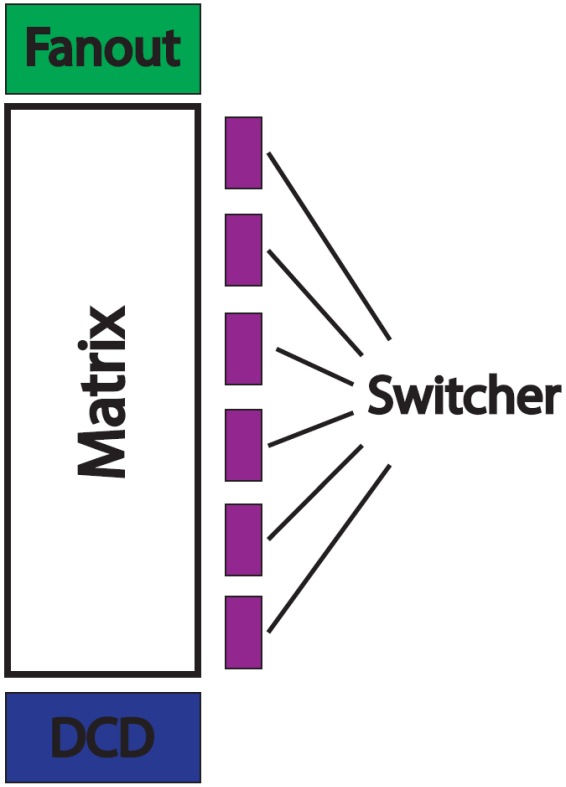
For the pilot run we have 3 wafer: W30,W35 and W36.

Each wafer has 6 modules/chips:

- Inner forward (IF)
- Outer forward (OF1)
- Outer forward (OF2)
- Outer backward (OB1)
- Outer backward (OB2)
- Inner backward (IB)

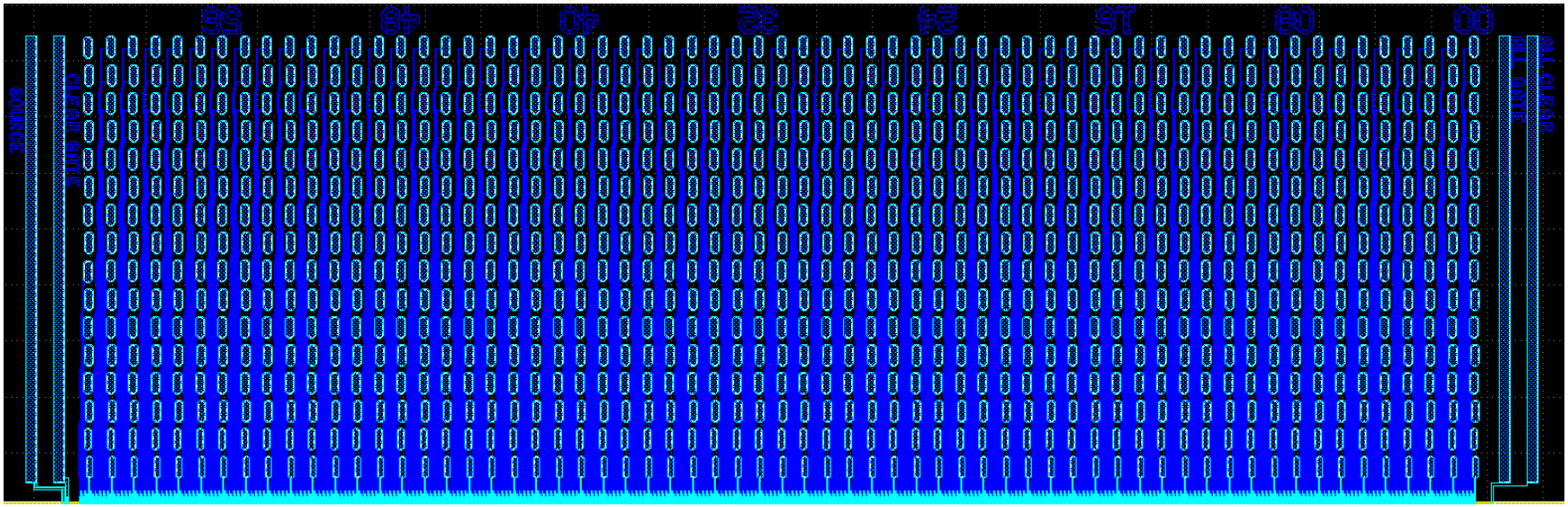
Wafer and chip layout





Fanout of type A (IF, OB1, OB2)

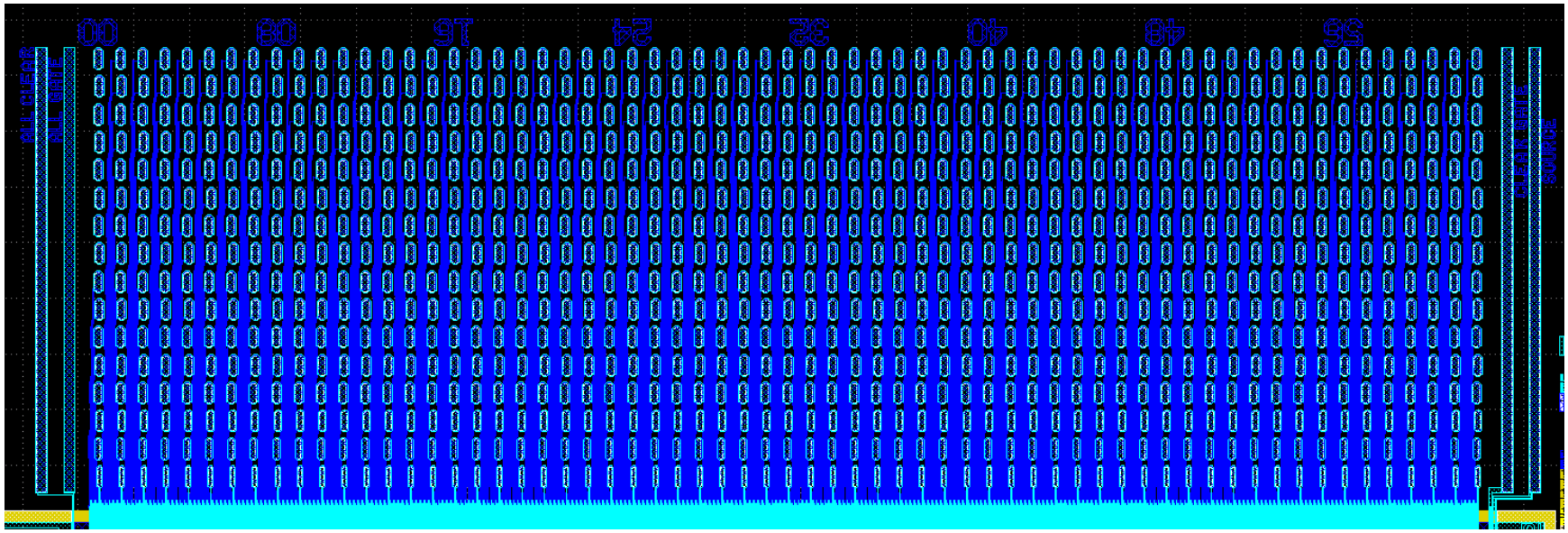
S



Configuration #1:

- SMU2 = All Clear (15V – static voltage 4)
- SMU3 = All Gates (2V – static voltage 3)
- SMU4 = Clear Gate (5V – static voltage 2)
- SMU5 = Source (0V – static voltage 1)

Fanout of type B (OF1, OF2, IB)

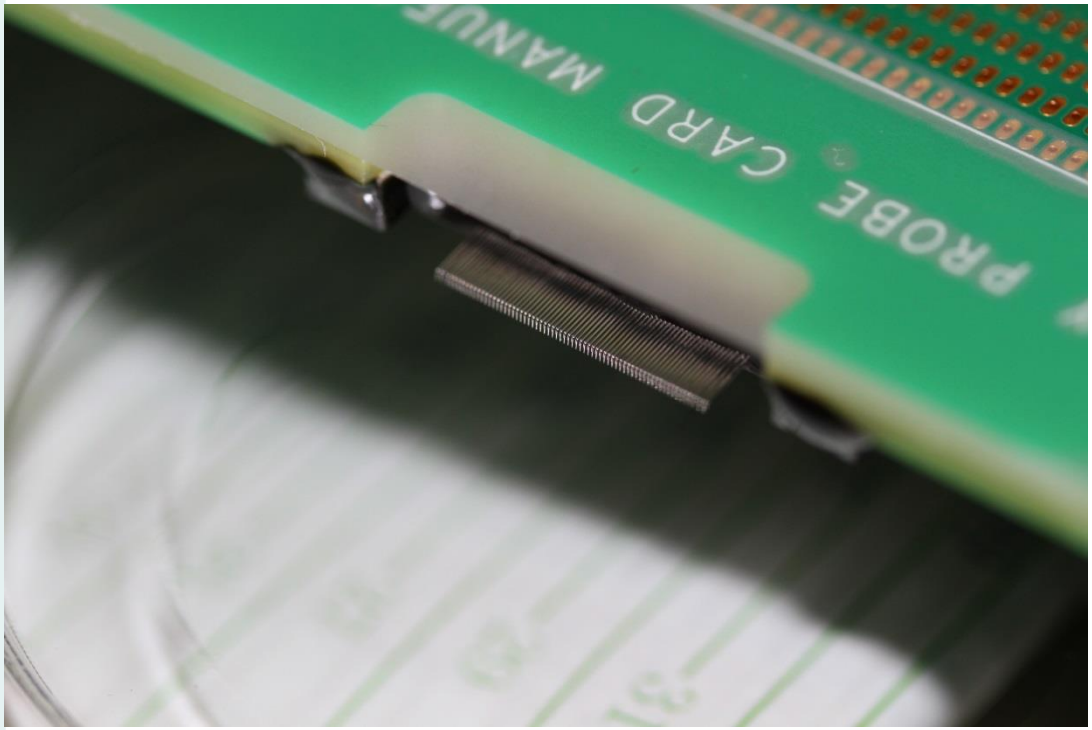


Configuration #2:

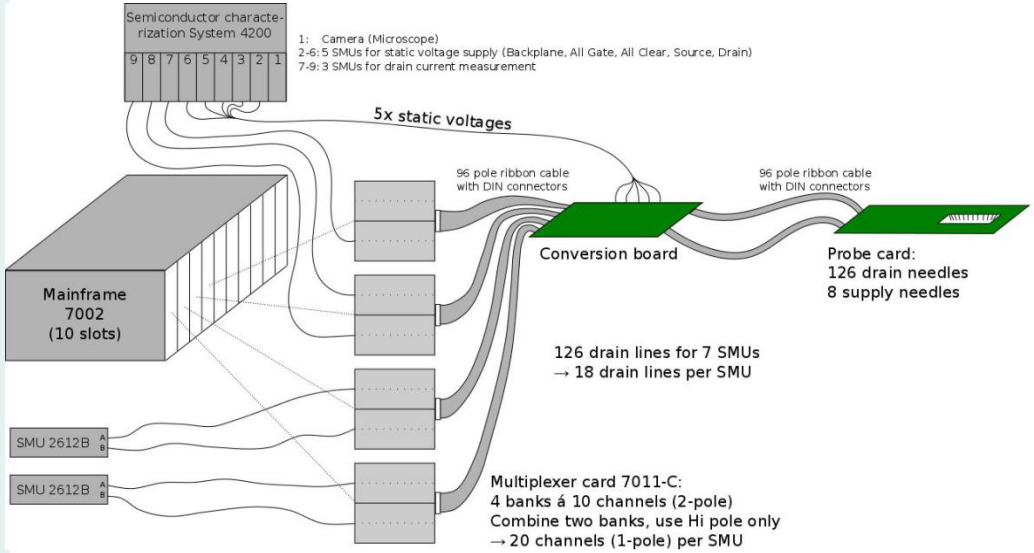
- SMU2 = Source (0V – static voltage 1)
- SMU3 = Clear Gate (5V – static voltage 2)
- SMU4 = All Gates (2V – static voltage 3)
- SMU5 = All Clear (15V – static voltage 4)

System description

- Probecard with 134 needles in total, arranged in two rows. 126 needles for the drain lines and 2x 4 needles for the static voltages.

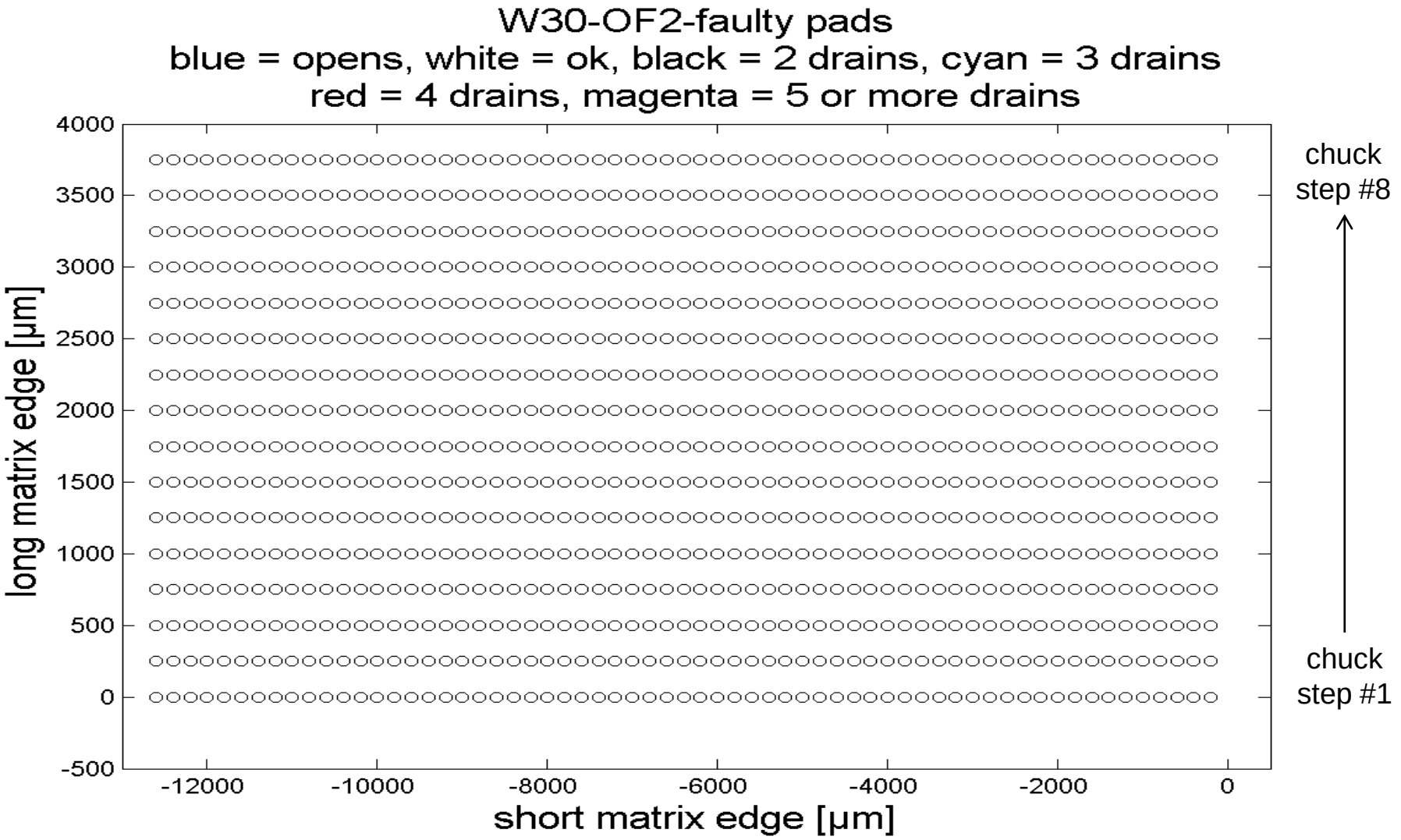


System description

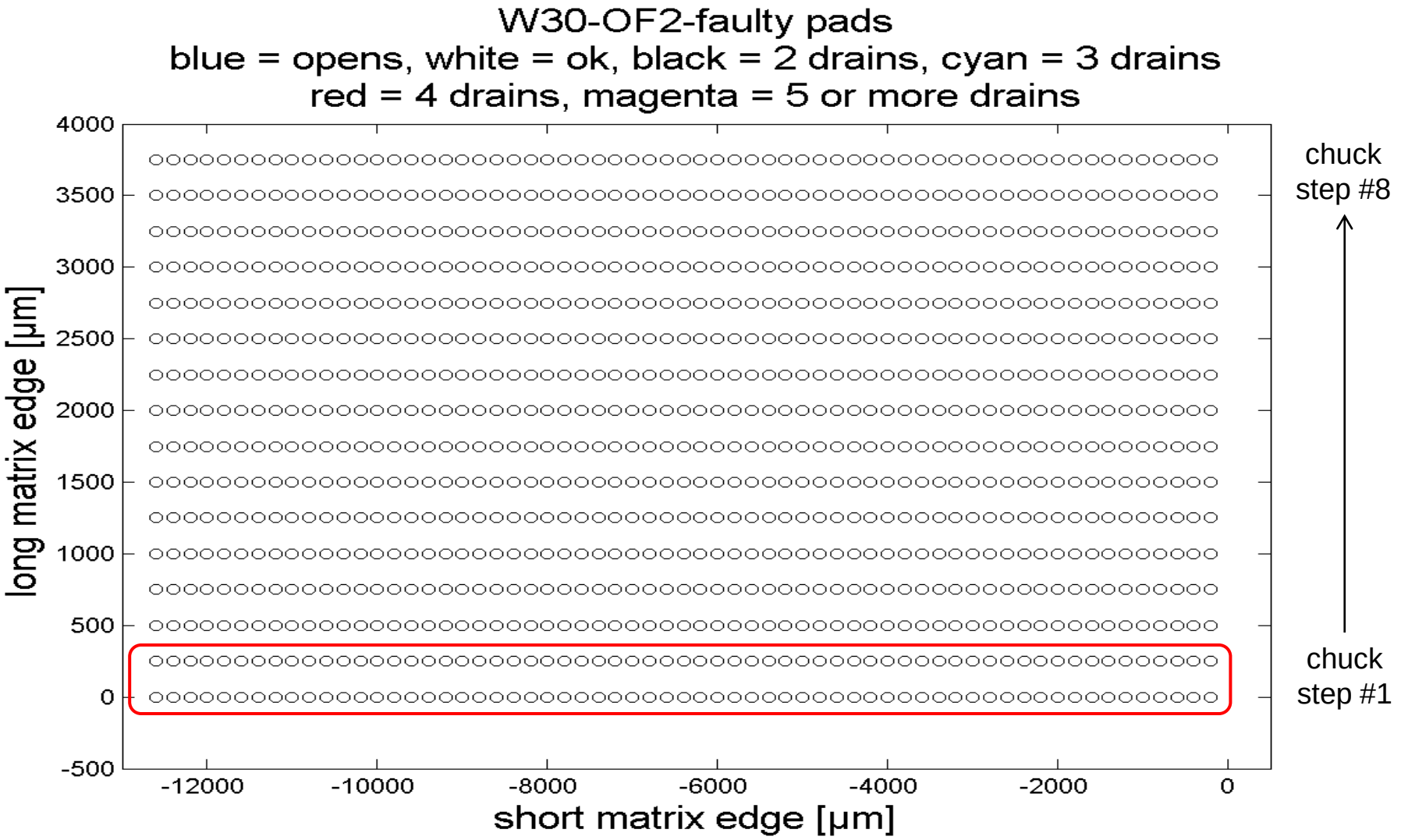


- Probecard with 134 needles in total, arranged in two rows. 126 needles for the drain lines and 4 needles per row for the static voltages.
- Probecard is connected via two ribbon cables to a conversion board
- Conversion board distributes the currents to the SMUs and the voltages to the probecard
- The 126 drain lines are connected to 7 SMUs → 18 drain lines per SMU
- The 4 static voltages are connected to 1 SMU each
- 1 SMU is used for the current sweep
- 1 SMU is used for the single needle for the gate rows.
- → 13 SMUs in total

Drain Groups, mapping, probing



Drain Groups, mapping, probing



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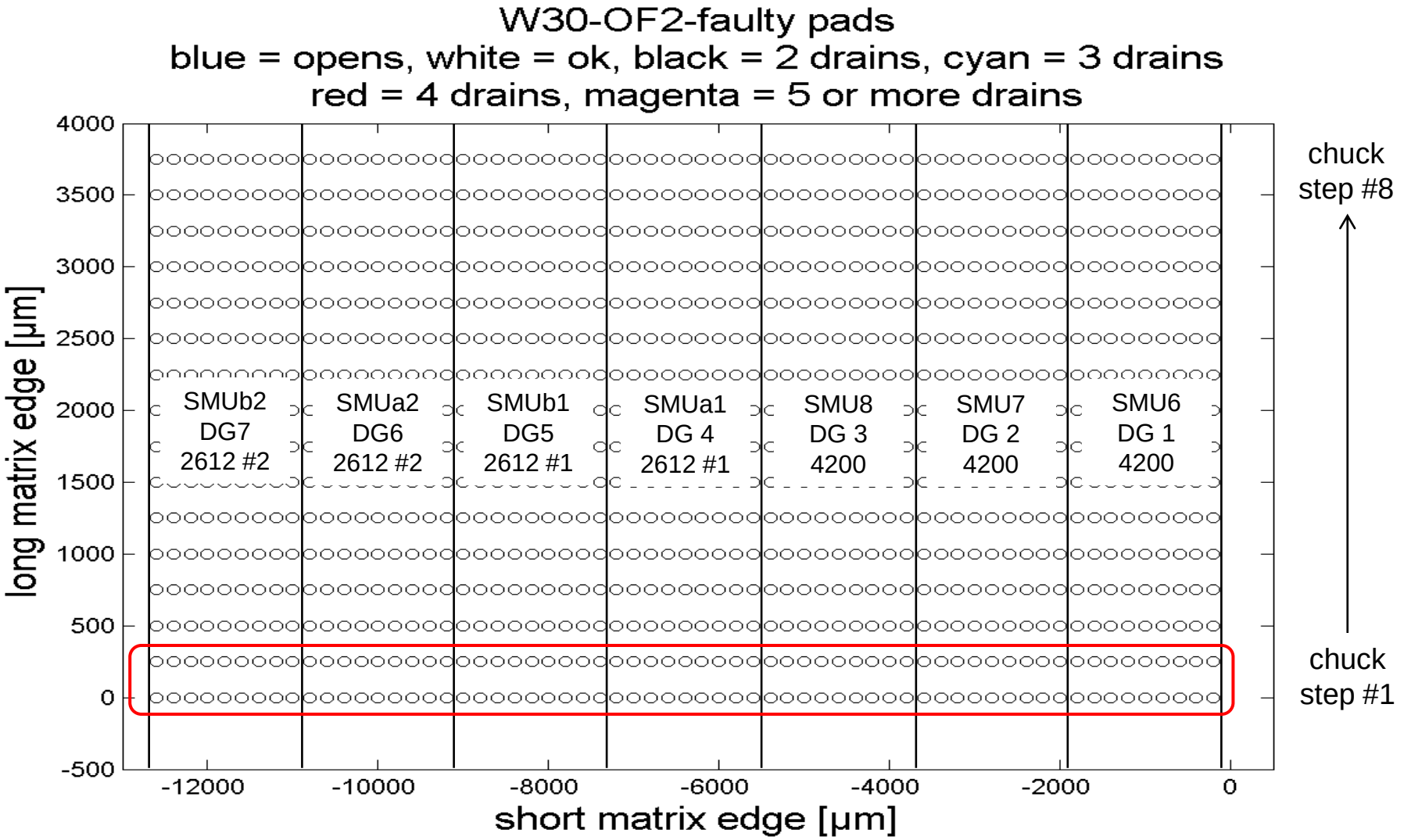

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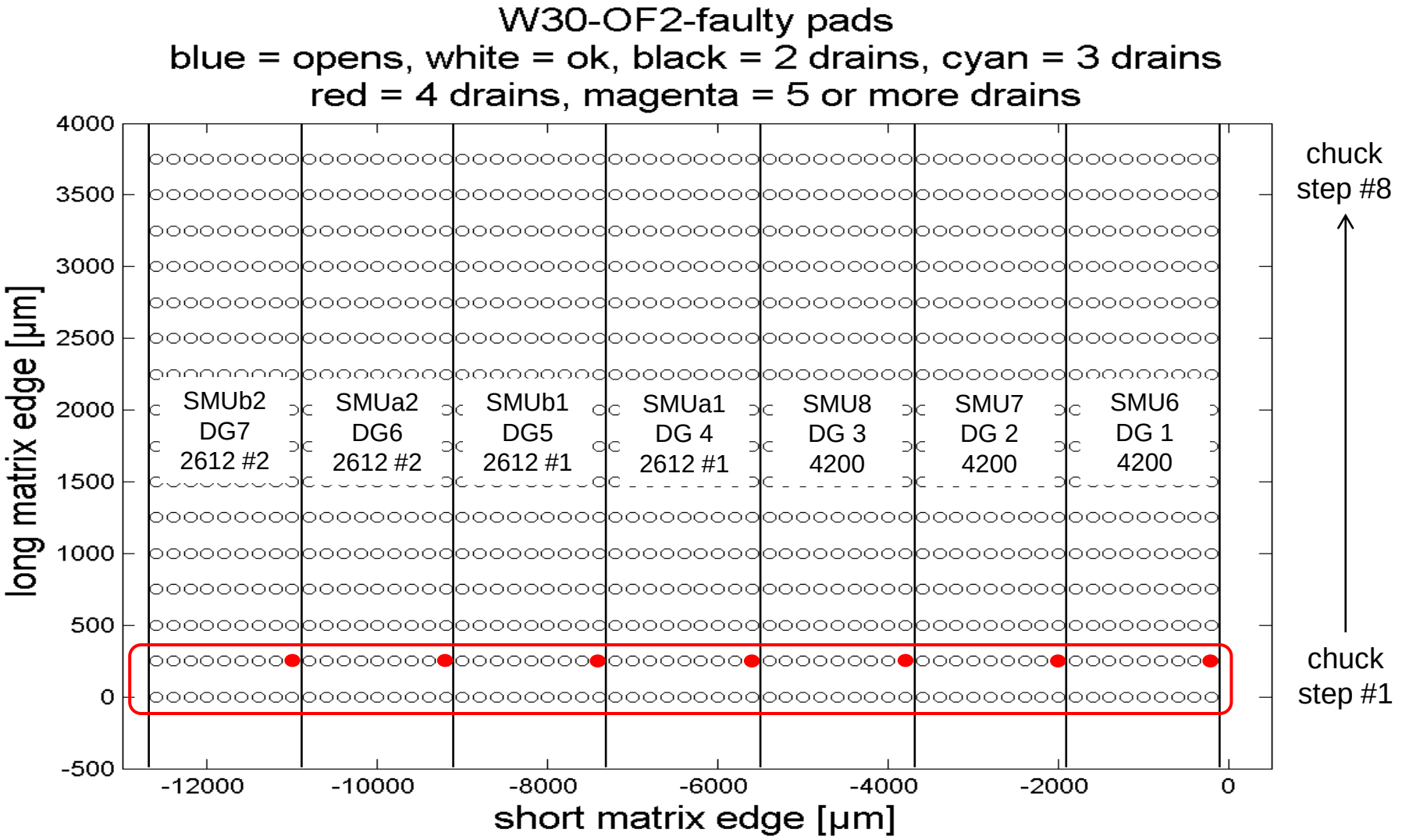

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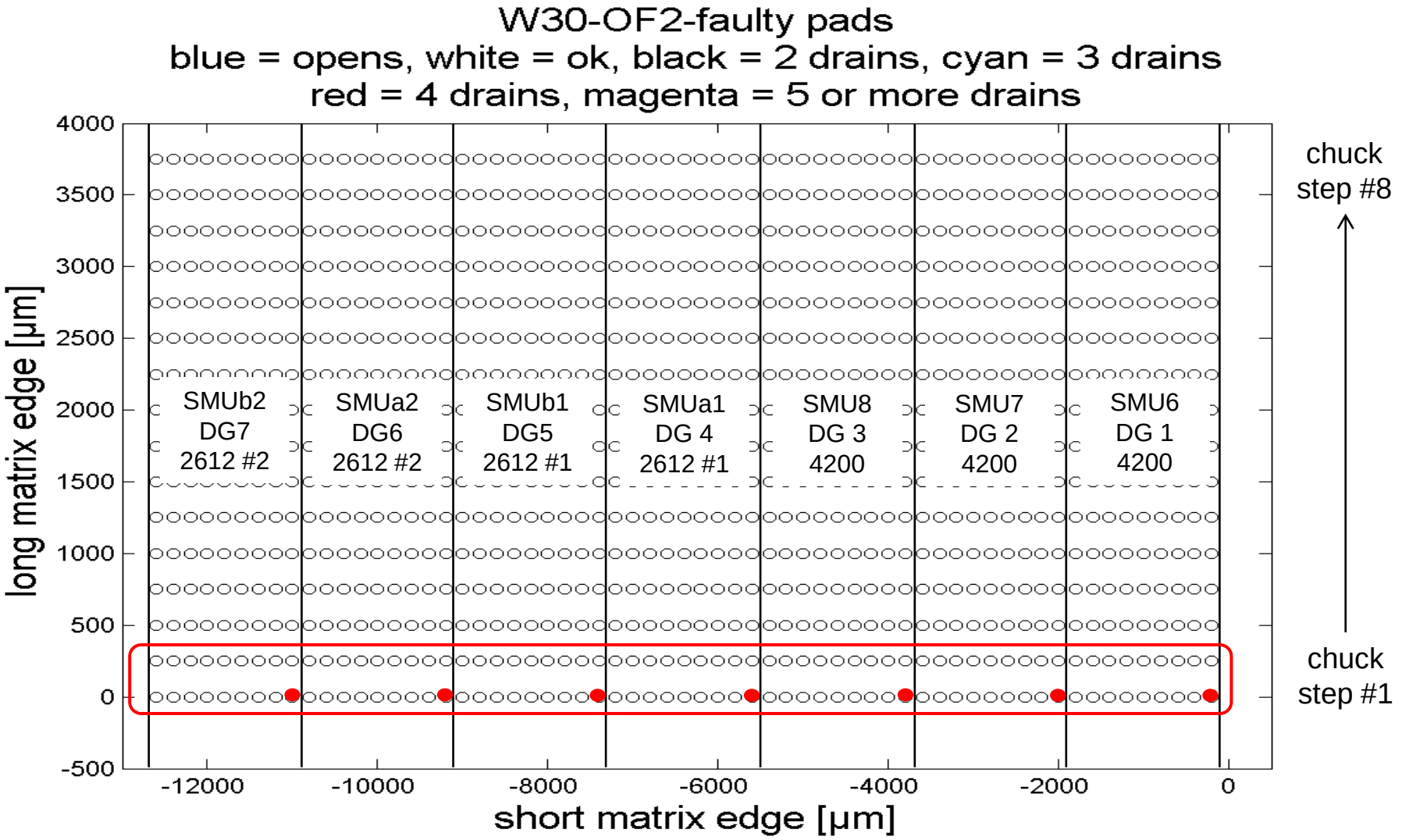

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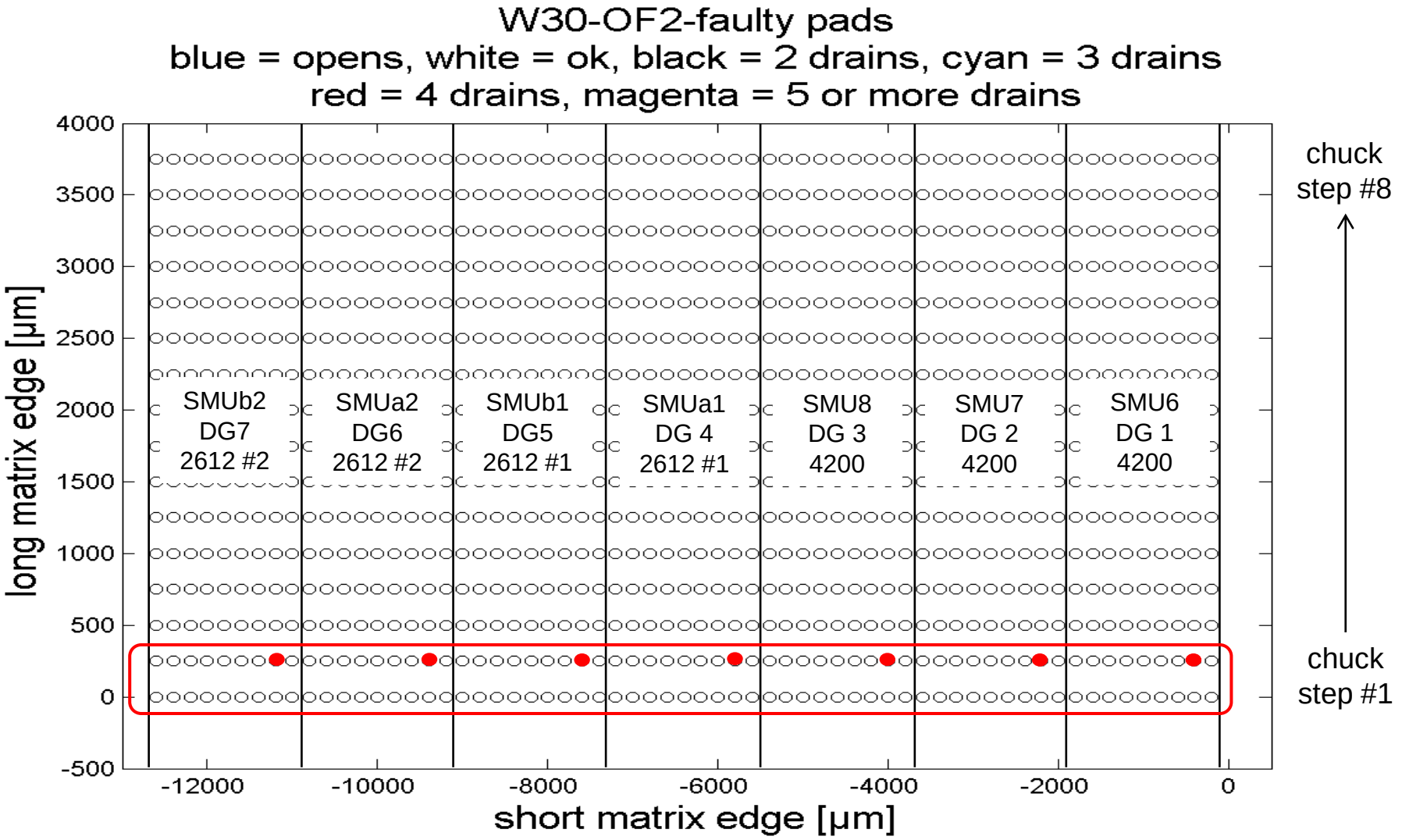

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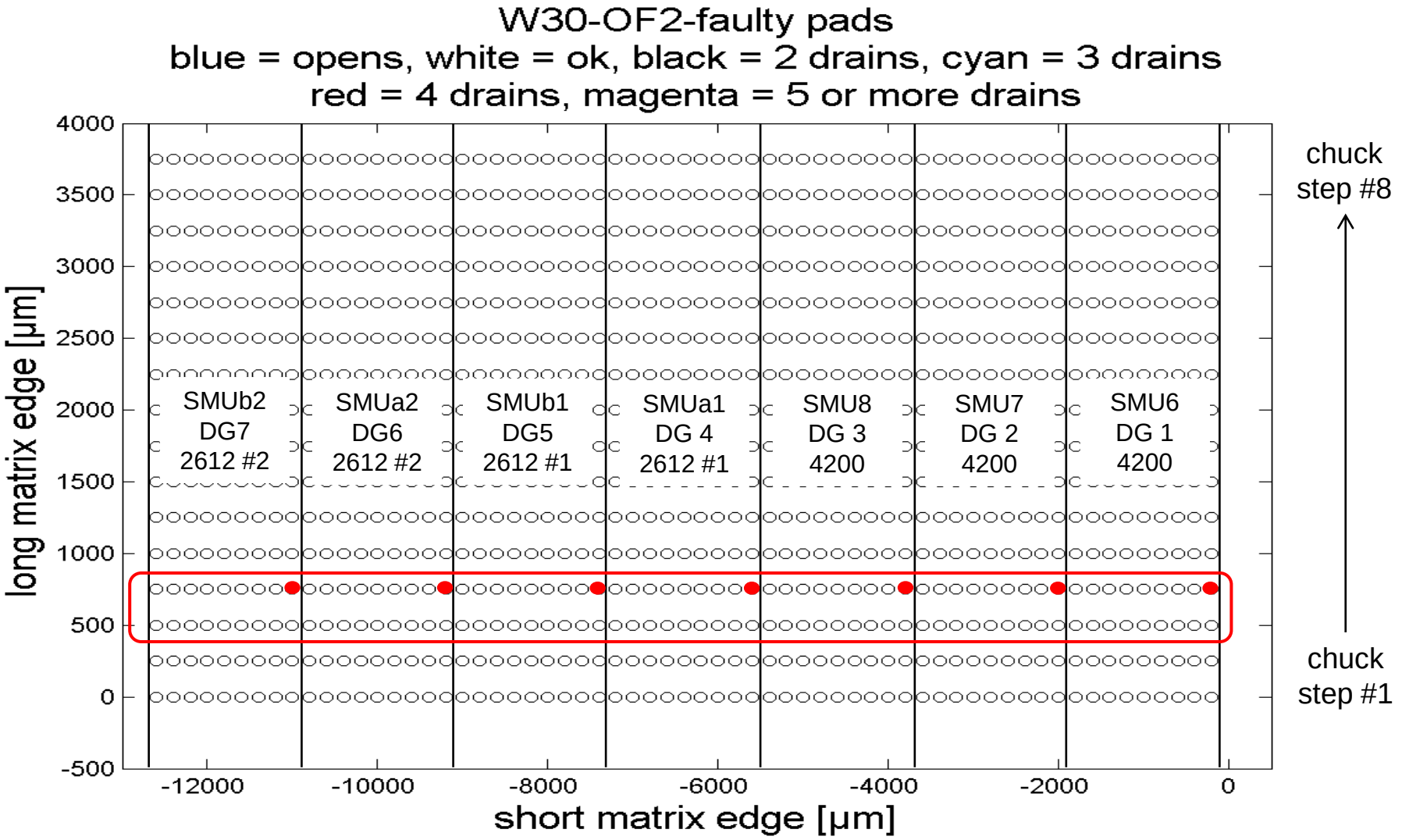
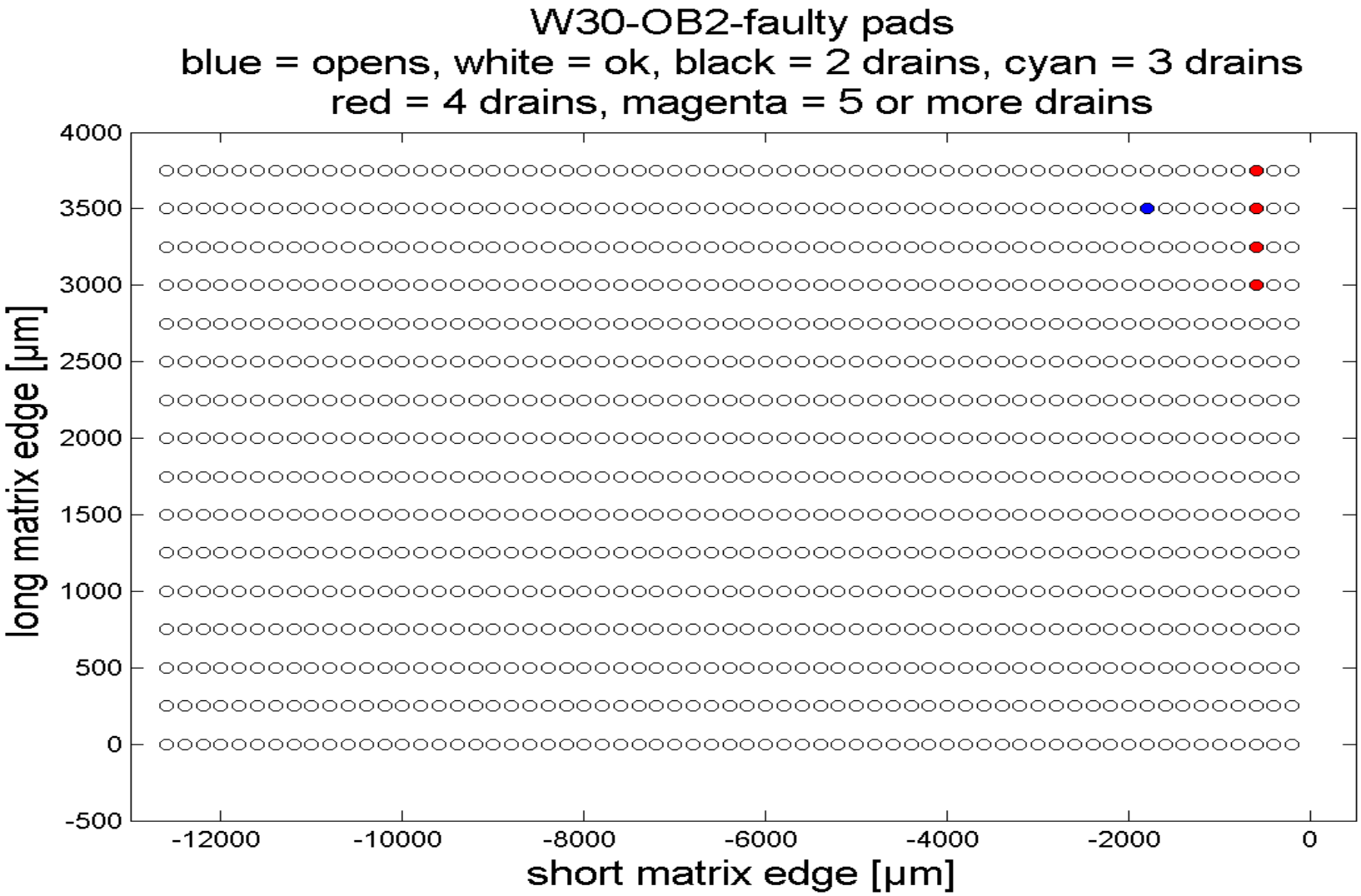


Mapping of the faults - Example



PXD-9-6 Batch II – 1st and 192nd gate row

First gate row						
	W30		W35		W36	
	opens	shorts	opens	shorts	opens	shorts
IF	0	83‡	0	0	0	0
OF1	1†*	0	0	0	0	0
OF2	0	0	0	0	0	0
OB1	0	2†	0	6*	0	0
OB2	1†	4***	0	5**	0	2†
IB	0	n.a.	bad	n.a.	0	n.a.

* Scratched during testing.
** Defect in the drain lines.
*** Drain lines shorted by a dirt particle.
† Fault not identified.
†* Particle involving different drain lines.
Bad = short between last gate and clear.
‡ Scratched by user during optical inspection. Last DCD not damaged.

Last gate row						
	W30		W35		W36	
	opens	shorts	opens	shorts	opens	shorts
IF	0	83‡	0	0	0	0
OF1	0	0	0	0	0	0
OF2	0	0	0	0	0	0
OB1	0	2†	0	6*	0	0
OB2	0	4***	0	5**	0	2†
IB	1	0	bad	bad	0	0

Modules currently in repair:

- W30: OB1 & OB2
- W36: OB2

Due to a discontinuity (layout bug) in the AG bus, the detection of shorts had to be performed on the last gate row test, while the detection of opens was still possible at the first gate row.

Yield considerations of the metal system

Yield (%)			
	W30	**W35**	**W36**
IF	75.0	100.0	100.0
OF1	100.0	100.0	100.0
OF2	100.0	100.0	100.0
OB1	99.8	99.4	100.0
OB2	99.6	99.5	99.8
IB	100.0	**0**	100.0

Rainer's Yield Criteria			
	W30	**W35**	**W36**
IF	3	0	0
OF1	0	0	0
OF2	0	0	0
OB1	1	1	0
OB2	1	5	1
IB	0	**4**	0

Yield calculated taking into account the following equation:

$$Yield(\%) = \frac{1}{10} \cdot [D - D_S]$$

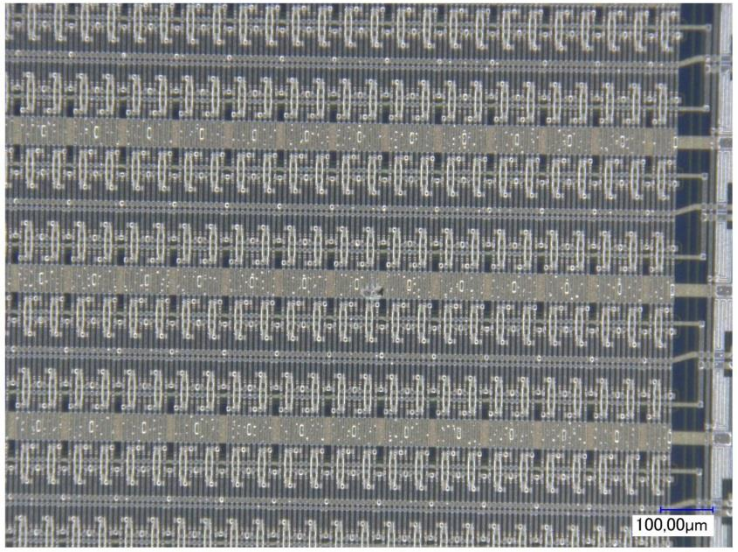
With D the total number of drain lines (1000) and D_s the number of drain lines involved in the short.

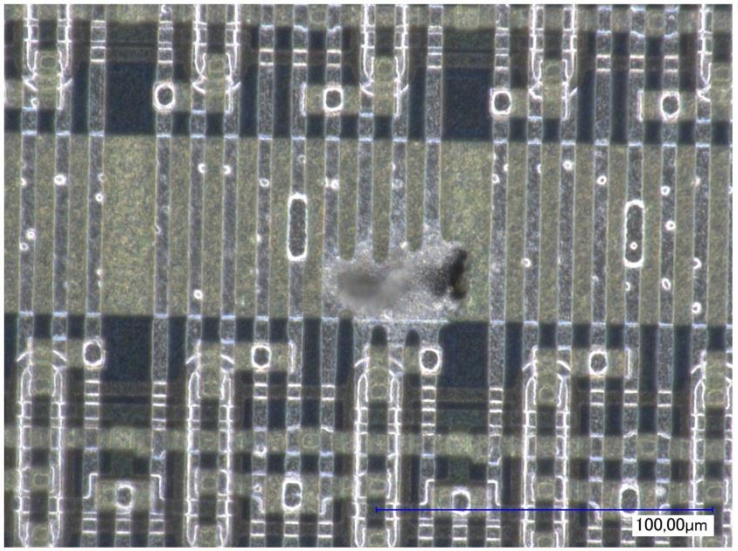
Rainer's criteria for yield calculation:

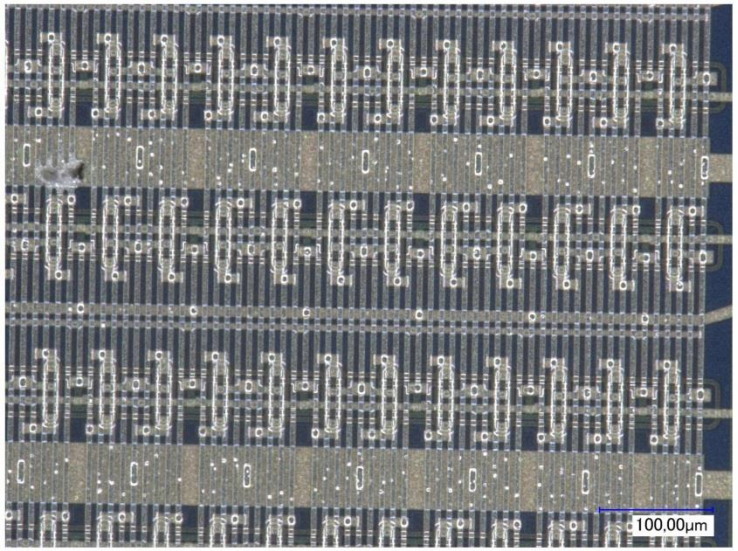
0: no faults
1: pixel or column* (drain line) level faults
2: row level faults
3: high impact faults
4: lethal faults
5: to be clarified

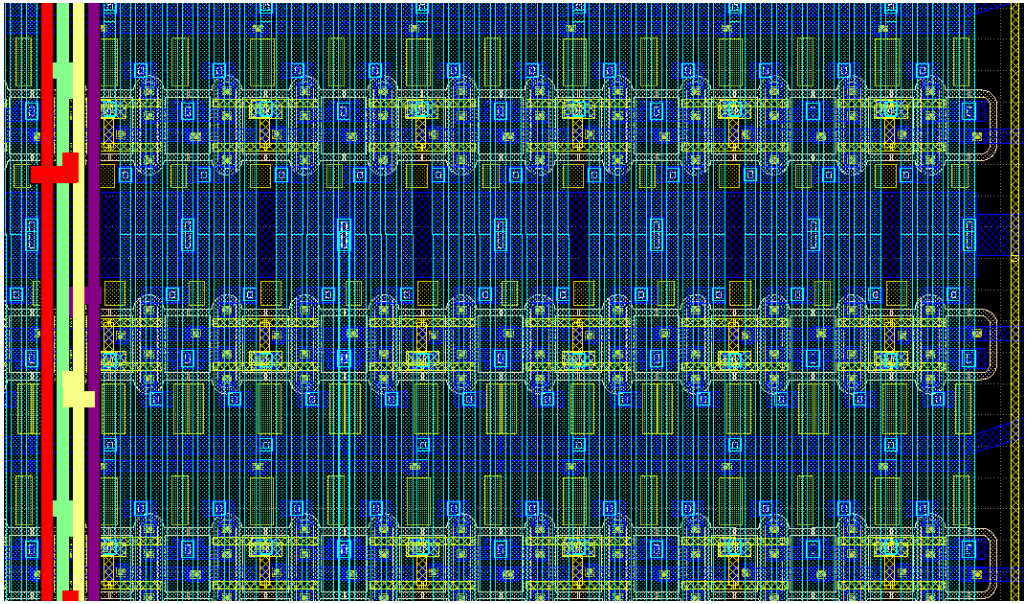
* Column level faults in Al2 can be repaired by rework (grade 1 → 0).

W30 – short in OB2

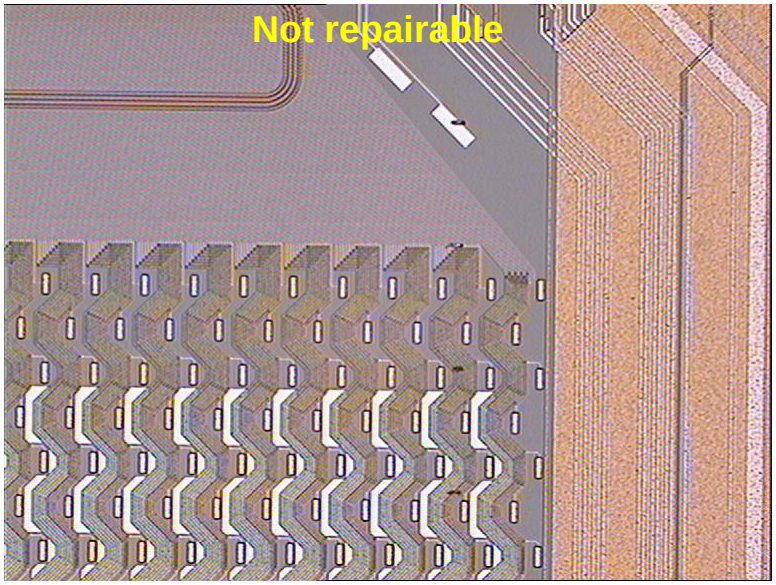


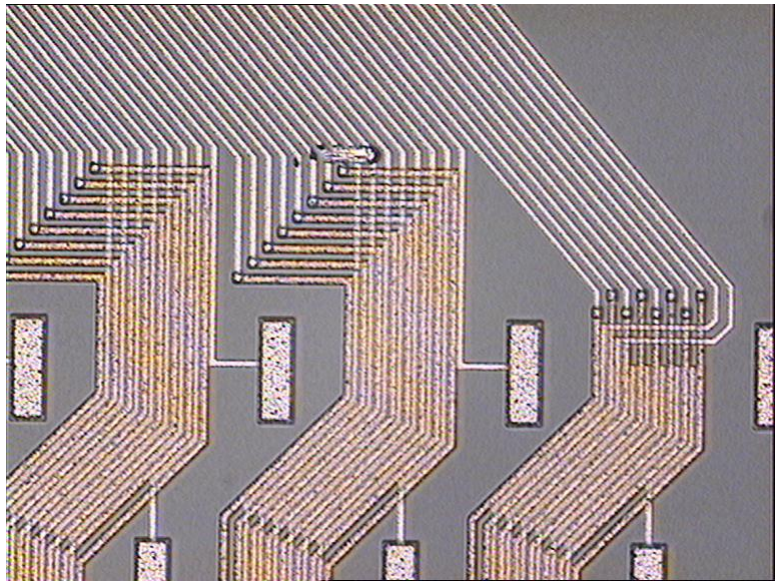


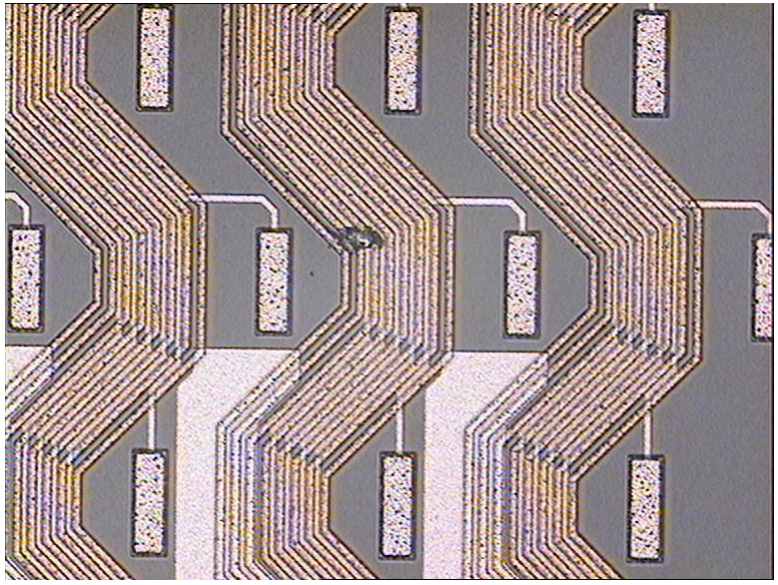


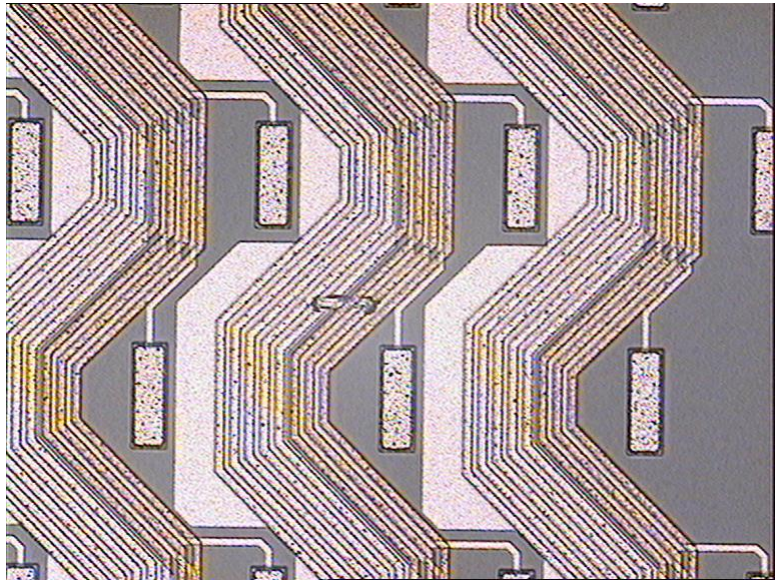


W35 – shorts (due to scratches) in OB1









System issues/failures

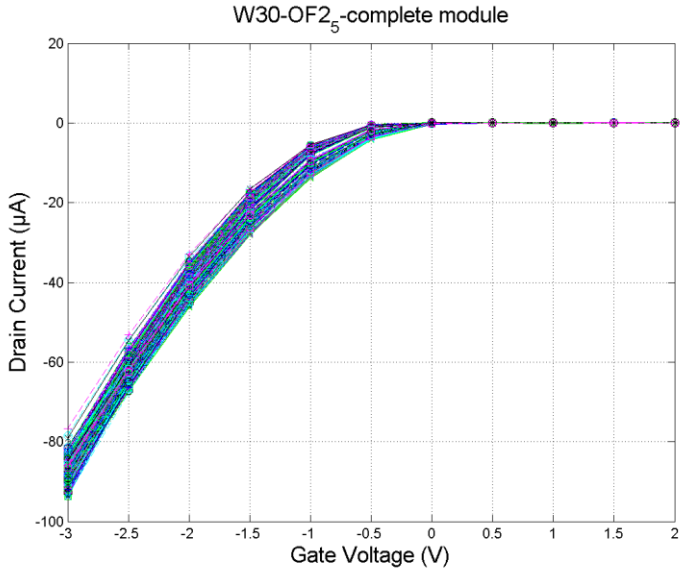
1. Chuck non planar →
   - Bad probing in the right hand side of the fan-out (source in conf #2)
   - Bad contacts (higher contact resistance ➔ smaller I_{ds}) for higher chuck steps

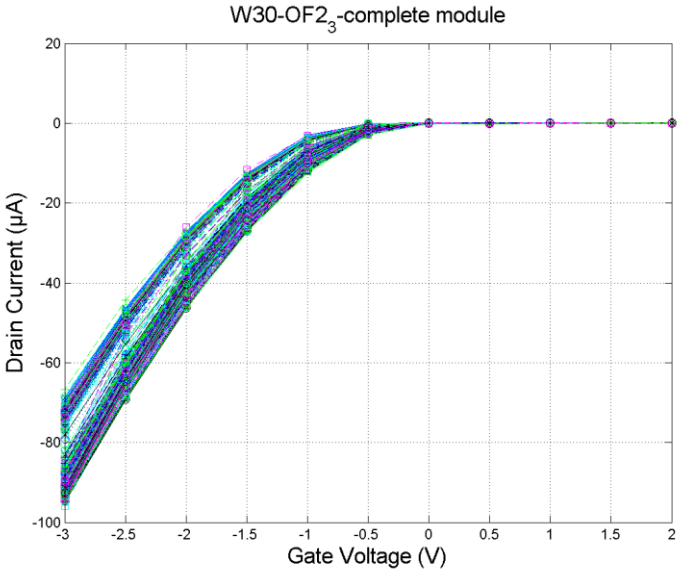
2. Electrical failures (due to contact problem in SMU2 preamp of Keithley 4200) →
   - System freeze
   - Bad characteristics due to wrong applied voltage (AC/conf #1 or S/conf #2)

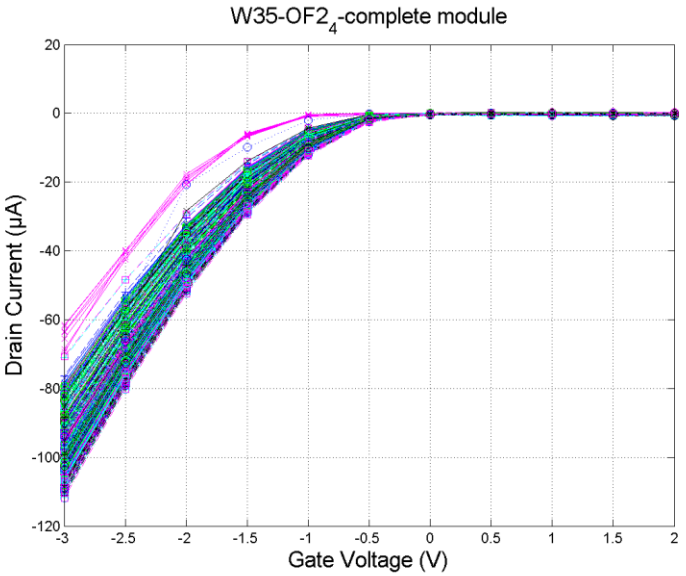
3. Electrical failures (in Keithley 2612 – not explaied yet) →
   - System freeze

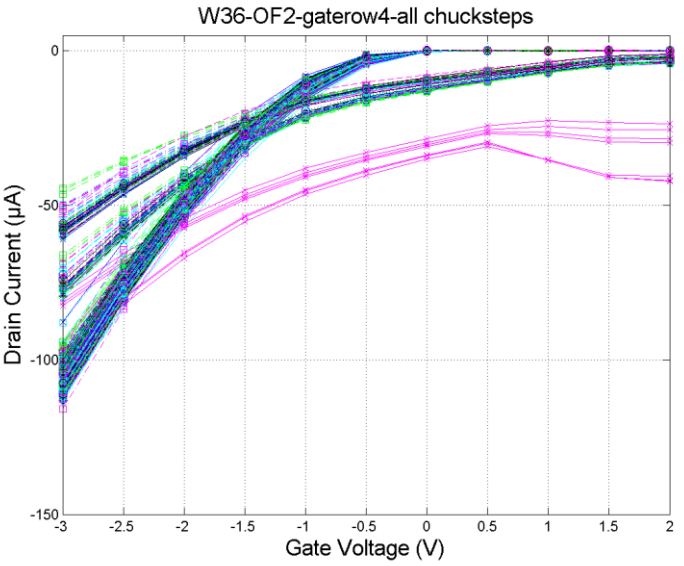
4. Software failures (fully understood) →
   - KITE (DAQ software) crash
   - System freeze if data folder remotely accessed

Examples


W30-OF2$_5$-complete module
Drain Current (µA)
Gate Voltage (V)

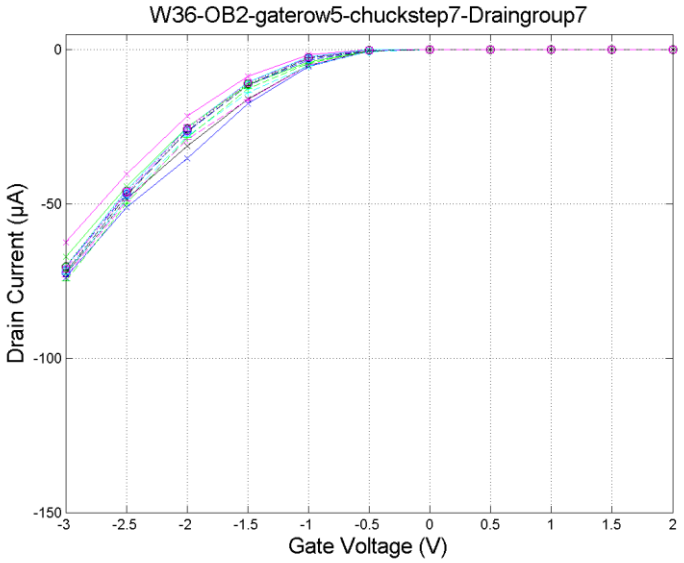

W30-OF2$_3$-complete module
Drain Current (µA)
Gate Voltage (V)


W35-OF2$_4$-complete module
Drain Current (µA)
Gate Voltage (V)


W36-OF2-gaterow4-all chucksteps
Drain Current (µA)
Gate Voltage (V)

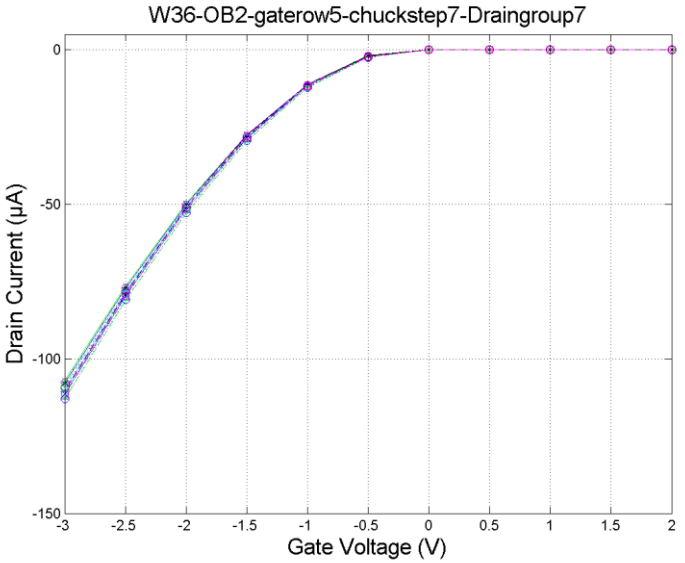
System failures

Bad contacting



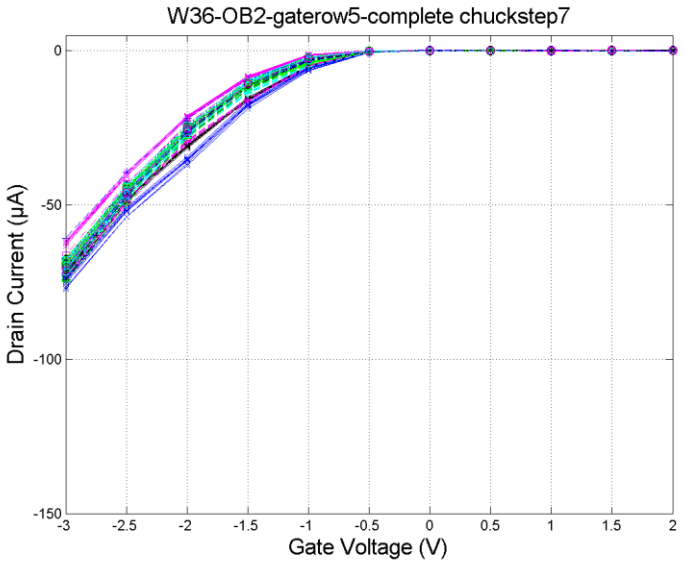
measurement
→
repeated

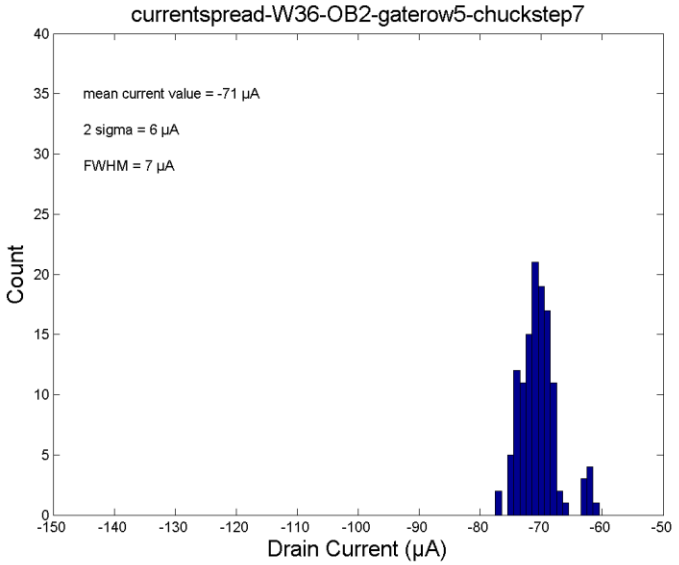
good contacting?



System failures

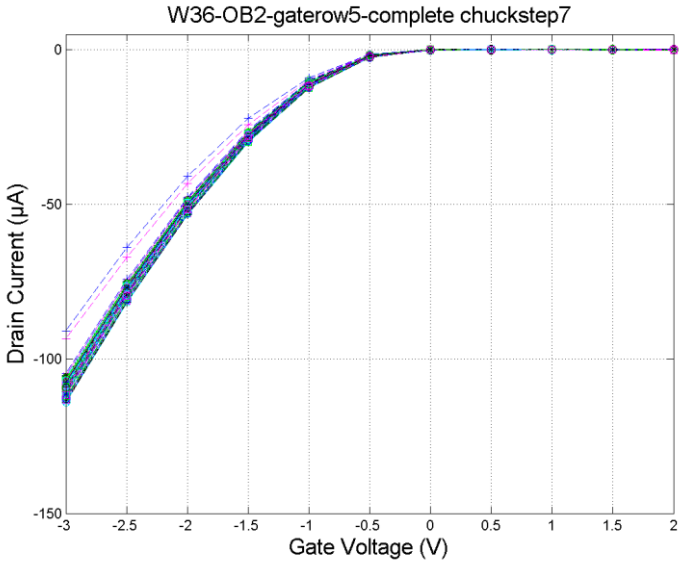
Bad contacting

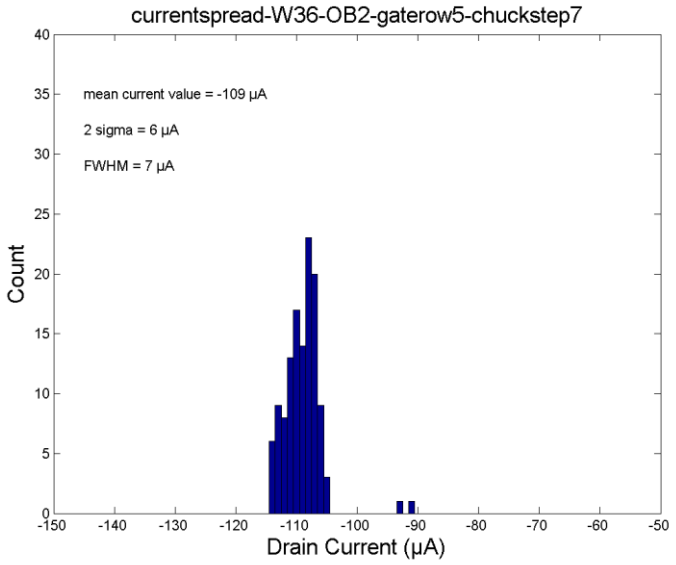




measurement
→
repeated

Better contacting





Conclusions and future plans

- The actual setup is reliable for yield measurements (opens & shorts), but needs modifications to provide reliable high precision measurements (pedestal spread, V_t calculation).
- The yield measured for all the three wafers is high, with only one chip (out of 18) not usable.
- Some of the chips with identified shorts in the drain lines will have rework, starting this week.
- We propose to proceed with processing of W30 and W36 for the next testing phase, i.e. periphery (balcony + End Of Stave) characterisation (detection of opens & shorts) using the atg machine.
- And to keep W35 as a test wafer for precision measurements using the improved system.
- W35 will be further processed in the near future, i.e. end of April.

Thank you for your attention!