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DEPFET

Active Pixel Detector

Pedestals and Power: What to learn from Hybrid 6 and Test Beam

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Hybrid 6.0

- PXD6 - J00 on Hybrid 6

Capacitive Coupled ClearGate
50x75 µm2 pitch
768 drain lines (256x3 DCD/DHP)
120 gate/clear lines (4 Switcher)

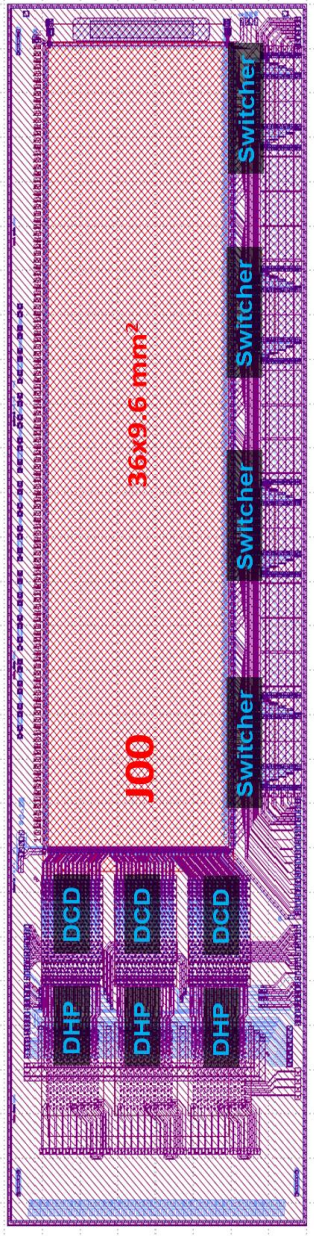
DCDBv2, DHP0.2, SwitcherB1.8G
Speed: 250 MHz
→ Broken during power down

- PXD6 - I00 on Hybrid 6

Capacitive Coupled ClearGate
50x100 µm2 pitch
768 drain lines (256x3 DCD/DHP), only DCD0, DHP0 assembled
120 gate/clear lines (4 Switcher)

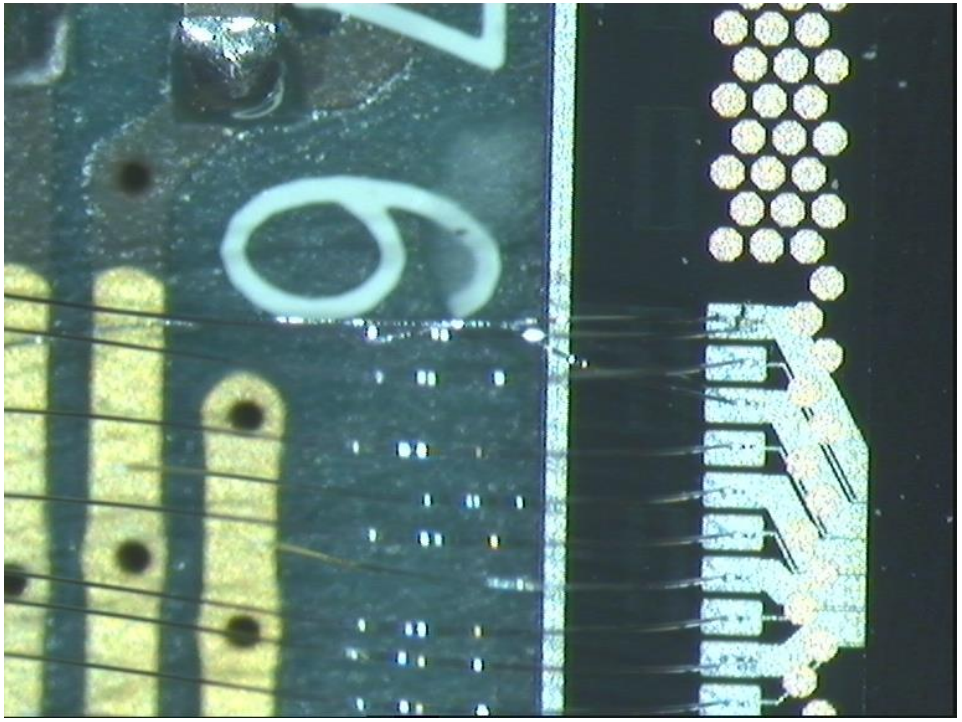
DCDBv2, DHP0.2, SwitcherB1.8G
Speed: 250 MHz

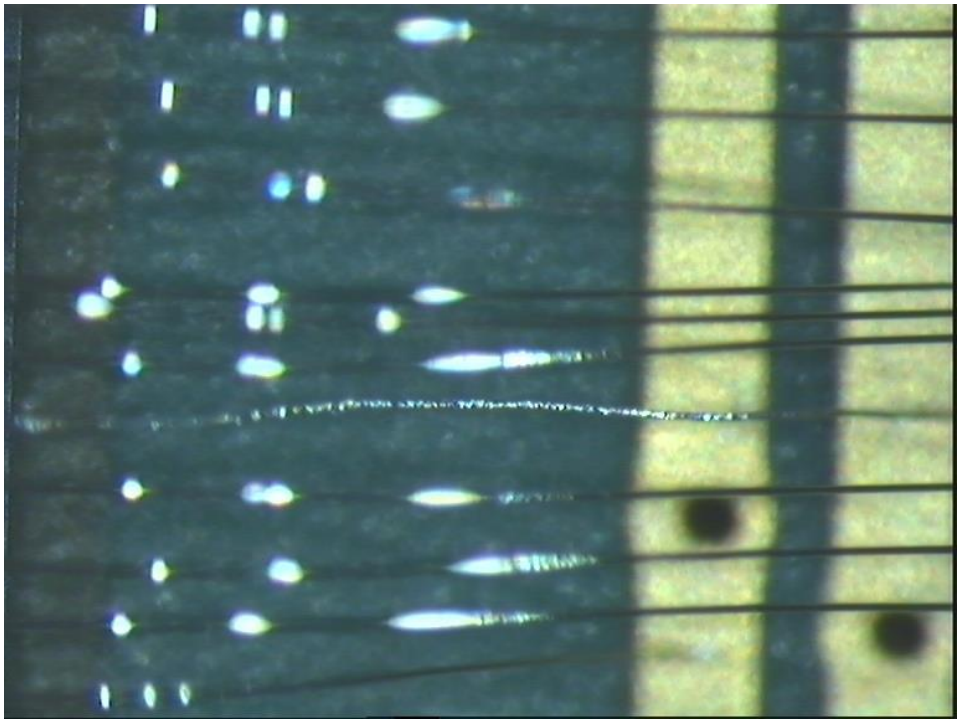
- DHE and Power Supply



Melted Wirebonds

Bug in the power down sequence → Fixed (some wire bonds melted)





Two good options for not melting wirebonds:

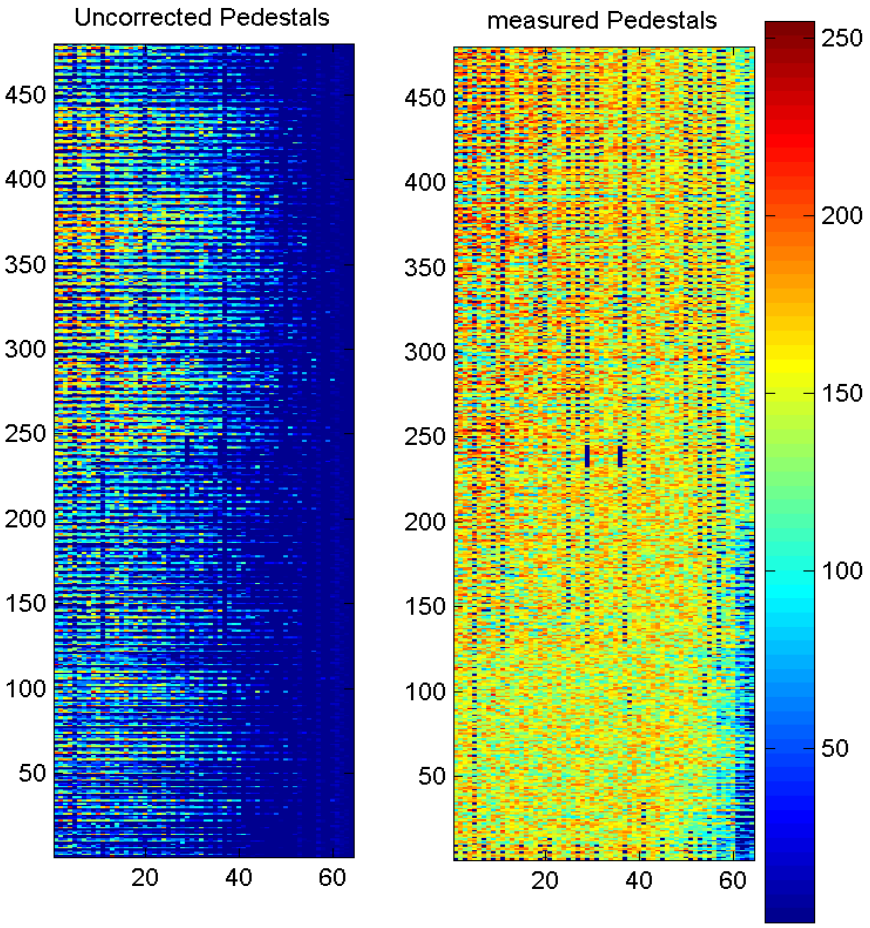
- Instant (emergency) powerdown
- Gracefull (slow) powerdown **with current limits**

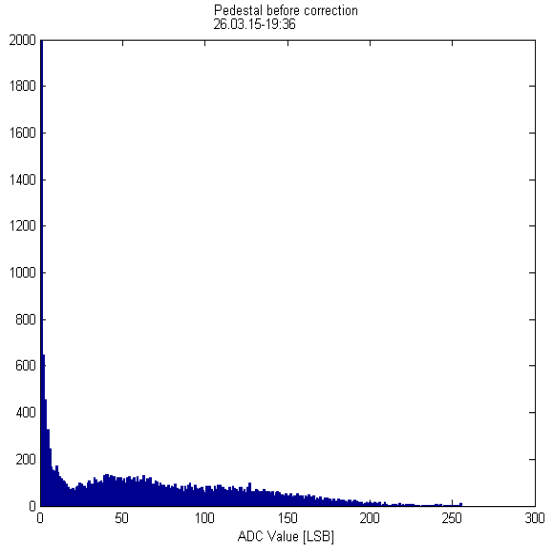
A bad option for not melting wirebonds:

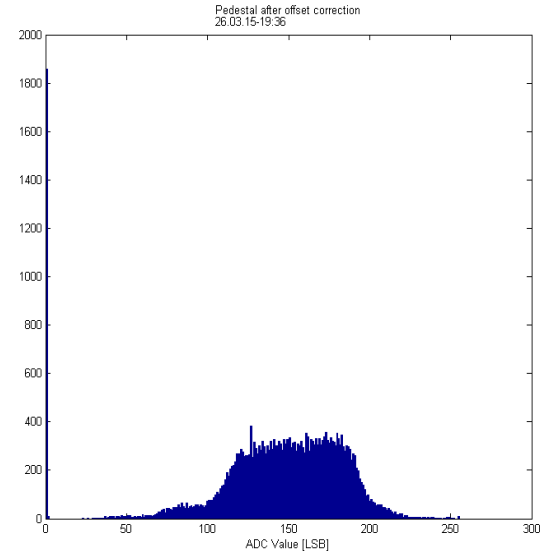
- Rely on the user to not make stupid things

Hybrid 6.0

Pedestal compression I00

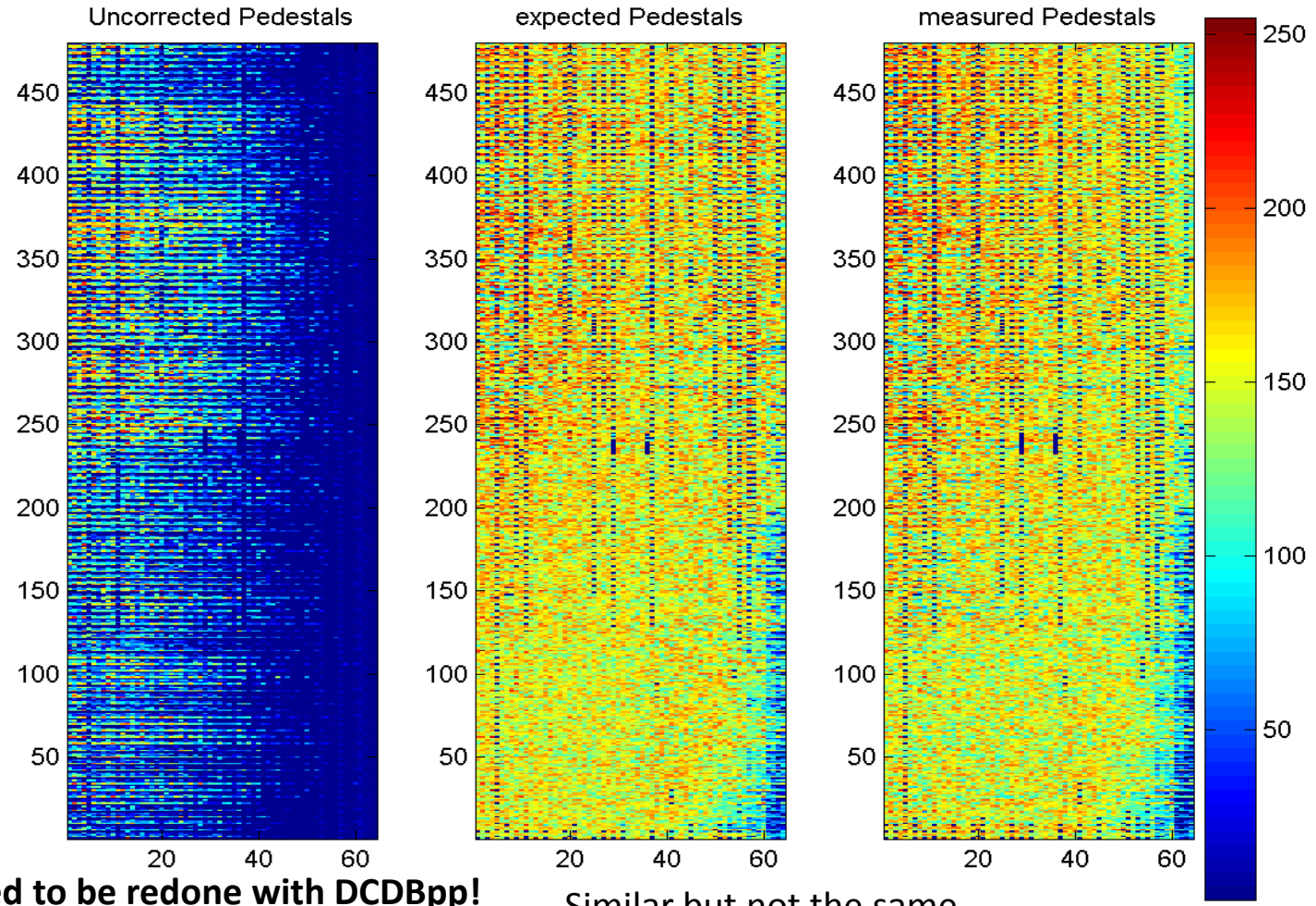






Power routing: the 3 DCDs show different pedestal distribution.
Gradient over columns observed in J00

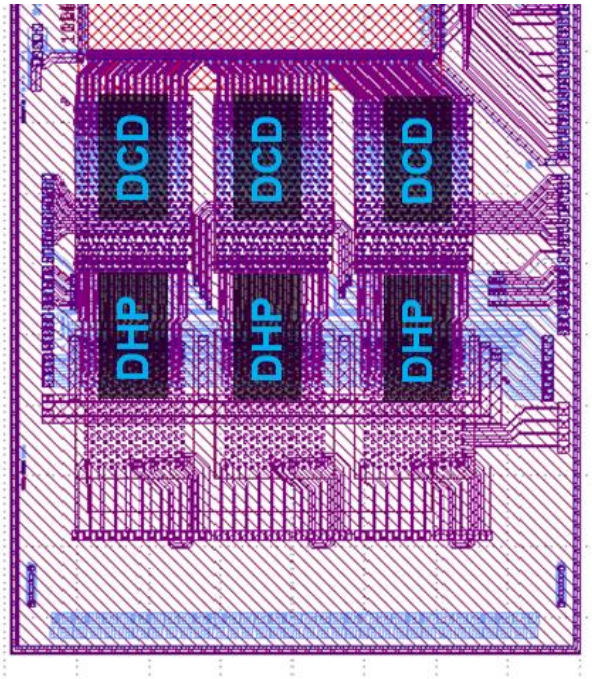
Hybrid 6.0 Offset correction (I00)

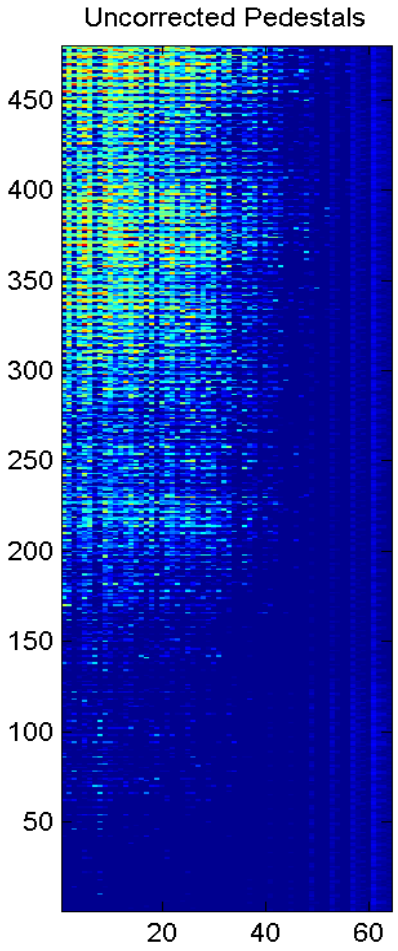


Measurements need to be redone with DCDBpp!
Strength, intersymbol interference etc…

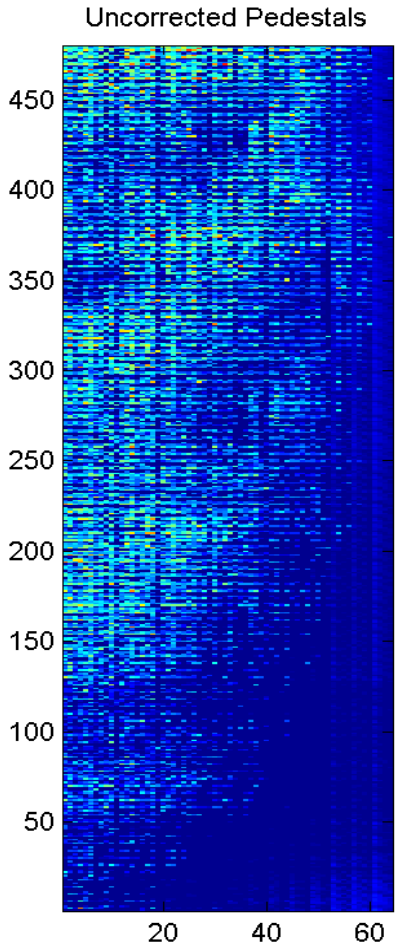
Similar but not the same.
Offset DAC can have crosstalk with other offset DAC values or the value it had before.

Hybrid 6.0 DCD Powering and Gradients (J00)

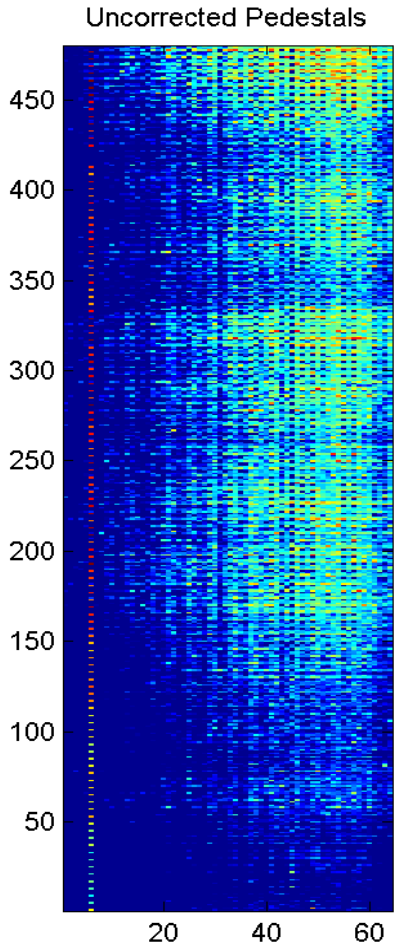




Powered from the left

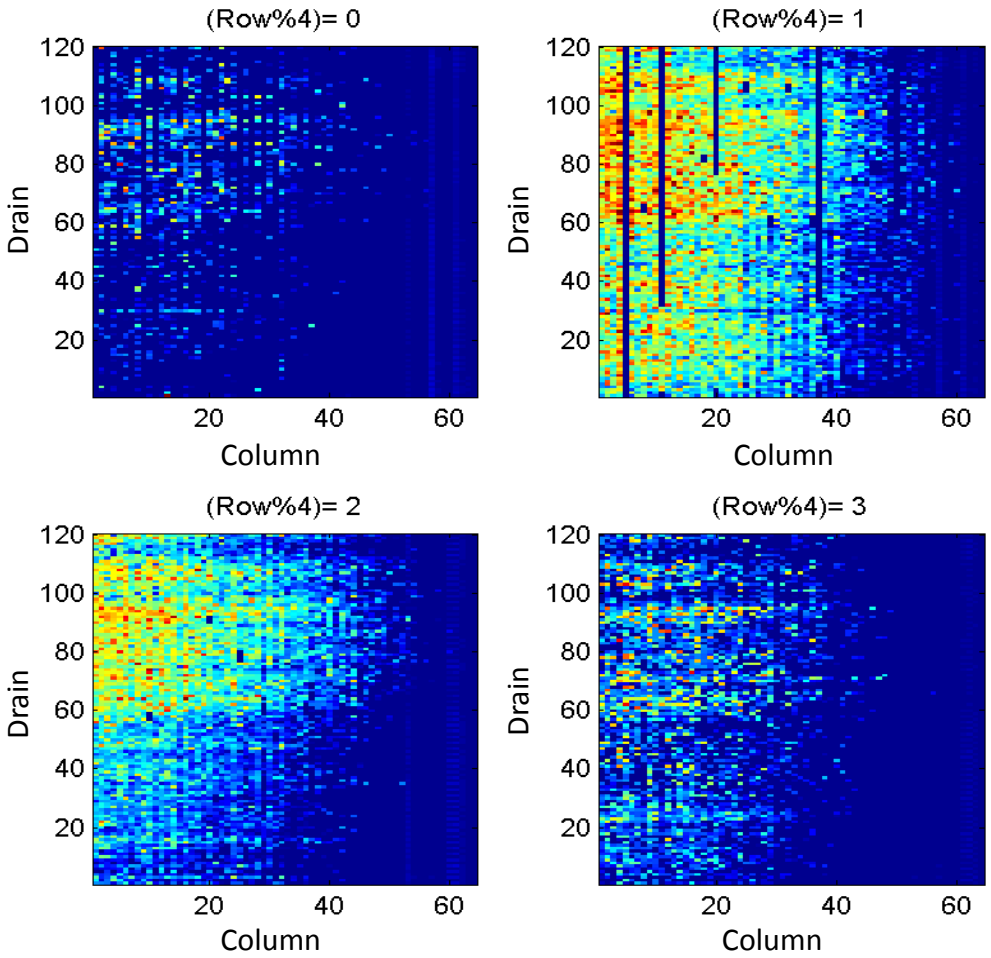


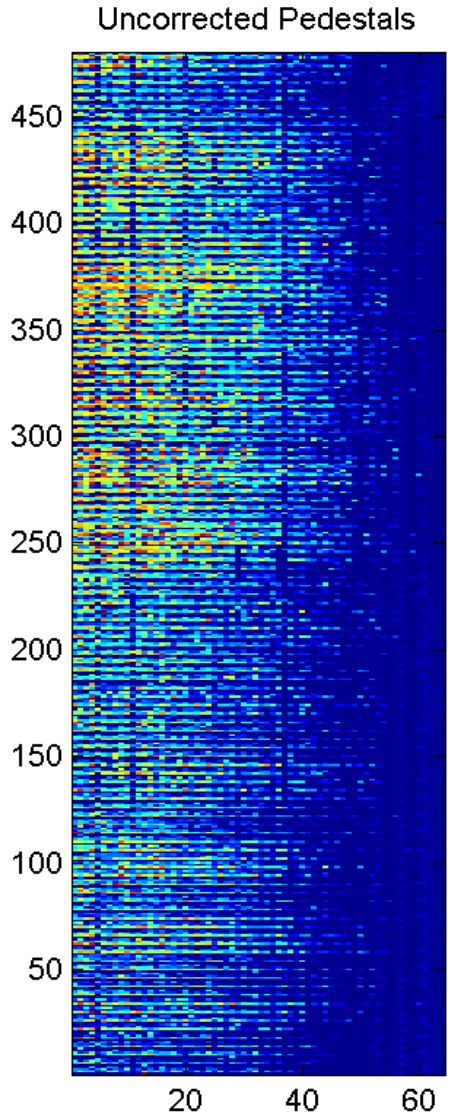
Analog from left
Digital from right



Powered from the right

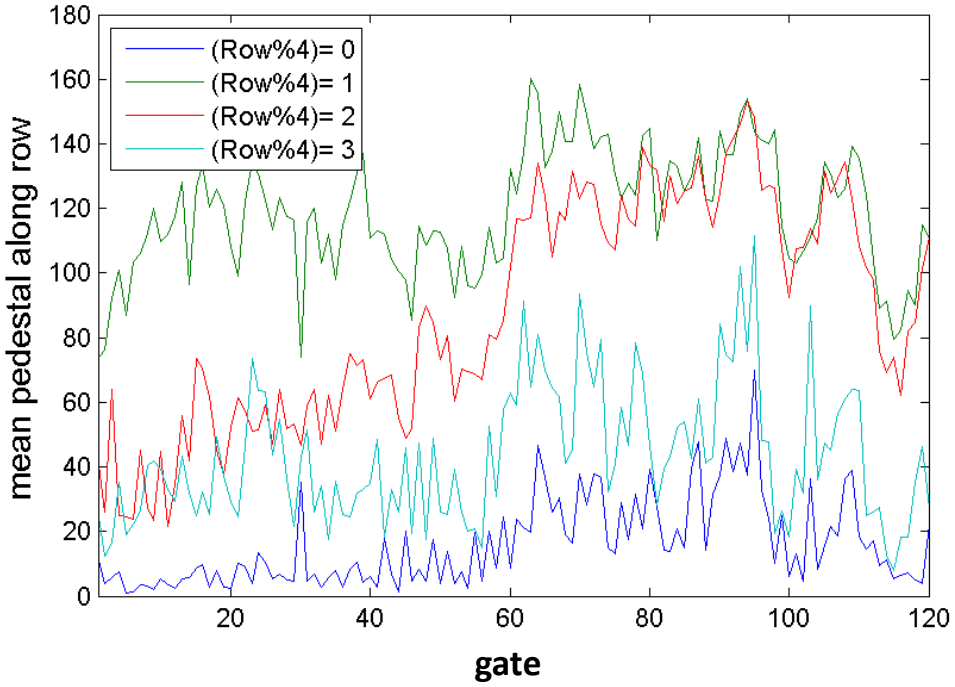
Hybrid 6.0 Rows seperated (I00)

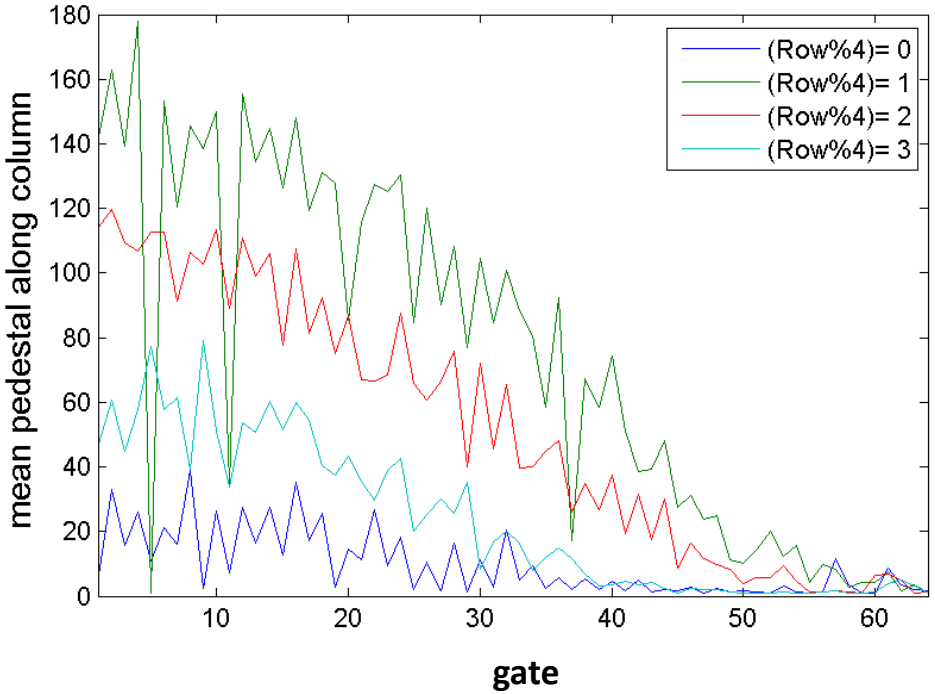




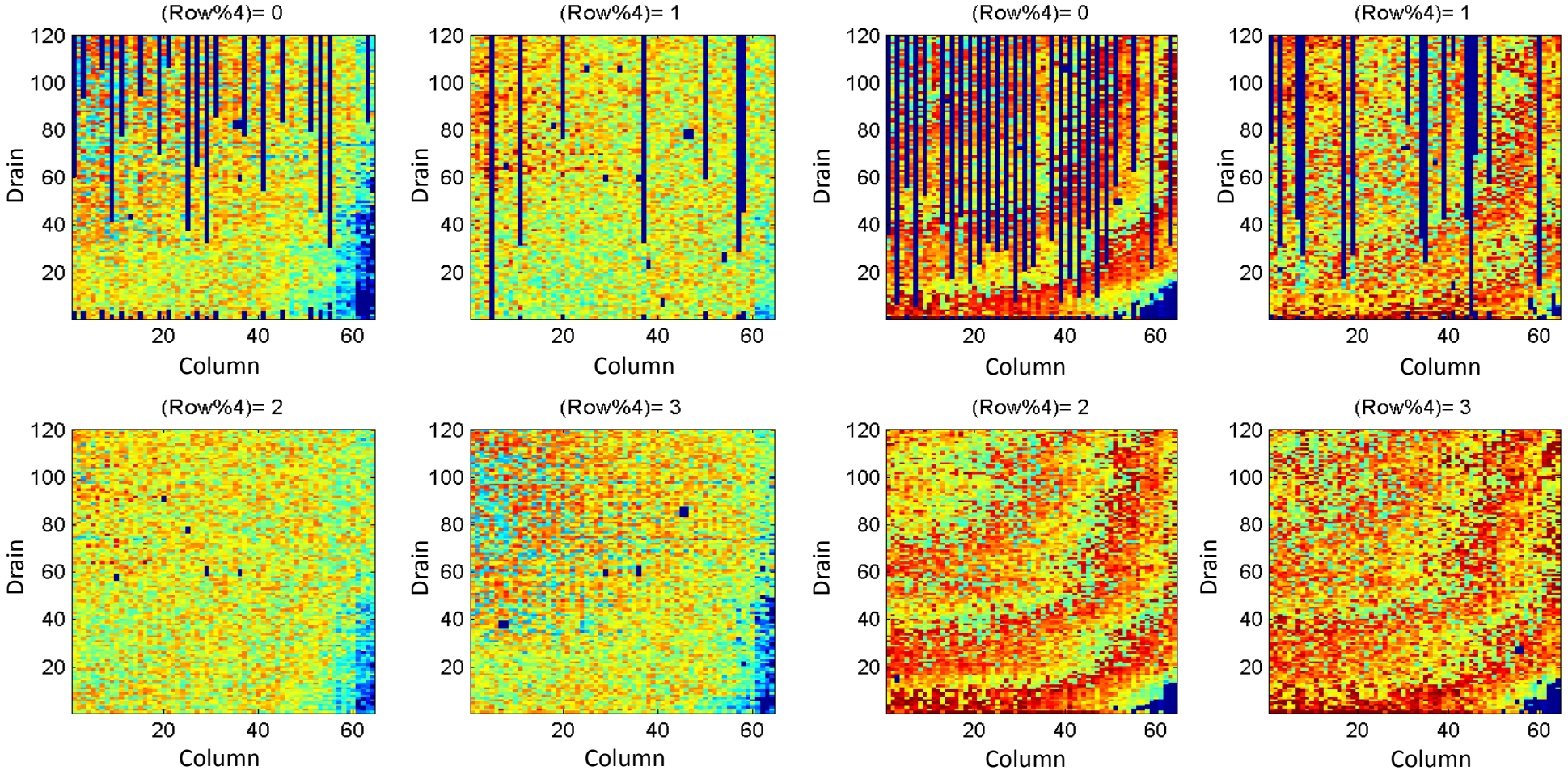
Some pedestal effects are static and could be mitigated by static DAC

Pedestal pattern projected (I00)



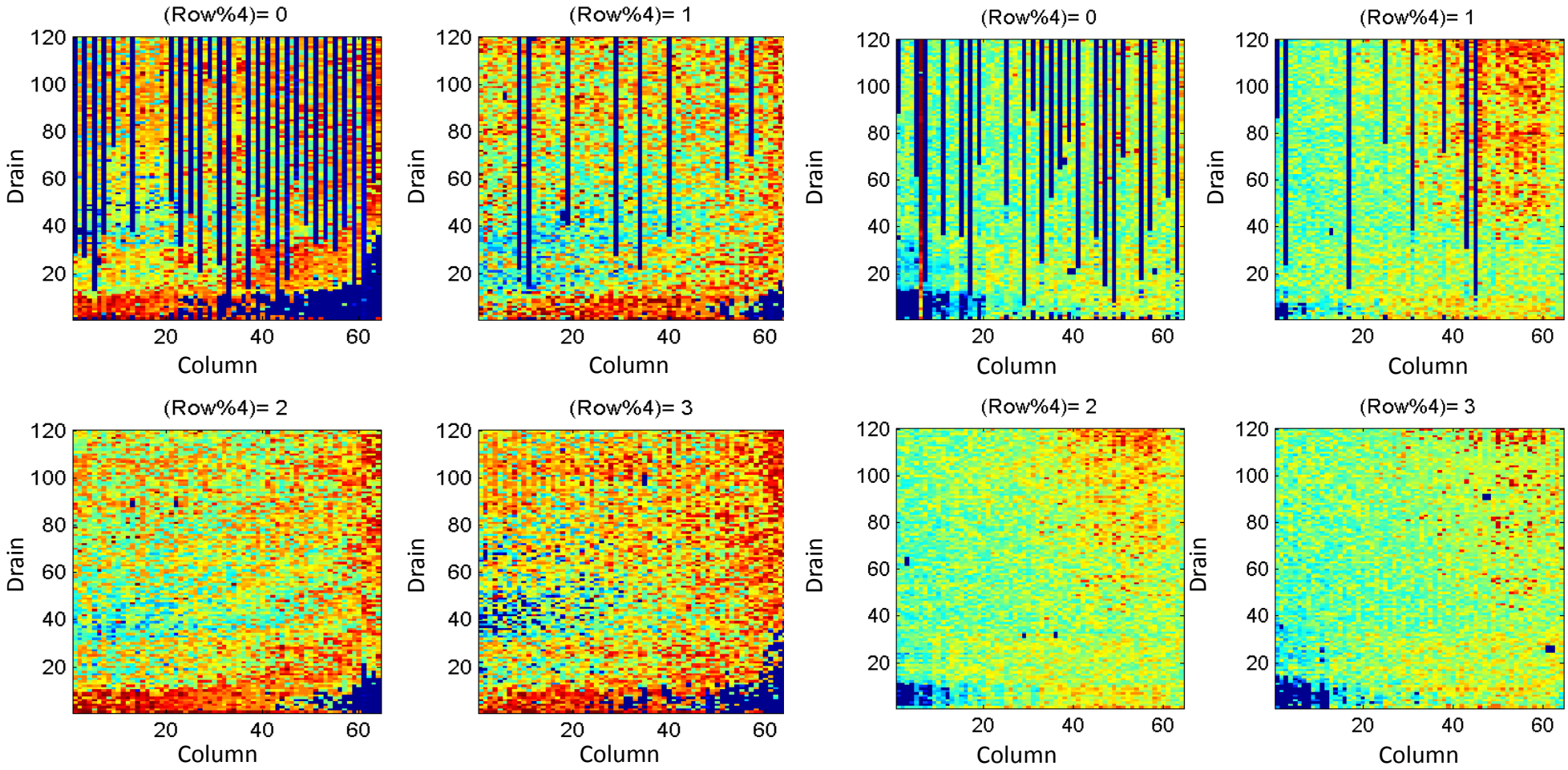


Unconnected drains



I00 DCD0 **J00 DCD0**

Unconnected drains



J00 DCD1 **J00 DCD2**

Conclusions

- Powering:
  - Needed to power up one by one?
  - For DHPT not
  - For DCDB?
- DCDB is unconfigured after power up
  - Possibility of standard configuration after Powerup? Especially to have analog switched off?
- Static differences on PXD6 observed, expected for PXD9 (even/odd row)
  - Possibility of having a static offset bit in DCDB?
  - What is the available data for PXD9? Is there a trend?

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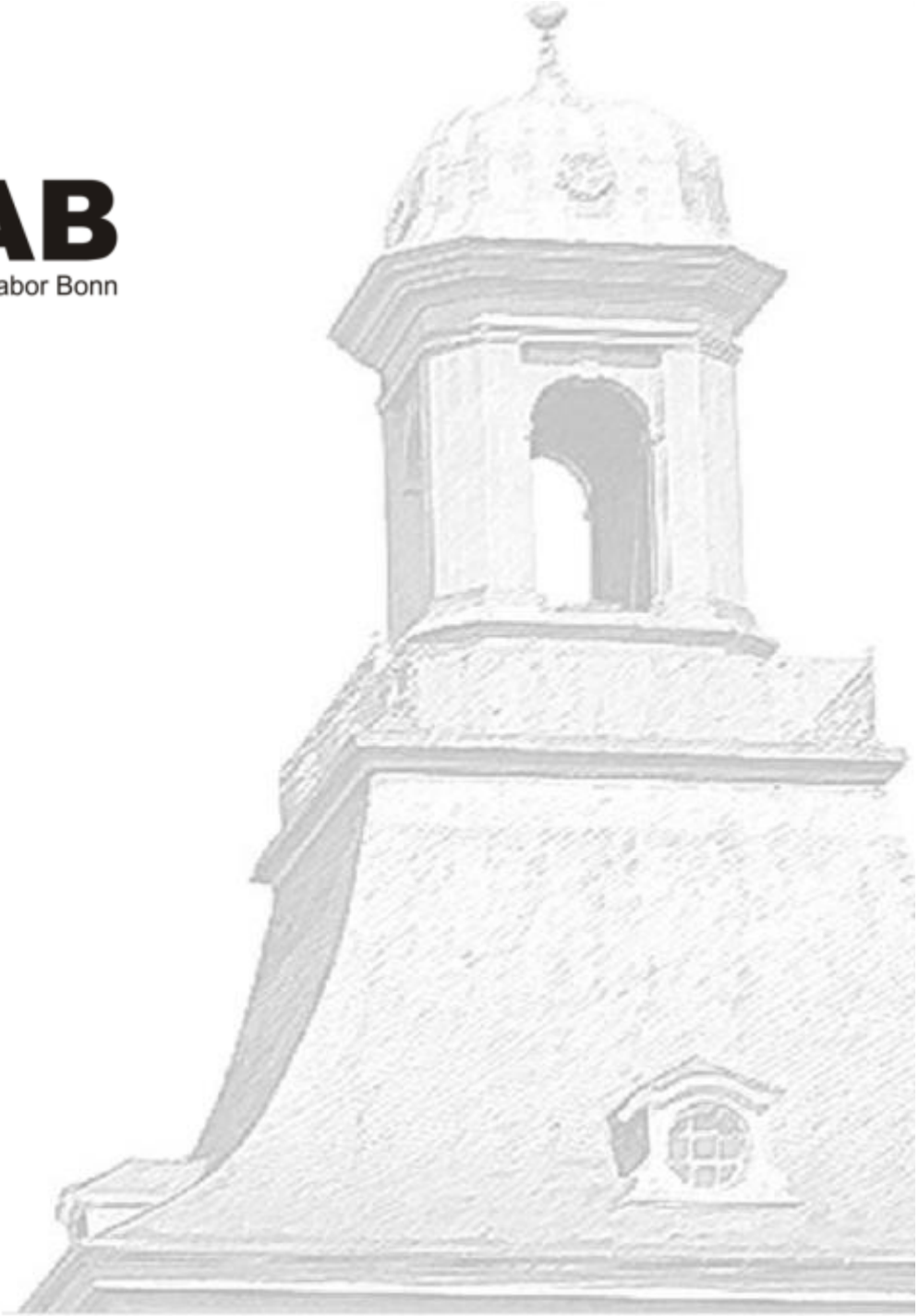

Thank you

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