



Gated Mode on Hybrid 4

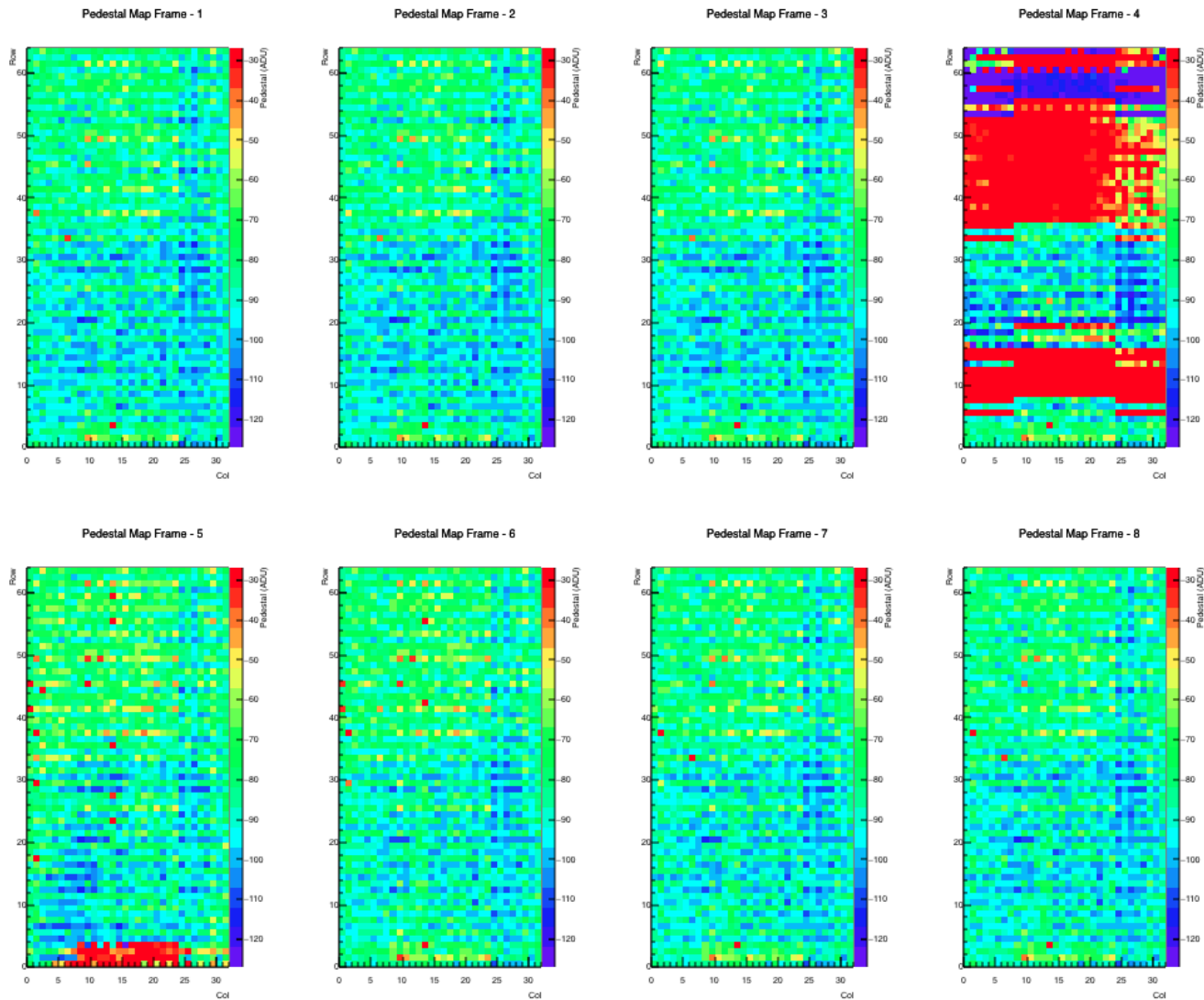
Gated Mode with RO – 1200ns



Gated Mode with RO – 400ns



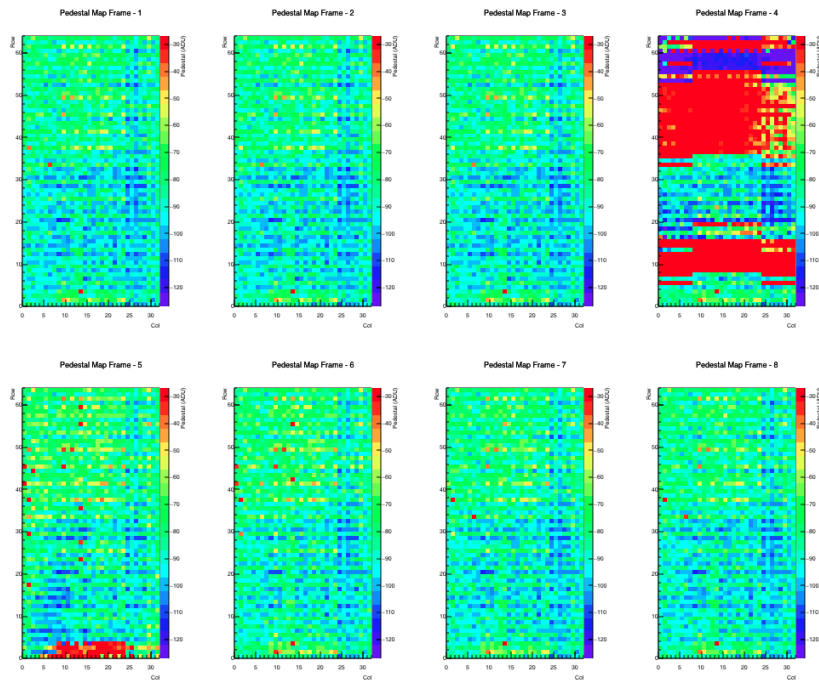
Gated Mode with Read Out – all Frames



Gate Mode with RO – 1200ns

Gated Mode with Read Out – all Frames

- Start of the gated mode shifted by ~ 100ns (one row) (may be due to bad FPGA delay setting)
- Question: how do the pedestals change?
- Would the analog CMC help



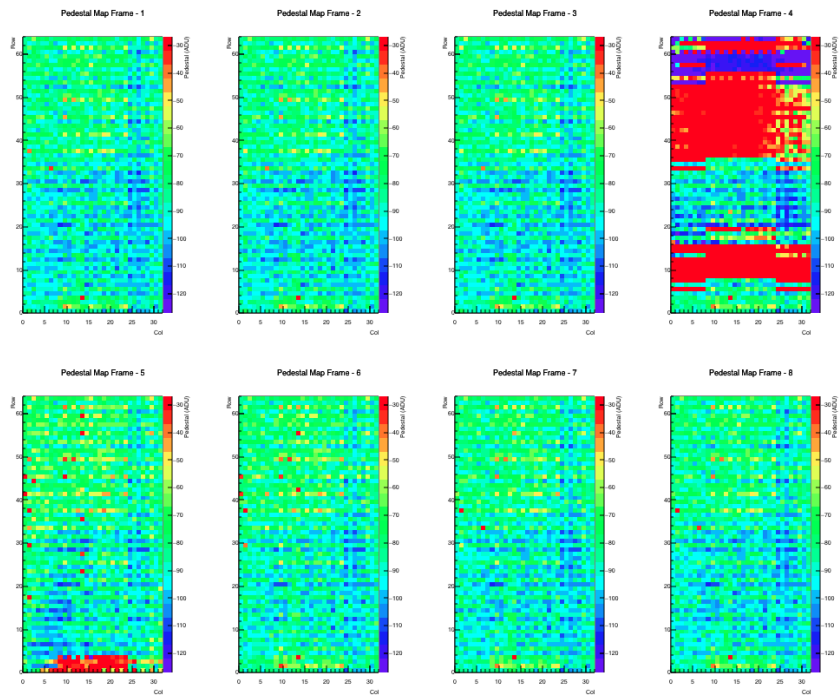
Gate Mode with RO – 1200ns

Pedestal and Common Mode

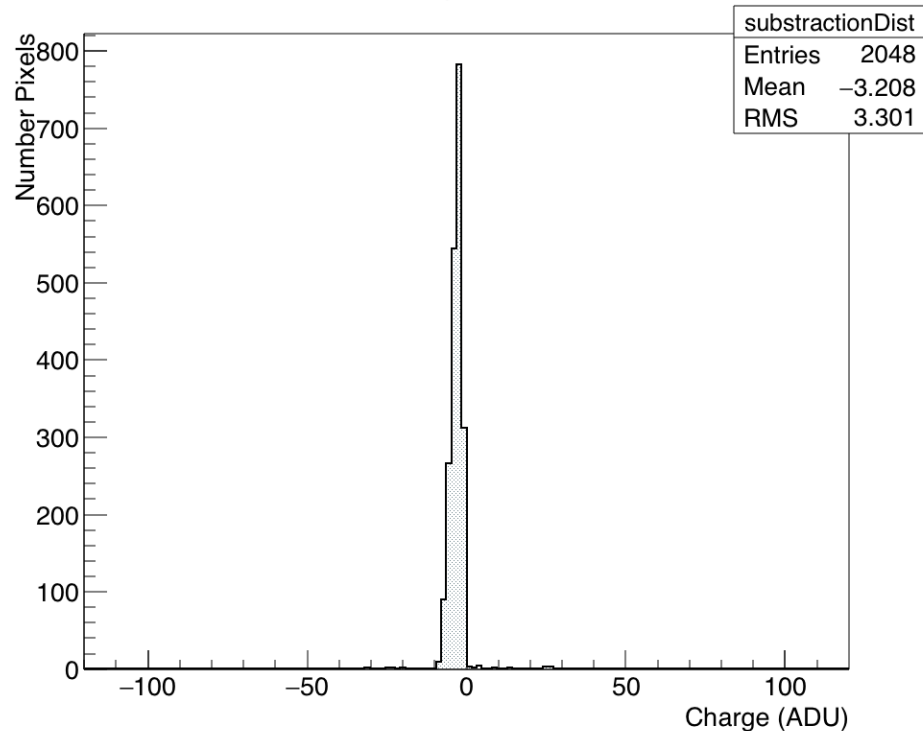
Three methods of pedestal and common mode correction:

- 1) Pedestal \rightarrow offline CMC
- 2) Offline CMC \rightarrow Pedestal
- 3) Analog CMC \rightarrow Pedestal \rightarrow offline CMC

Pedestal → offline CMC



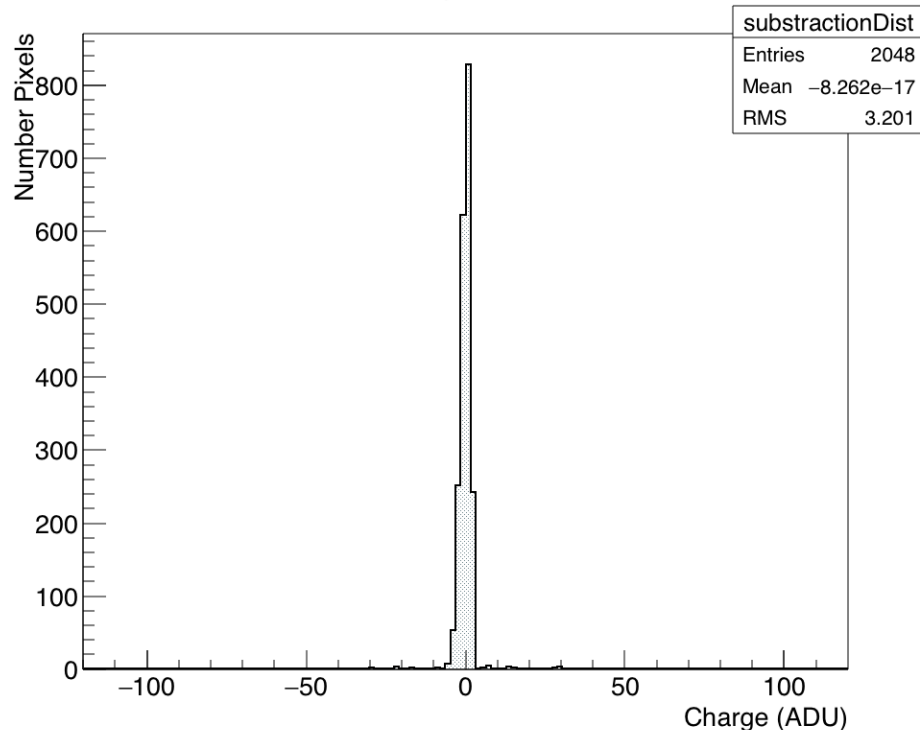
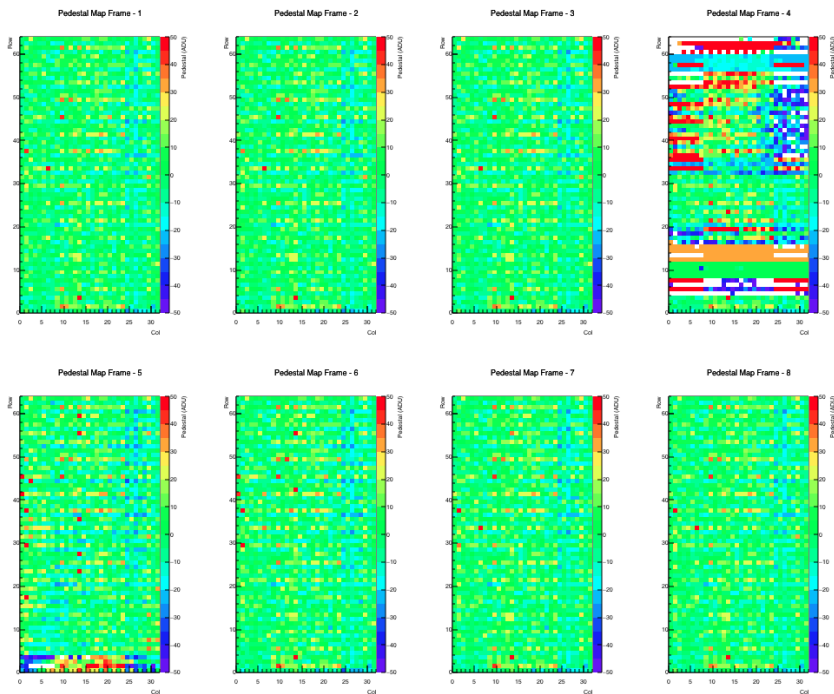
Subtracted Charge Distribution (1 - 6)



Gate Mode with RO – 1200ns

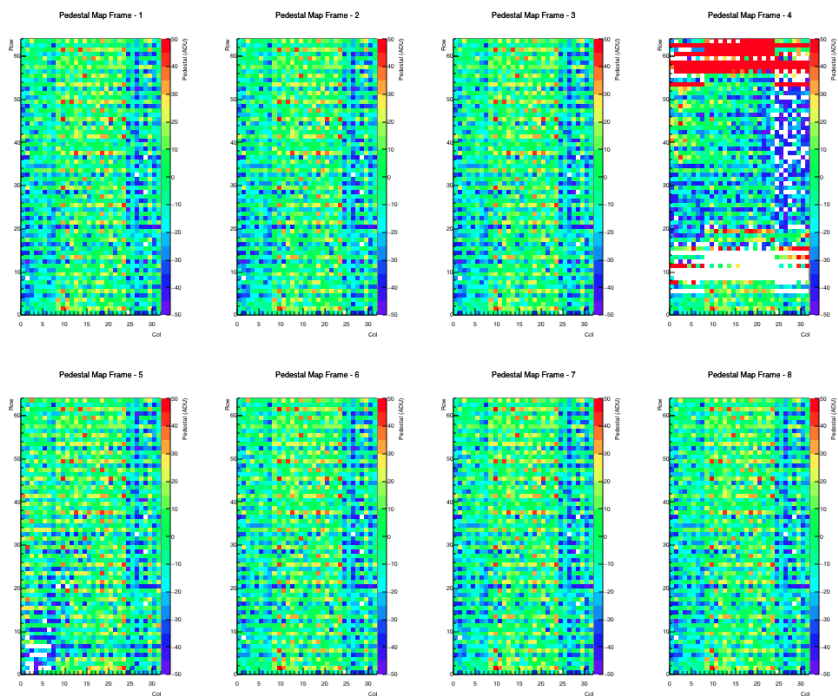
Offline CMC → Pedestal

Subtracted Charge Distribution (1 - 6)



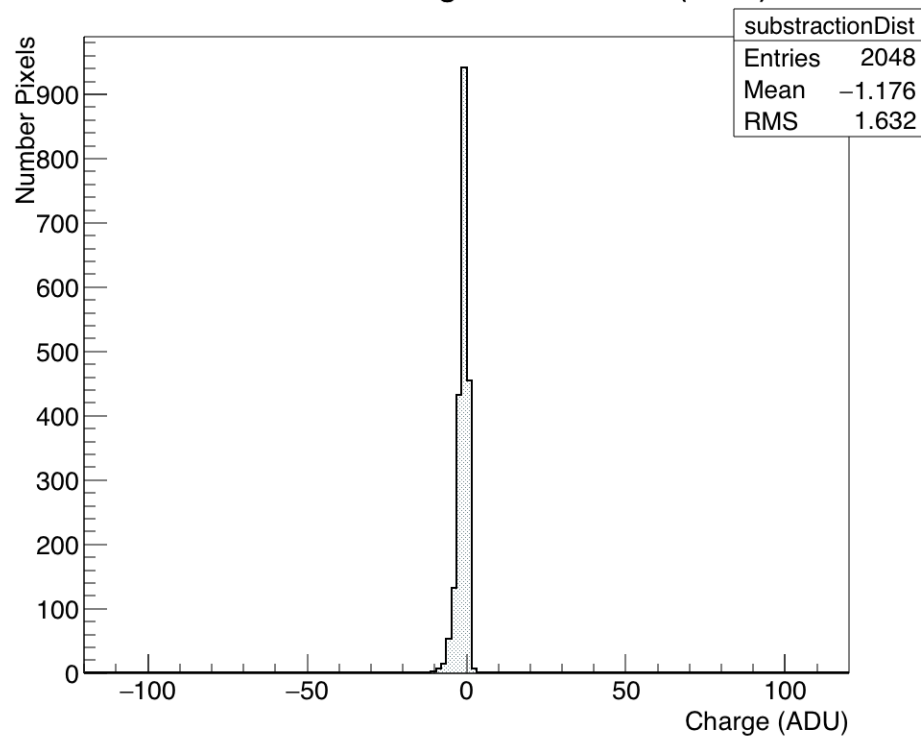
Gate Mode with RO – 1200ns

Analog CMC → Pedestal → offline CMC



Gate Mode with RO – 1200ns

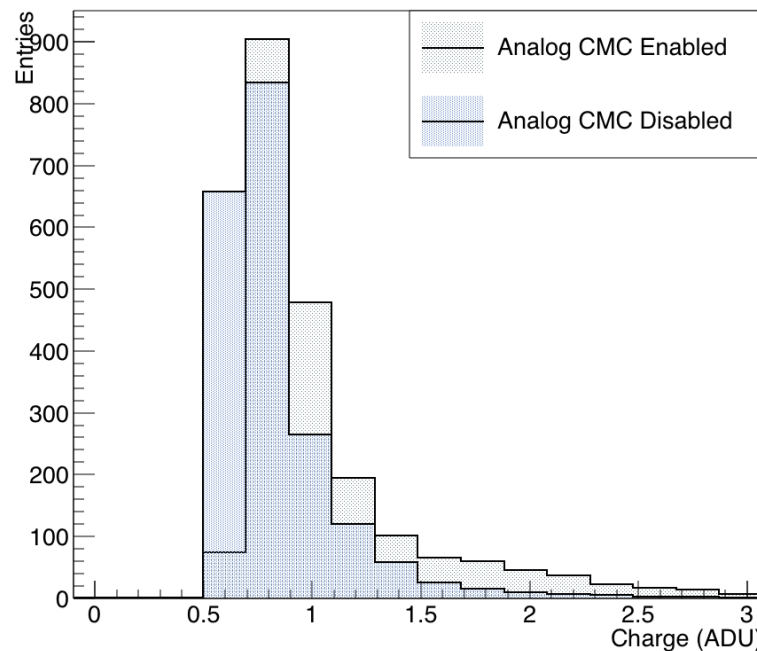
Subtracted Charge Distribution (1 - 6)



Analog Common Mode Correction in the DCDPP

- DCDPP provides an analog CMC which can be switched on and off by software
- TIA is disconnected from AmpLow (still the current of AmpLow changes only by less than 10% for 128 channels)
- VDDA current increases (for 256 channels we reach the current limit of the used power supply prototype)
- Noise increases when analog CMC is on

Noise Distribution Comparison



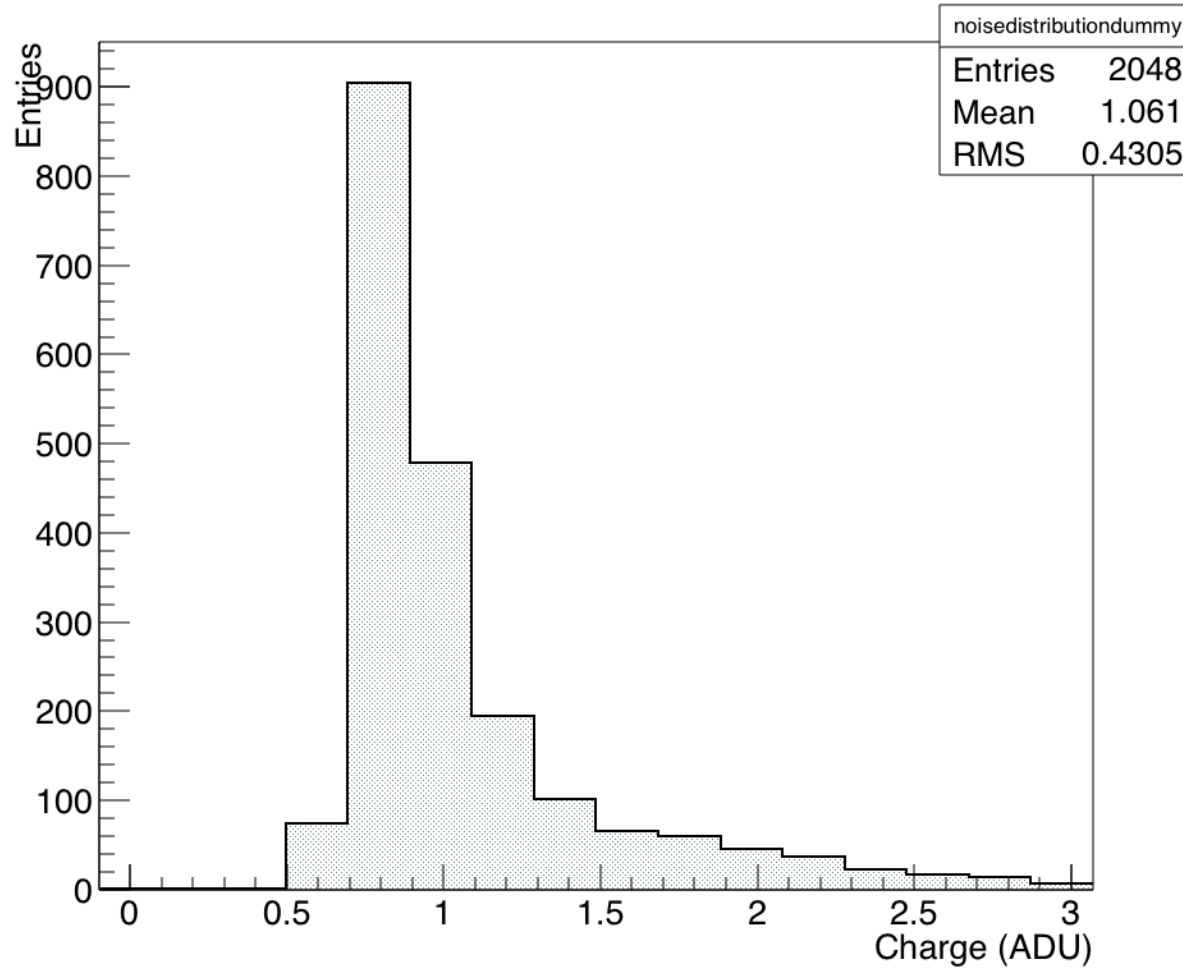
Summary

- Gated mode can be applied with the SWBv2 in a fast way (has to be confirmed for the capacitive load of a large matrix)
- Significant change of the pedestal during the gated mode
 - For the gate mode with RO: how to handle data in DHPT?
- Analog CMC seems to improve the pedestal variation (on a small increase of noise)
 - Analog CMC is also important to correct for inhomogeneous irradiation along z.
- We should write down how to test the analog CMC: setup, who and when

Backup

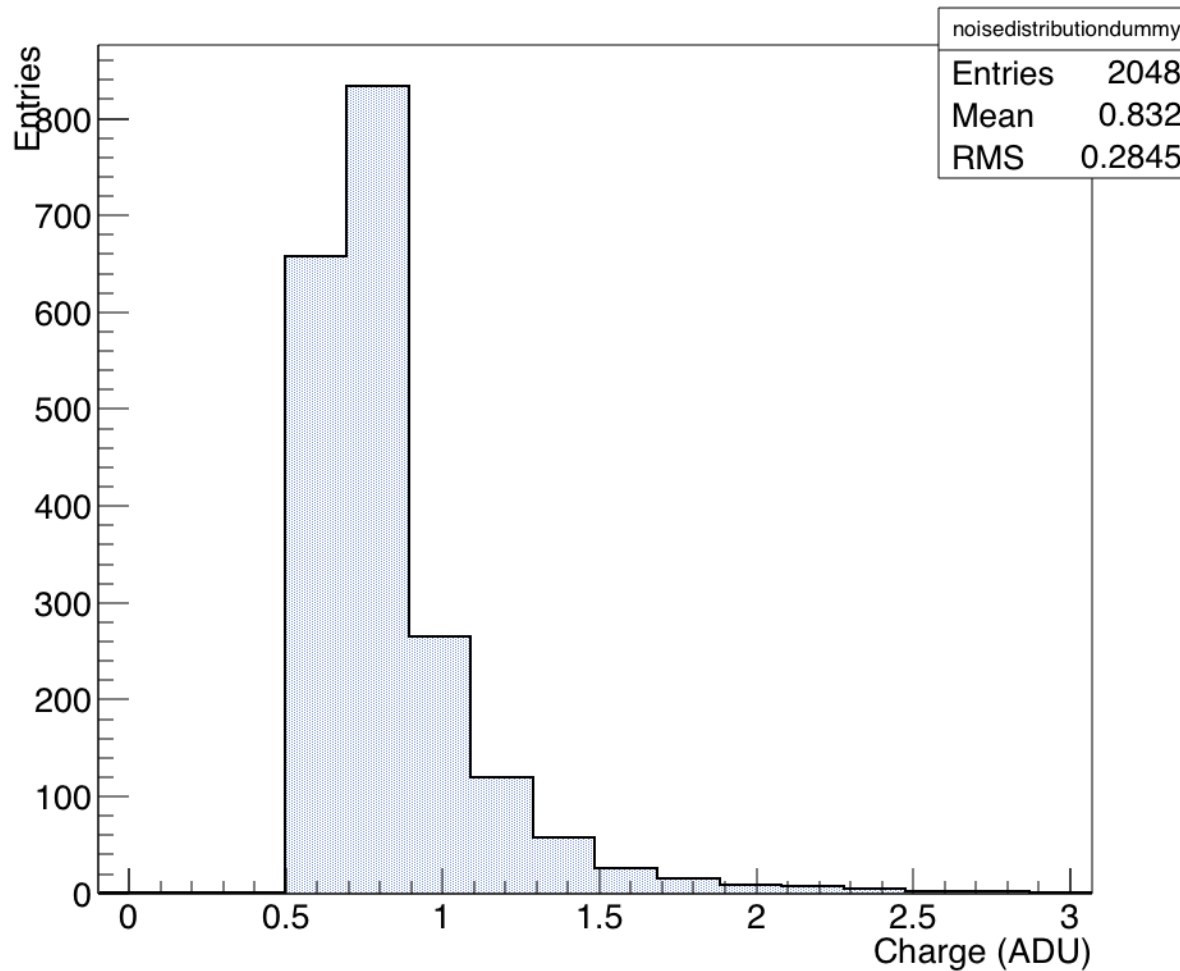
Analog CMC on

Noise Distribution Analog CMC Enabled

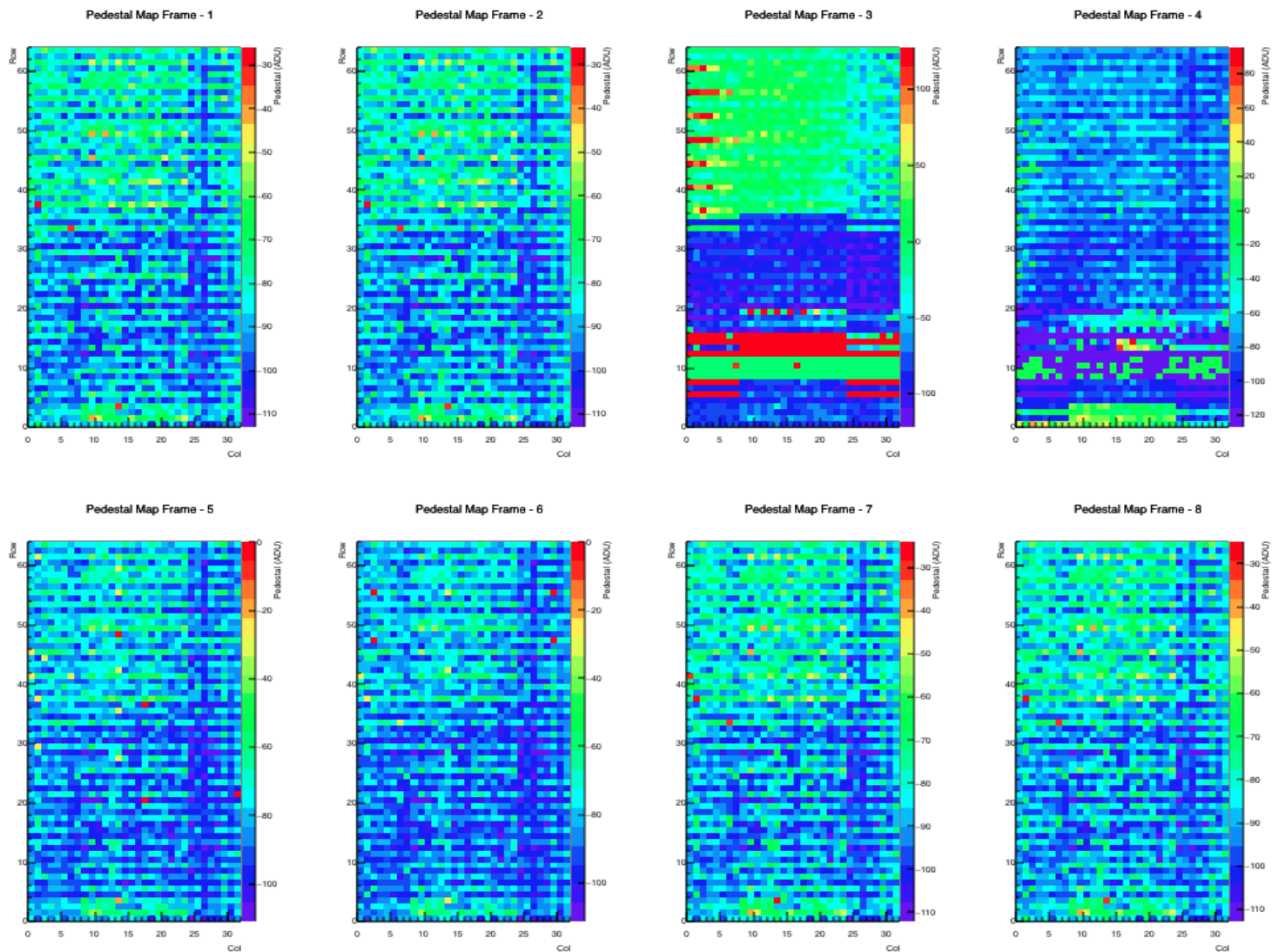


Analog CMC off

Noise Distribution Analog CMC Disabled



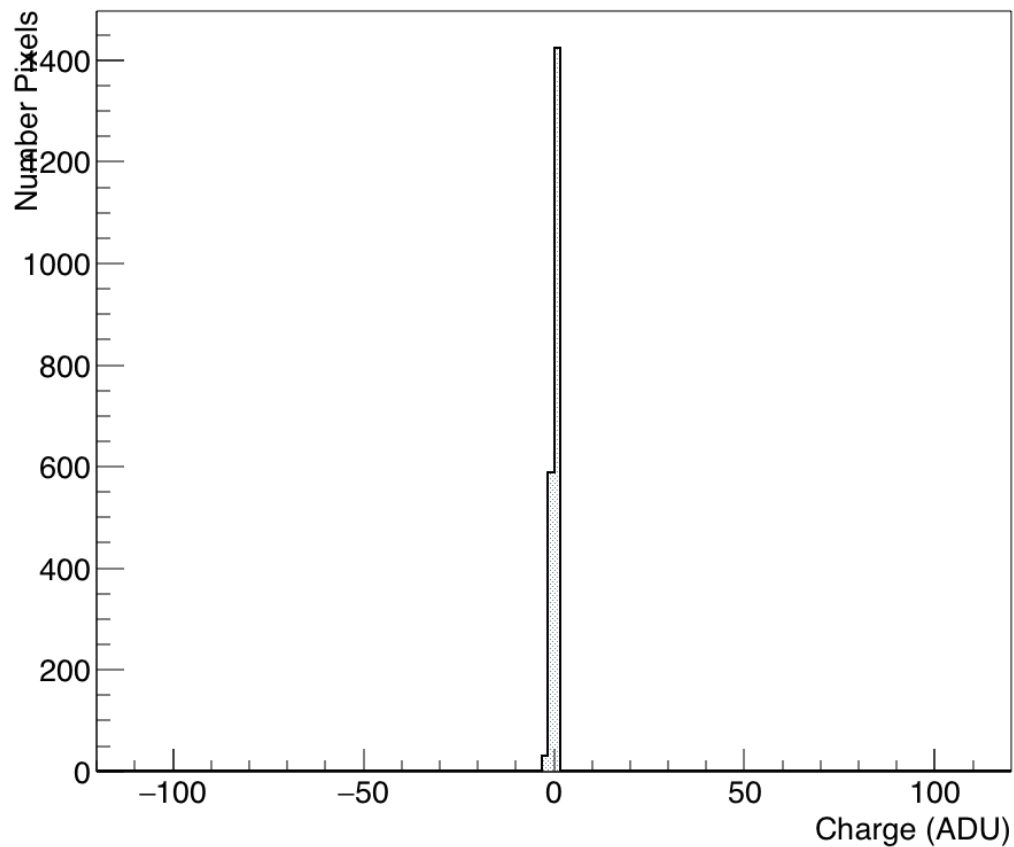
Gated Mode with Read Out – all Frames



Gate Mode with RO 1600ns during frame 3

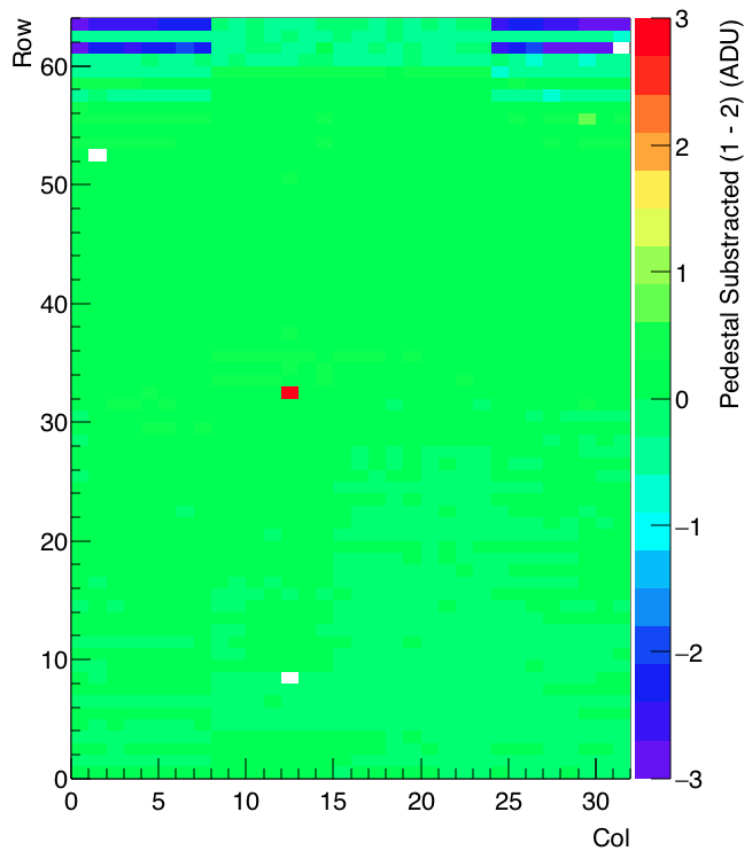
Subtracting Distribution Frame 1 – Frame 2

Subtracted Charge Distribution (1 - 2)



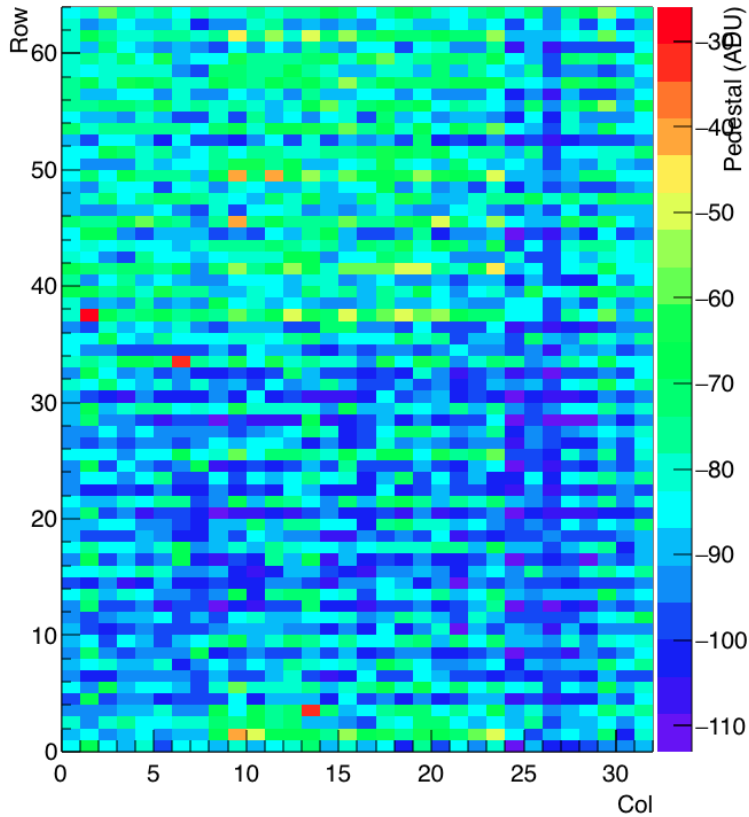
Subtraction Map Frame 1 – Frame 2

Pedestal subtraction Map (1 - 2)

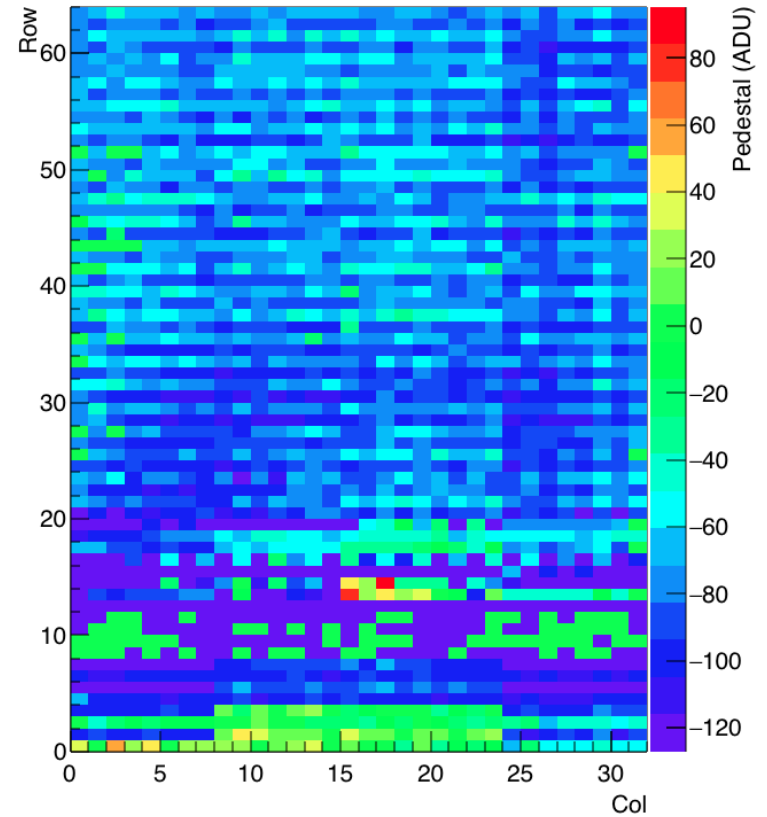


Comparison Pedestal Map R&C - Gated

Pedestal Reference Frame (1)

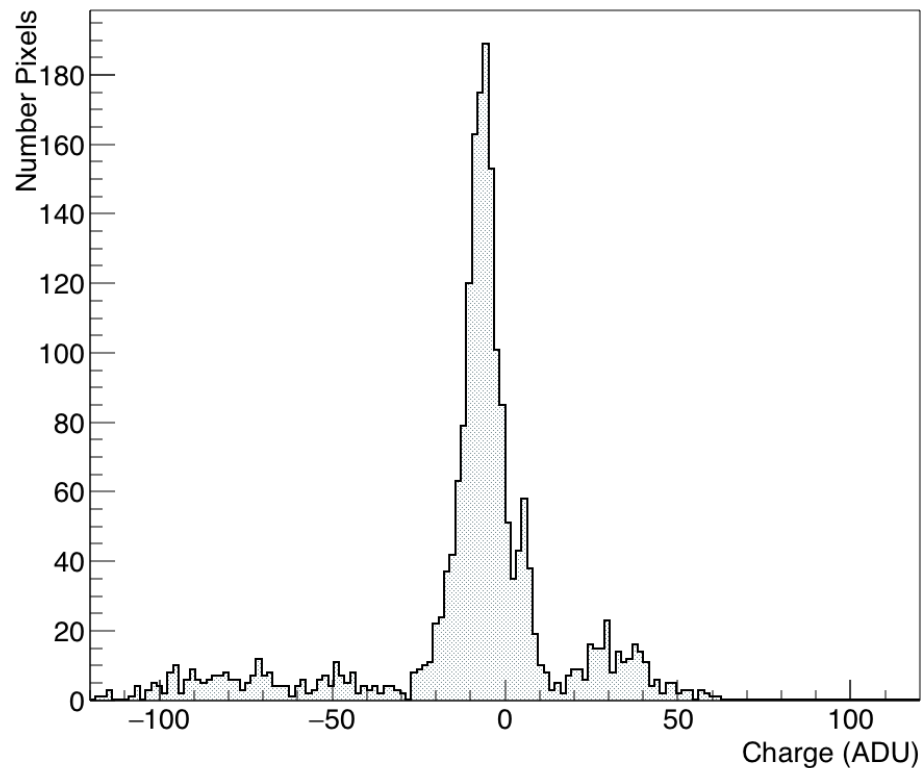


Pedestal Compared Frame (4)

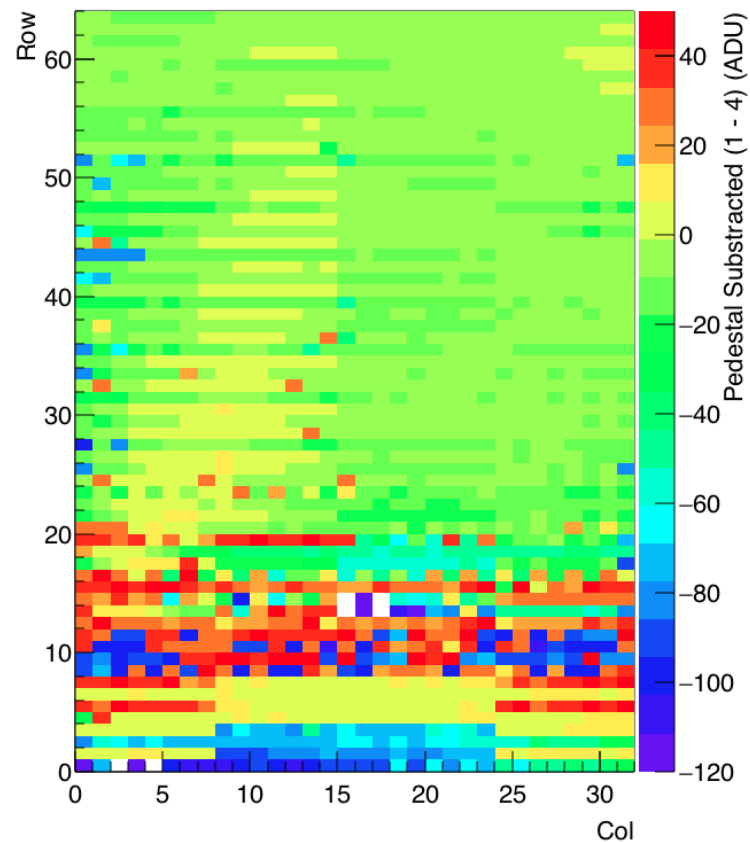


Subtracting Distribution Frame 1 – Frame 4

Subtracted Charge Distribution (1 - 4)

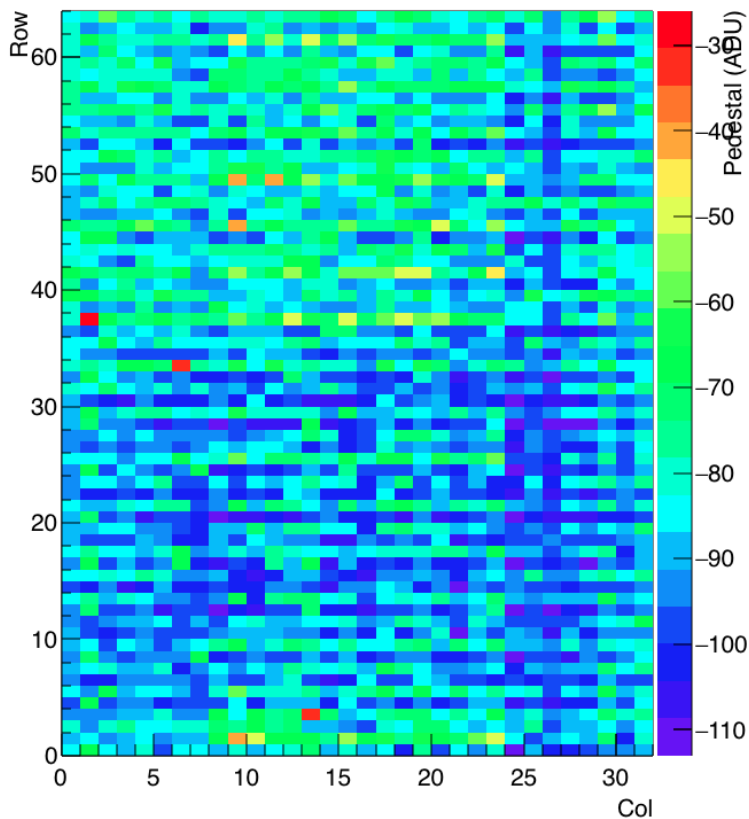


Pedestal subtraction Map (1 - 4)

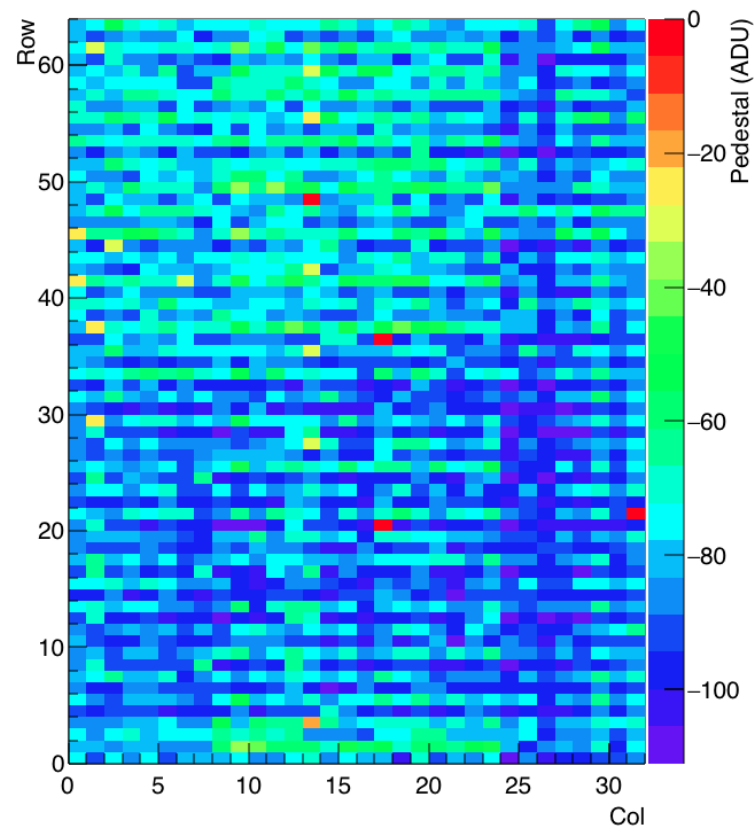


Comparison of Pedestal Map with normal mode after Gating (Frame 1 vs Frame 5)

Pedestal Reference Frame (1)

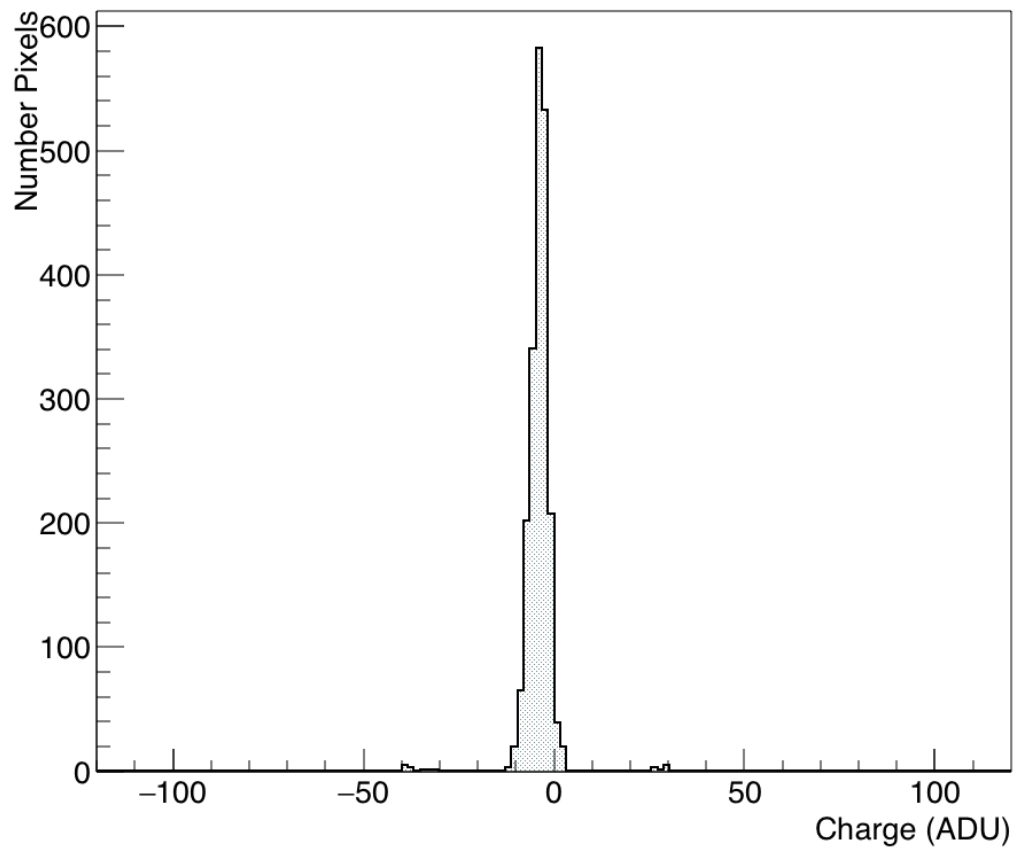


Pedestal Compared Frame (5)



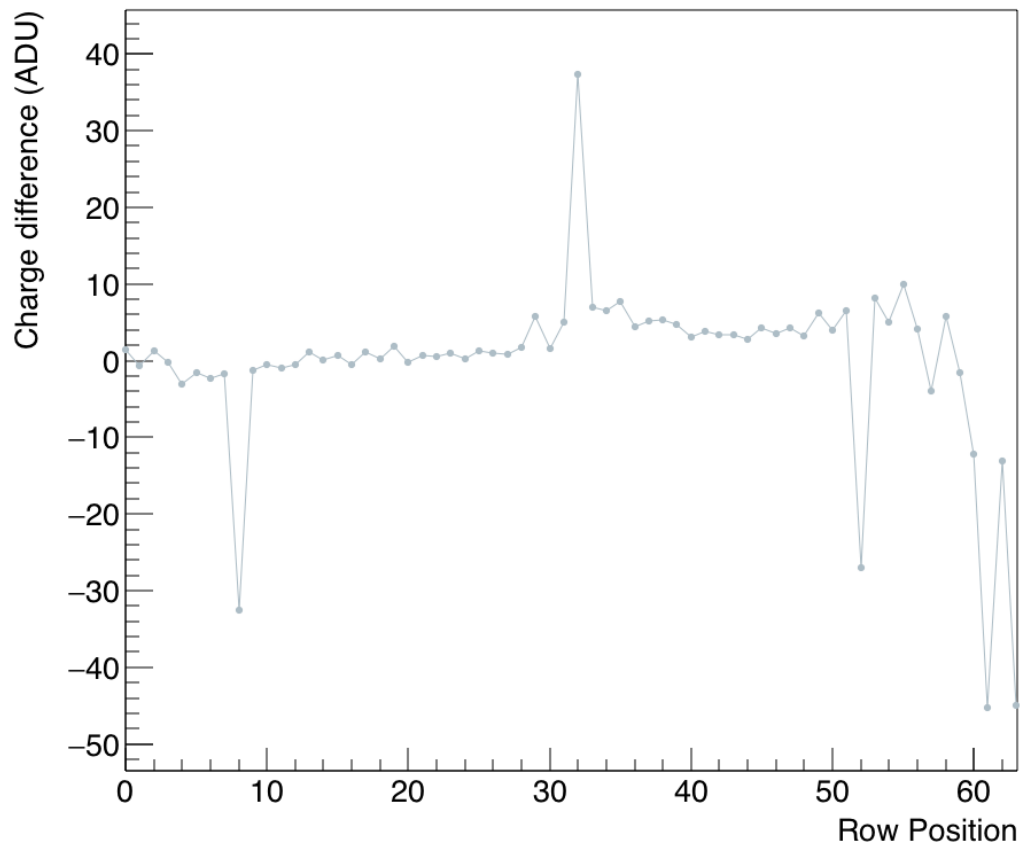
Subtracting Distribution Frame 1 – Frame 5

Subtracted Charge Distribution (1 - 5)



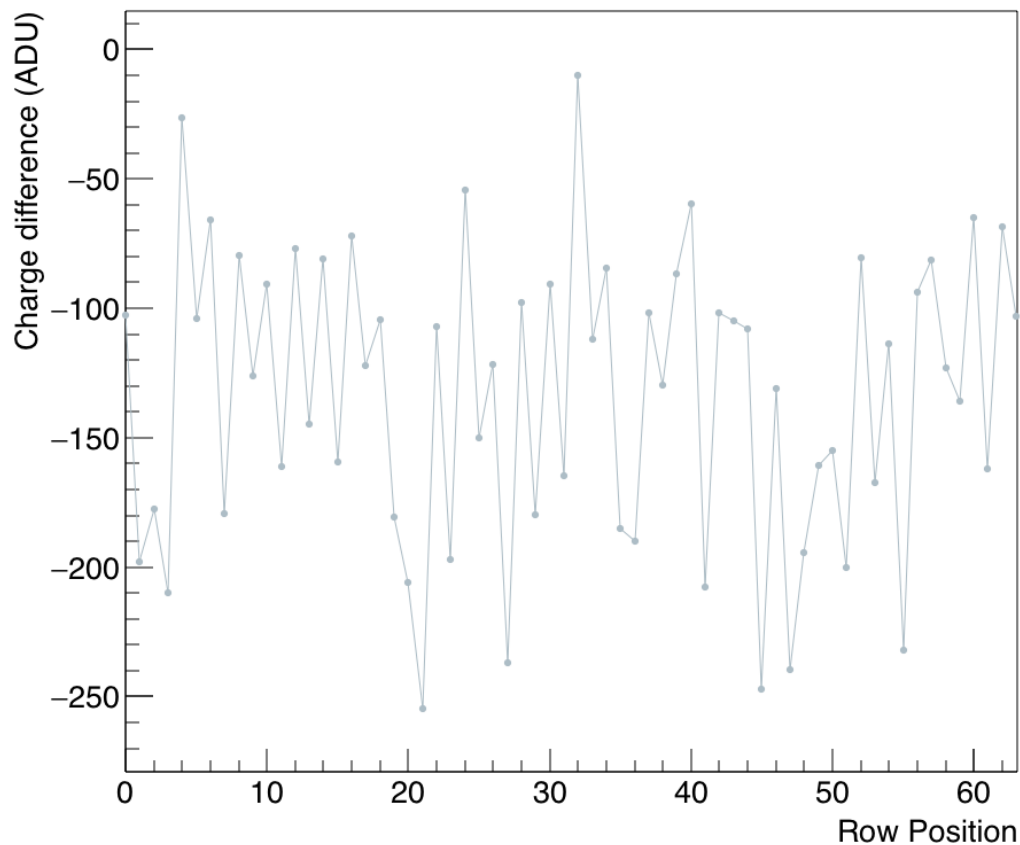
Subtract sum of rows of Frame 1 – Frame 2

Substraction of Charge in a Full Row (1 - 2)



Subtract sum of rows of Frame 1 – Frame 5

Substraction of Charge in a Full Row (1 - 5)



Subtract sum of rows of Frame 1 – Frame 4

Substraction of Charge in a Full Row (1 - 4)

