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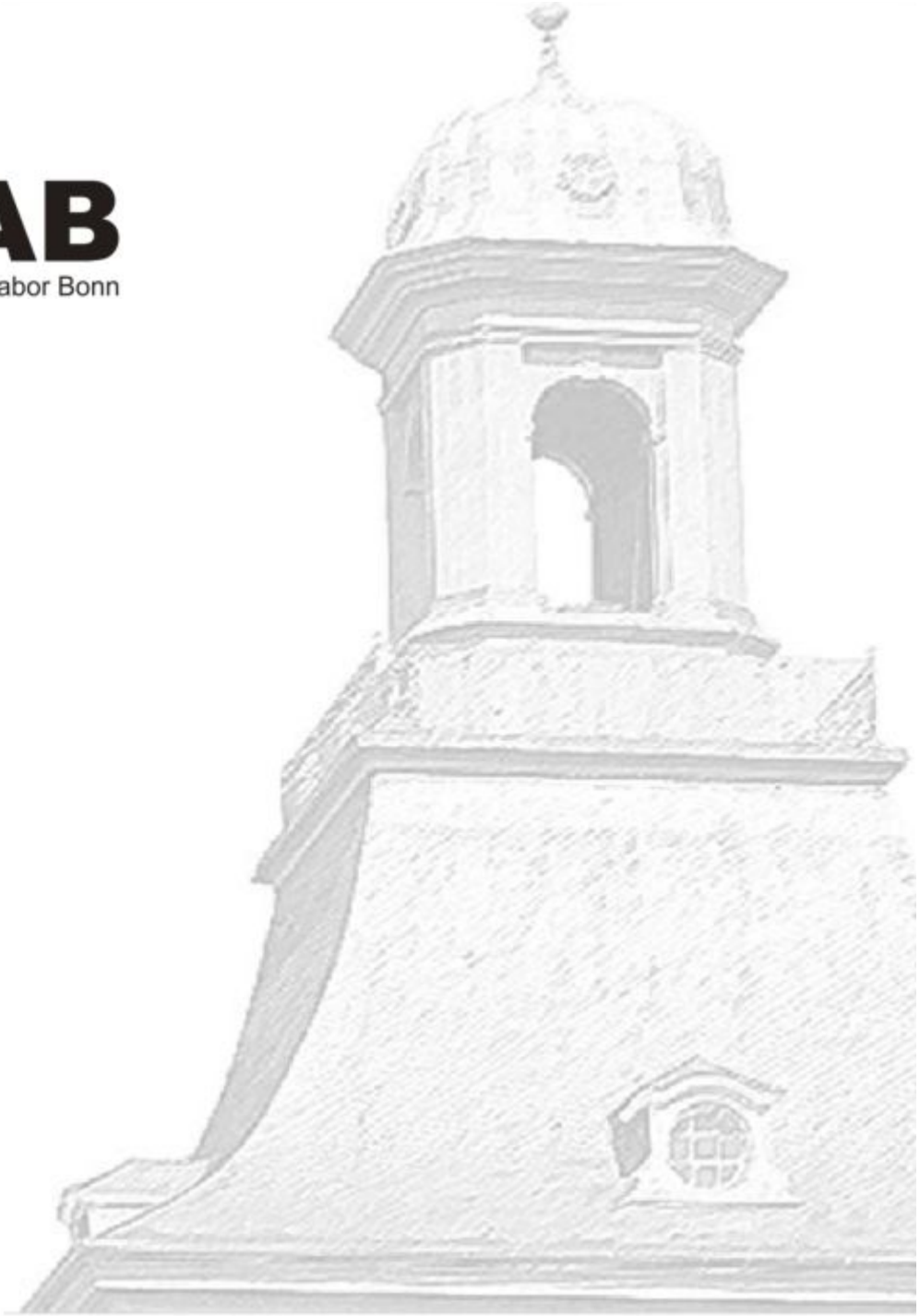

Design Review

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Needle Card testing

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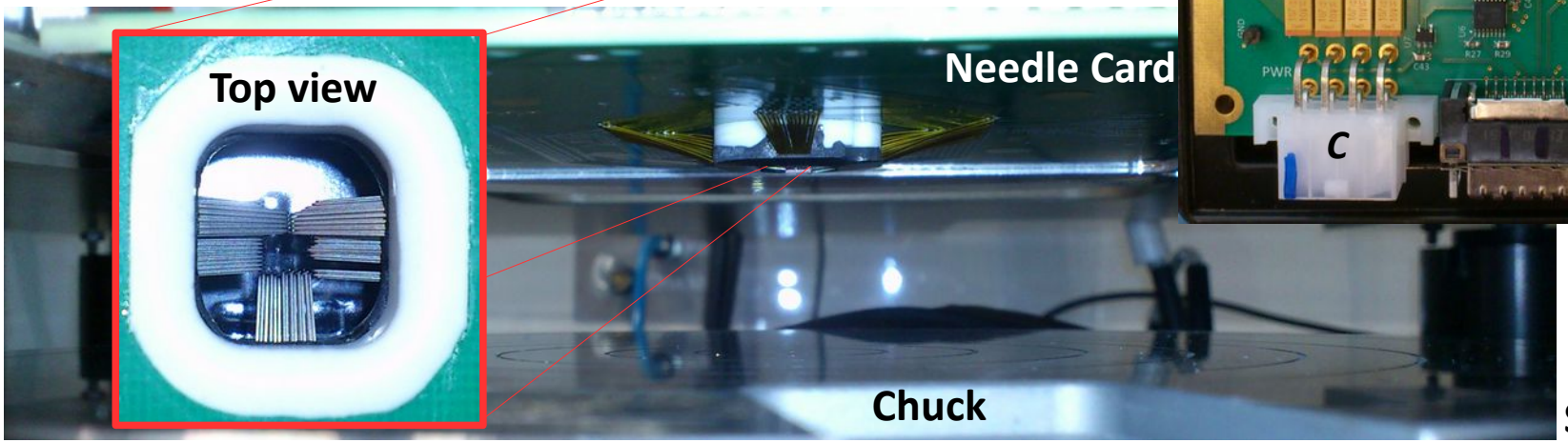
- Xilinx Spartan 6 (DCD emulator) A
- Cantilever Needles B
- Power Connector C
- Infini Band Connector to DHE (Link, JTAG) D



Side view

1. Check power consumption
   VDD 1.4V? DVDD 1.84V?
   GCK is OFF
   GCK is 62.5MHz?
   Check DVDD Power line on DHE site

2. Check JTAG registers

3. Check JTAG to DCD

4. Check Memory Error Counter

5. Check Memory (and 5.)
   - for all - read and write 0xaa, 0x55 and rnd
   a) data
   b) pedestals
   c) offset
   d) switcher seq

6. Switcher sequence generation
   a) Normal mode operation
   b) Gated moder operation
   c) delay setting

7. DCD offset
   a) delay setting

8. Check Link
   a) raw data dump
   b) CML parameter scan (eye-diagram)

9. DCD data
   a) delay setting
   b) read raw data mem via JTAG
   c) IDAC_LVDS_RX dependency
   d) DCD_VREF dependency

10. Check data processing
    - Data generation based on b,c,d -
    a) Triggerlength
    b) Pedestals
    c) Threshold
    d) Occupancy

11. Temperature Sensor
    Read out only

QUESTIONS:

Logging of all measurements results to be provided for each single tested DHPT1.0 (trackID for module debugging)
→ Naming scheme for ASICS?????

Operation parameters for PILOT run and ASICS testing???
Frequency?
Voltages?

Revision of next Needle Card board:

- Current board has no differential dcd clk → added to next revision
- More debug pins to check signals via oscilloscope
- Thicker board (currently 4 layer)

DCD <> DHPT communication

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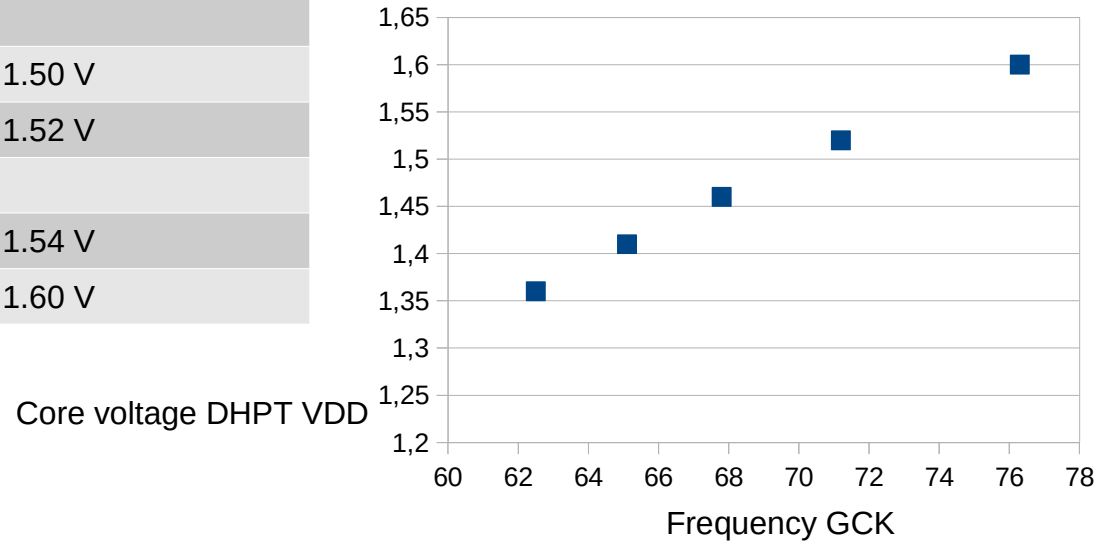
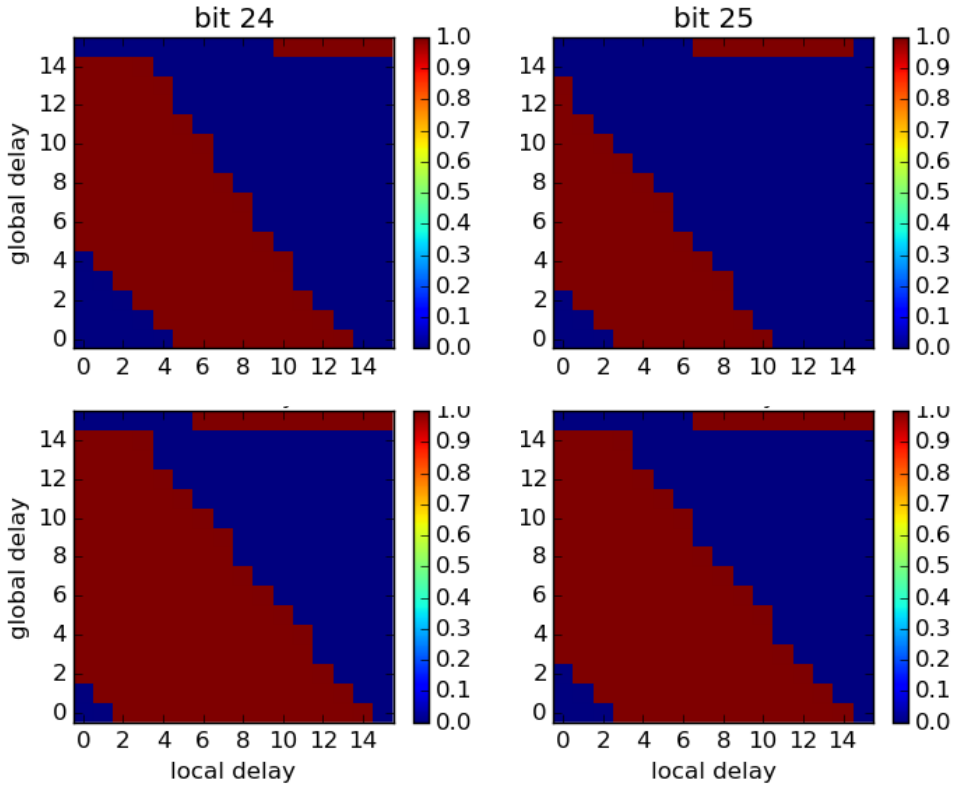
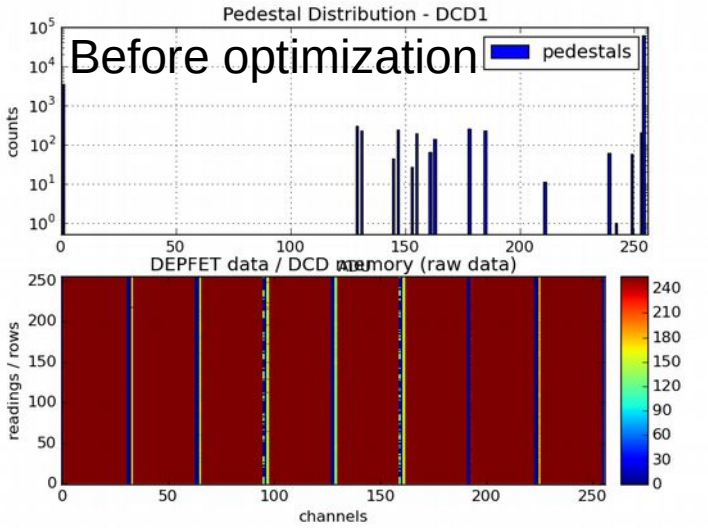
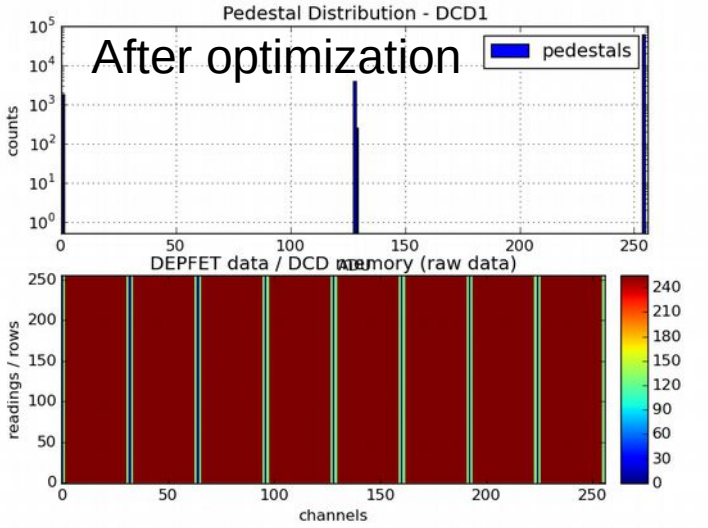
Established link	Frequency GCK	Core voltage DHPT VDD
0	62.5 MHz	1.33 V
1	62.5 MHz	1.36 V
0	65.1 MHz	1.40 V
1	65.1 MHz	1.41 V
0	67.8 MHz	1.42 V
1	67.8 MHz	1.46 V
0	71.2 MHz	1.50 V
1	71.2 MHz	1.52 V
0	76.3 MHz	1.54 V
1	76.3 MHz	1.60 V



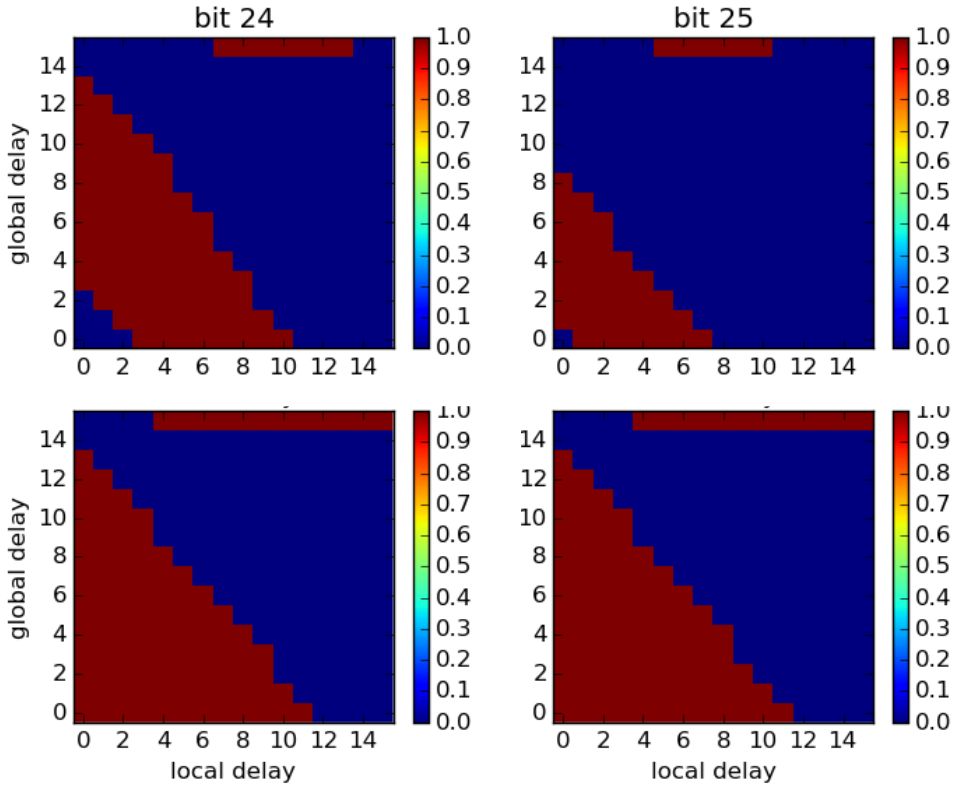
62.5 MHz @ 1.36 V
Region of right dly settings (according to Right testpattern readout)

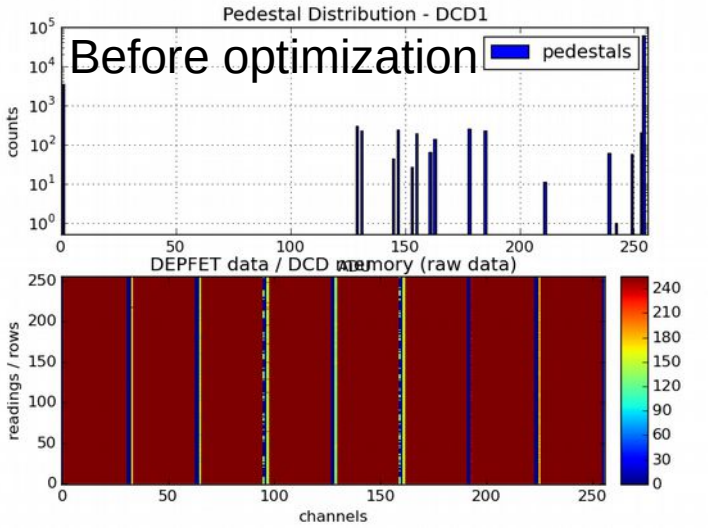


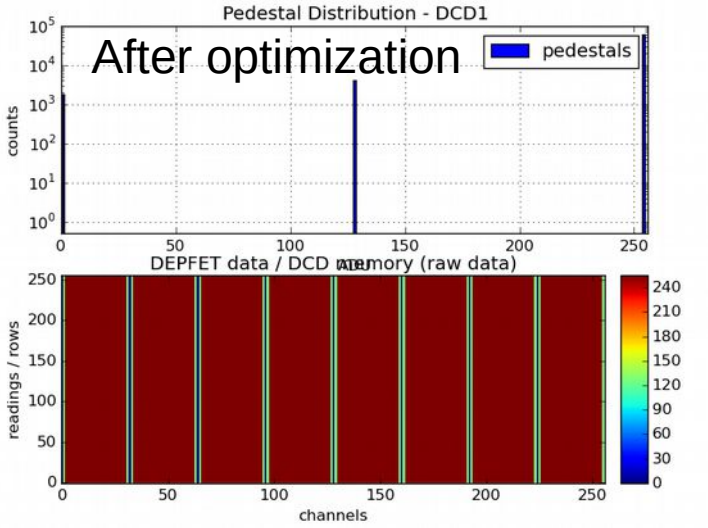




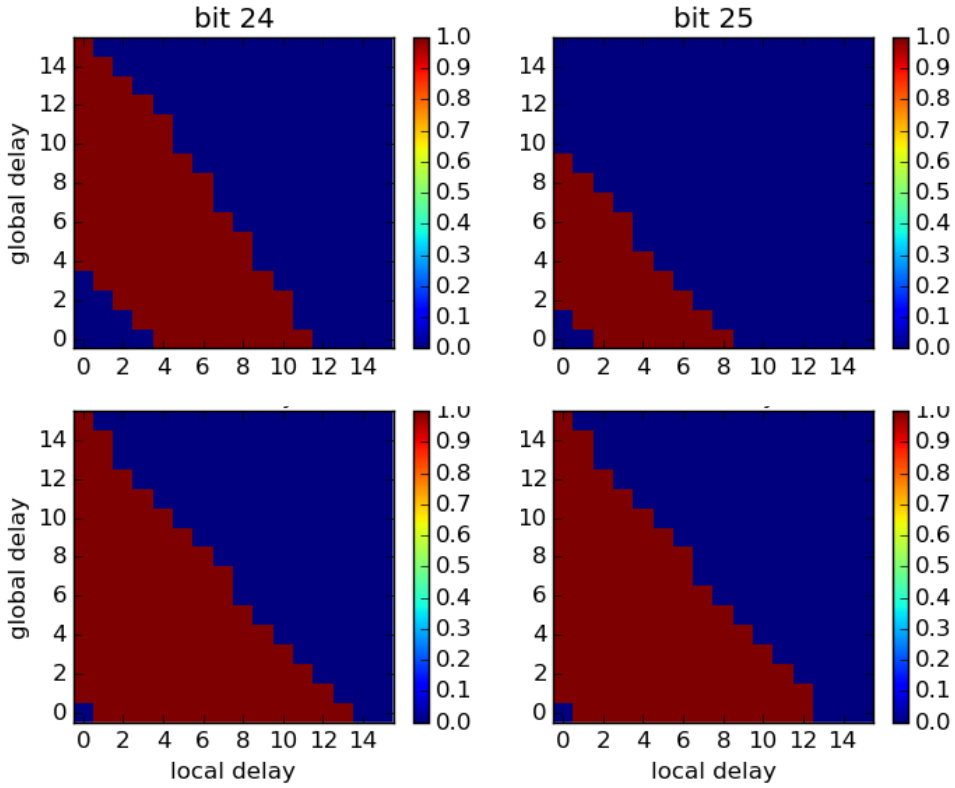
67.8 MHz @ 1.46 V
Region of right dly settings (according to Right testpattern readout)

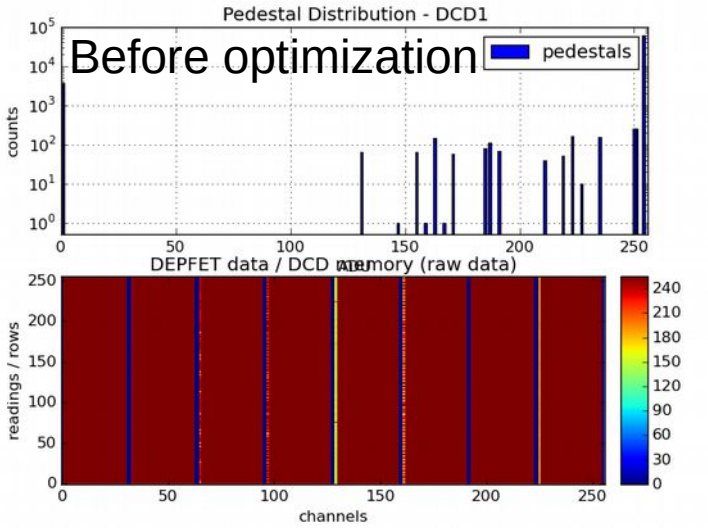


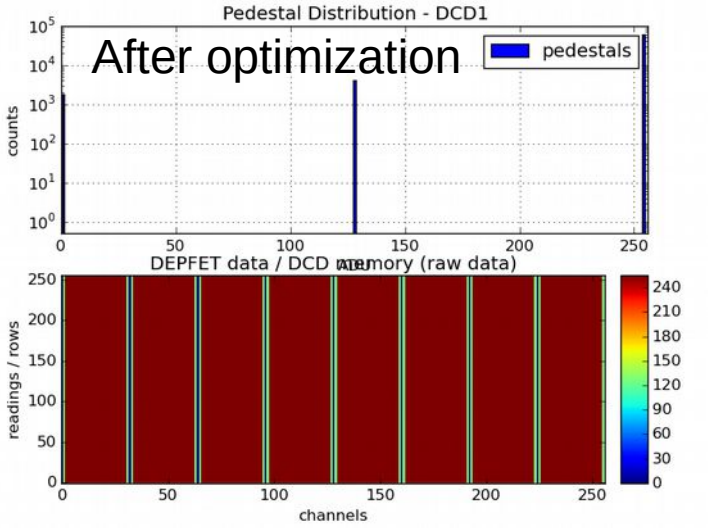




71.2 MHz @ 1.52 V
Region of right dly settings (according to Right testpattern readout)





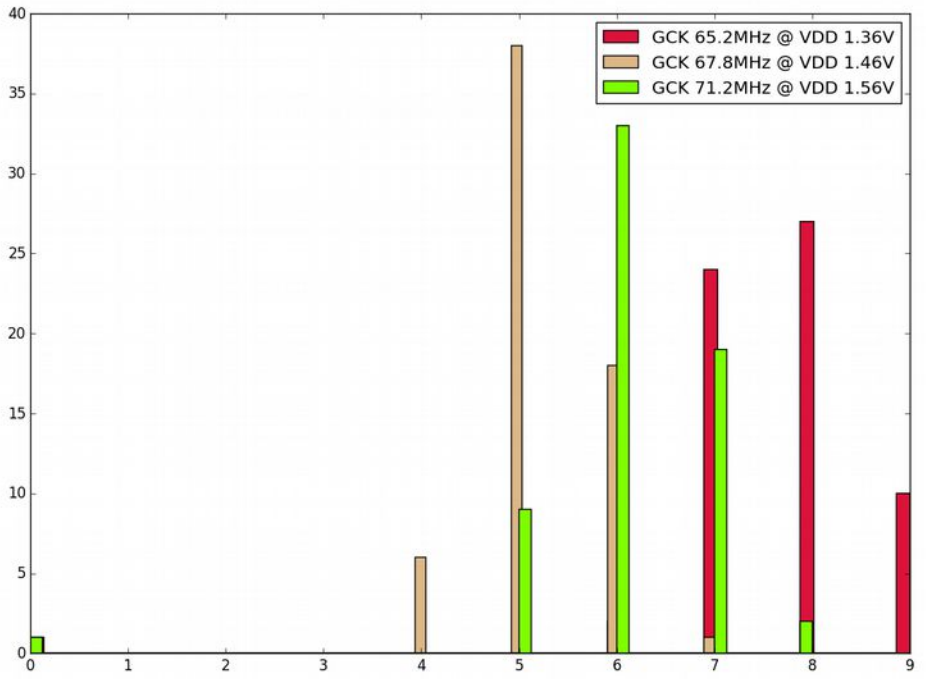


Histogram of distributions of optimized delay settings

Two effects:

Higher Voltages decrease the propagation time through one delay element (faster inverters)

Higher Frequencies decrease the period and the number of dly elements to shift by one period



- For all frequencies and voltages “Bit 8” is still wrong (even with 1.94V DCD VDDA)
  No common setting for all links with correct read out of the pattern

- **Further analysis needed**
  - → preliminary: parameter of good settings shrinks with higher frequencies