PXD9 Pilot Test Setups

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PXD9 Pilot - Test Setup

Test Setup	Aim	Status
Probe Card	Pixel Test	running
Flying Probe System	ASIC Power and data lines	Prepared Verification with metal dummy needed
Test Setup with Hybrid7	Module Test (DEPFET + ASICs)	In preparation
Test Setup with Kapton	Module Test + System Test	In preparation

Note: For the PXD9 Pilot we will not have a probe card test after component assembly (before kapton attachment).

PXD9 Pilot – Test Setup Component and Task Overview

Google spread sheet for overview of setup components and measurement tasks:

https://docs.google.com/spreadsheets/d/155aSvn3mvLV5qWFrh0GnLXhELrkM1Mf4Xqo_J7SGIs0/edit#gid=0

Pilot Run PXD9 Test Setup Components		
Component	**Institute**	**Person**
Mechanics		
setup for jig - fixation, stress relief	MPP	Tscharlie
Cooling		
PowerSupply		
Hameg HMP4040		
PowerSupply	LMU	Stefan
NOTAUS for PS	LMU	Stefan
BreakoutBoard	LMU	Stefan
Fan for PS	LMU	Stefan
Green cables (MixedDSub)	LMU	Stefan
Banana cables (4pairs)		
DHE		
DHE	TUM	Dima & Igor
DHE Carrier Board	TUM	Dima & Igor
DHE Fan	TUM	Dima & Igor
DHE Power Connector	TUM	Dima & Igor
JTAG USB Adapter		
Option1 - Hybird7:		
cables		
Glenair cable (connector - connector)		
Infiniband cable (connector - connector)		
RJ45 cable (connector - connector)		
jig for Hybrid7 (similar to EMCM)	MPP	Tscharlie
Option2 - Kapton:		
cables		
Glenair cable (connector - wires to be soldered)		
Infiniband cable (connector - wires to be soldered)		
RJ45 cable (connector - wires to be soldered)		
jig for Kapton	MPP	Tscharlie

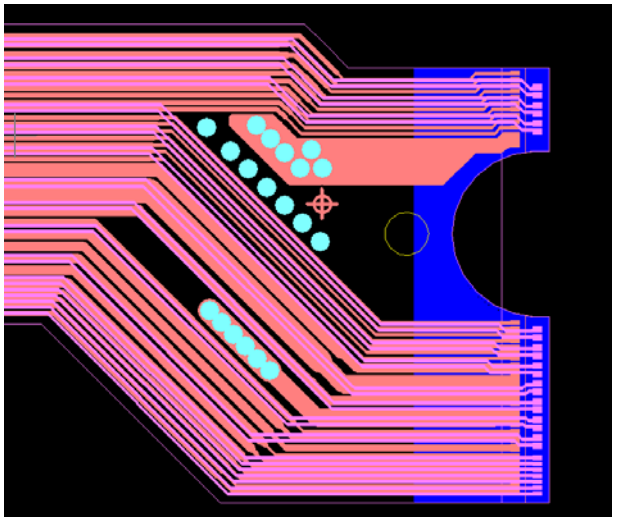
#	Task	
1	Power up ASICs	
2	sanity check: voltages and currents	
3	configure JTAG	TO DO: readout of temperature
4	sanity check: voltages and currents; high speed links; DHPT temperature	
5	check boundary scan (incl. DHPT-DCD links)	
6	scan DHPT link paramters (amplitude, boost, delay)	TO DO: write script
7	digital test pattern, delay scan	
8	program SWB sequencen (192 channels) - DHPT output still off	TO DO: find optimal sequence
9	increase DCDPP current limit	
10	enable DCDPP analog part: analog CMC off, no pedestal correction	
11	sanity check: voltages and currents	
12	enable DHPT to SWB control signals	
13	Probe Switcher Control Signals	- not possible on PXD9
14	power up DEPFET voltages	list of voltages - Rainer
15	sanity check: voltages and currents;	
16	raw data read-out	all DHPTs simultanously, Pixel mappin
17	check: pedestal distribution, noise	
18	check: response on light (laser)	
19	sampling point scan	
20	optimization of DEPFET voltages,	
21	store pedestal values for 2-bit DAC offset correction	
22	upload pedestals for zero suppressed readout	memory mapping (timing)
23	trigger zero suppressed frames (no data should arrive)	
24	Laser spot (move laser accros the matrix)	
25	Source measurement	

PXD9 Pilot – Test Setup with Kapton

280mm

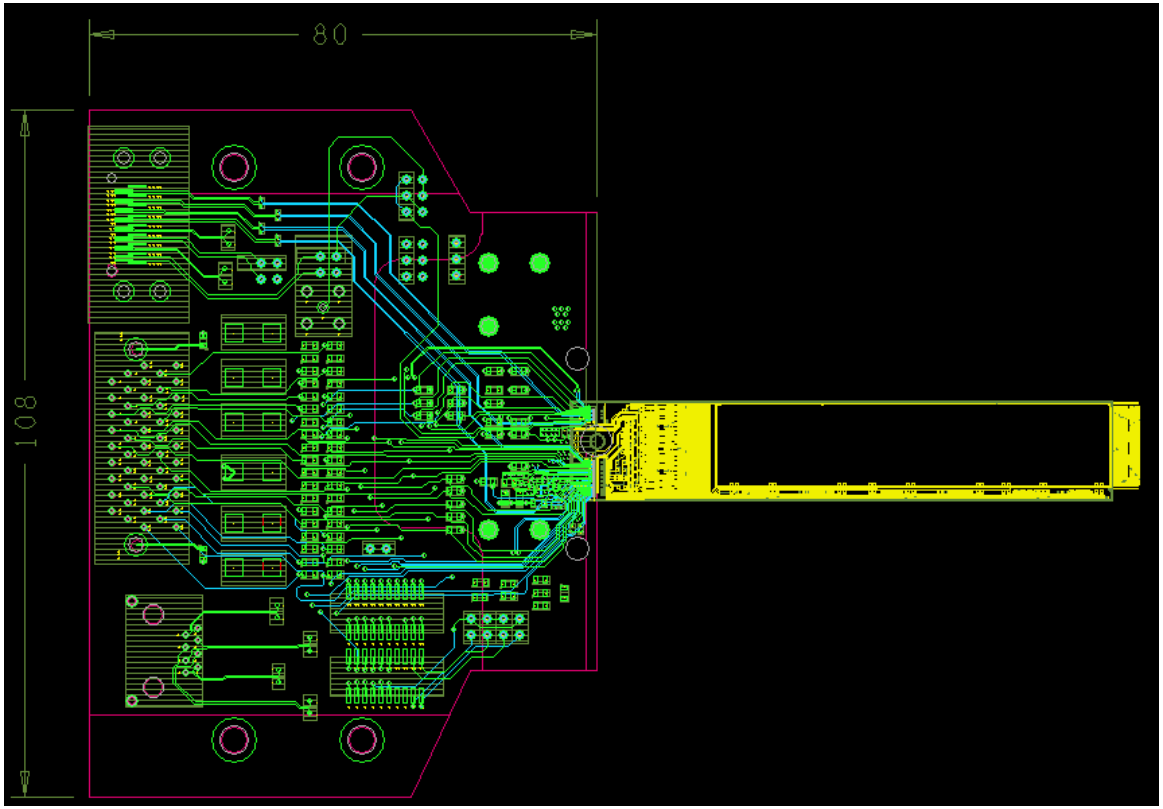
430mm

Wirebond fanout for outer backward module (OB) and inner forward



- test full signal path (kapton + data patch panel + cable)
- Combined data patch panel + power patch panel needed (by Stefan Rummel)

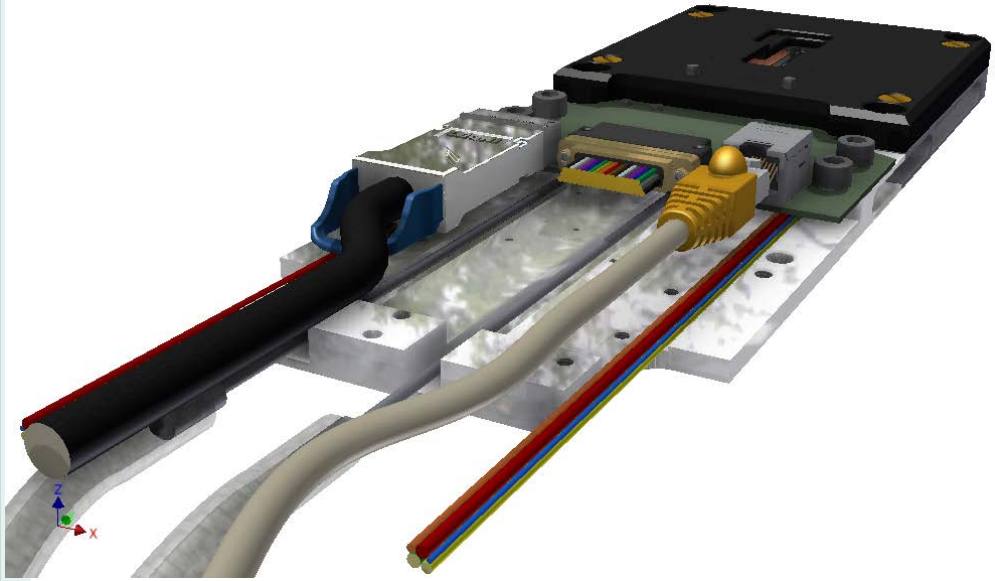
PXD9 Pilot – Test Setup with Hybrid 7

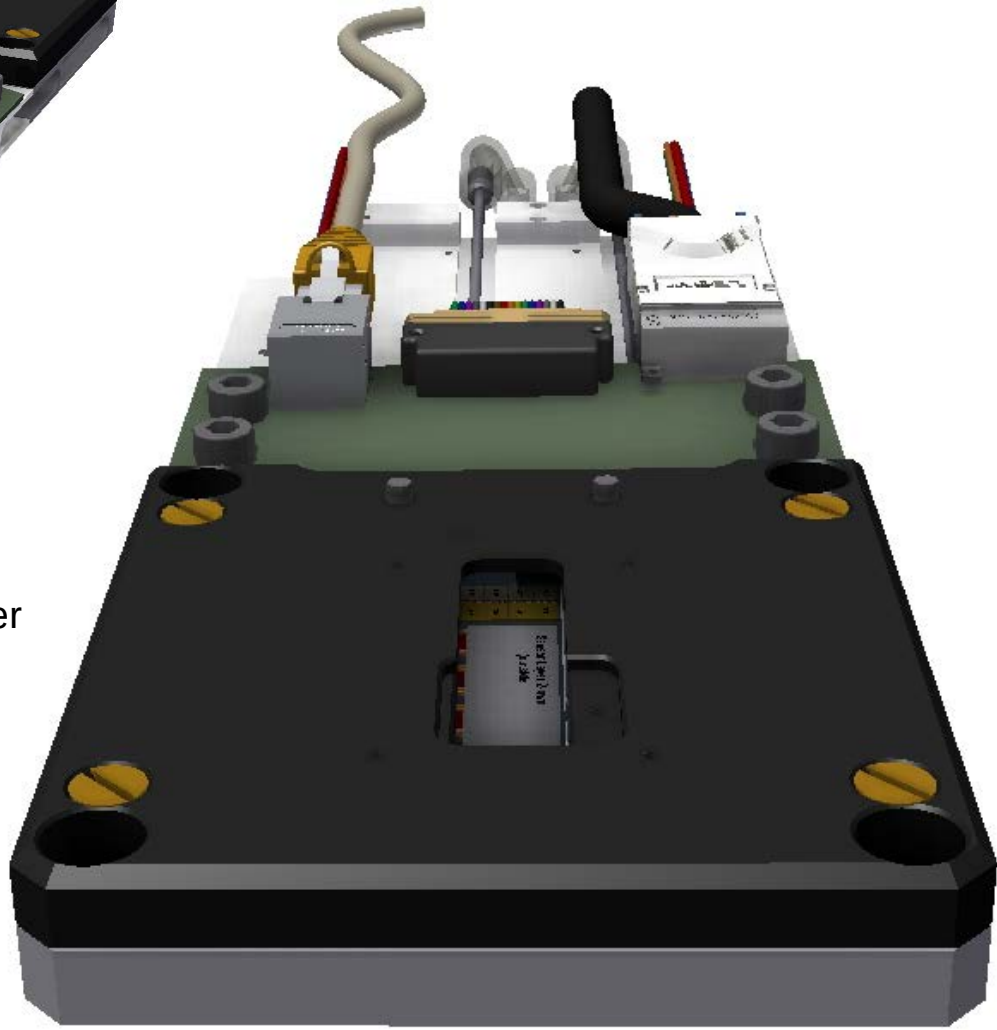


Hybird7 (for Outer Backward and Outer Forward – 2 different layouts) are in preparation:

- Layout for Outer Forward is finalized
- Lead time for PCBs 4 weeks
- Mechanical holder in preparation (in MPP workshop)
- **Focused on PXD test rather system test (much shorter traces, more decoupling)**

PXD9 Pilot – Test Setup with Hybrid 7





- re-use of EMCM boxes (still long lead time)
- Opening in the box (top and bottom) for laser and beam test

What is ready/missing for PXD9 testing?

What is ready?

- Switcher sequence for 192 channels ready
- Automatic JTAG configuration of DHPT1.0, DCDPP and SWB
- Procedure to automatically power up/down the DEPFET pixels and ASICs
- Fast display of raw data (python based)

What is missing?

- More experience with the various components like DHE and Power Supply
- Gated-Mode support by the DHE
- Test analog common mode correction on the EMCM
- Documentation: test setups components, test plan for PXD9, allowed voltages (including limits if the sense line connection is lost)
- Software:
  - Automatic measurement routines
  - **Improvements in stability and speed**