# PXD Flex Cable
# Prototype Characterization
# (V2.1/2.2 + Production sample)
# Update

H.Krüger 20.5.2015

# Outline

- Devices under Test
  - Taiyo Flex V2.1 (1st production)
  - Taiyo Flex V2.1 (2nd production)
  - Kaupke Flex V2.2

- TDR and TDT Measurements

- Results
  - DC resistance
  - TML impedance
  - Frequency depended attenuation

- Proposed design changes

# Flex Cable Prototypes

- Same design (MPI) produced by two different manufacturers (Taiyo, Kaupke)
  - length: 490mm
  - layers: 4
- Two productions by Taiyo (identical design data, V2.1)
- Kaupke design data with smaller via hole (0.2mm instead of 0.35mm, V2.2)
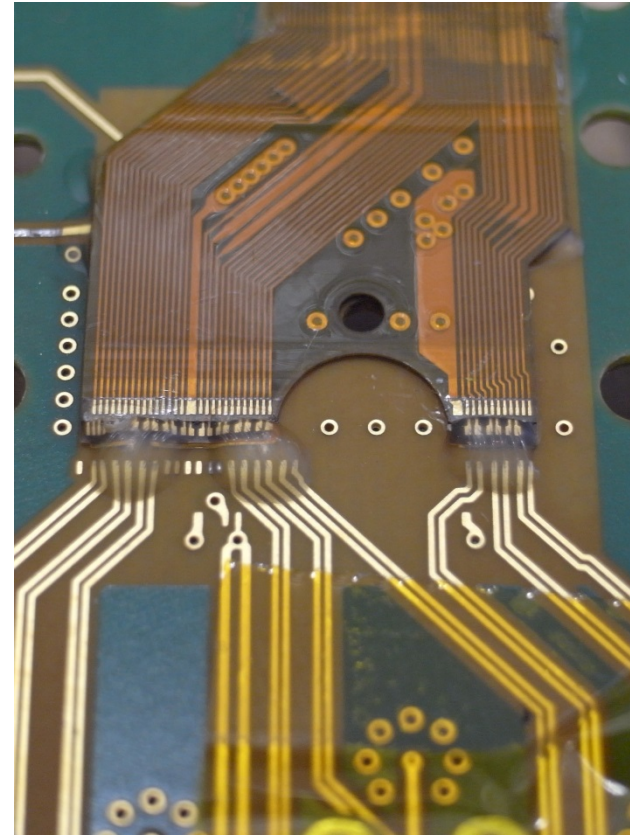- Kaupke and Taiyo apparently use different layer stacks (see measurement data)
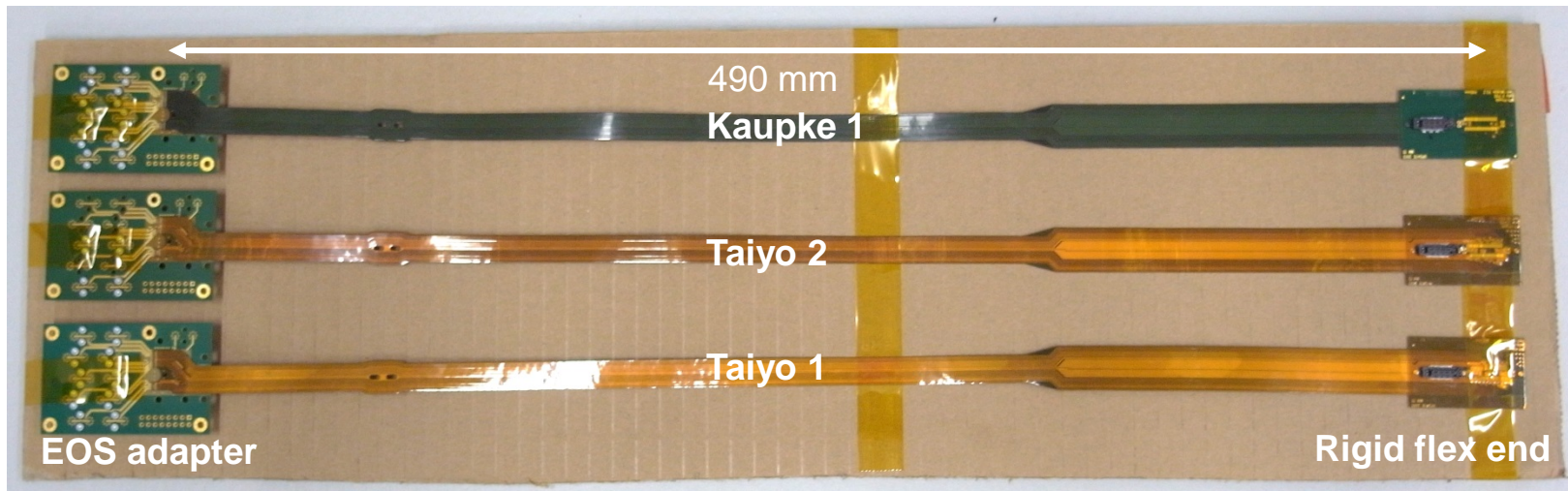


Flex cable prototypes with EOS adapter boards

# Flex Cable – Module Side

- Adapter PCB to connect micro coax cables to the flex cable
- Two 25µm Al wire bonds per line, potted
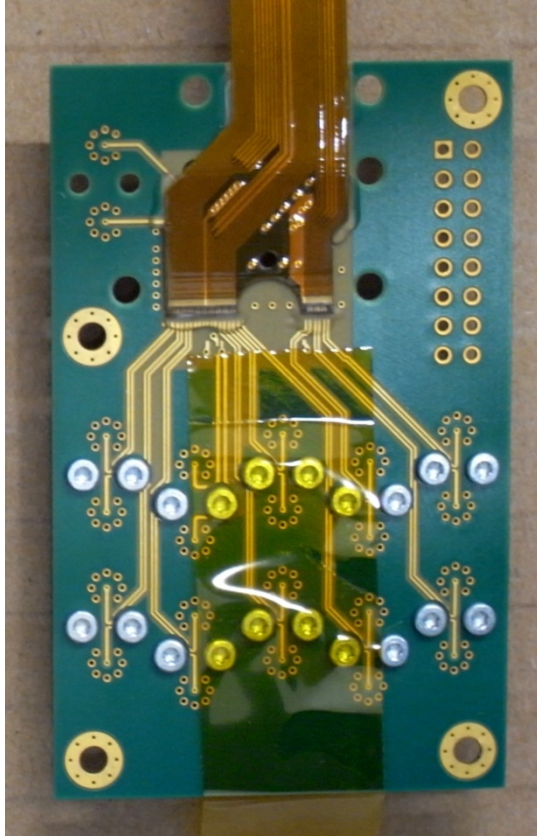


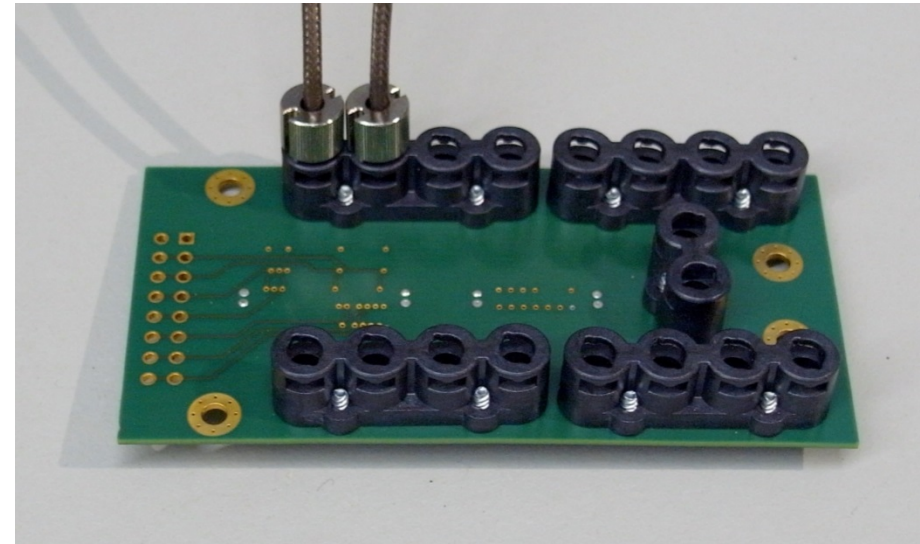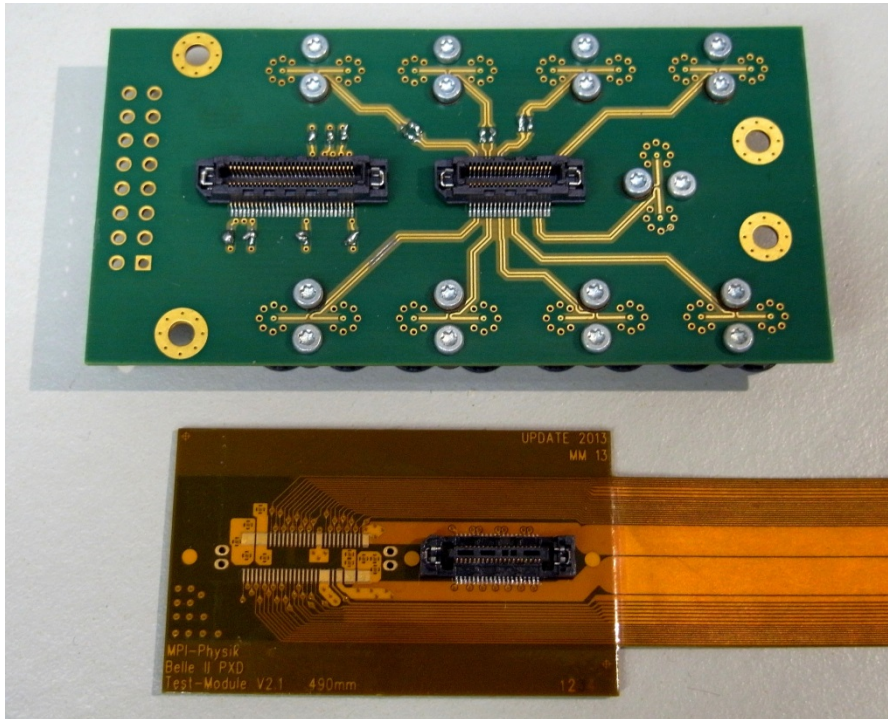Flex adapter PCB, soldered and wire bonded to flex cable
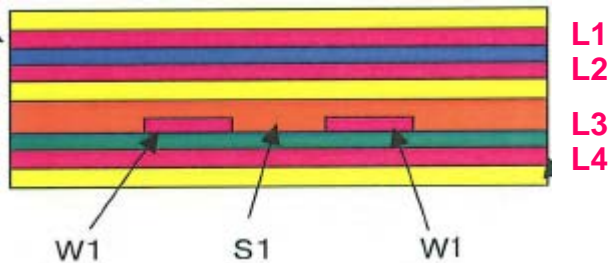


Wire bond detail

# Flex Cable – Patch Panel Side

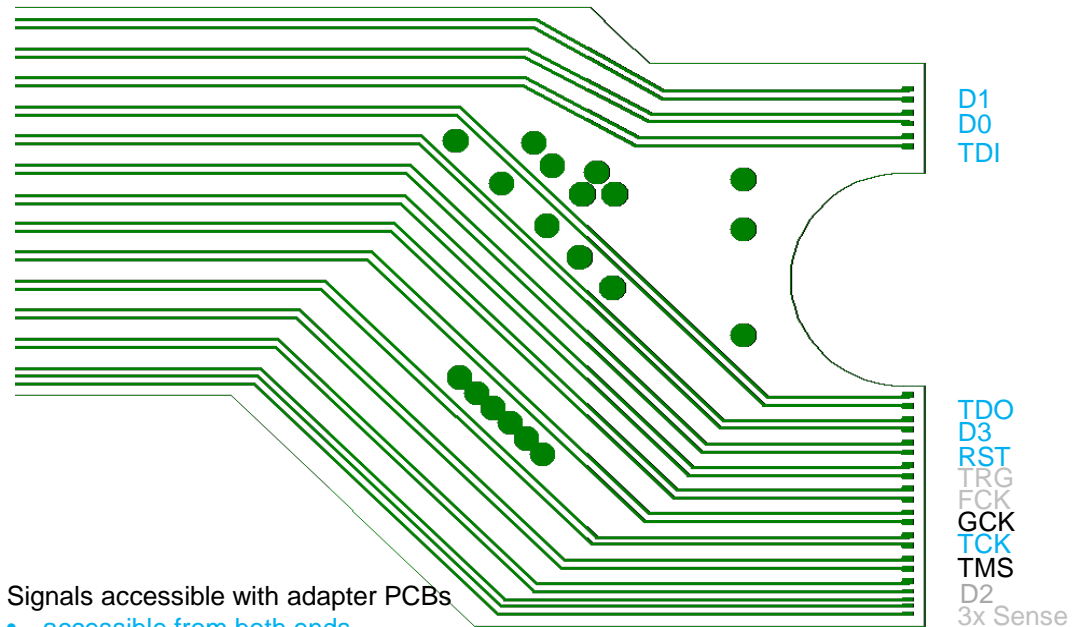- Adapter PCB to connect micro coax cables to the rigid patch panel

# Design Details

- Impedance controlled differential pairs (most critical for Gbit link data lines D[3:0])
- Design goals
  - $100\Omega$ diff. impedance ($\pm\ 10\Omega$)
  - low DC resistance ($< 8\Omega$)
  - good x-talk immunity



Layer stack (cross section), width (W)
and spacing (S) of diff. lines on layer 3



Signals accessible with adapter PCBs
- accessible from both ends
- accessible from module side only
- not accessible

Flex cable layout at module side, layer 3 shown only

# Measurement Methodology

- Digital Sampling Oscilloscope (DSA)
  - Very high input bandwidth (up to 30GHz)
  - Precision sample & hold at inputs
  - High resolution delay sweep of S&H trigger (sub ps)
  - Low speed, high resolution ADC (14 bit, 200ksps)

➔ Very accurate amplitude and timing resolution (works for periodic signals only)



DSA with two dual channel TDR / Sampling modules connected to DUT with differential lines
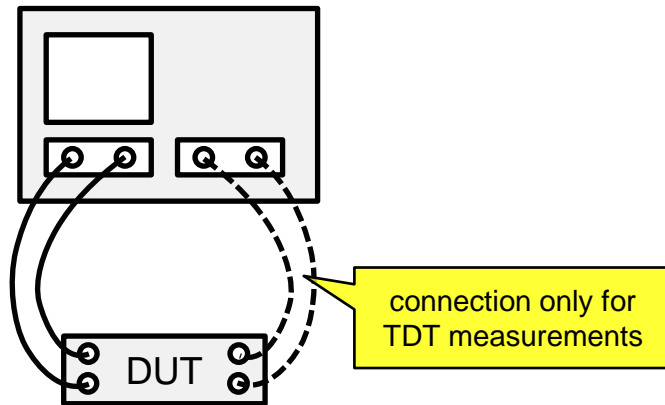
DSA with two dual channel TDR / Sampling
modules connected to DUT with differential lines
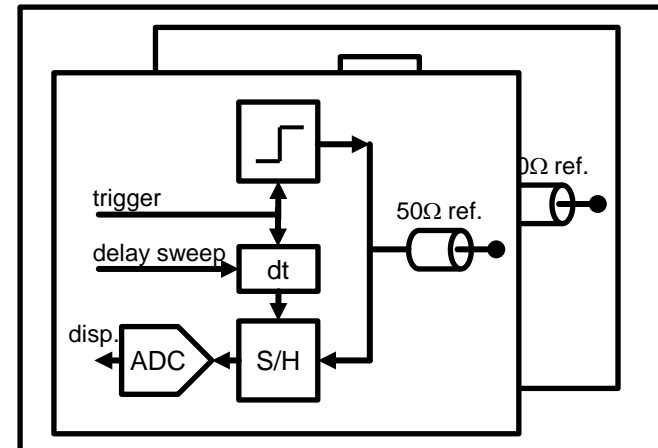
Dual channel TDR / Sampling module
(step voltage generator and sampling
stage can be activated independently)

# Time Domain Reflectometry (TDR)

- **Same TDR module** generates a voltage step and samples the reflected waveform
- Amplitude of reflected wave is proportional to the **impedance** along the DUT: $V_r(t) \propto Z(x)$
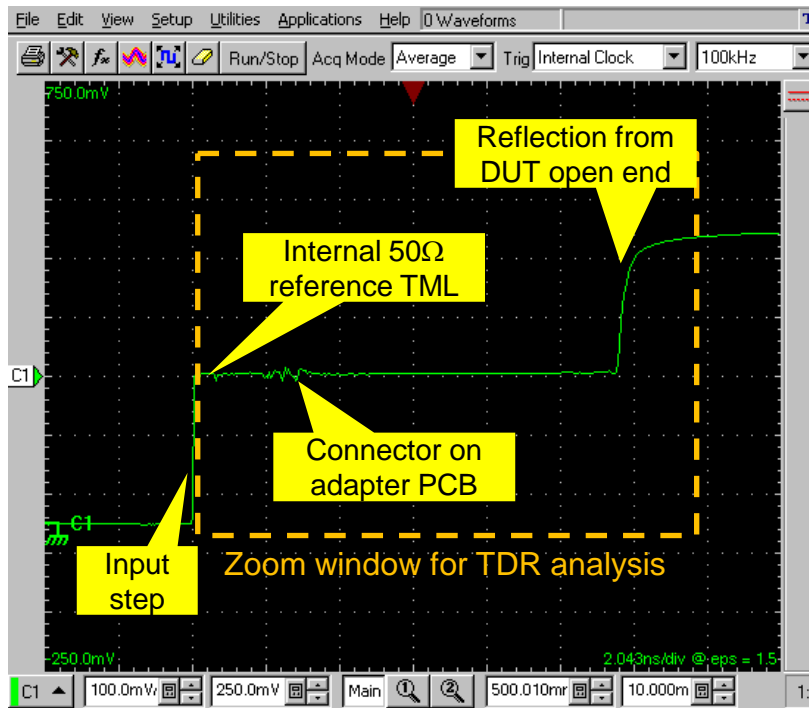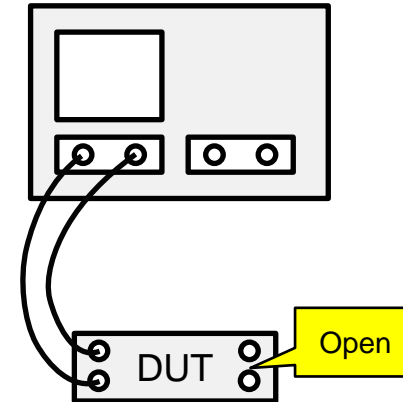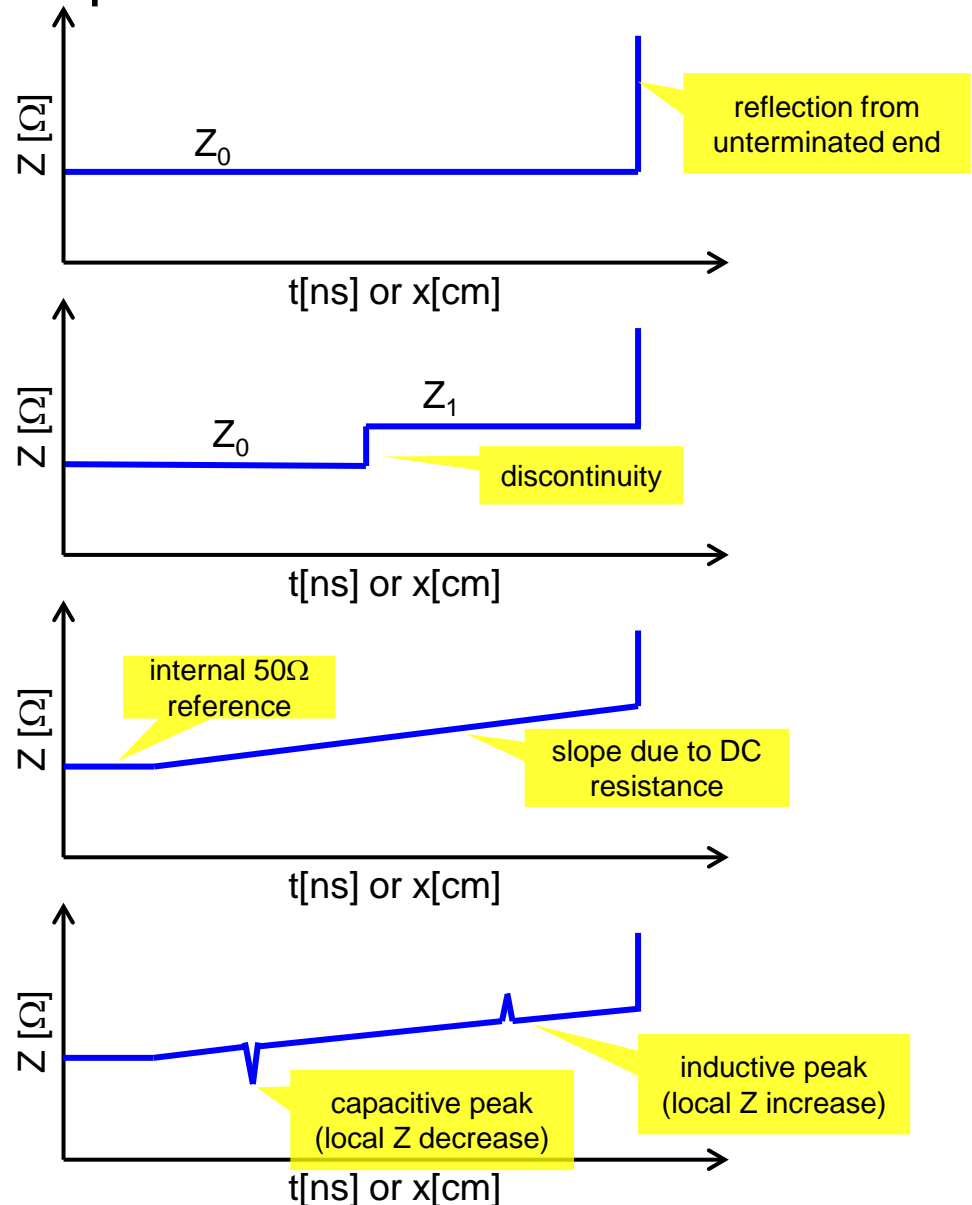


Measured TDR waveform
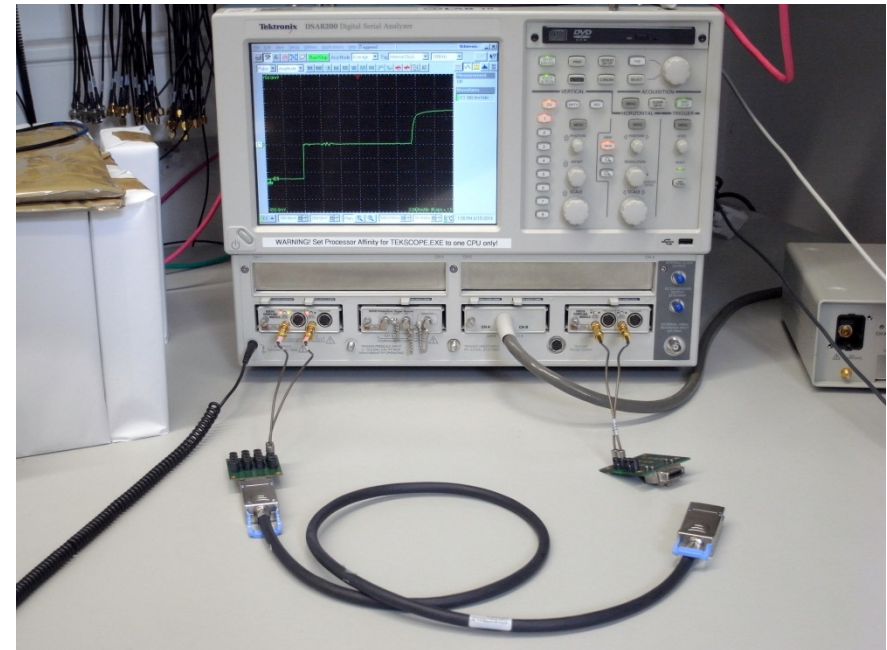


TDR setup with 1m Infiniband cable as DUT

# How to interpret TDR Data

- Ideal transmission line



- TML with change in impedance



- TML with finite DC resistance



- TML with distortions
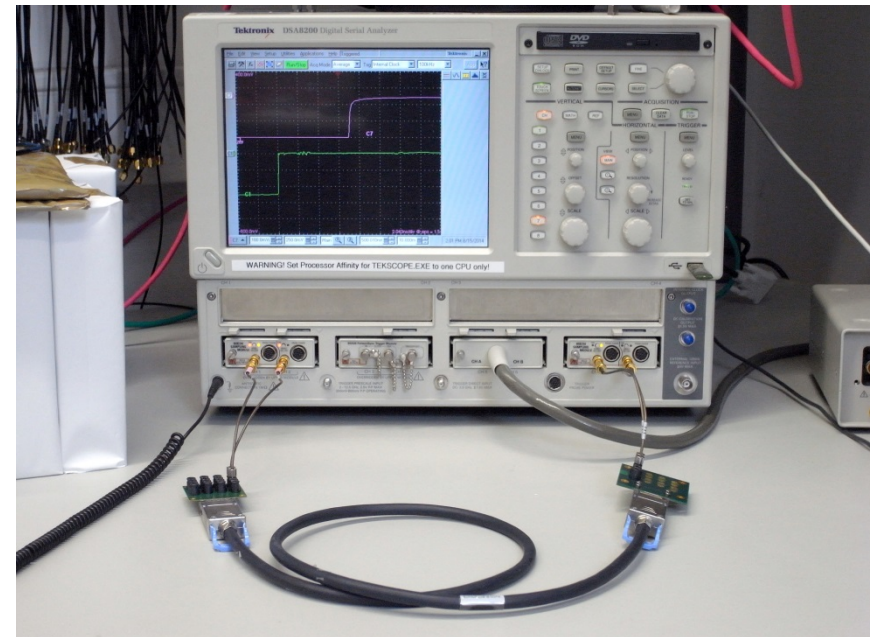
$$Z_0(x) = \sqrt{\frac{L'(x)}{C'(x)}}$$

# Time Domain Transmission (TDT)

- **One TDR module** generates the voltage step and the **second one samples** the transmitted waveform

- Analysis of input and output step functions yield the **transfer function *H(s)*** of the DUT
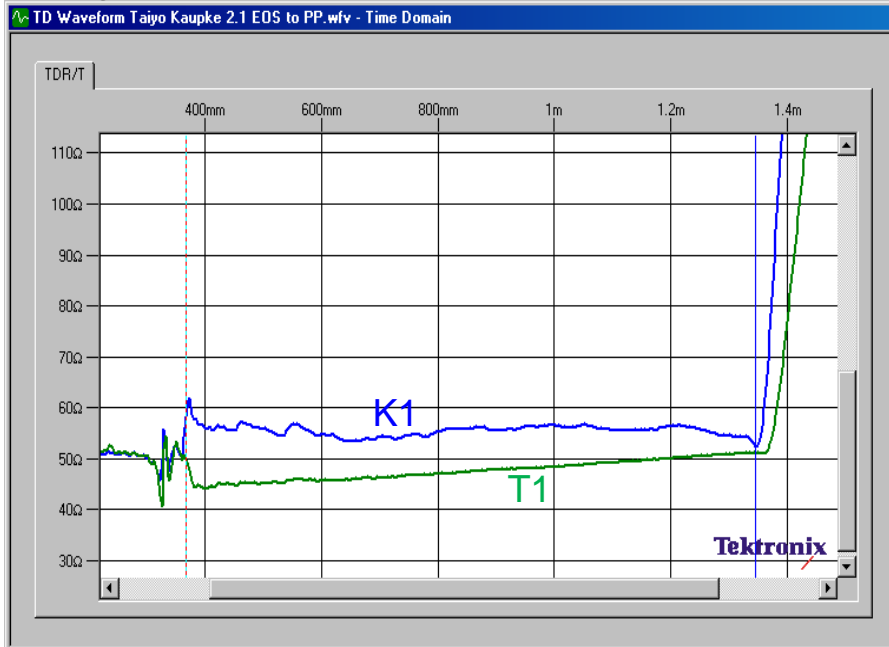


connection for TDT measurement

DUT



Measured TDT waveform
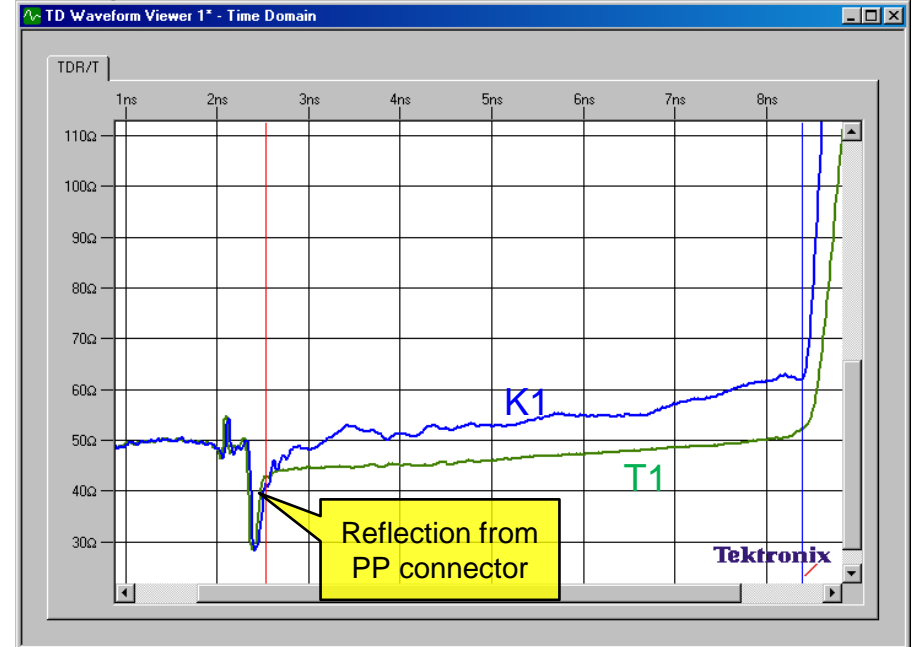
Transmitted step

Input step
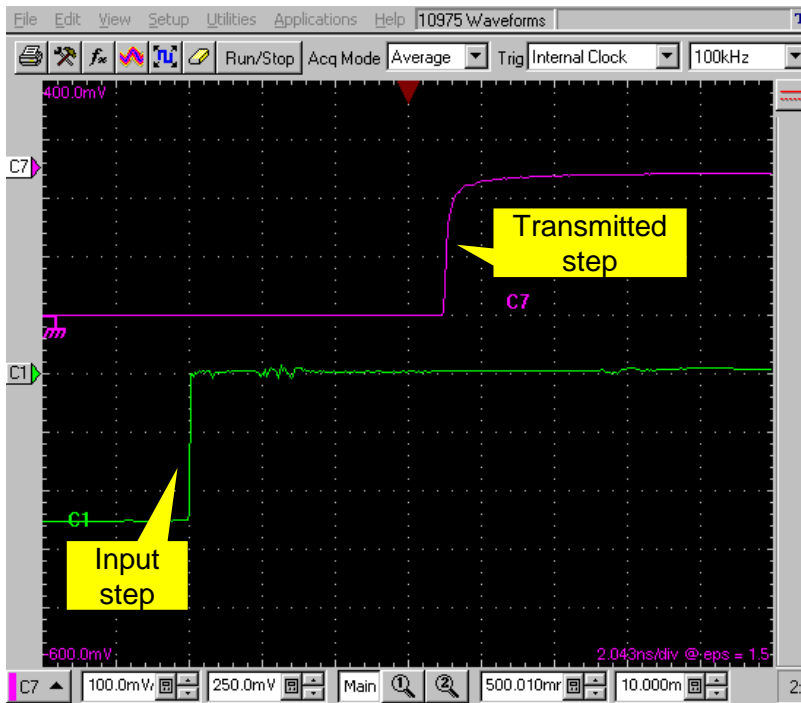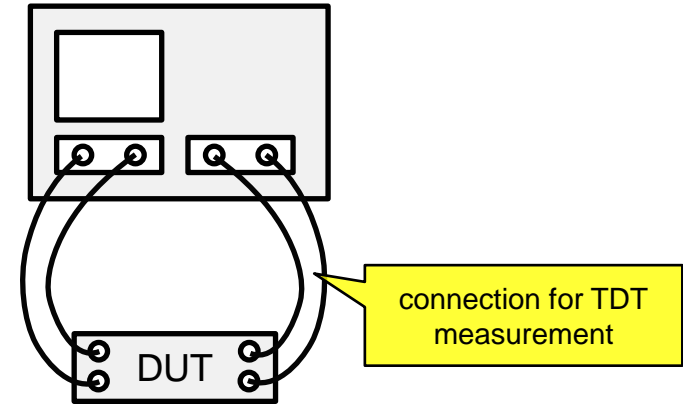


TDT setup with 1m Infiniband cable as DUT

# Impedance Measurements (TDR)
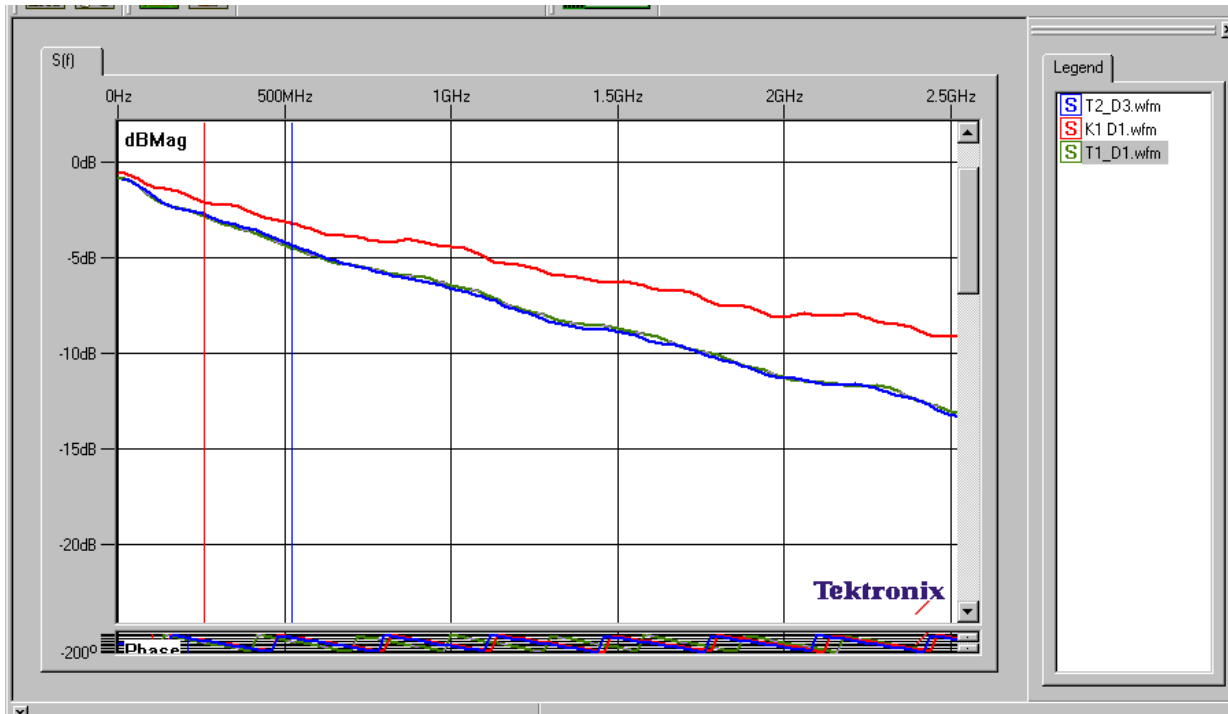
Signal from module side, patch panel side open

Signal from patch panel side, module side open



| DUT | Diff. line impedance | Dielectric constant | Comment |
|-----|---------------------|--------------------|---------|
| T1 (Taiyo) | 89$\Omega$ | 3.1 | Impedance constant along the cable |
| K1 (Kaupke) | 90 - 116$\Omega$ | 2.8 | Impedance increases towards the module side of the cable |

# Attenuation Measurements (TDT)



| DUT | DC resistance (from DVM) | Attenuation @ 800 MHz | Attenuation @ 1.6GHz |
|---|---|---|---|
| T1 (Taiyo) | 7.64Ω | 5.75dB | 9.03dB |
| K1 (Kaupke) | 6.78Ω | 4.19dB | 6.55dB |

# Proposed Design Improvements

- Poor alignment of data and power connectors (SAMTEC ST4) on patch panel
- Mounting holes diameter on PCB (0.67mm) much larger than connectors alignment pins dimension (0.45mm x 0.15mm)

➔ Recommendation: Reduce hole size to 0.5mm
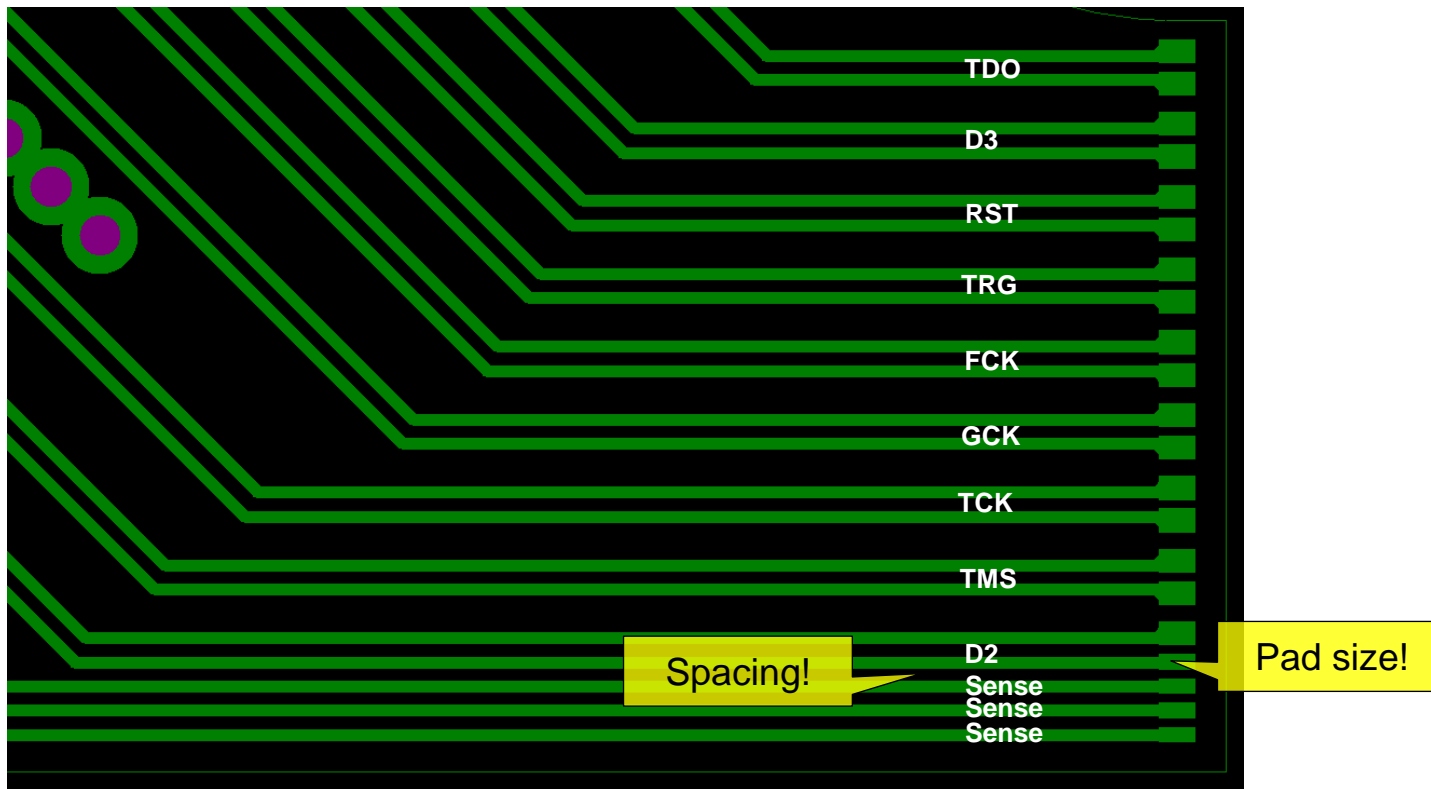


∅ 0.67 mm
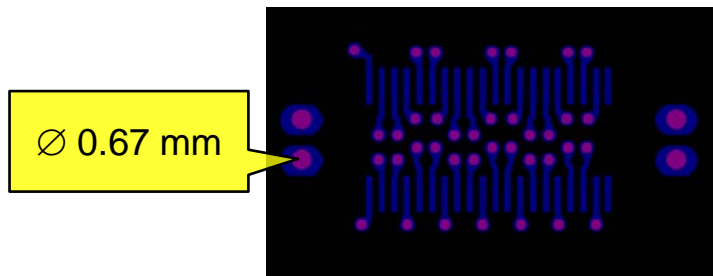
Footprint in current design
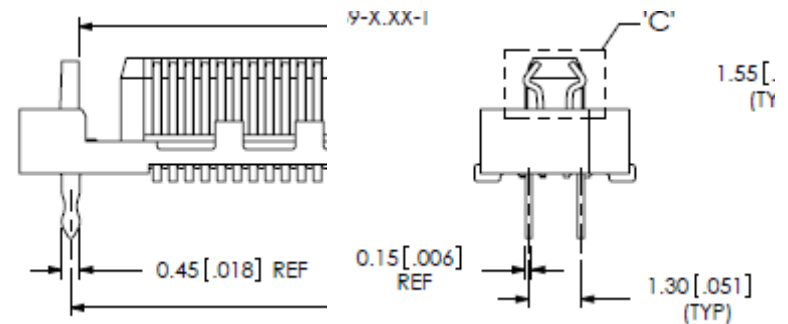


Samtec data sheet
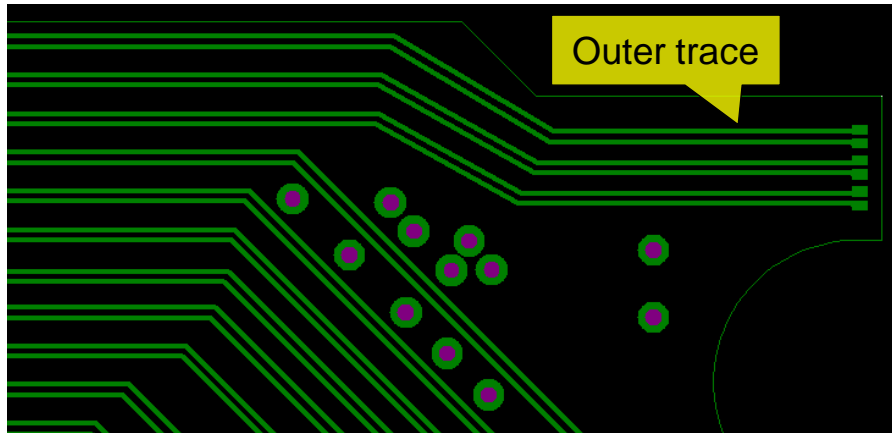
# Differential Lines Routing Details

- D2 differential lines with little spacing to adjacent sense lines

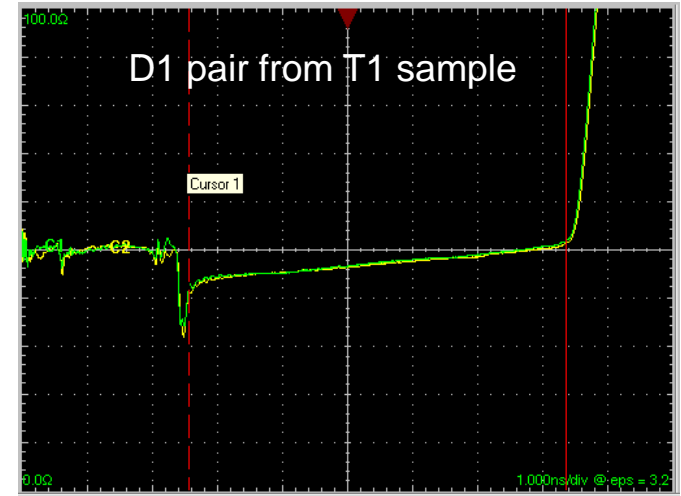→ Increase spacing between D2 and sense lines (remove RST and FCK lines)
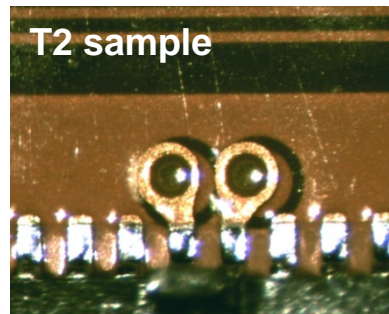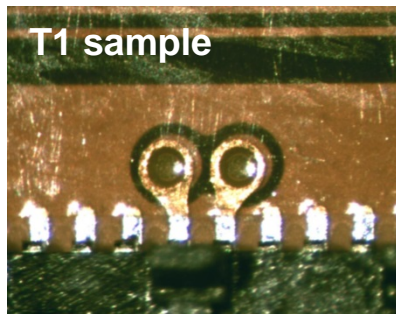
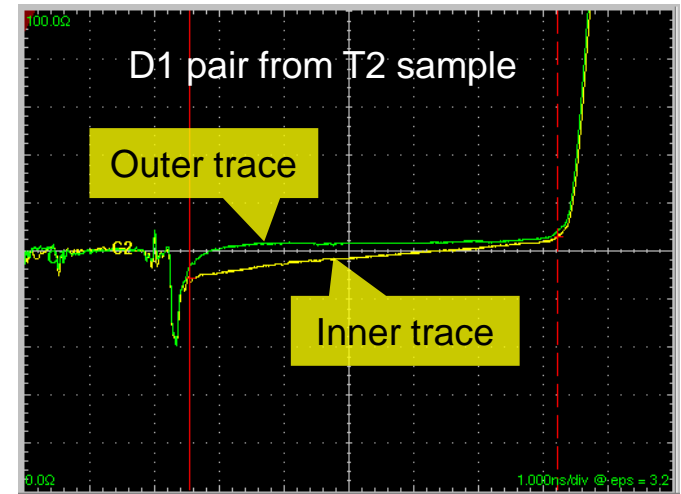# Differential Lines Routing Details

- Lines routed at the edge are critical



Outer trace

D1
D0
TDI



D1 pair from T1 sample

- Layer misalignment?



T1 sample

T2 sample

Zoom to PP data connector



D1 pair from T2 sample

Outer trace

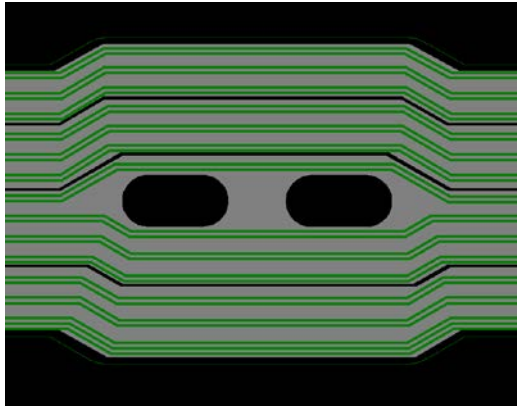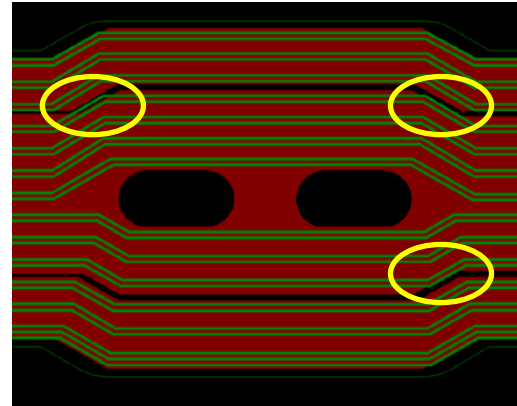Inner trace

# Differential Lines Routing Details

- Non optimal alignment between ground planes and signal lines



Reference plane (→ infinite width)

differential strip line

Reference plane (→ infinite width)

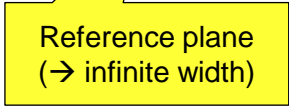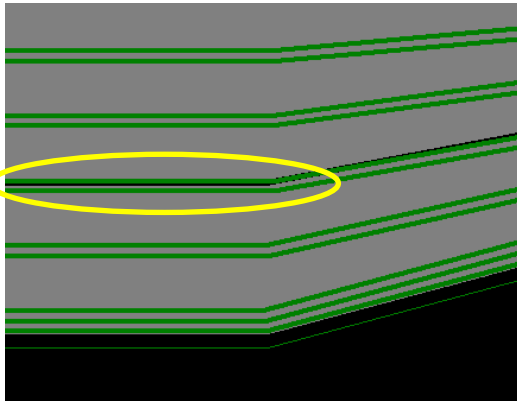Signal layer vs. layer 4 plane (ok)          Signal layer vs. layer 2 plane (bad)
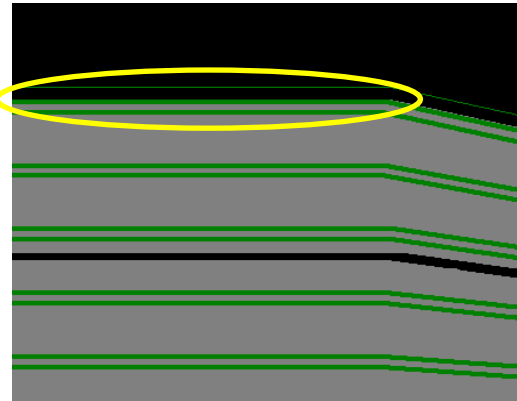
- Signal lines too close to the ref. plane edge or split between planes
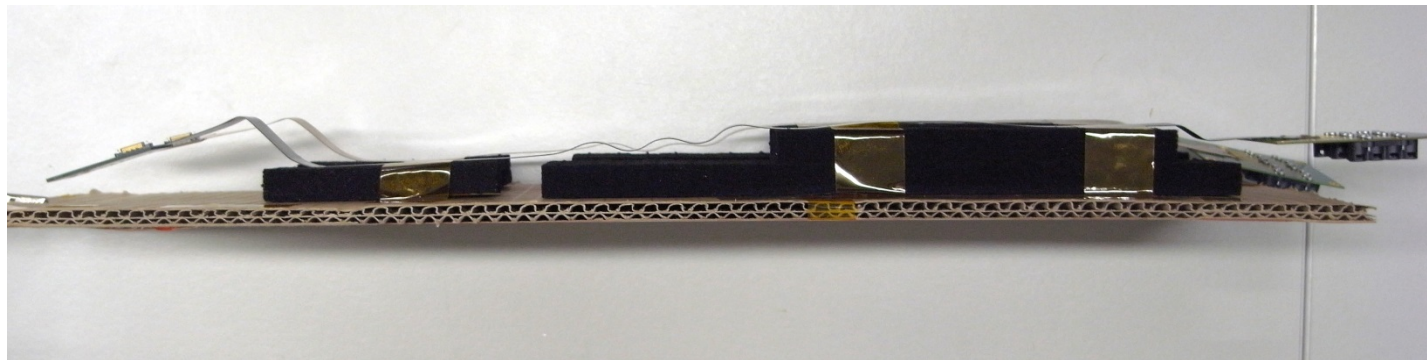


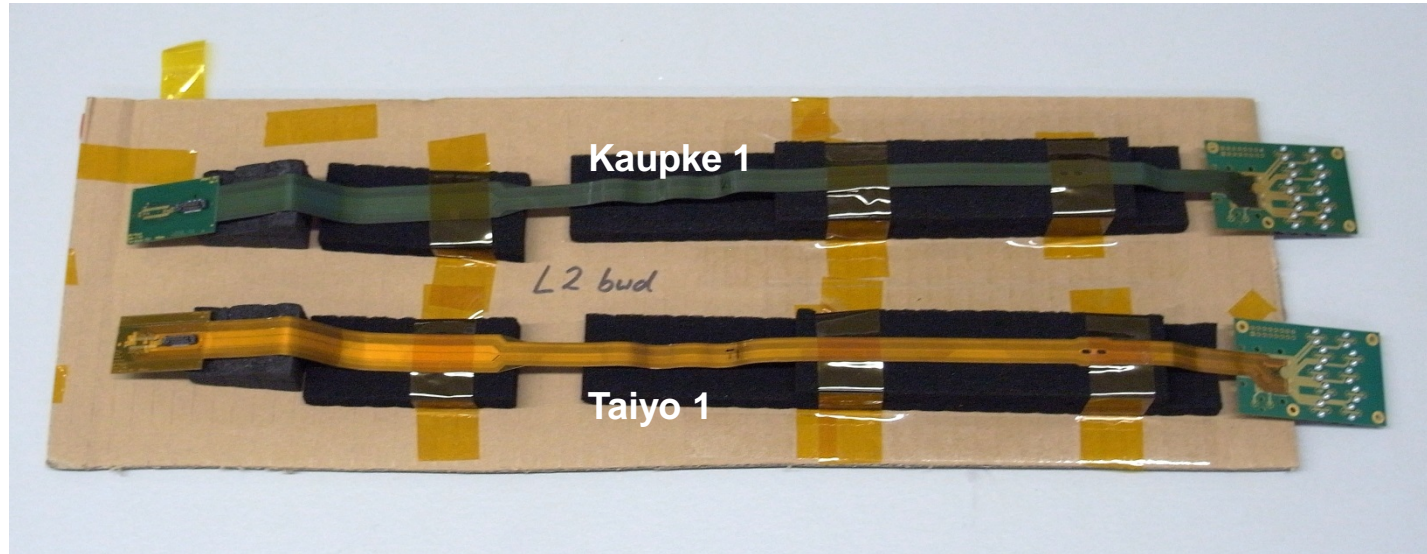Diff. pair split between planes (bad)          Diff. pair too close to edge (bad)

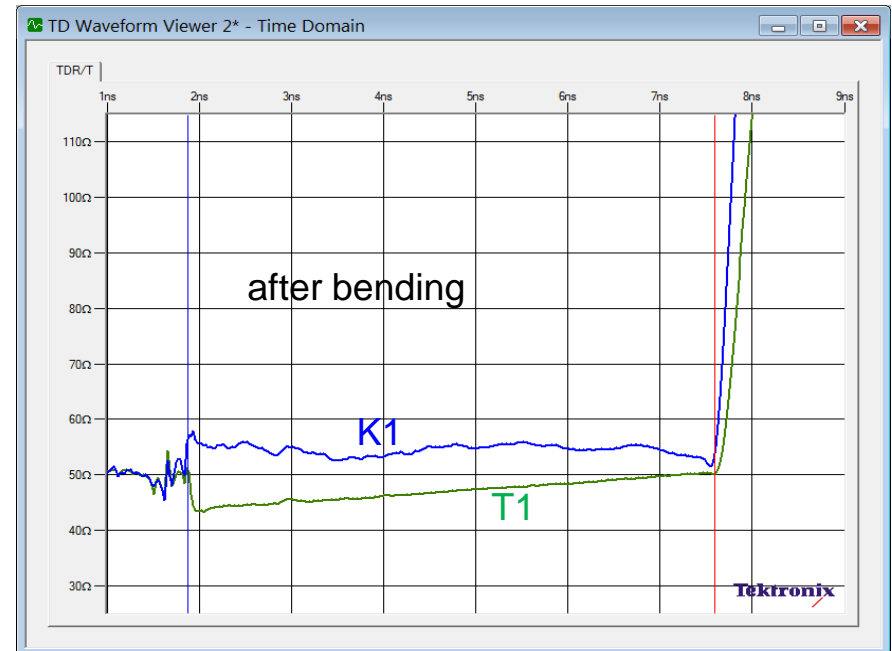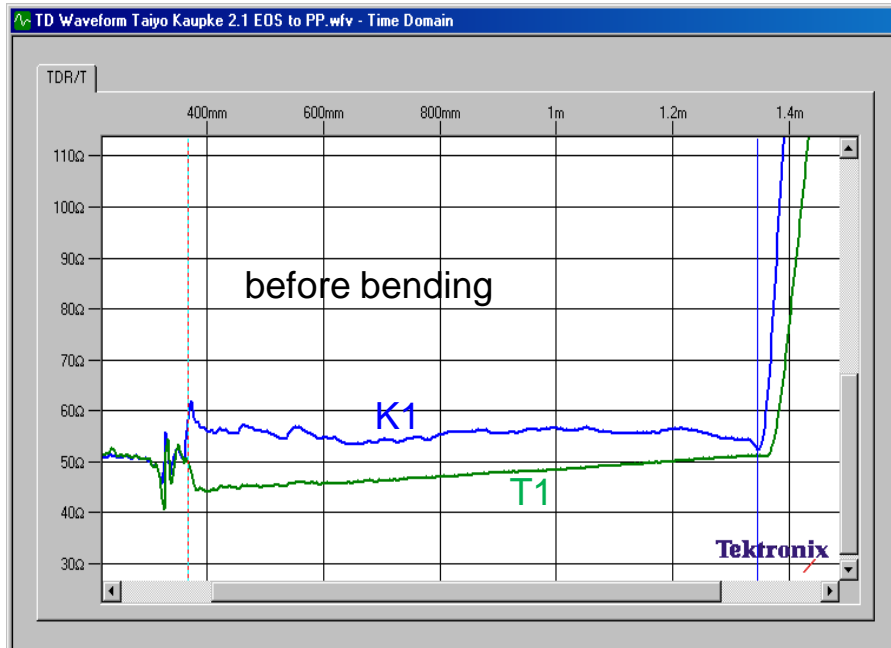Similar details on patch panel and module connector region

# Cable Bending



- The K1 flex is keeps the shape nicely, while T1 flex, being less rigid, tends to loose the pre-bends slightly

# TDR before and after Bending
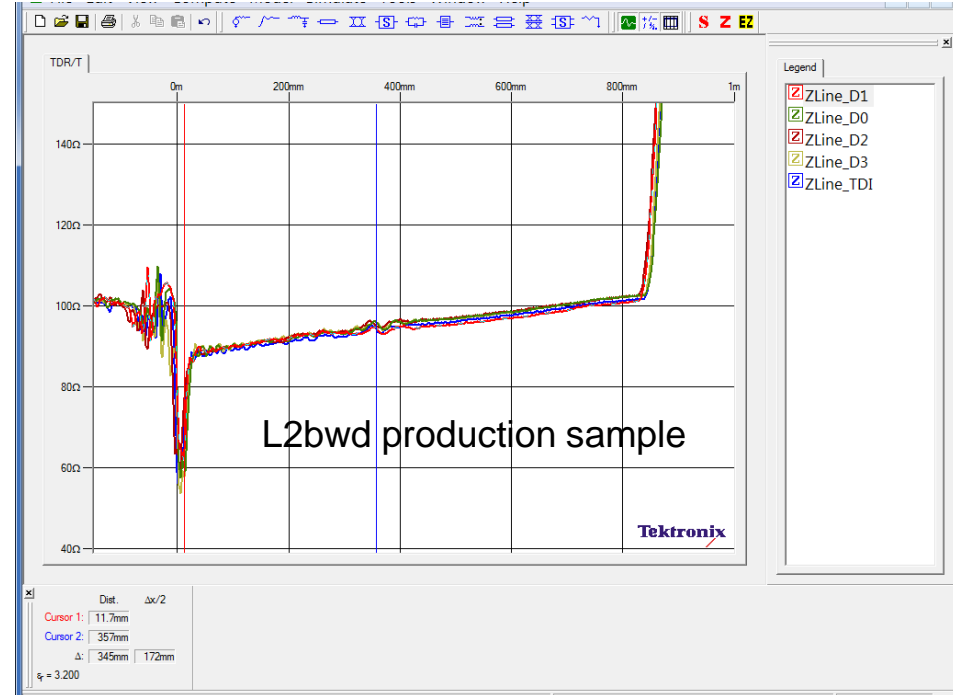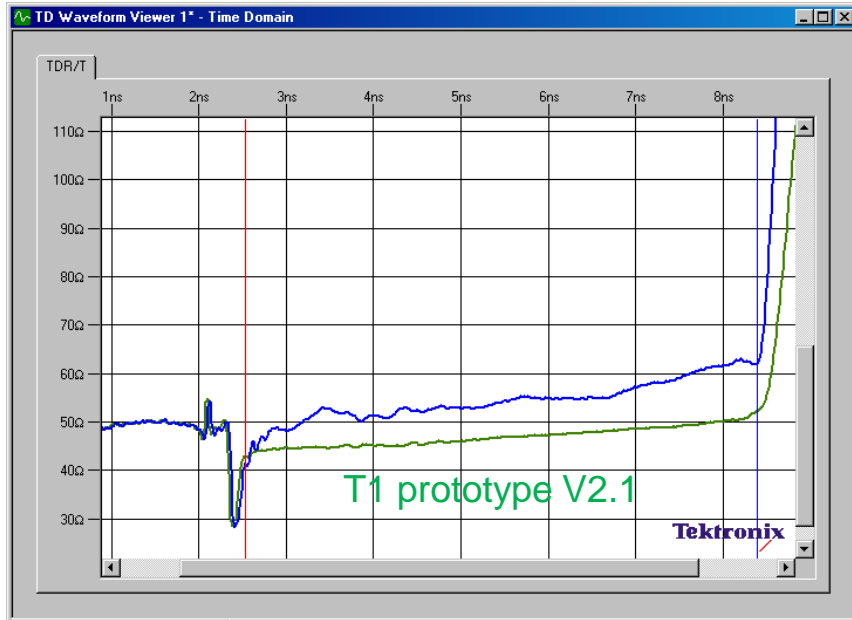
Signal from module side (D3), patch panel side open



- TML impedance is not influenced by cable bending

# First Production Sample "L2bwd"



T1 prototype V2.1



L2bwd production sample

- Production sample "L2bwd" (very similar to prototype "T1")
  - $Z_0 \sim 90 \; \Omega$
  - $R_{DC} \sim 9 \; \Omega$
- No Impedance distortion for lines running close to the cable outline (TDI)

# Summary

- Taiyo prototypes
  - T1 and T2 samples have very similar electrical properties
  - $Z_0 = 89\Omega$, $R_{DC} = 7.6\Omega$
  - $\varepsilon_r = 3.1$
  - Attenuation @ 800MHz = 5.8dB

- Kaupke prototype
  - $Z_0 = 90\text{-}116\Omega$ (changes along cable), $R_{DC} = 6.8\Omega$
  - $\varepsilon_r = 2.8$
  - Attenuation @ 800MHz = 4.2dB

➔ Kaupke seems to use a different layer stack (cable more rigid and slightly thicker)
  - Less attenuation
  - Higher impedance
  - Lower $\varepsilon_r$

# Summary II

- Full cable setup (flex + PP + short TWP + PP + long TWP) needs to be evaluated to assess the overall signal integrity

- High frequency damping (skin effect, dielectric losses)
    - can be partially compensated by pre-emphasis (DHP) and equalization on the receiver side (DHH/FPGA)

- Absolute TML impedance
    - Kapton cable layer stack and line geometry

- Impedance discontinuities (**Pre-emphasis does not compensate this!**)
    - Analyze TDR measurements and check critical PCB layout regions (edges, connectors, vias etc.)