Testing of Readout Electronics for Belle II Pixel Detector

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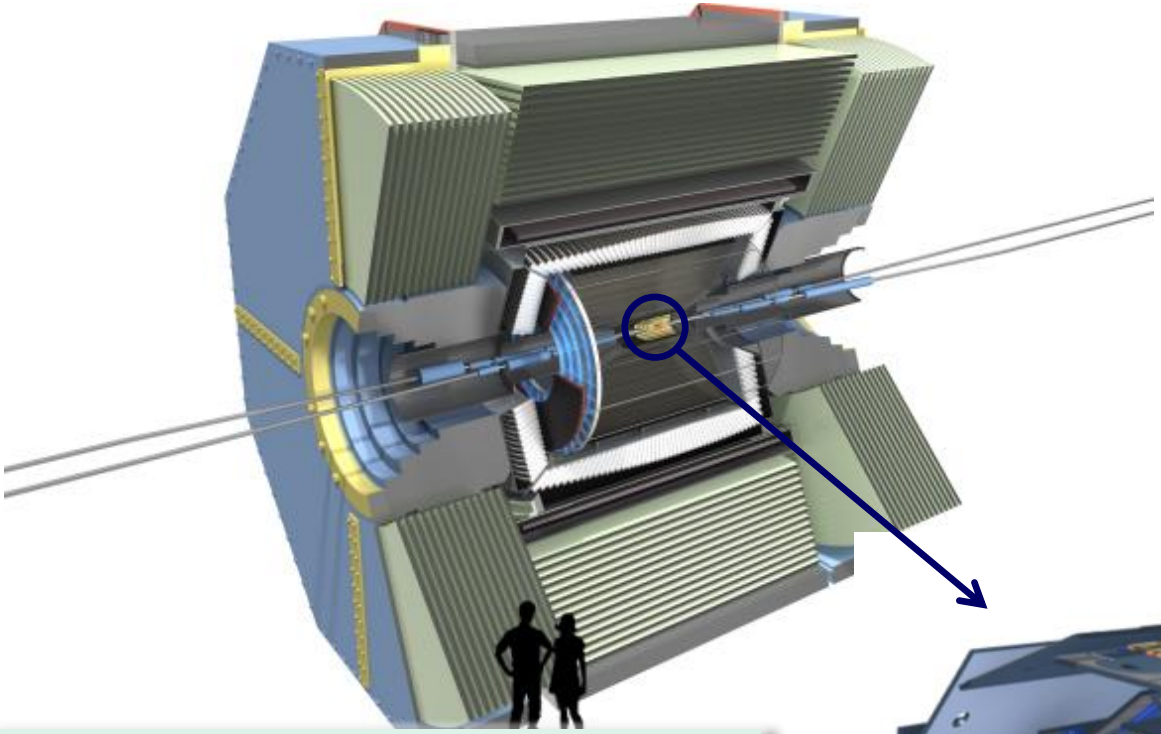
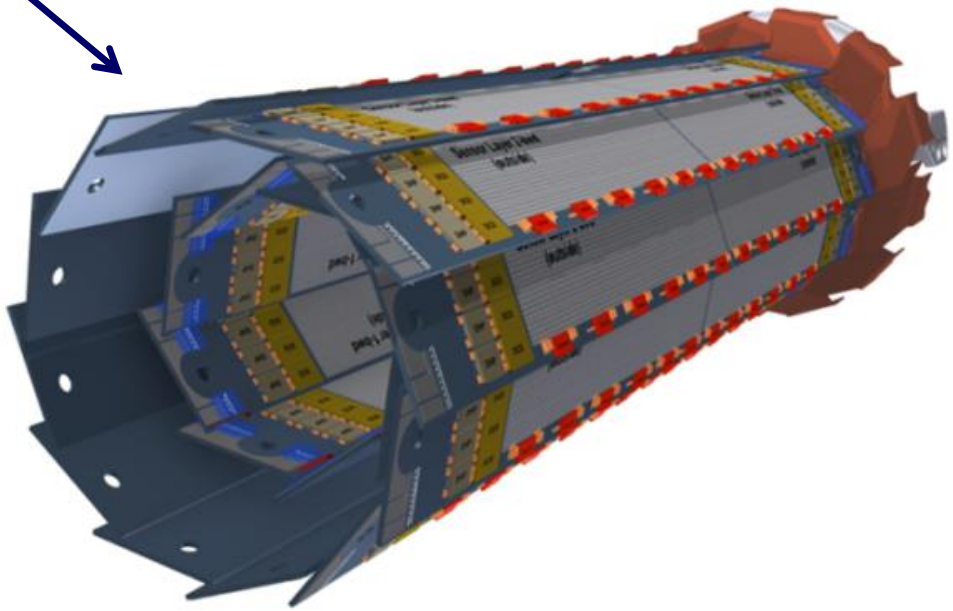
Pixel Detector – Belle II



- Occupancy of detector ~1%
- Spatial Resolution ~15µm



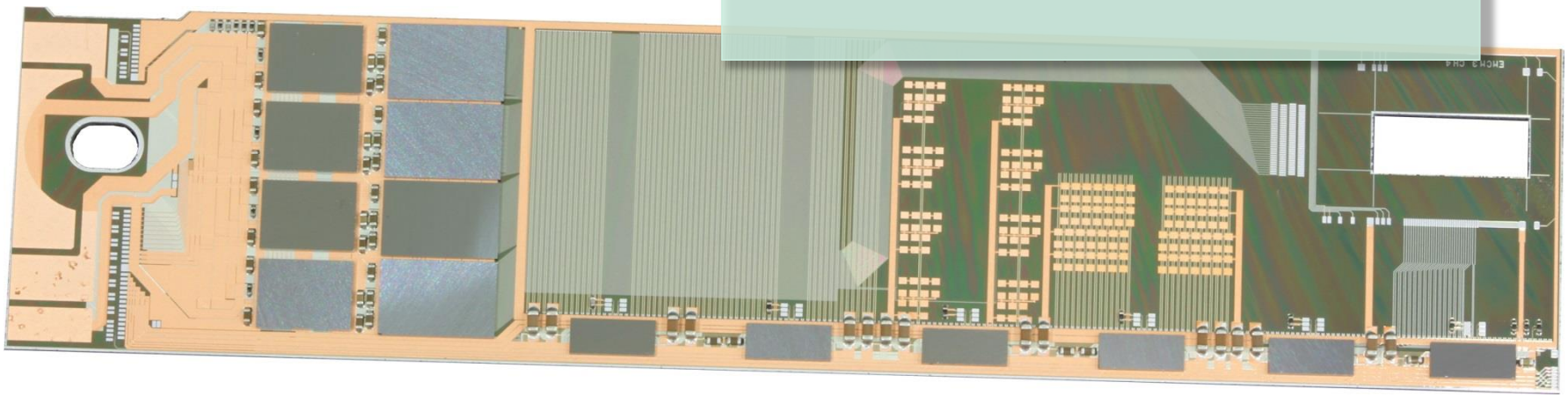
- Two Layers of DEPFET Pixels
- Distance from IP: 14mm, 22mm
- 40 half ladders
- Pixel size (50x55µm² and 50x85µm²)

Electrical Multi Chip Module – EMCM

Fully functional half ladder without DEPFET

Test

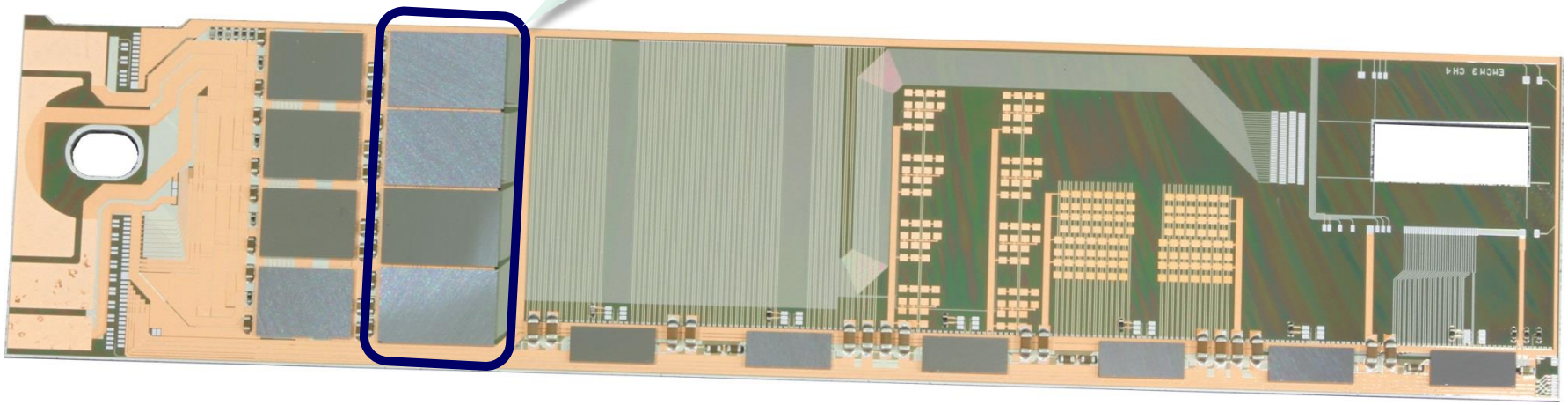
- Technological feasibility
- Probing of Signals & Voltages
- Electrical Performance



Electrical Multi Chip Module – EMCM

4 x DCD

Drain Current Digitizer



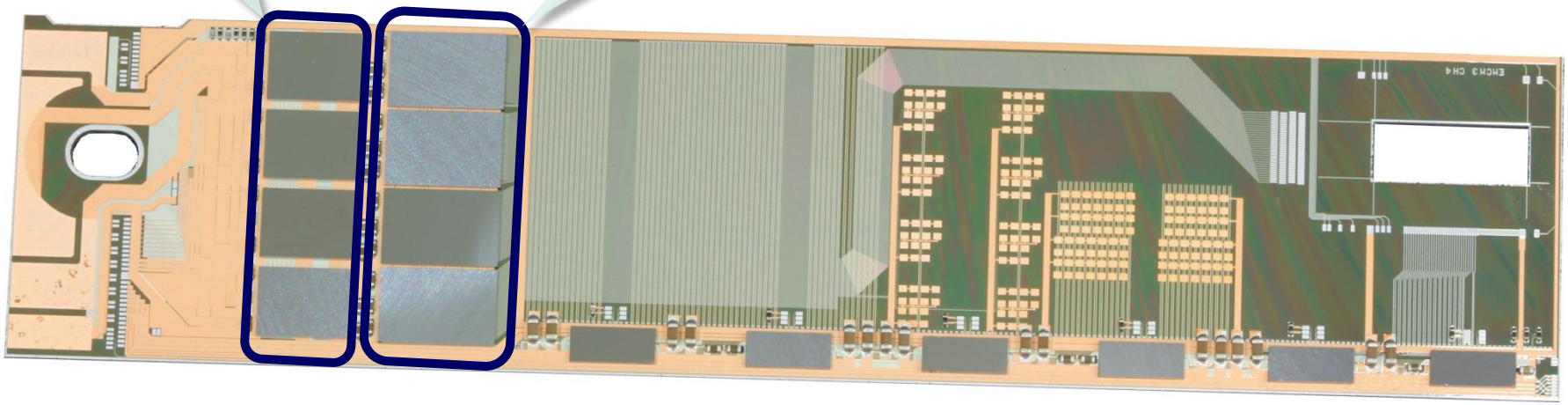
Electrical Multi Chip Module – EMCM

4 x DHP

Data Handling Processor

4 x DCD

Drain Current Digitizer



Electrical Multi Chip Module – EMCM

4 x DHP

Data Handling Processor

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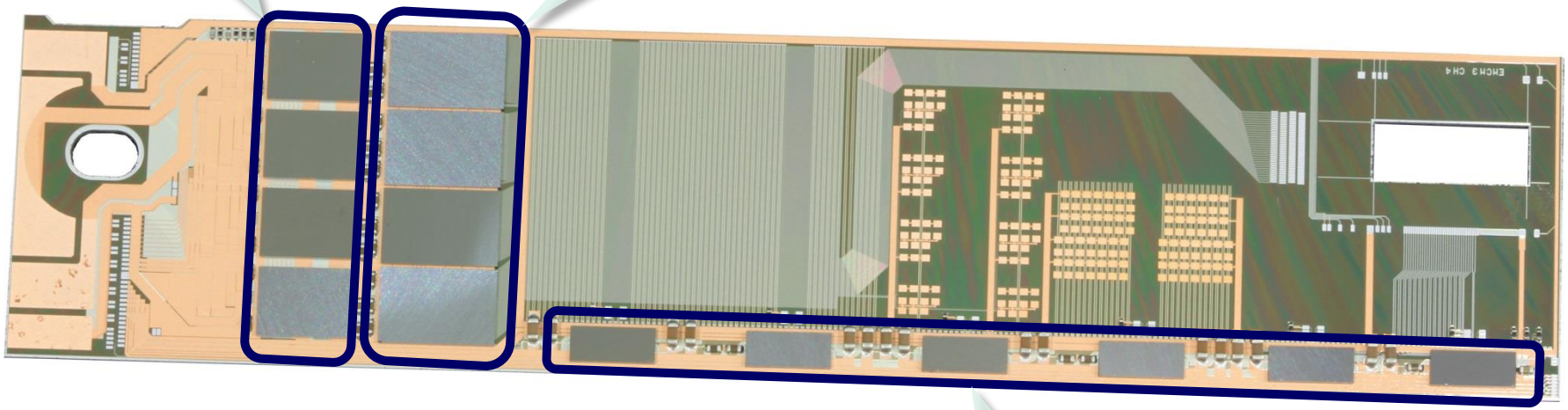


6 x Switcher

Electrical Multi Chip Module – EMCM

4 x DHP

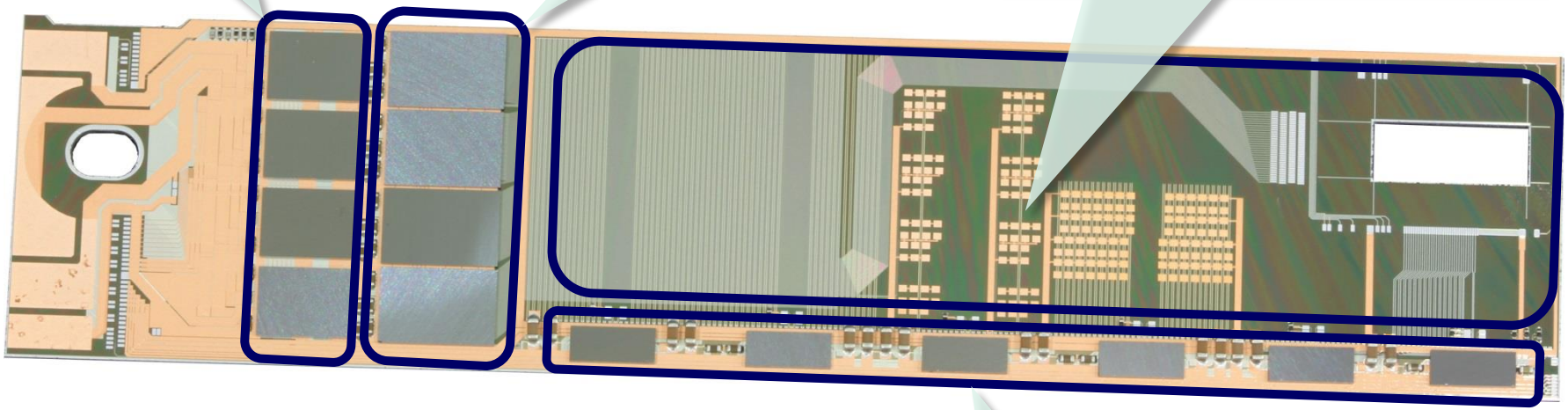
Data Handling Processor

4 x DCD

Drain Current Digitizer

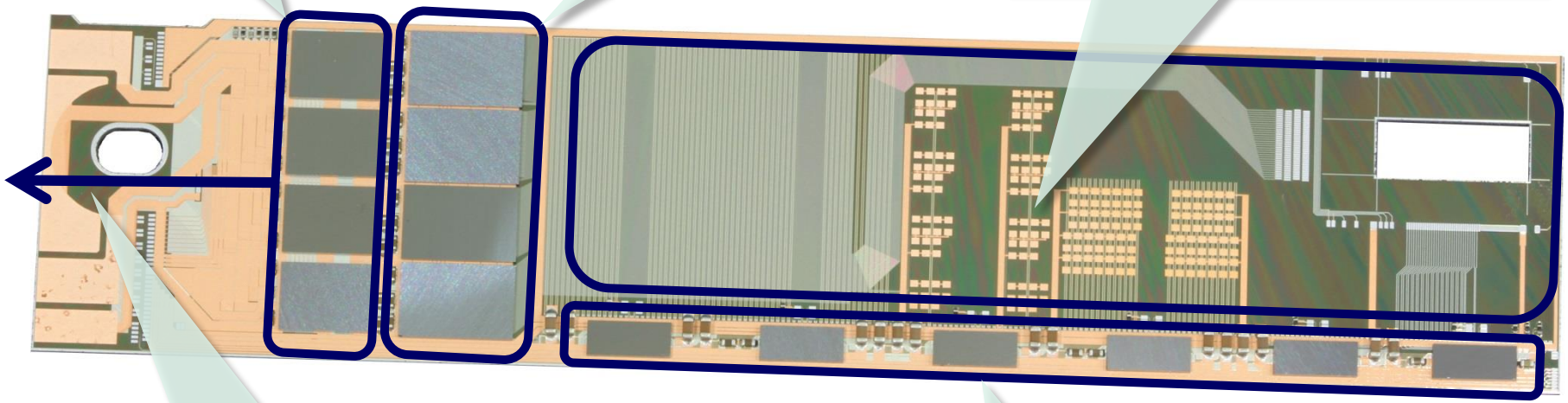
Space for Matrix

→ Test Structures

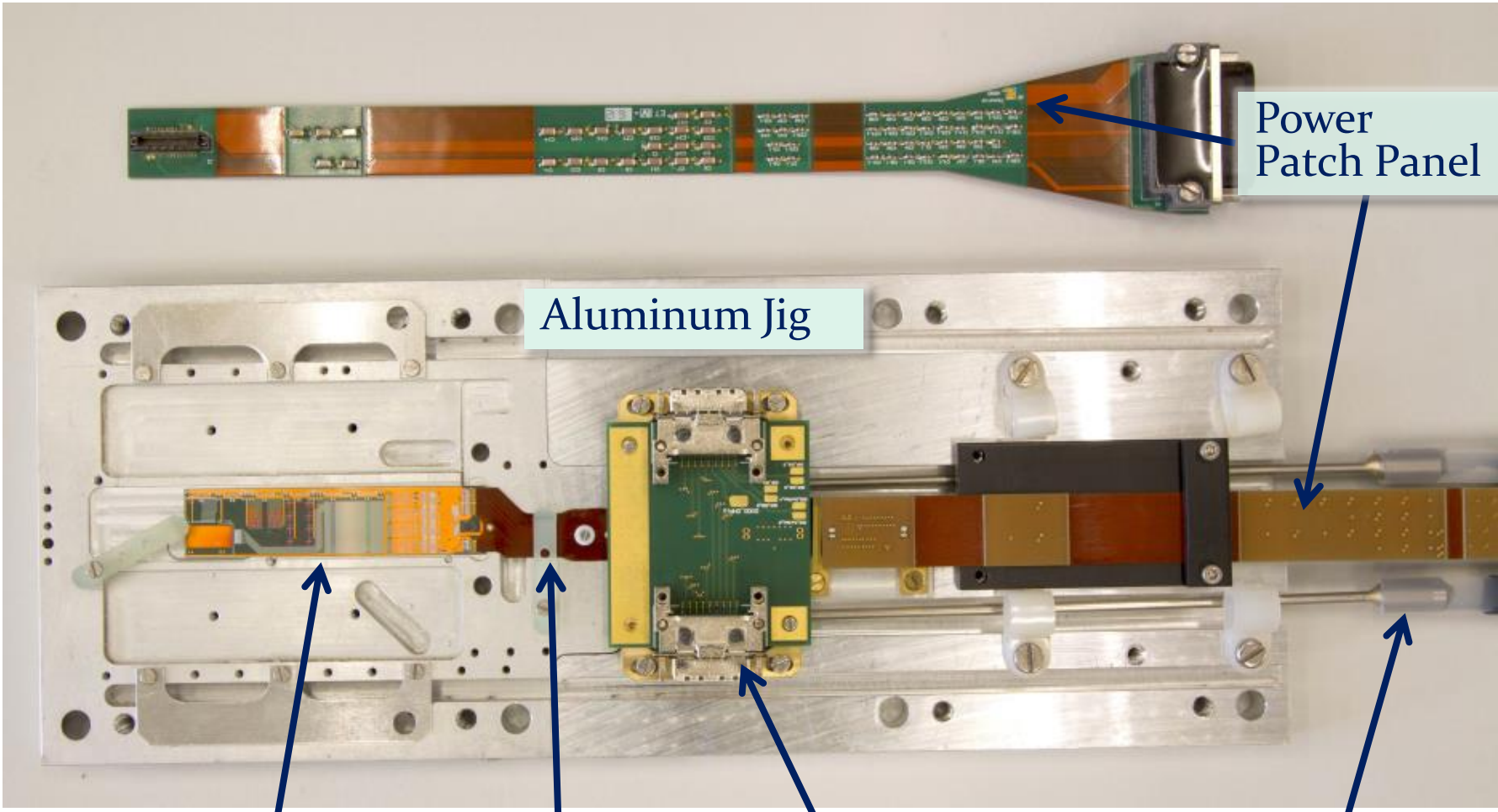


6 x Switcher

Electrical Multi Chip Module – EMCM



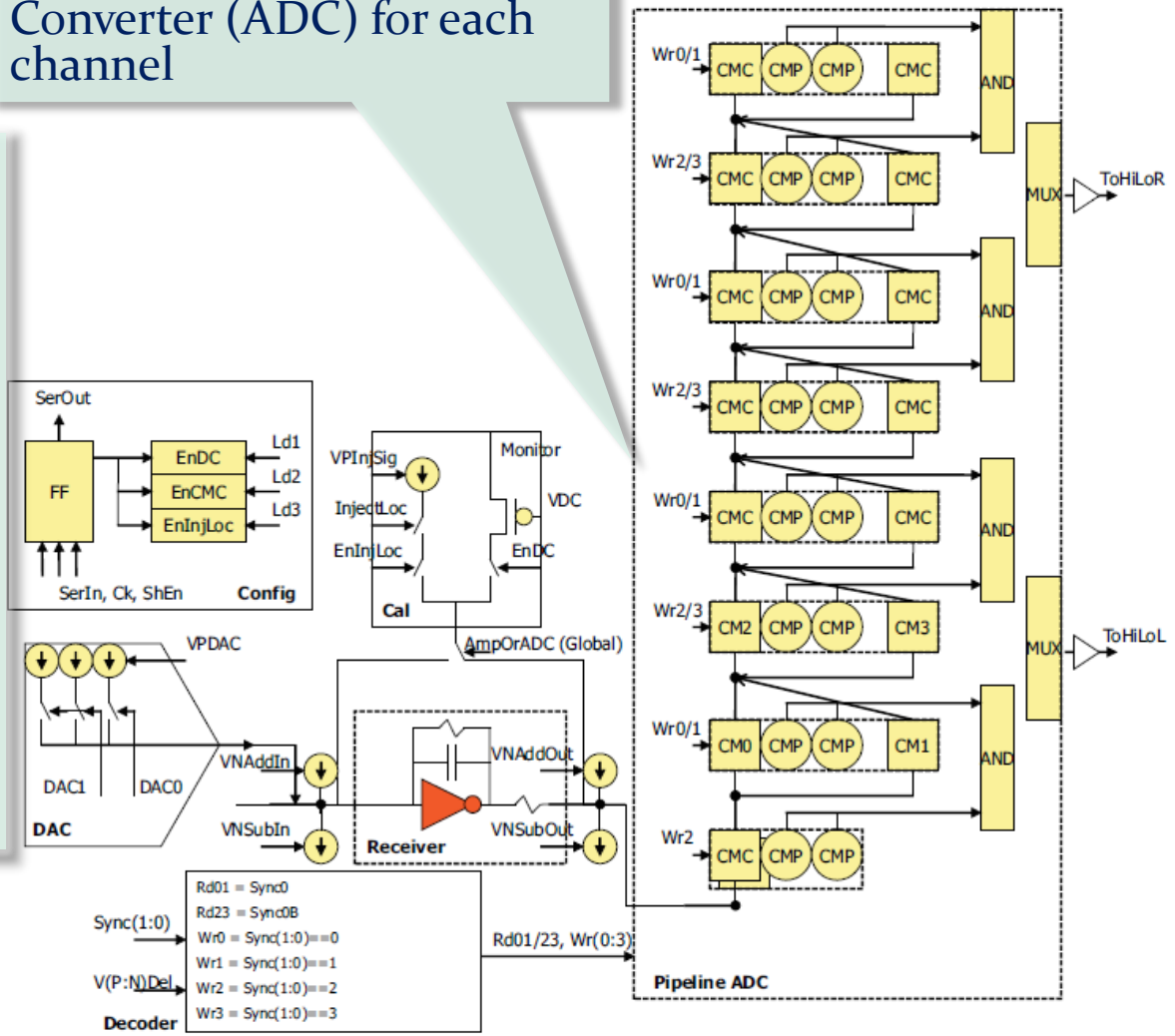
EMCM Periphery



Drain Current Digitizer – DCD

- Receives and digitizes DEPFET currents
- 256 analogue input channels
- 8 digital output buses (32 channels multiplexed to 1 bus)
- Bump bonded (soldered)
- 3240µm x 4969µm

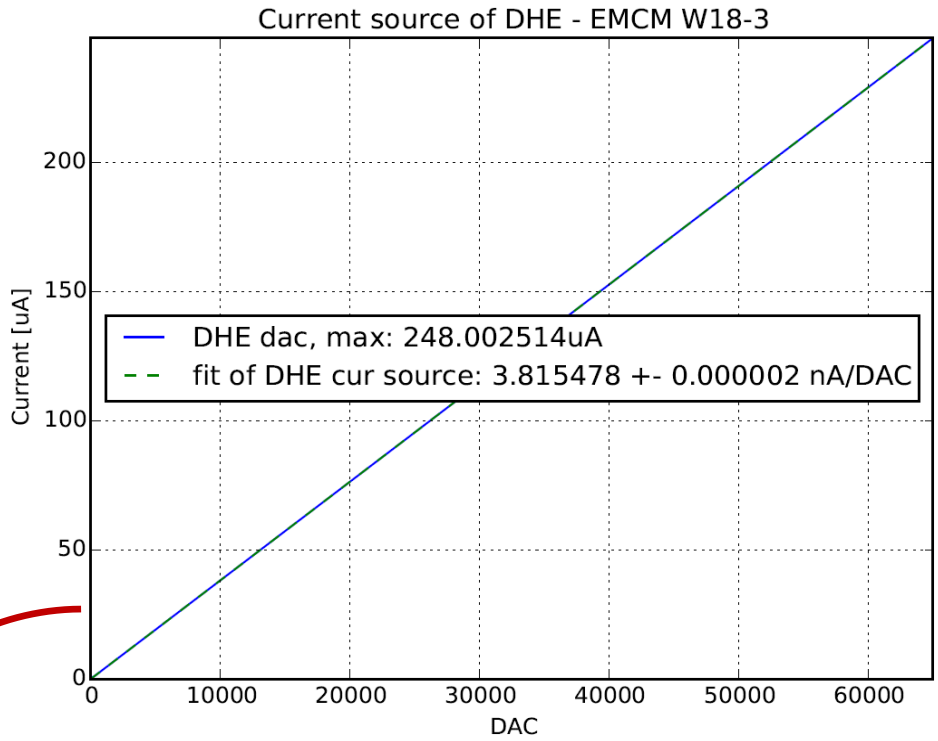
Two cyclic Analog Digital Converter (ADC) for each channel

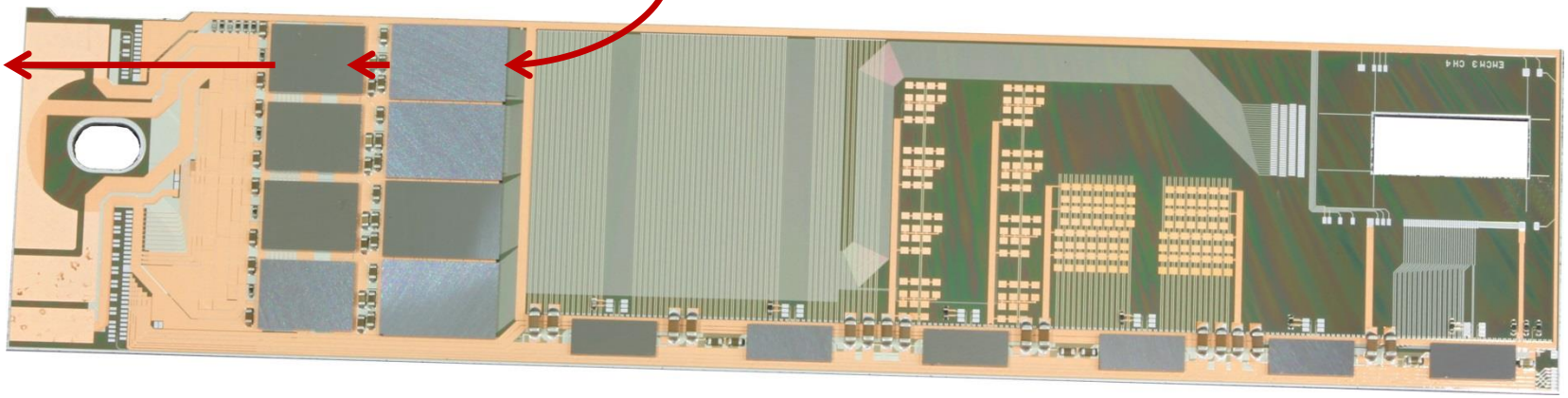


Calibration of ADCs

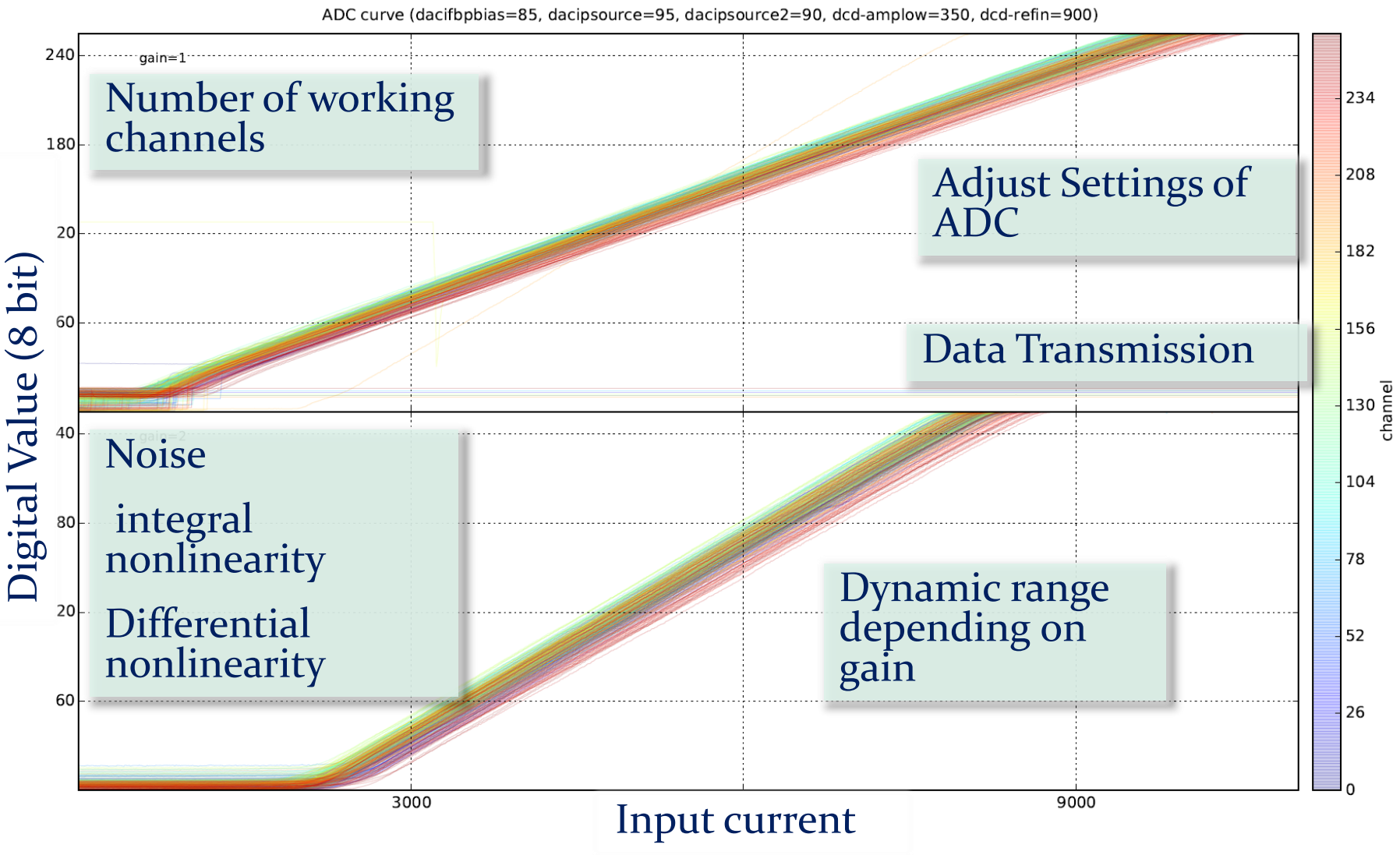
External Current Source

- linear
- low noise
- fast
- 248µA in 65000 steps



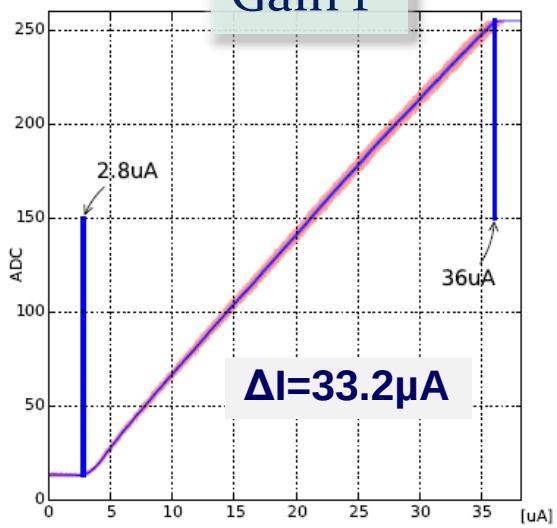


ADC Transfer Curves

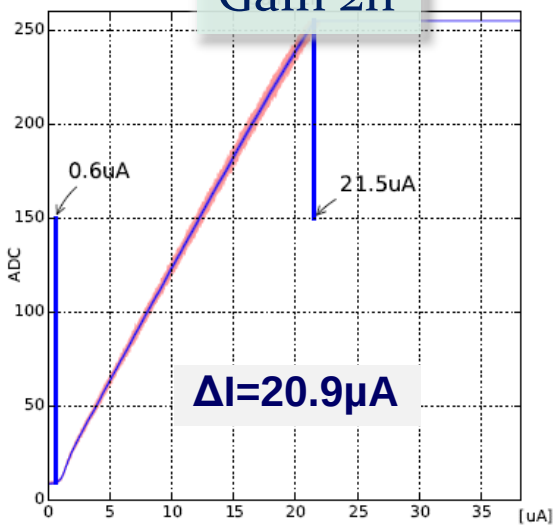


Dynamic Range for Gain Settings

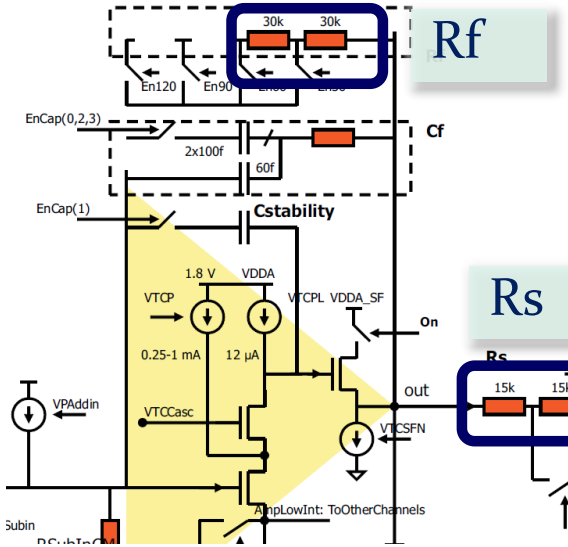
Gain 1



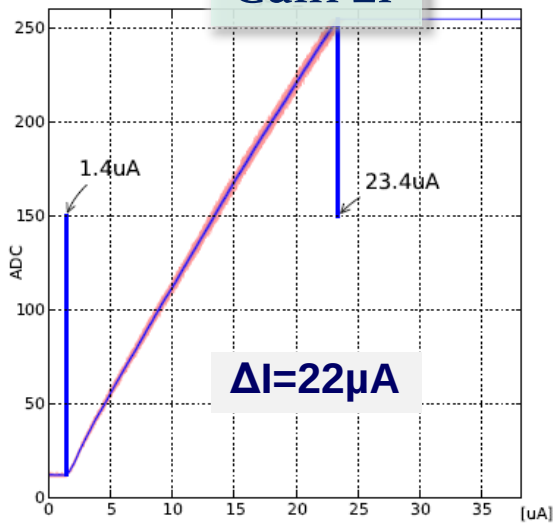
Gain 2h



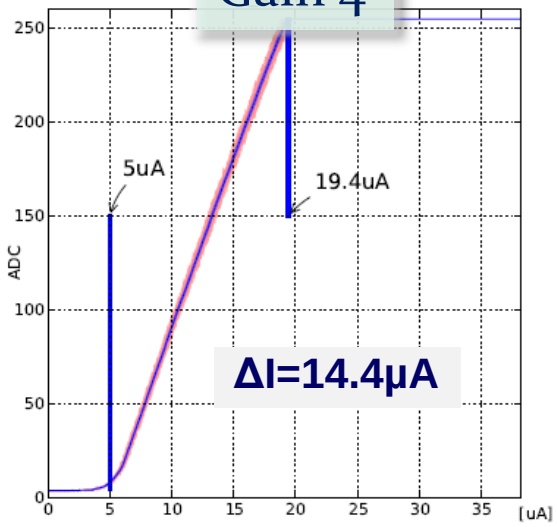
Rf



Gain 2l



Gain 4



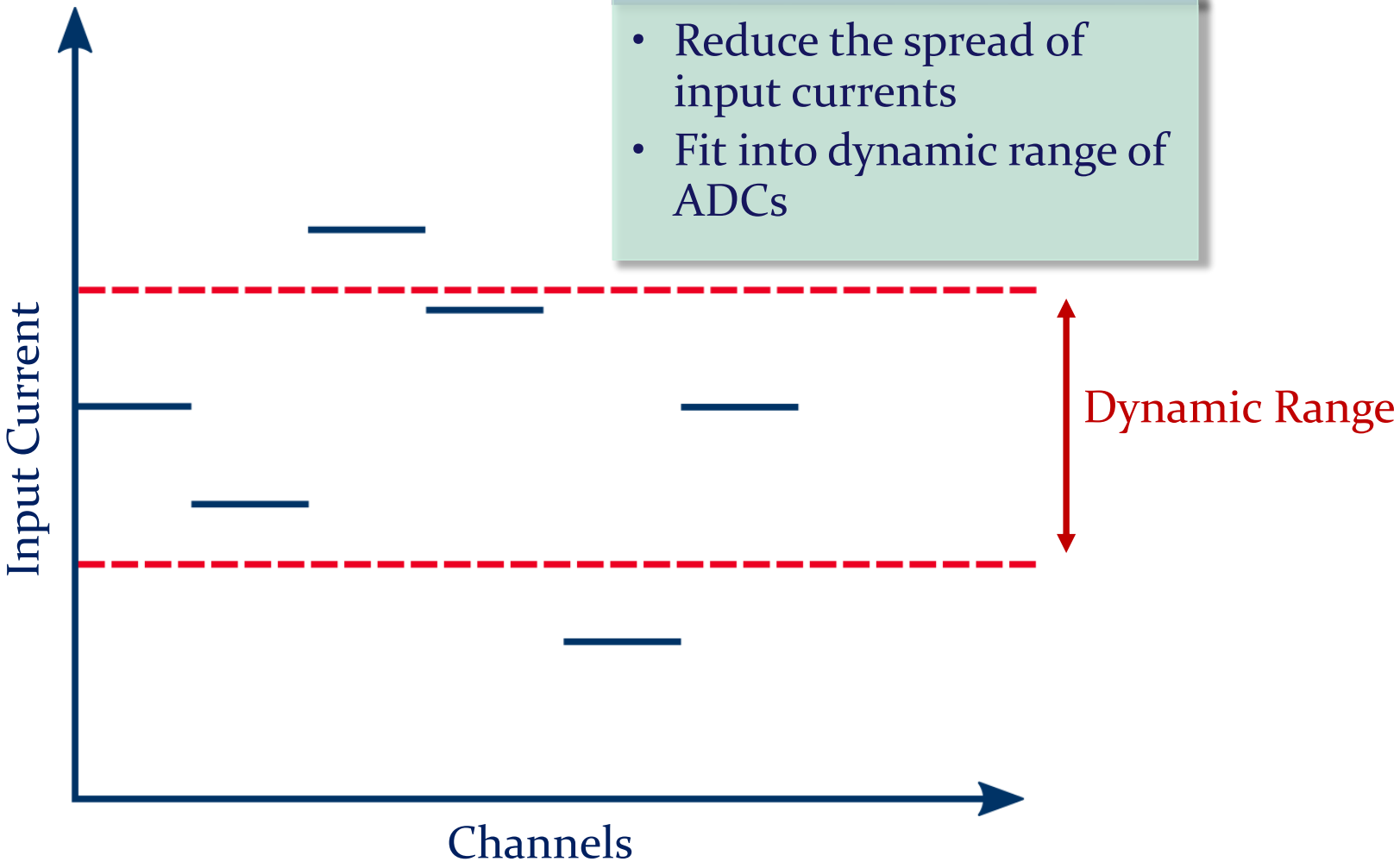
$$G \sim \frac{R_f}{R_s}$$

Rf	Rs	Gain
30kΩ	30kΩ	1
30kΩ	15kΩ	2h
60kΩ	30kΩ	2l
60kΩ	15kΩ	4

2 Bit Offset Compensation

Goal

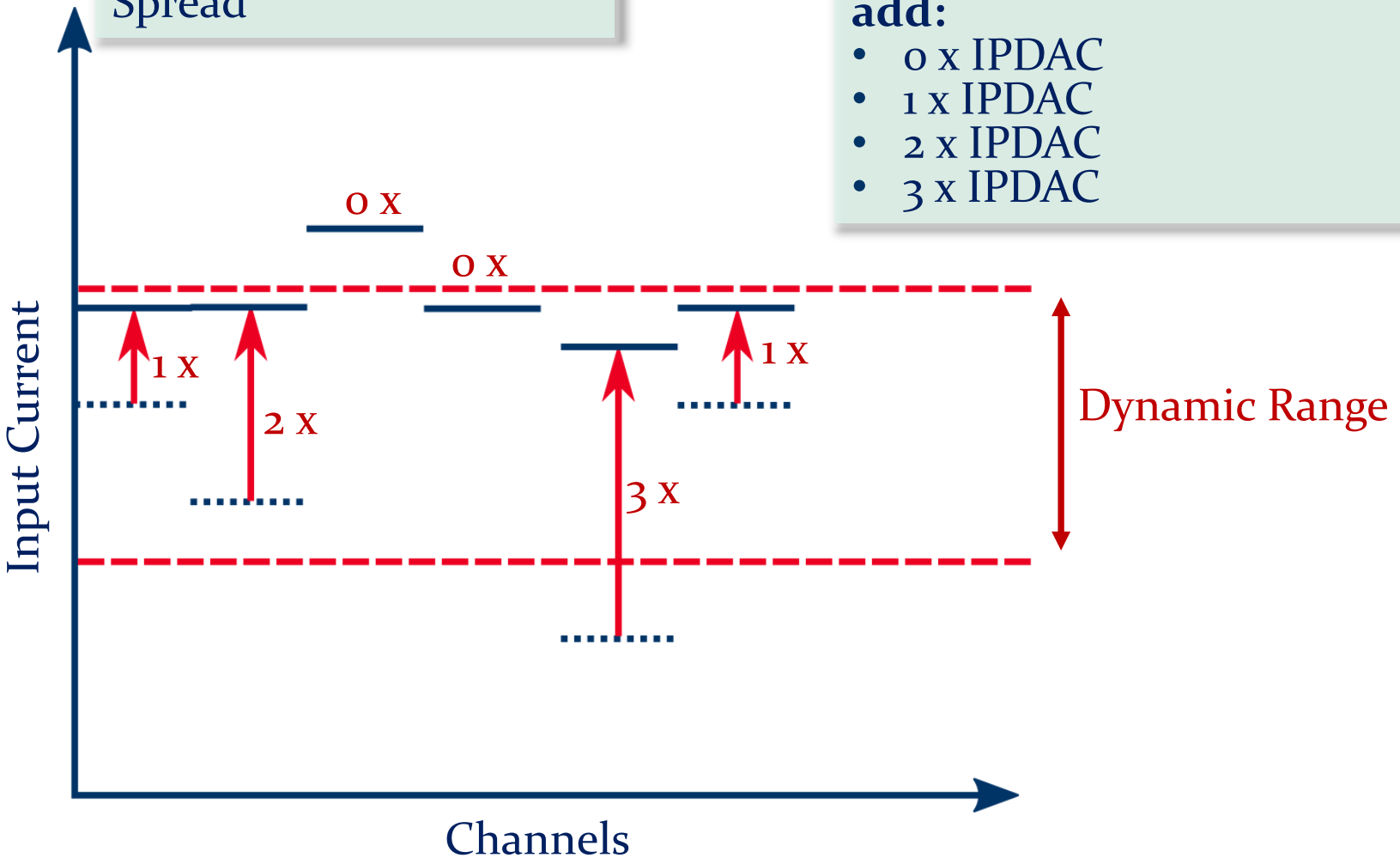
- Reduce the spread of input currents
- Fit into dynamic range of ADCs



2 Bit Offset Compensation

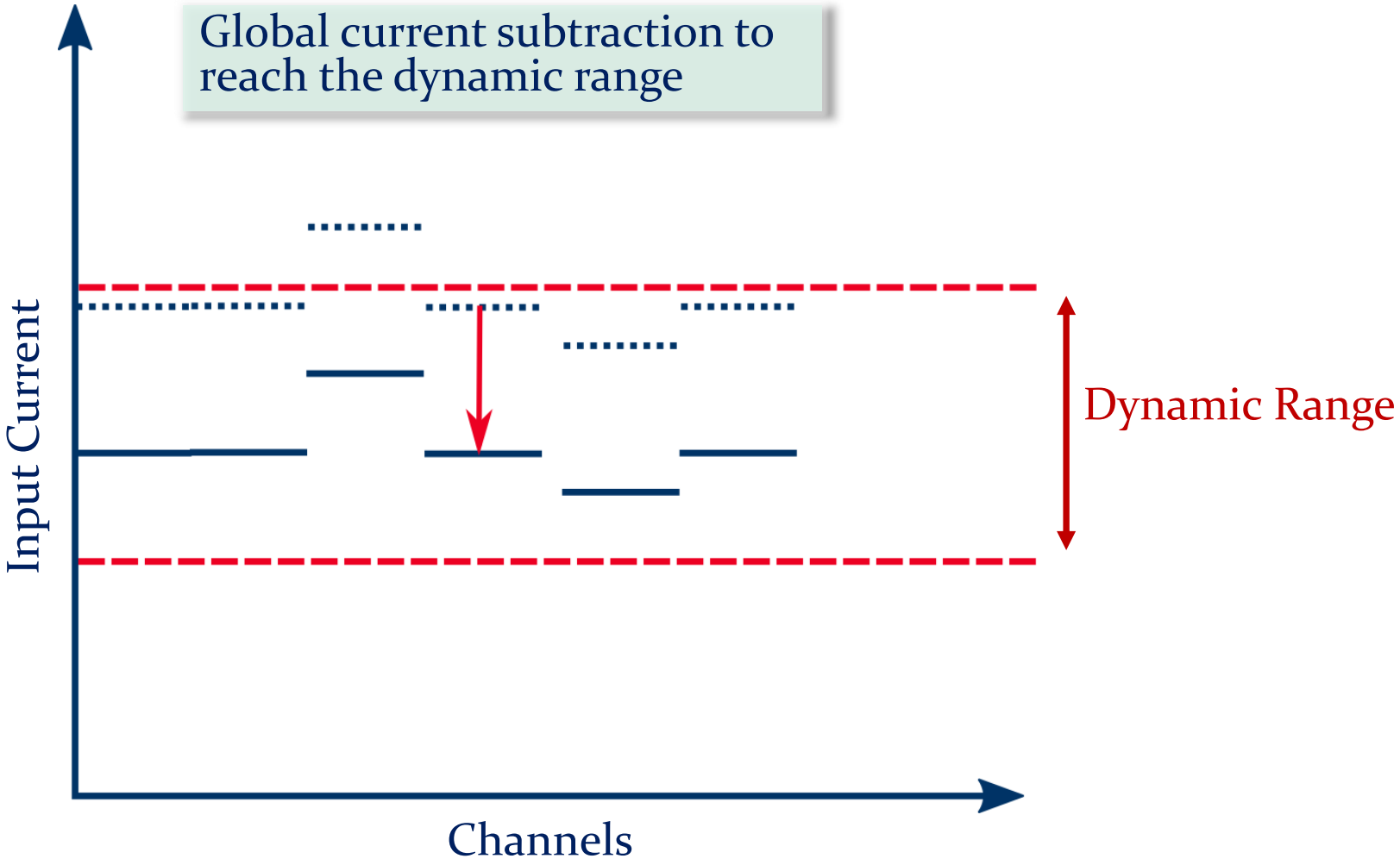
Reduction of Pedestal Spread

add:
- 0 x IPDAC
- 1 x IPDAC
- 2 x IPDAC
- 3 x IPDAC

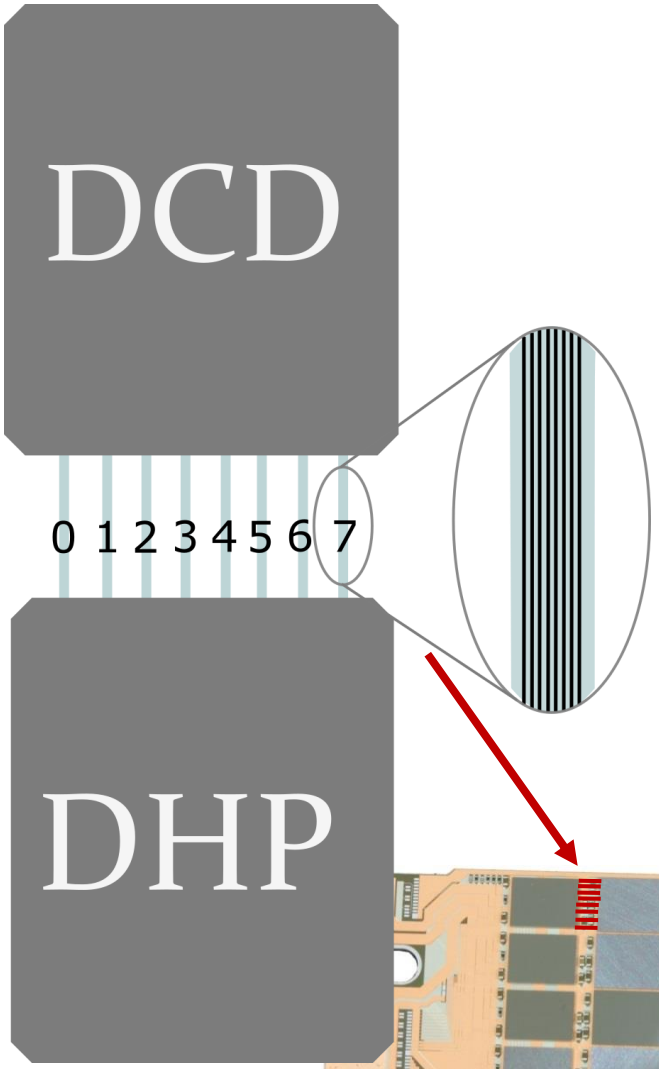


2 Bit Offset Compensation

Global current subtraction to reach the dynamic range



Data Transmission – DCD to DHP

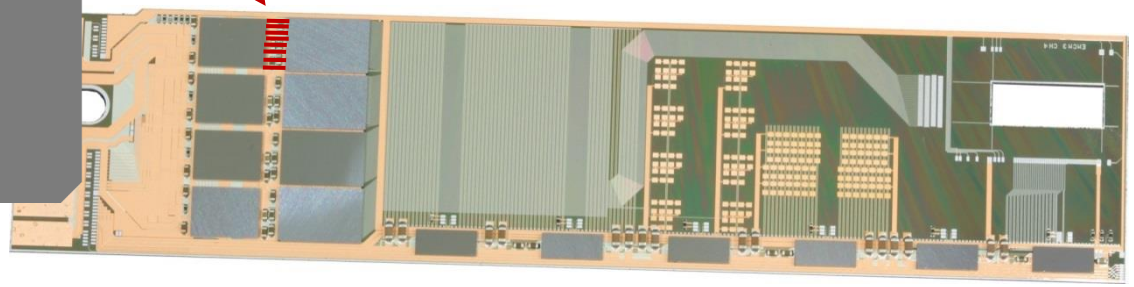


8 Data Buses

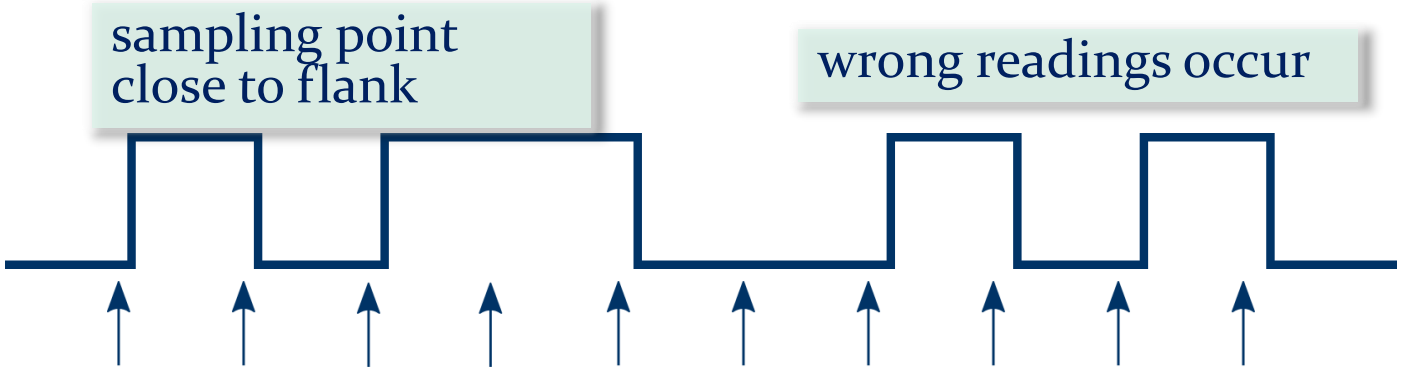
- 32 channels multiplexed to 1 data bus
- 8 data buses for 256 channels

8 Transfer Lines per Data Bus

- each data line has 8 bit
- 64 transfer lines in total



Sampling Point



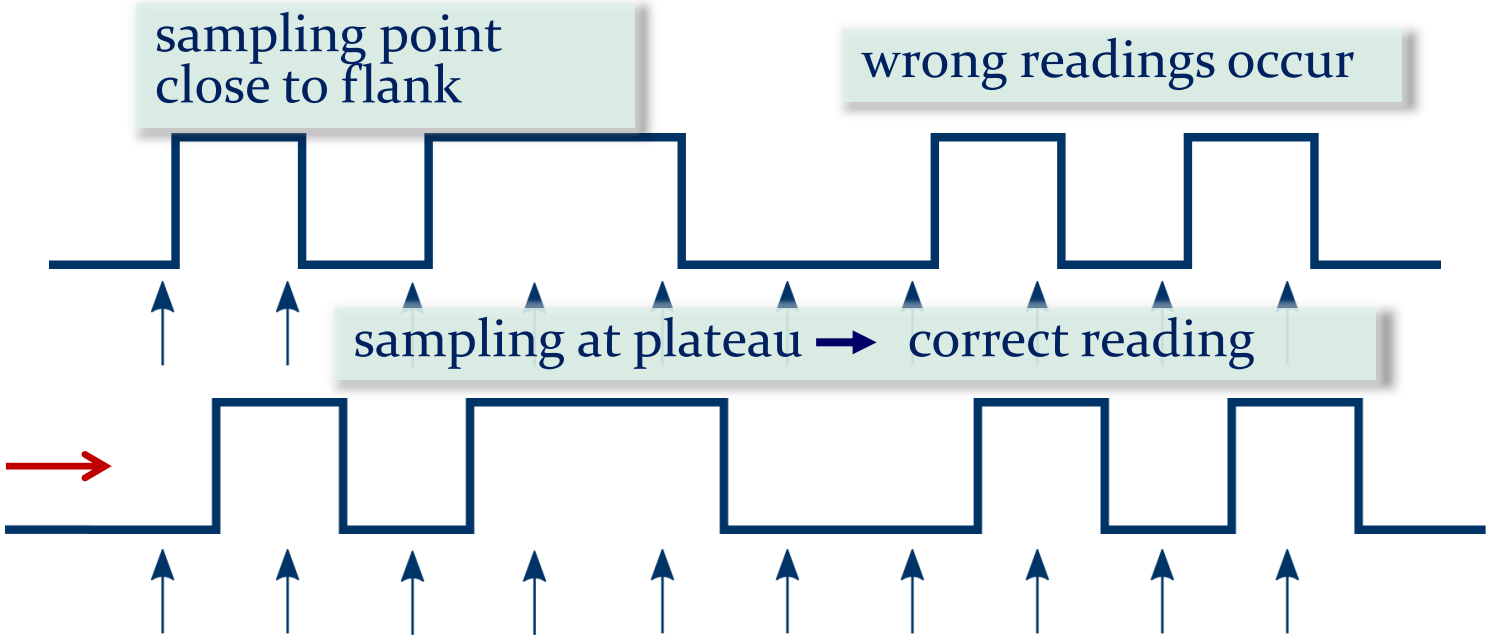
Local Delay

- single channel
- up to 15 delay elements

Global Delay

- all channels
- up to 15 delay elements

Sampling Point



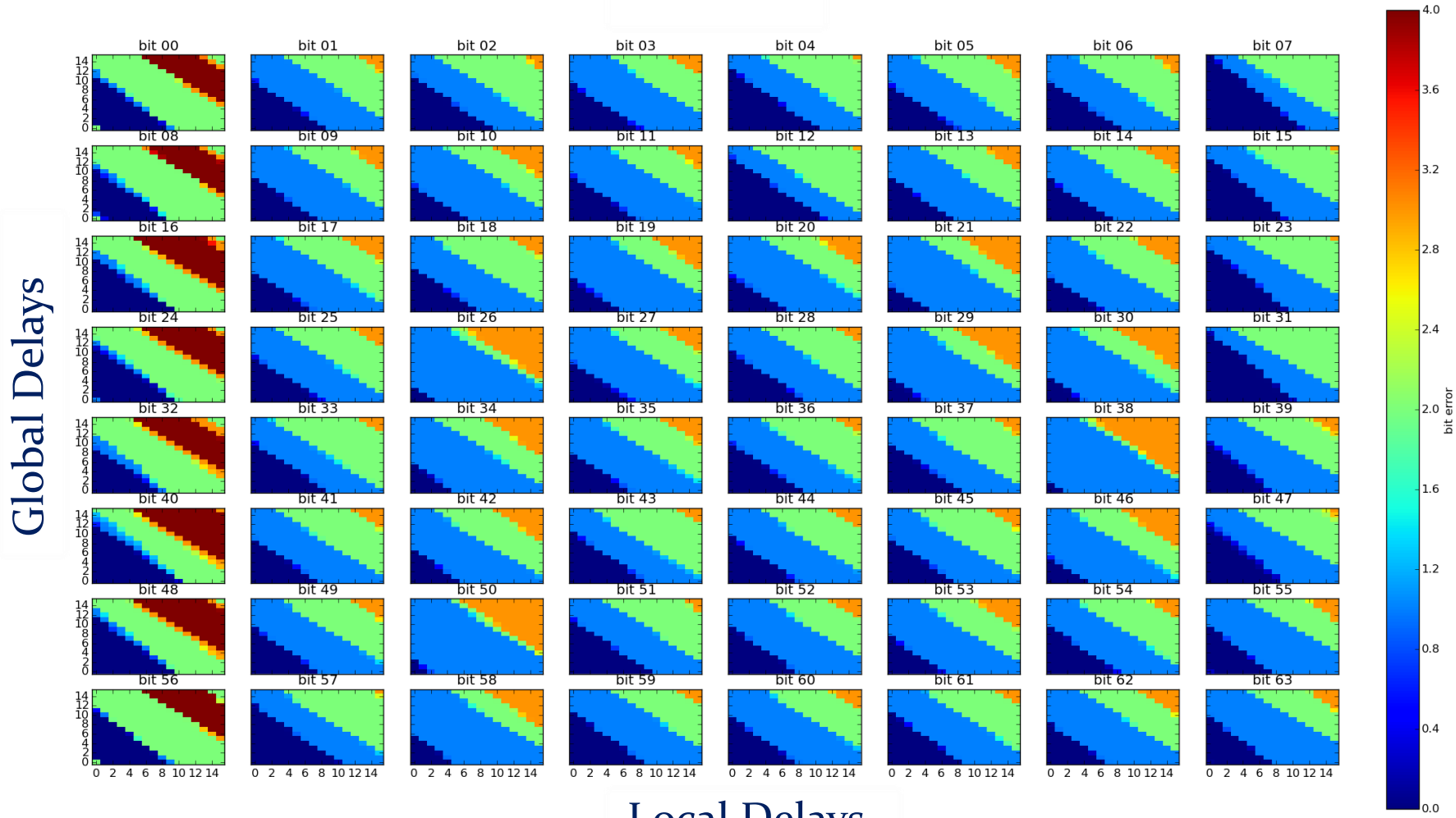
Local Delay

- single channel
- up to 15 delay elements

Global Delay

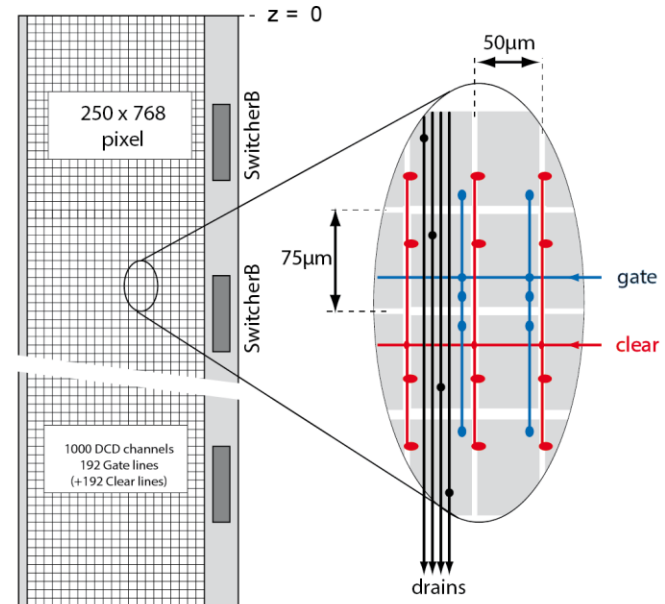
- all channels
- up to 15 delay elements

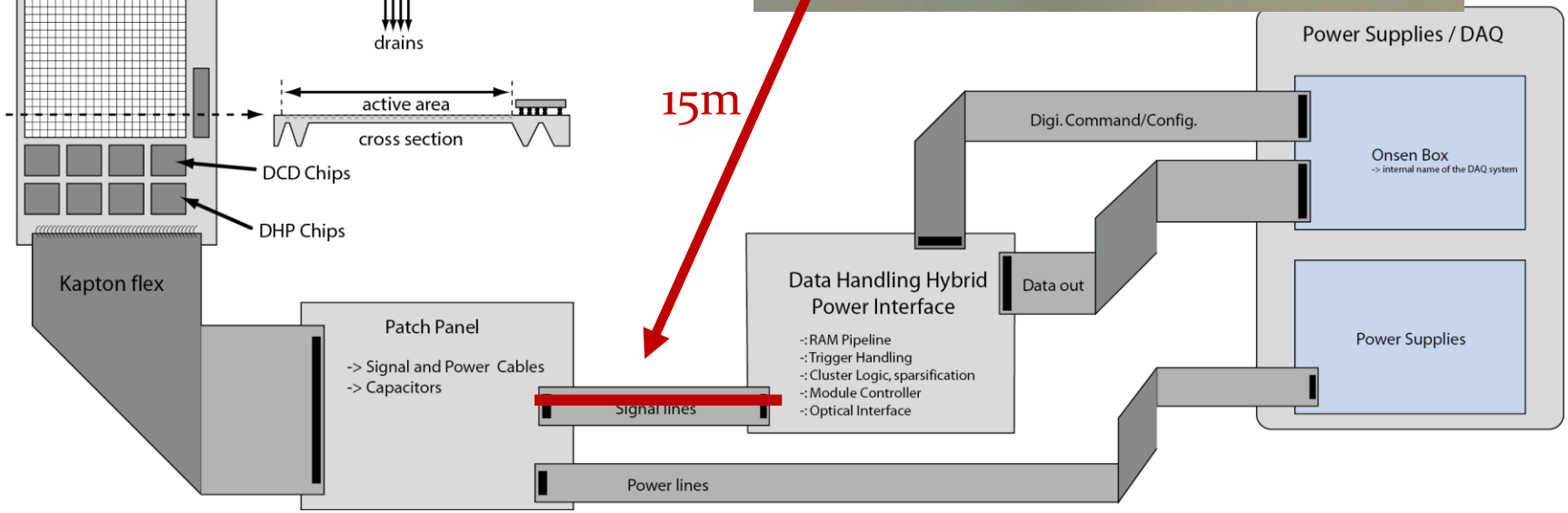
Delay Space



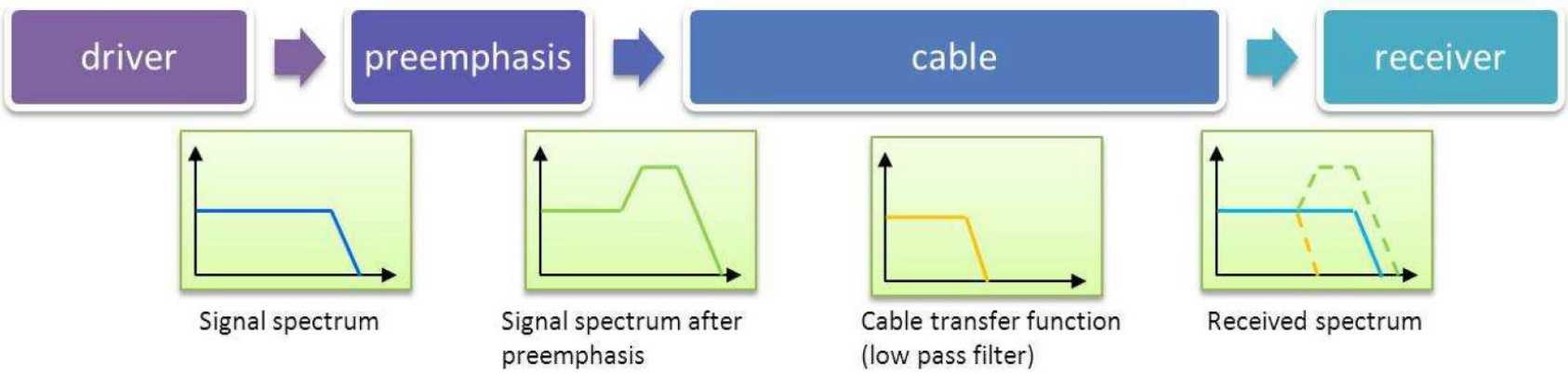
Dark Blue: correct transmission

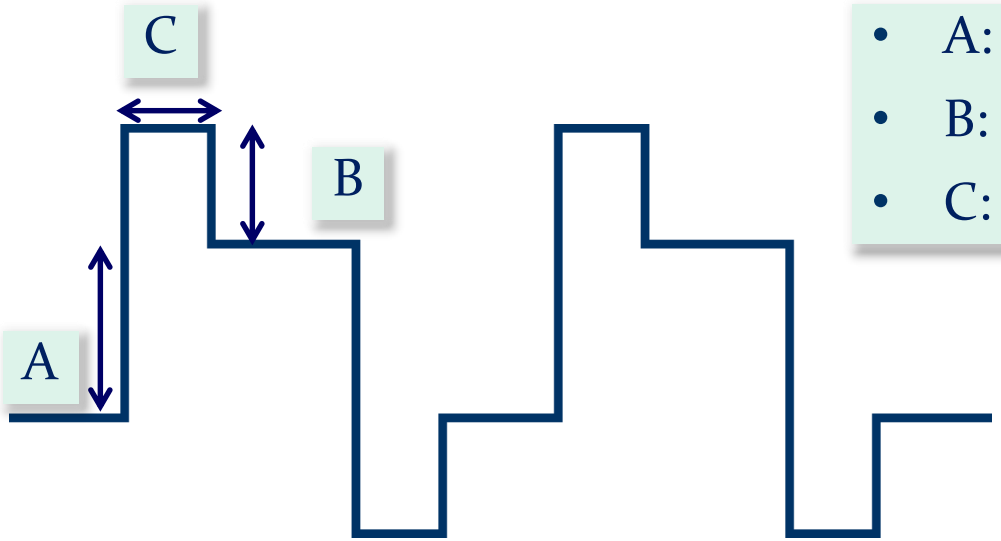
Data Transmission – DHP to DHH





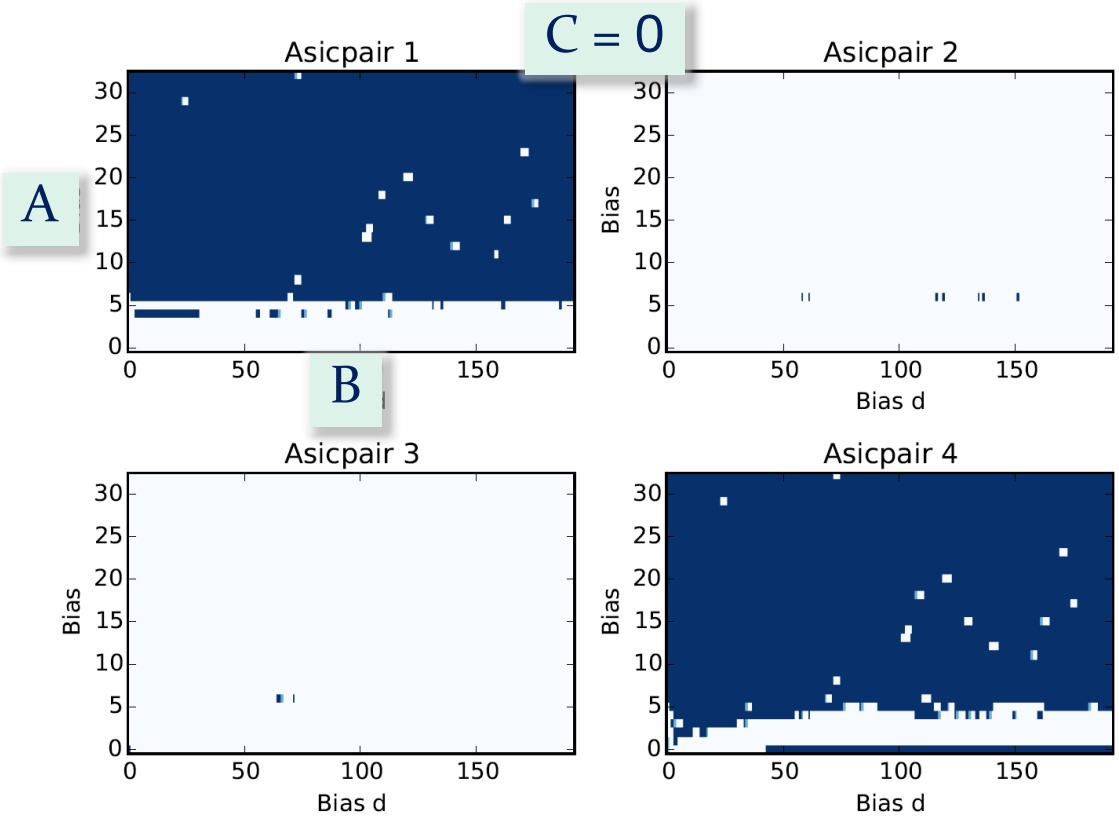
Data Transmission – DHP to DHH

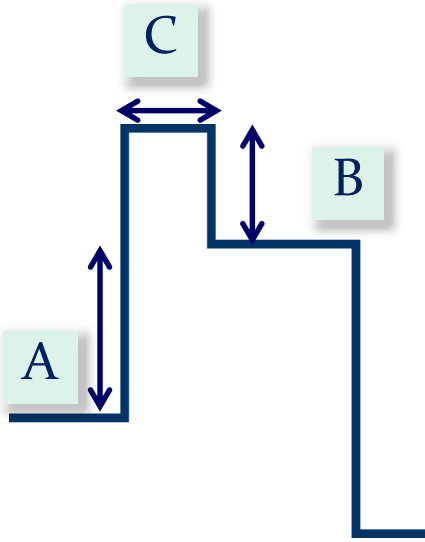




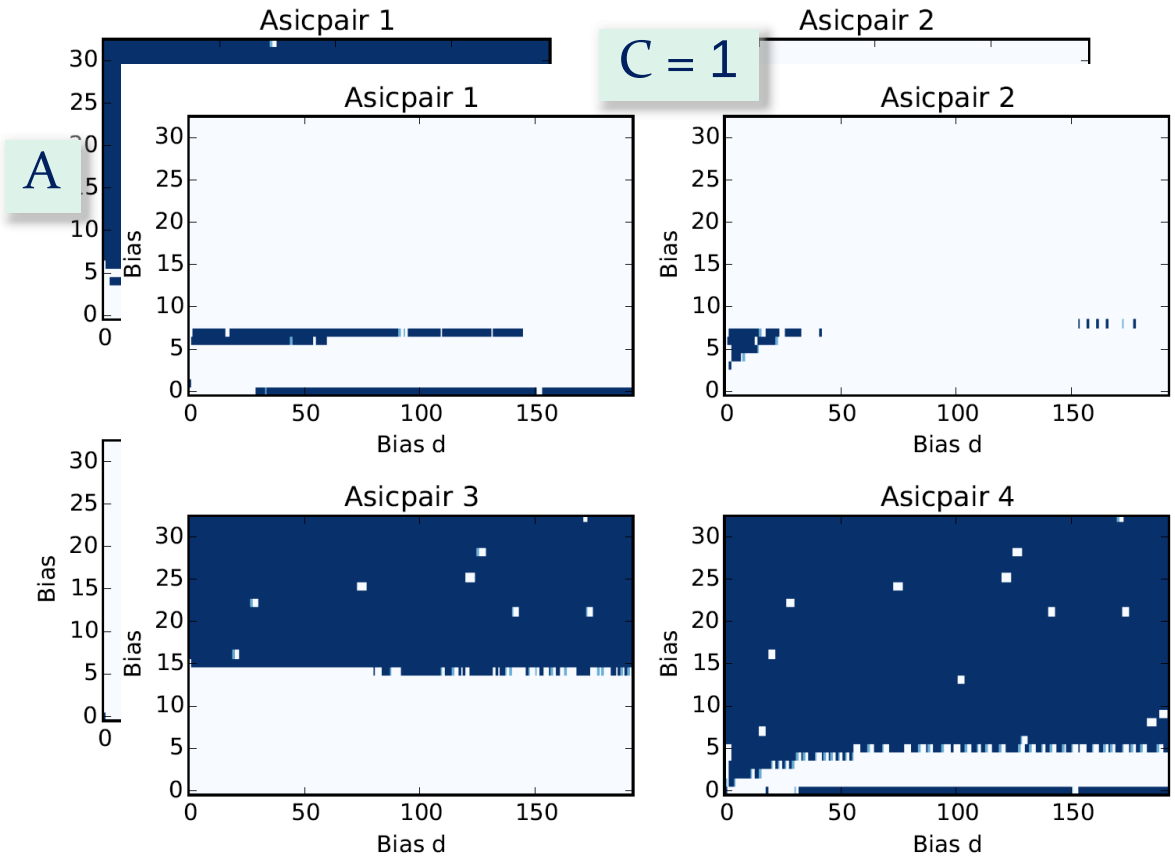
- A: Signal Amplitude
- B: Overshot Amplitude
- C: Overshot Width

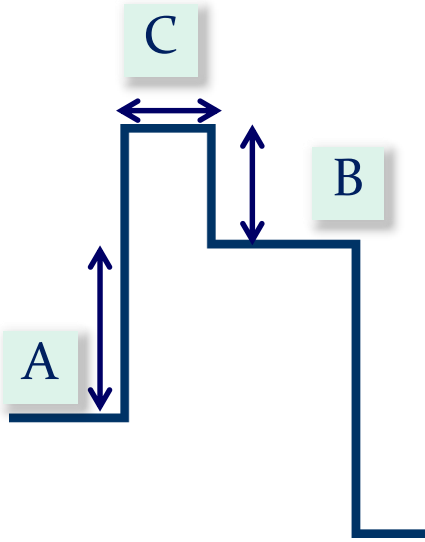
Data Transmission – DHP to DHH





Data Transmission – DHP to DHH





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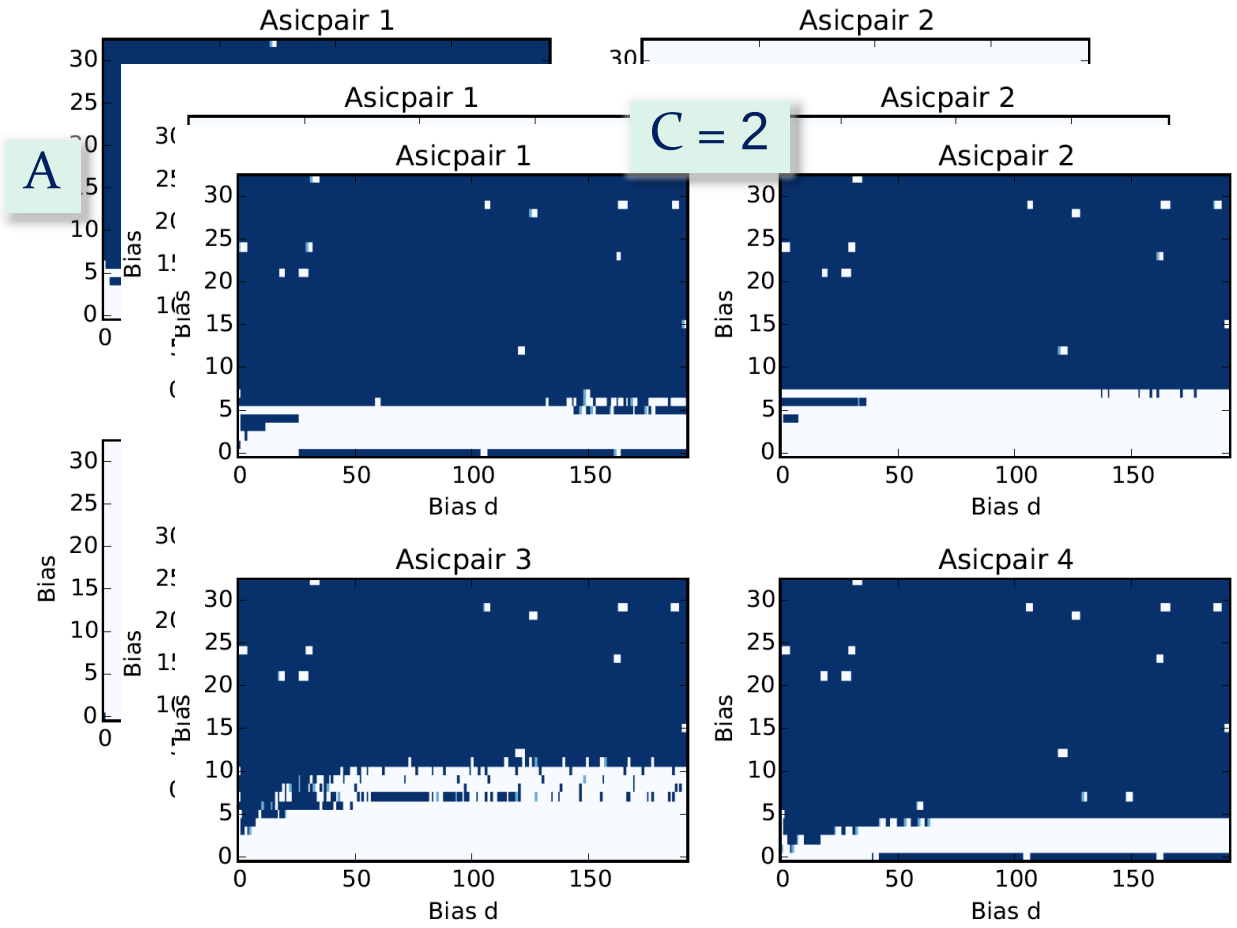
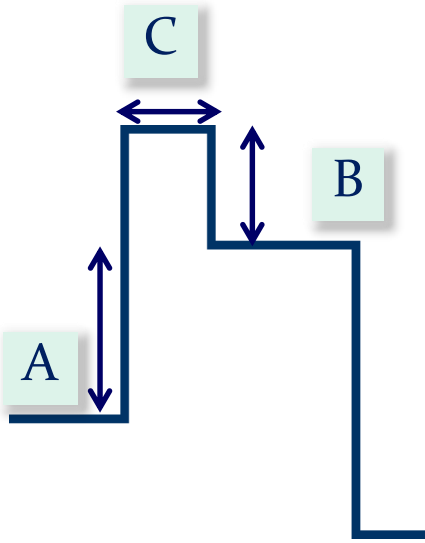
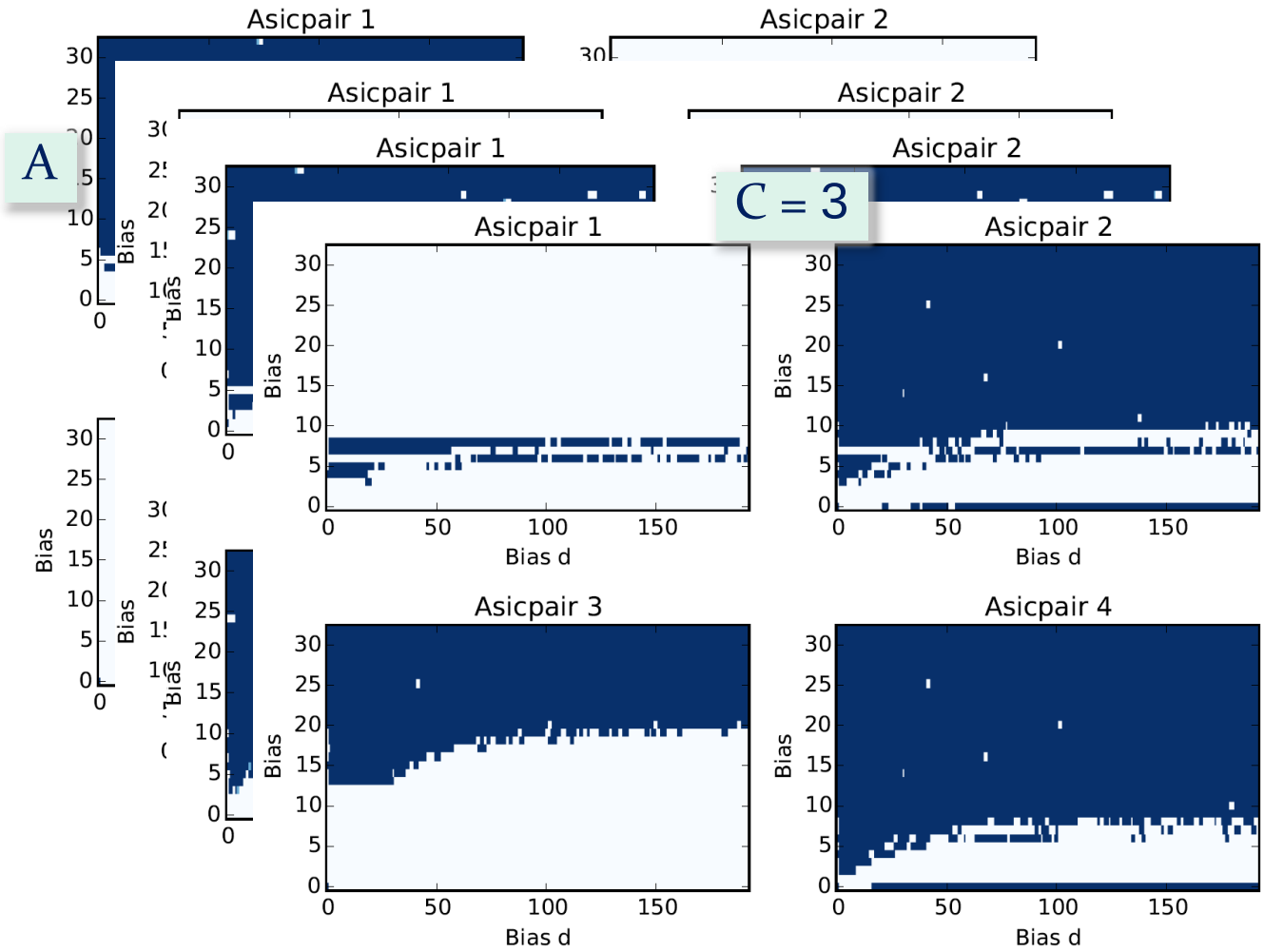
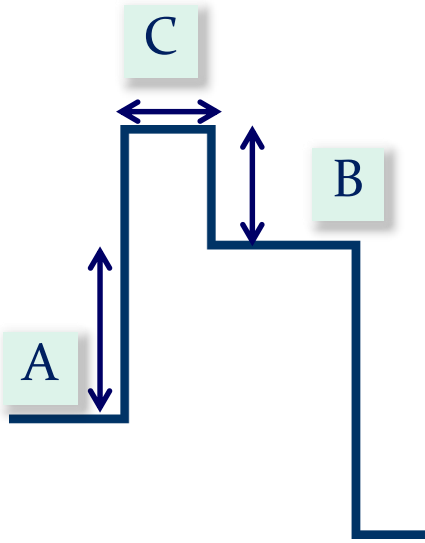




Data Transmission – DHP to DHH





Summary

- **EMCM – Half Ladder without DEPFET**

- **ADC Transfer Curves**
  - Dynamic Range for Gain Settings
  - 2 Bit Offset Compensation
  - Data Transmission
  - ADC Settings

- **Outlook**
  - Operation and characterization of a small test matrix on EMCM
  - Final modules will be tested and characterized starting from August