**General remarks**

For coordination reasons, it would be helpful if the management could present one, agreed-upon schedule.

**Specific recommendations for each ASIC**

**Switcher**

**General comments:**

* Generally in good shape:
	+ Concept proven
	+ Performance: only concern is speed of Clear signal
* Required changes look modest
* Concern regarding radiation hardness of the HV transistors
* We endorse performing detailed tests of the Gated Mode operation

**Specific charged items:**

1. **The maturity of the chip design**

**Quite mature.**

1. **Completeness and quality of documentation.**

**Comprehensive Specification document lacking. Reference Manual is a good start, needs to be expanded to include performance requirements.**

1. **Status of performance tests (stand alone and on system level).**

**Additional Gated Mode testing needed. Further radiation hardness testing likewise needed.**

1. **Known problems and mitigation/correction plans.**

**Main issue understood and plausible corrective plan proposed. Needs to be implemented.**

1. **Missing measurements and tests.**

**Addressed above.**

1. **Work plan (responsibilities, milestones).**

**Recommend clarifying test program leading to ASIC revision. Designer needs to clarify scope of modification, which will drive the schedule.**

1. **Schedule for next submissions.**

**June submission plausible, if consistent with above estimates.**

1. **QA strategy.**

**General test plan looks reasonable. The committee expresses concern regarding the proposed ASIC modifications to support multiplexed testing (additional HV-LV conversion, output multiplexing).**

Recommendations:

* End users should review Reference Manual for completeness
	+ Are pin table listings sufficient?
	+ Interface control description adequate?
* Recommend creating Hardware Description Language description of Gating functionality
* Concern regarding radiation hardness of the HV transistors
* We endorse performing detailed tests of the Gated Mode operation
* We recommend investigating long-term burn-in/stress testing of HV operation

**DCD**

**General comments:**

* Basic architecture looks well suited to the requirements
* The committee expresses serious concerns about the details of the ADC implementation
	+ Unclear if problems observed are sensitivities to process parameters
	+ Further design work needed

**Specific charged items:**

1. **The maturity of the chip design.**

**We forsee significant additional design effort to address concerns regarding the ADC implementation**

1. **Completeness and quality of documentation.**

**A comprehensive Specification Document is lacking. Reference Manual is a good start, needs to be expanded to include performance requirements.**

1. **Status of performance tests (stand alone and on system level).**

**Strongly recommend further testing to understand variety of pathologies observed. Further ASIC/channel testing statistics are needed.**

1. **Known problems and mitigation/correction plans.**

**Matching of observation with simulation is mandatory.**

1. **Missing measurements and tests.**

**More an issue of understanding results observed that missing measurements. Encourage further, cross-checked analyses.**

1. **Work plan (responsibilities, milestones).**

**Highly important that before next submission these problems are fully understood, to avoid excessive risk in resubmission.**

1. **Schedule for next submissions.**

**Given the above concerns, a February submission seems very aggressive. Items above must be resolved prior to submission. Verifying Monte Carlo spreads will likely take time, and sufficient time should be allocated.**

1. **QA strategy.**

**Generally looks OK.**

Recommendations:

* Better understanding of noise performance and instabilities needed
* Consider an SEU test of the DCD
* More work is needed prior to a next submission. Submission schedule should be driven by the readiness to address the above issues.
* Careful consideration should be given to assess risk versus rewards of the changes proposed.

**DHP**

**General comments:**

* Specifications still not concisely presented
* Overall architecture looks very sound
* Cannot put all effort on the ASIC side. System engineering of cabling and interconnects, and an agreed-upon model for output load is needed.
* Complexity makes testing difficult

**Specific charged items:**

1. **The maturity of the chip design.**

**Data flow, PLL, synthesized logic are very mature. Remaining concern is in the verification of the high-speed interfaces.**

1. **Completeness and quality of documentation.**

**Specifications for output loads and timing are needed for signals in Table 1 of the Manual. For such a complex device, a more comprehensive document many be required.**

1. **Status of performance tests (stand alone and on system level).**

**Most IP Block / Task items test results well documented. Remaining issues well presented.**

1. **Known problems and mitigation/correction plans.**

**Proposed further testing seems adequate.**

1. **Missing measurements and tests.**

**Finer step TID testing, SEU testing. Channel masking and Overflow handling tests self-identified.**

1. **Work plan (responsibilities, milestones).**

**Not clear who is doing what to provide further testing and by when. A detailed model of the cabling needed to complete output driver redesign.**

1. **Schedule for next submissions.**

**June submission seems plausible given proposed testing schedule. A rigorous internal review of the proposed changes should be held prior to release for submission.**

1. **QA strategy.**

**Proposed quality control plan seems adequate.**

Recommendations:

* Characterize the electrical properties of the external interconnects and cables.