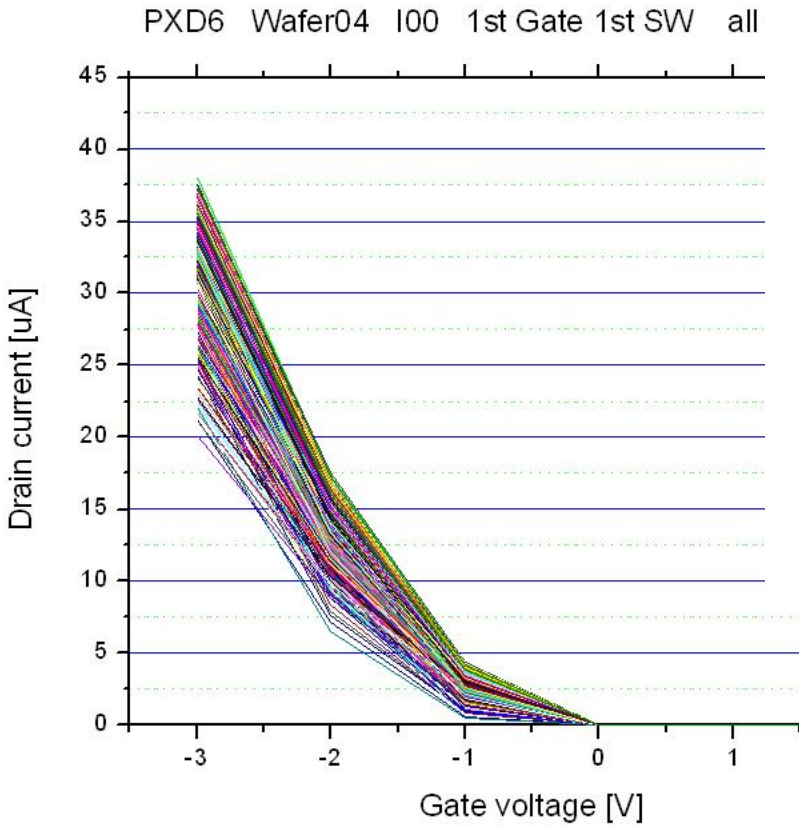
Belle2- ASIC Review
July 2015

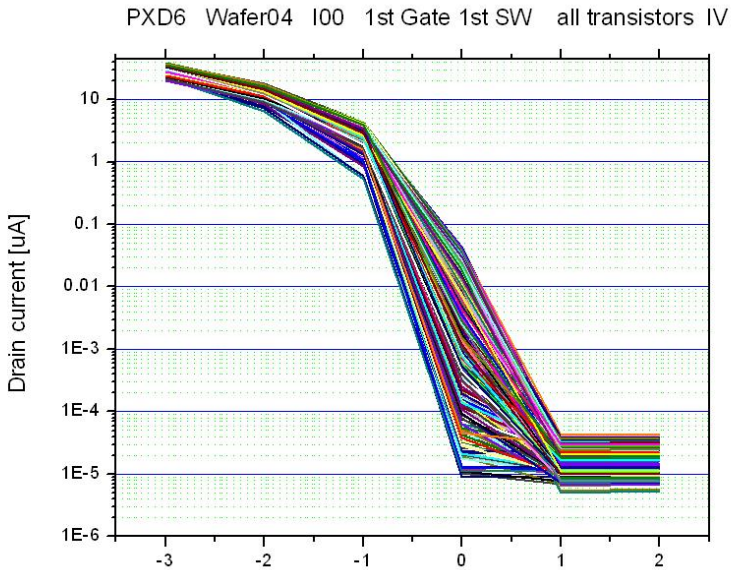
Pedestal spread (sensors)

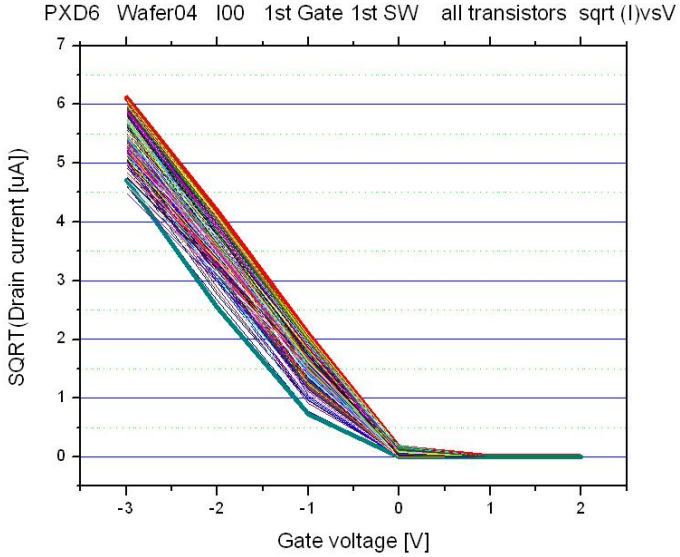
Preparation

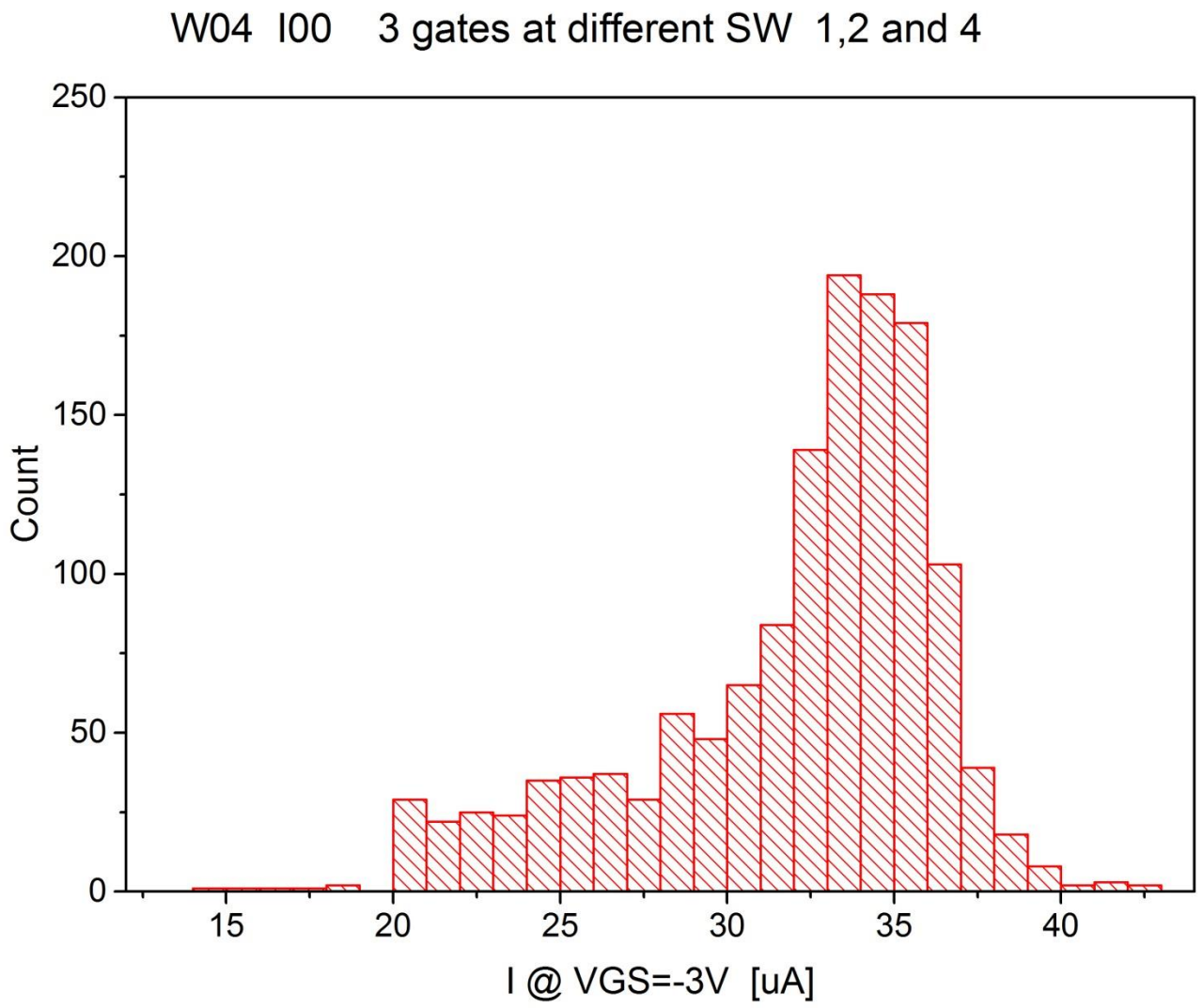
PXD6 results

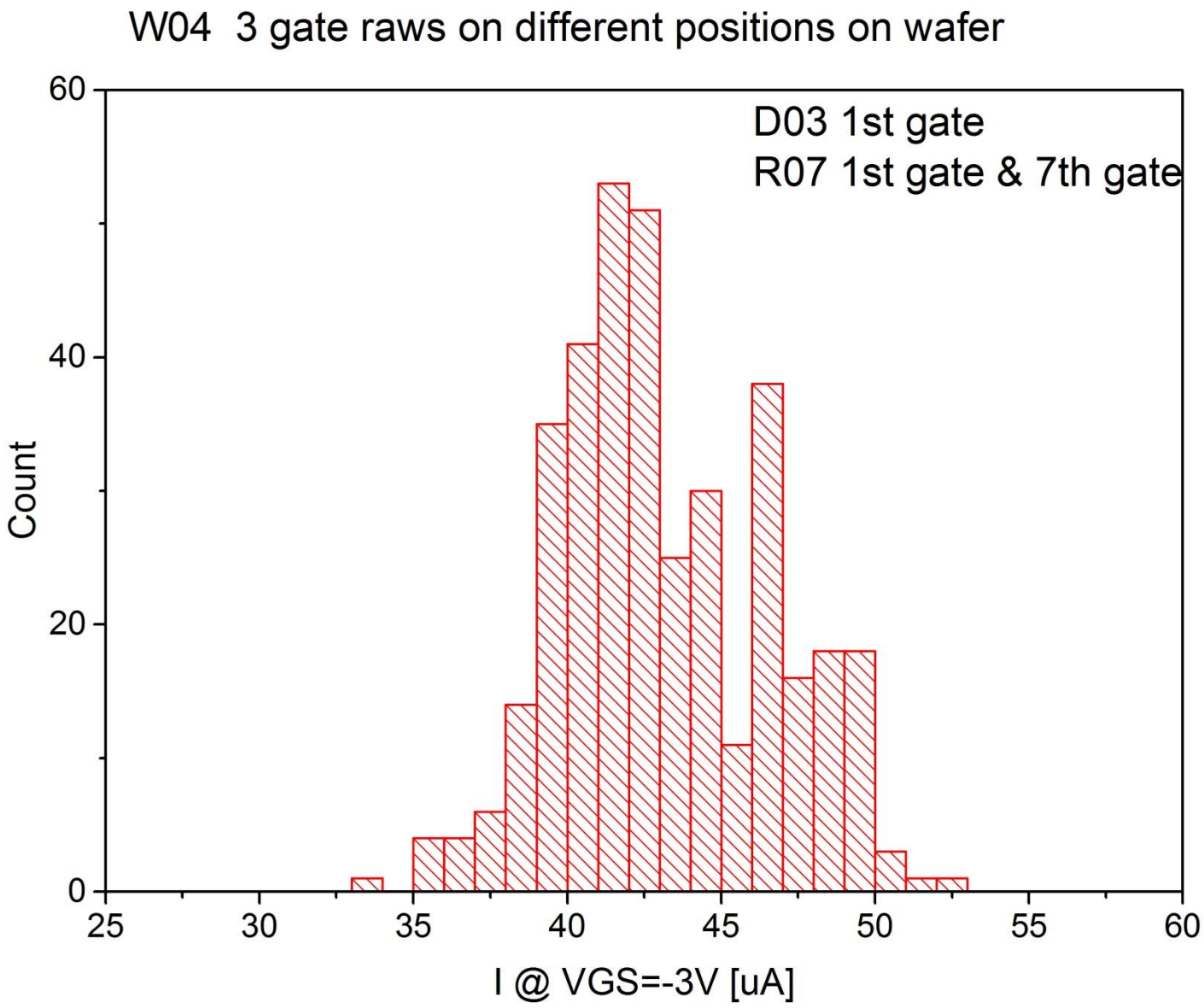
768 Depfets – Big Matrix I00 first row

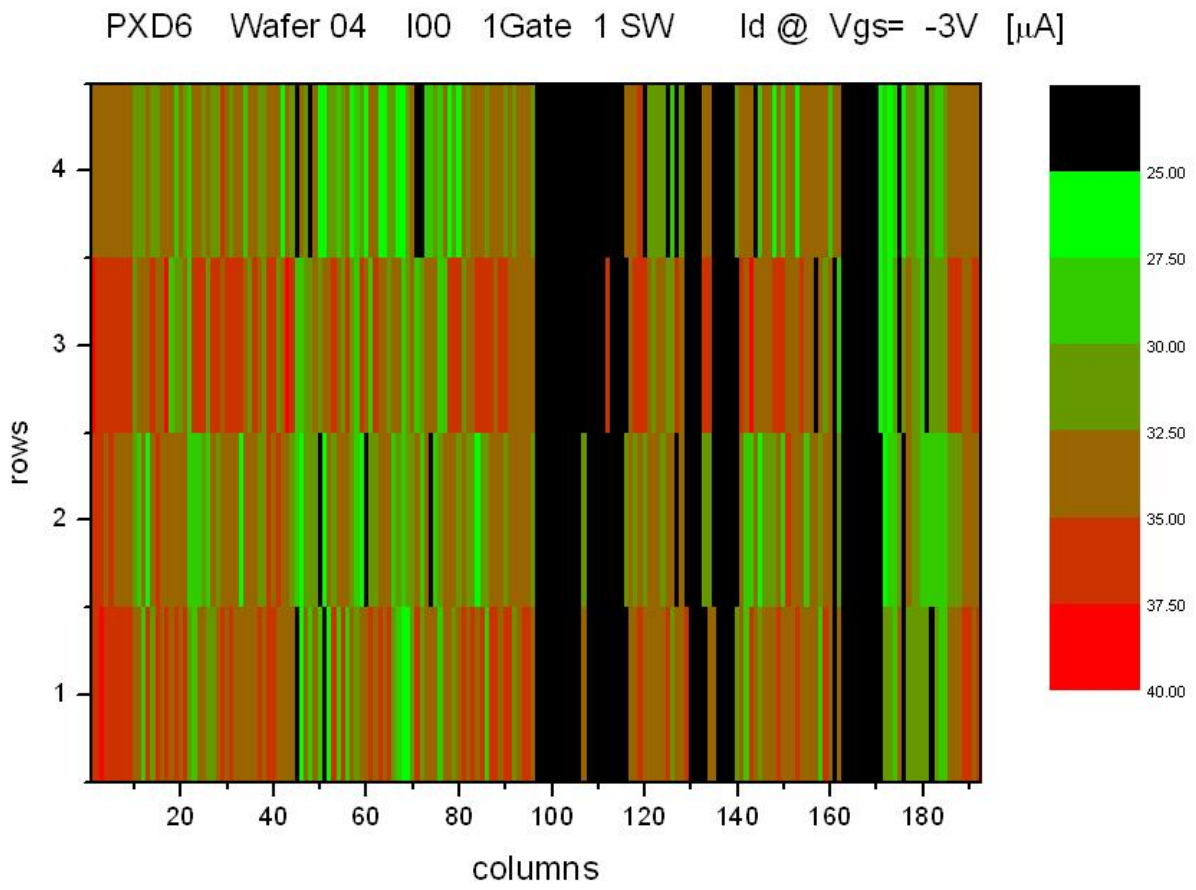


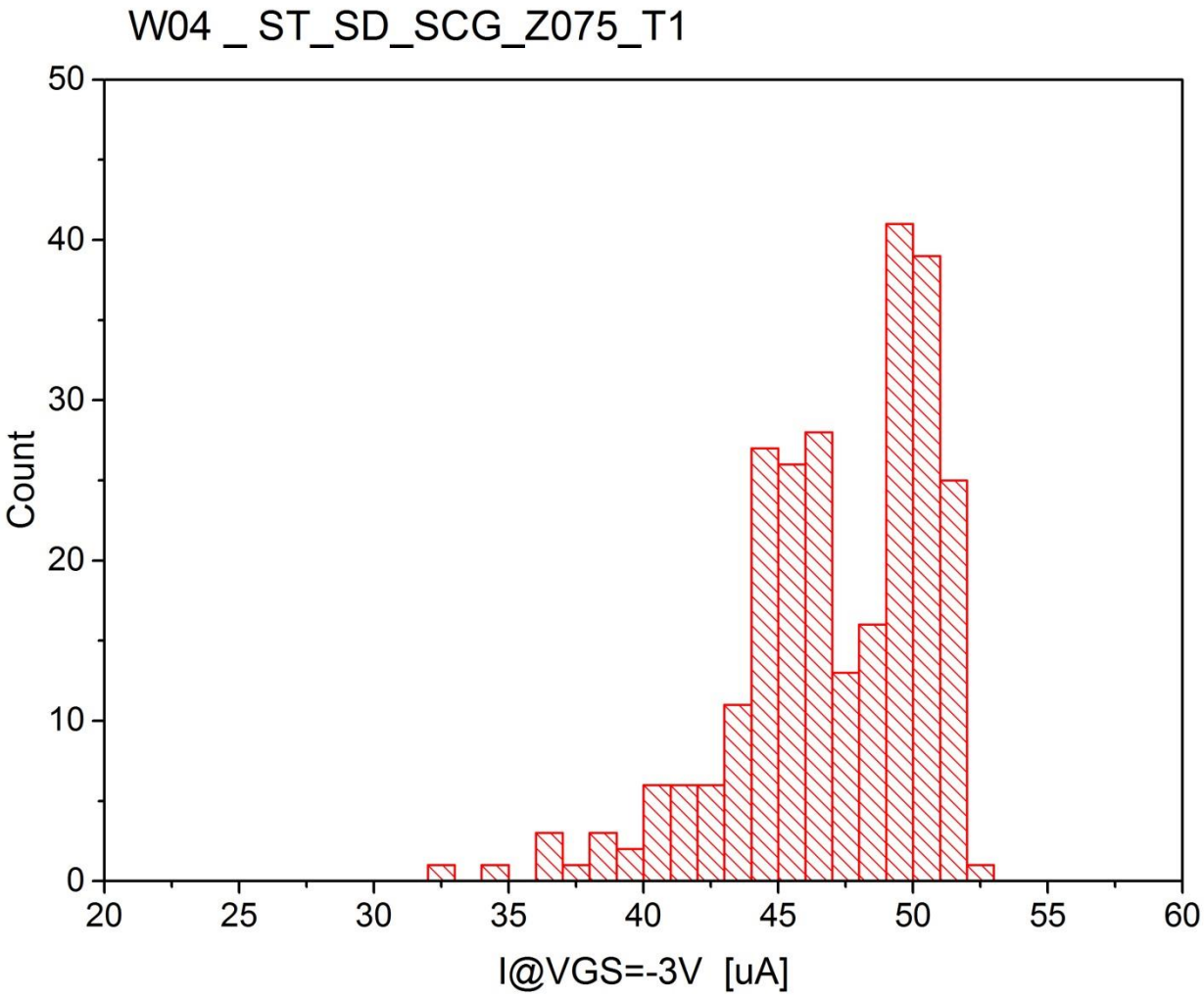





W04 I00 3 gates at different SW 1,2 and 4
Count
250
200
150
100
50
0
15
20
25
30
35
40
I @ VGS=-3V [uA]


W04 3 gate raws on different positions on wafer
D03 1st gate
R07 1st gate & 7th gate
Count
0
20
40
60
25
30
35
40
45
50
55
60
I @ VGS=-3V [uA]


PXD6 Wafer 04 I00 1Gate 1 SW Id @ Vgs= -3V [µA]
rows
columns
4
3
2
1
20
40
60
80
100
120
140
160
180
25.00
27.50
30.00
32.50
35.00
37.50
40.00


W04 _ ST_SD_SCG_Z075_T1
Count
I@VGS=-3V [uA]
0
10
20
30
40
50
20
25
30
35
40
45
50
55
60

Possible reasons for pedestal variations

A) Parasitic Source resistors (gap between Source implant and active channel)
(repaired in PXD9: see last Seeon talk)

B) Gate length (litho, etching)

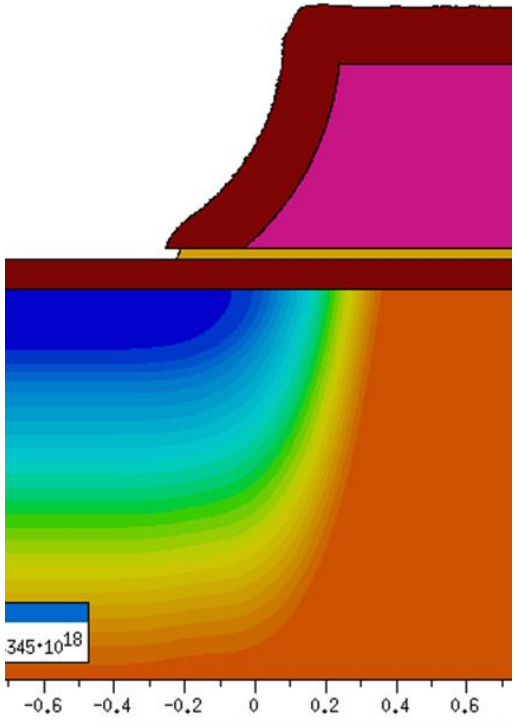
B) Threshold voltage (Implantation, gate oxide thickness, Vfb)

C) Bad channels (poly etch relicts during implantations)

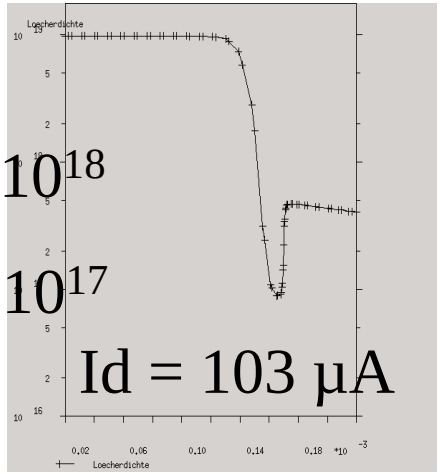
A) Parasitic Source resistor

VG = -3V, VD= -3V

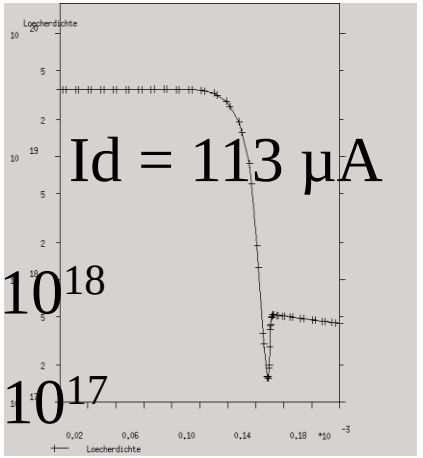
Implant before oxidation



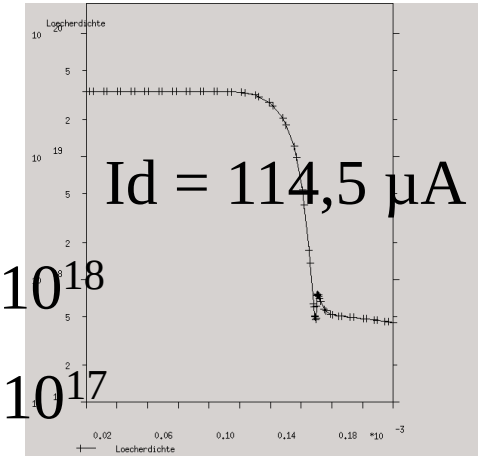
after Ox.



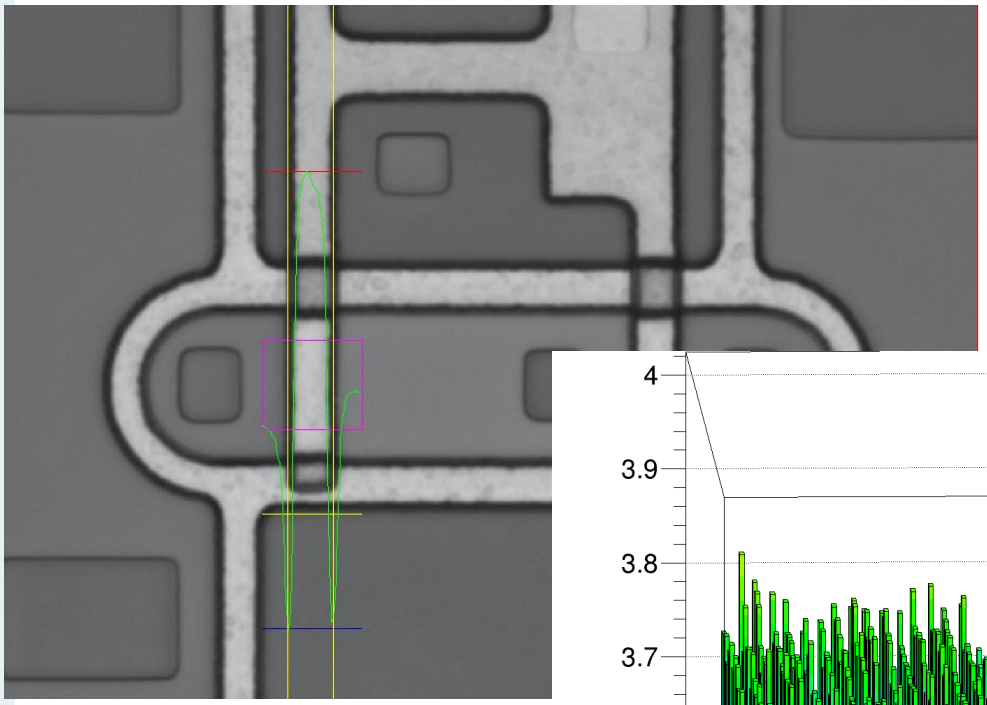
before Ox.

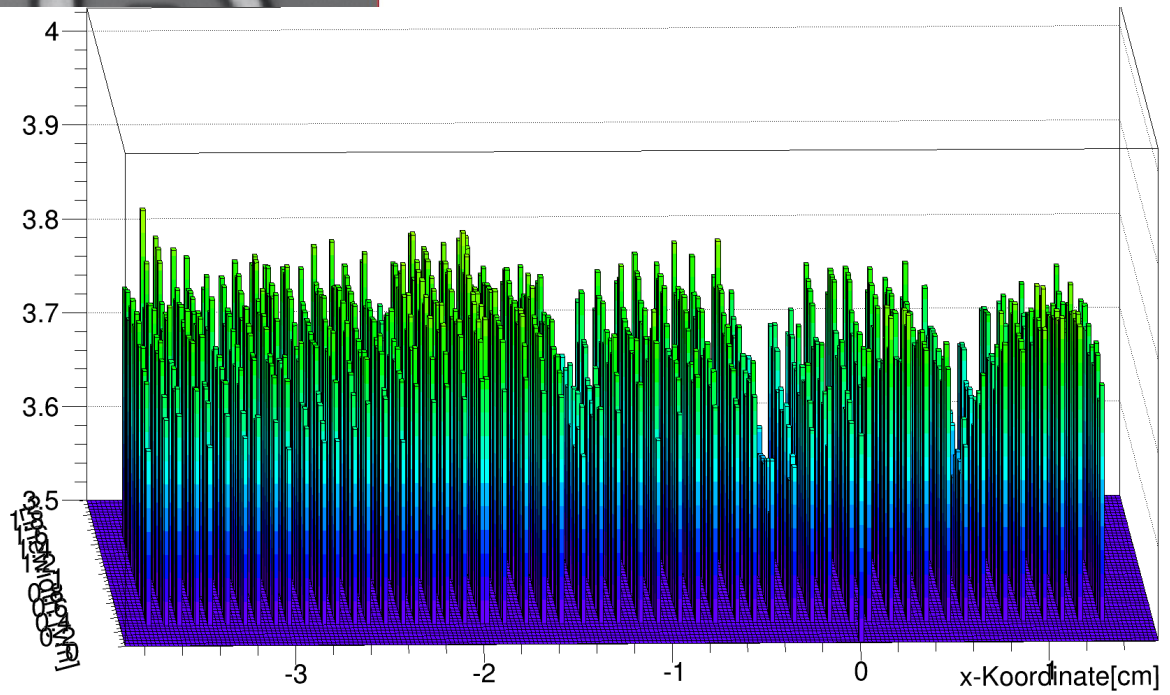


before oxidation
+ optimized
implantation
parameter

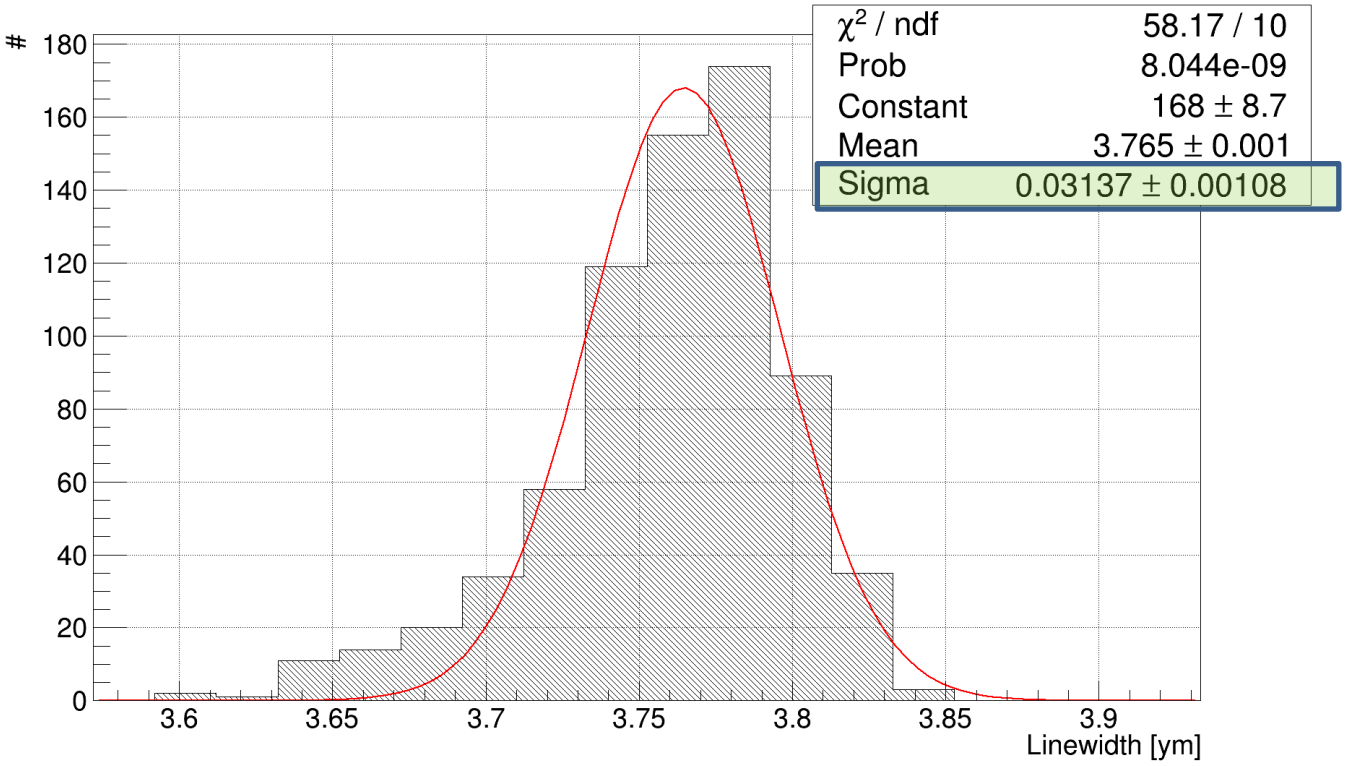


B) Gate length variation – measured at PXD9-3 Wafer 28

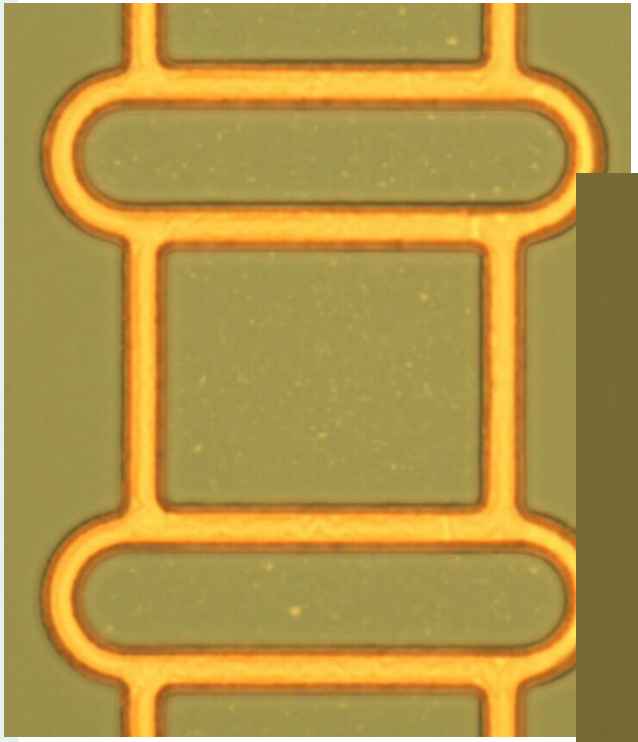




PXD9-3 W28 OF2

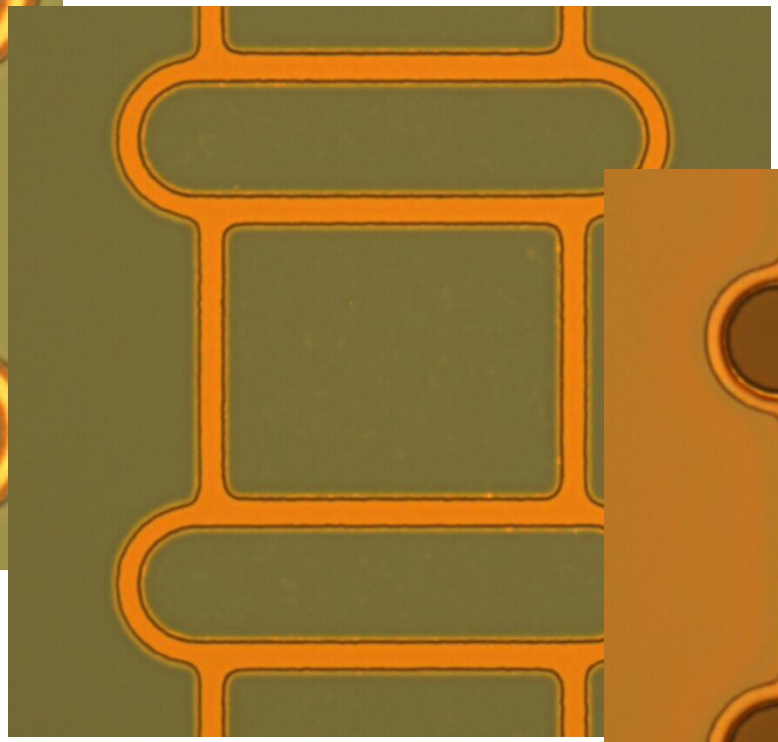


C) Bad Channels: Implantation through poly etch relichts



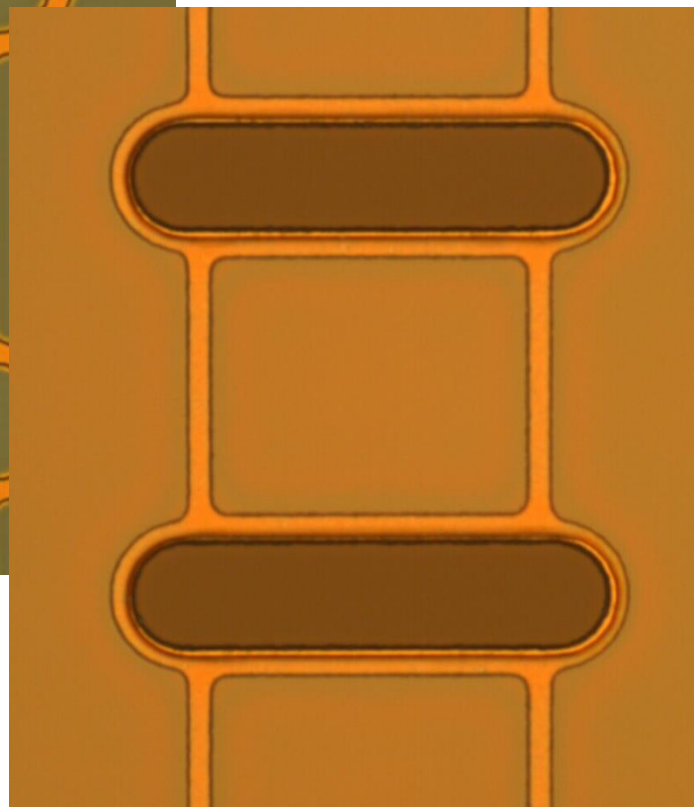
After etching

Shallow p implant
(PXD6)



After removal

Shallow p implant
(PXD9)



After nitride etch

D) Implantation dose variations

In the DEPFET channel:

2 subtracting doses: Internal Gate + shallow p (threshold adjustment)
in the range of 10^12cm-2

Implanter specification: < 0.5% (rms), measured 0.3%

2 x 0.5% = 1% corresponds to 10^10cm-2 dose variation

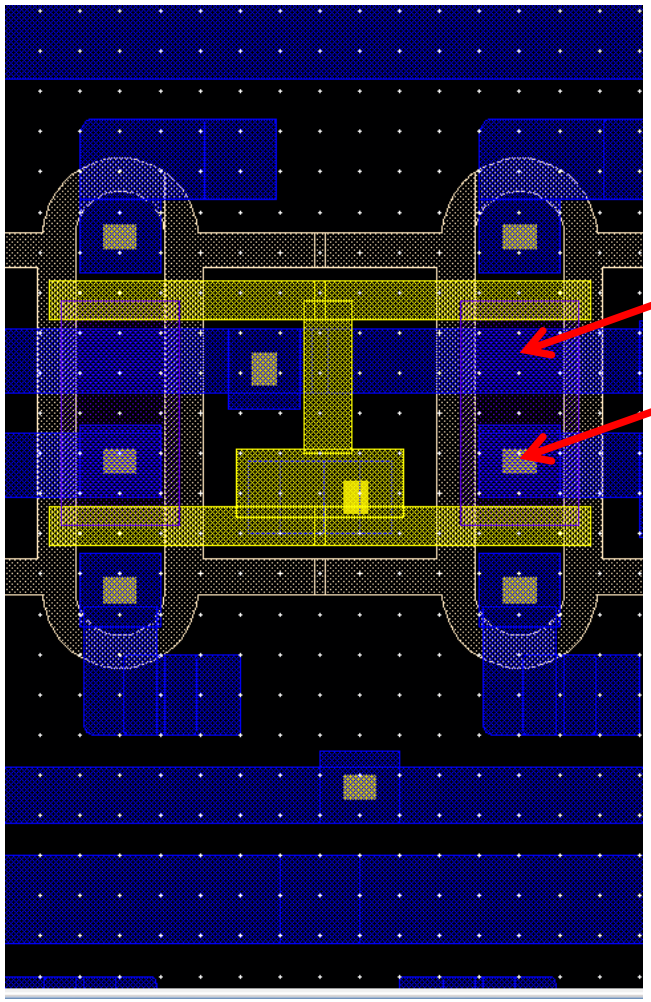
PXD9:

-> thresh. variation 40mV -> 3µA @gm=75µS (Vgs=-3V)

Drain currents PXD9 - W35 (22000,12000 pixel)

$V_G = -3\,V, V_{DS} = -5\,V$	Average current [-µA]		pedestal spread [µA] (2 σ)		Threshold voltage [V]	
$V_{AC} = 15\,V, V_{CG} = 5\,V$	OF1	OF2	OF1	OF2	OF1	OF2
switcher1 gaterow1	121	114	21 (7)	17 (6)	0,051	-0,016
switcher1 gaterow2	119	113	16 (6)	17 (5)	0,039	-0,020
switcher2 gaterow1	127	122	20 (8)	23 (9)	0,093	0,055
switcher2 gaterow2	126	123	22 (8)	24 (9)	0,098	0,061
switcher2 gaterow3	124	-	13 (5)	-	0,081	-
switcher2 gaterow4	123	-	15 (6)	-	0,073	-
switcher3 gaterow1	119	123	15 (5)	18 (6)	0,025	0,059
switcher3 gaterow2	120	123	17 (5)	16 (5)	0,029	0,057
switcher3 gaterow3	120	-	16 (6)	-	0,026	-
switcher3 gaterow4	121	-	17 (6)	-	0,054	-
switcher4 gaterow1	125	124	19 (7)	25 (10)	0,102	0,081
switcher4 gaterow2	124	124	15 (5)	16 (5)	0,095	0,085
switcher4 gaterow3	124	-	13 (5)	-	0,093	-
switcher4 gaterow4	125	-	15 (6)	-	0,102	-
switcher5 gaterow1	122	120	19 (7)	23 (7)	0,090	0,097
switcher5 gaterow2	122	120	14 (5)	14 (5)	0,087	0,061
switcher5 gaterow3	123	-	16 (5)	-	0,109	-
switcher5 gaterow4	121	-	17 (6)	-	0,090	-
switcher6 gaterow1	122	120	15 (5)	19 (6)	0,074	0,055
switcher6 gaterow2	120	120	17 (6)	15 (5)	0,058	0,050
switcher6 gaterow3	122	-	15 (6)	-	0,076	-
switcher6 gaterow4	121	-	17 (6)	-	0,067	-
Total average	122,3	120,50	16,5 (6,0)	18,9 (6,5)	0,073	0,052

Implications (ii)



Yield lesson from PXD6:
Relaxing the topology

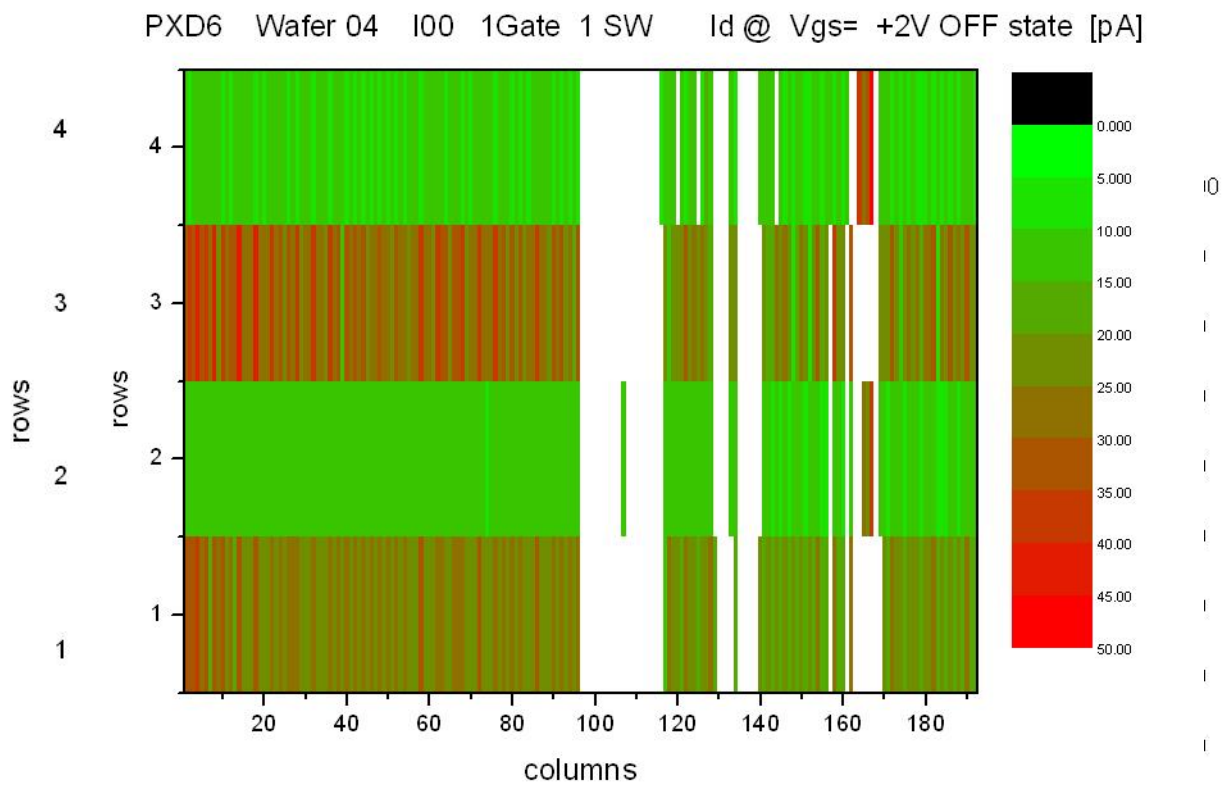
Clear line must run parallel to Source
-> asymmetric Source contact

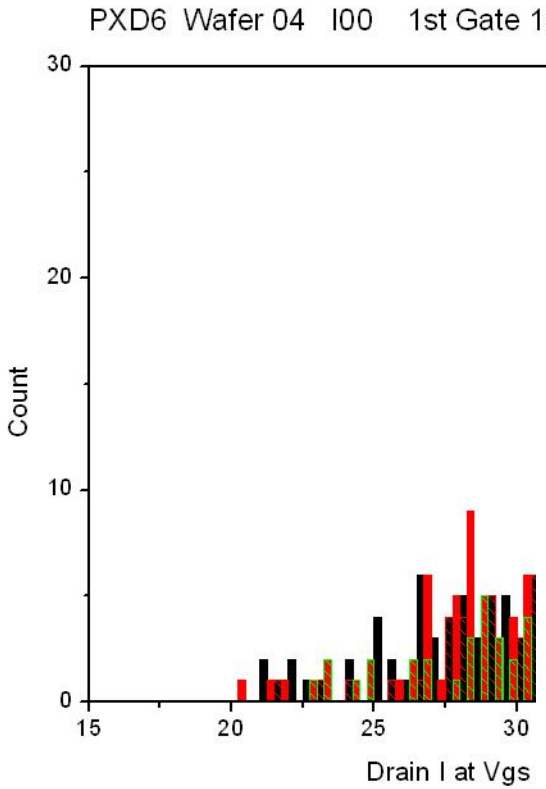
Sheet resistance 300Ohm/sq.
(3x lower than in the old technology due to better implant activation)

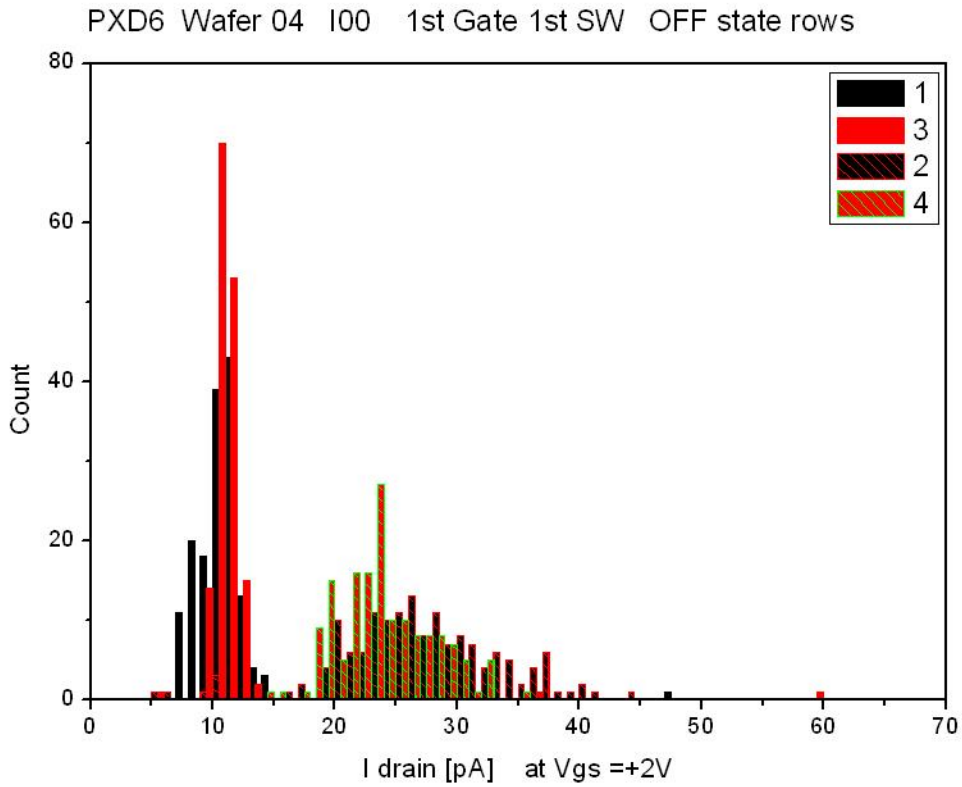
Estimation: @Id=80µA, gm=50µS

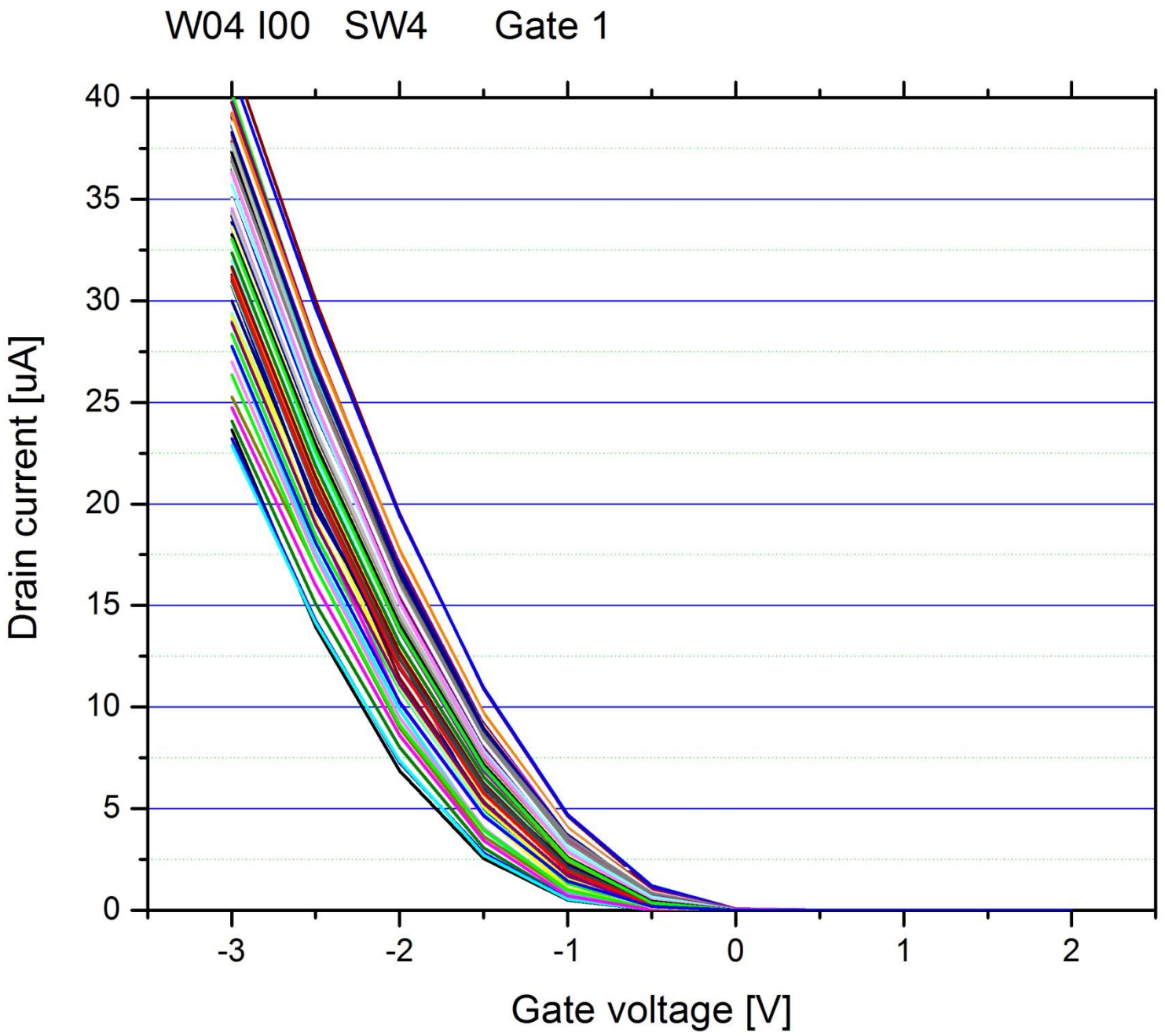
-> $\Delta I \approx 4\mu A$

We will see an odd-even behavior but no change with radiation


PXD6 Wafer 04 I00 1Gate 1 SW Id @ Vgs= +2V OFF state [pA]
rows
rows
columns
4
3
2
1
20
40
60
80
100
120
140
160
180
0.000
5.000
10.00
15.00
20.00
25.00
30.00
35.00
40.00
45.00
50.00


PXD6 Wafer 04 I00 1st Gate 1st SW ON state rows
1
Count
Drain I at Vgs
0
10
20
30
15
20
25
30


PXD6 Wafer 04 I00 1st Gate 1st SW OFF state rows
1
3
2
4
Count
I drain [pA] at Vgs =+2V
0
20
40
60
80
0
10
20
30
40
50
60
70


W04 I00 SW4 Gate 1
Drain current [uA]
40
35
30
25
20
15
10
5
0
-3
-2
-1
0
1
2
Gate voltage [V]