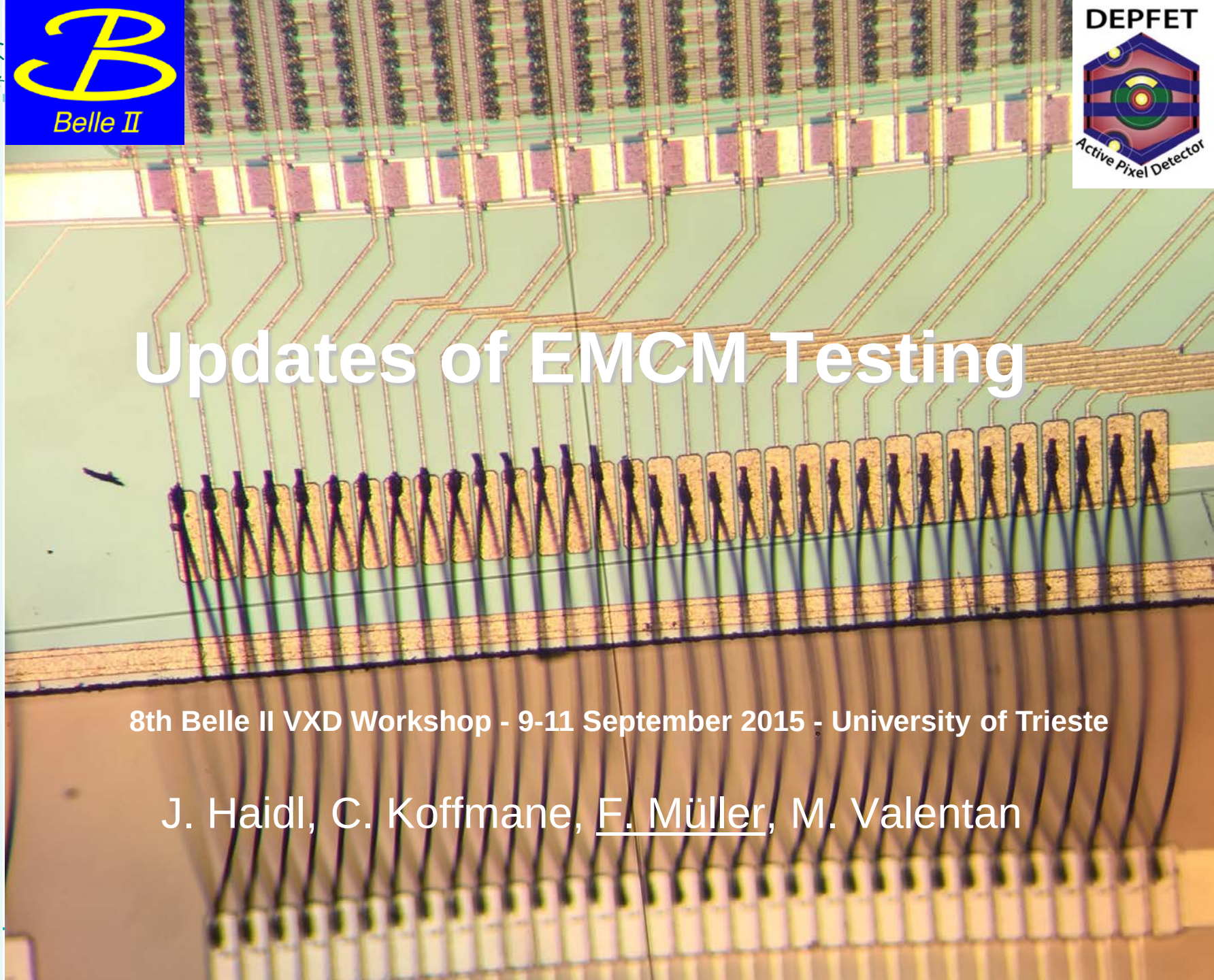
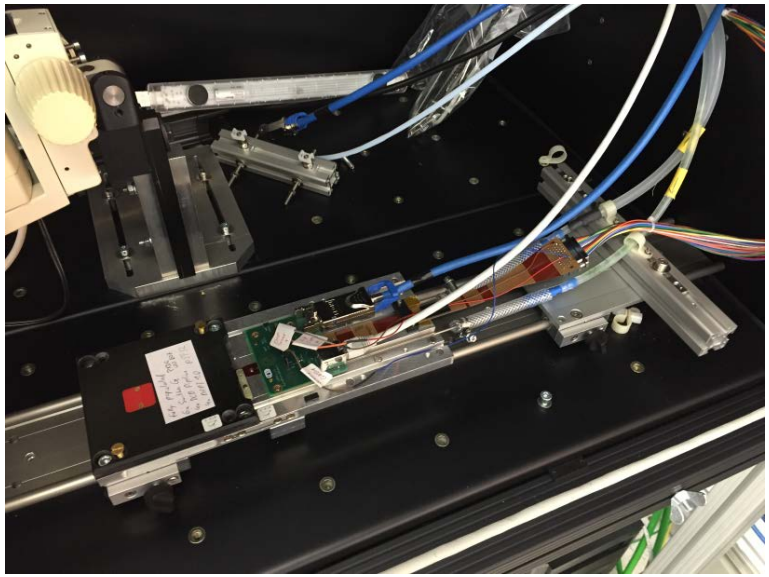


Updates of EMCM Testing

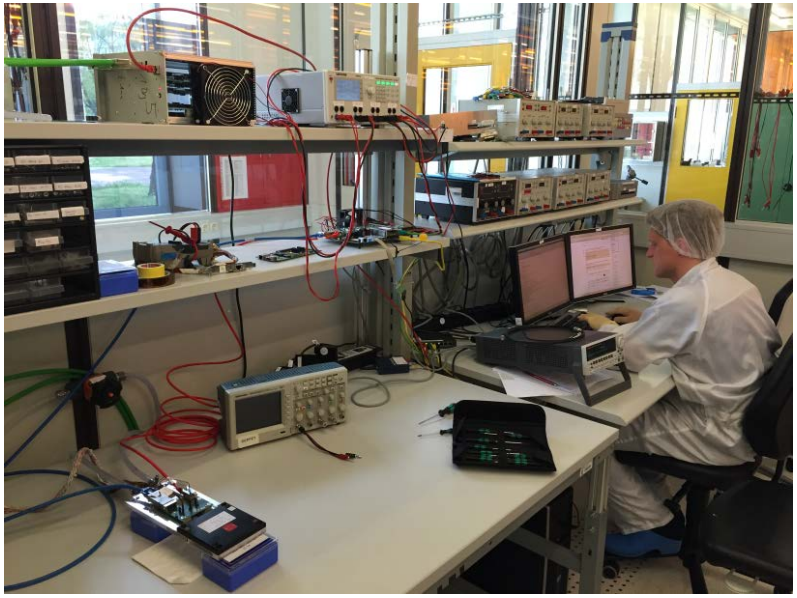
8th Belle II VXD Workshop - 9-11 September 2015 - University of Trieste

J. Haidl, C. Koffmane, F. Müller, M. Valentan

Setups in HLL

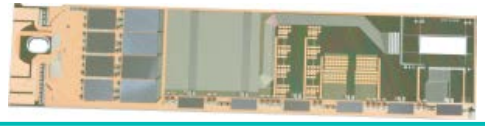


EMCM Setup (pxdtest2)



EMCM Setup (pxdtest3)

Probecard Setup



Overview of EMCMs

Fully populated, i.e. 4x DHPT1.0, 4xDCDpp, 6x SwitcherB18v2

existing (DHPT & DCDpp)

- W17-3 (problems with cooling (jig)) => damaged
- W18-3 (matrix attached)

irradiated:

- W31-3

new:

- W18-4
- W31-4 (will move to TUM)

More details: => Database www.hephy.at/hephydb

Please use the database

Software

Goal for all setups:

- Common operating system
  - All PCs are running with Scientific Linux 6.x (Bonn, Göttingen, HLL, MPP, (TUM))
- Common folder structure (~/cs-studio ~/epics ~/system-config ….)
  - Installation script: system-installation and system-configuration – settings for own PC can be easily set in an ini-file
  - svn: https://belle2.cc.kek.jp/svn/groups/pxdonline/epics/trunk/pxd-testsetup/system-config
- Common connections (PS, DHE) – 1 PC for 1 setup
  - 2 Network cards (Internet & Setup (SlowControl DHE,PS, HS-link)
- Common Software / Measurements & Analysis
  - Python environment
  - svn: https://belle2.cc.kek.jp/svn/groups/pxdonline/epics/trunk/css/analysis
  - svn: https://belle2.cc.kek.jp/svn/groups/pxdonline/epics/trunk/css/dhh)
- Keep track of devices (which device is used in which setup)
  - DataBase http://www.hephy.at/hephydb
- Issue Tracker (common discussions, bug report, information etc.)
  - https://belle2.cc.kek.jp/redmine/projects/pxdhardware

Software Organization

Elog Server (digital log book): http://elog.mpp.mpg.de/DEPFET/

Account: valentan@mpp.mpg.de

Database (components & transfers/shipping tracking): http://www.hephy.at/hephydb

Account: valentan@mpp.mpg.de

Depfet Twiki

Account: http://twiki.hll.mpg.de/bin/view/TWiki/TWikiRegistration

Redmine (Issue Tracker FAQ, Bug report, information, etc.)
https://belle2.cc.kek.jp/redmine/projects/pxdhardware

Account: KEK Twiki Account, see https://belle2.cc.kek.jp/~twiki/bin/view/TWiki/TWikiRegistration (use standard BelleII username and password)

SVN Repositories:

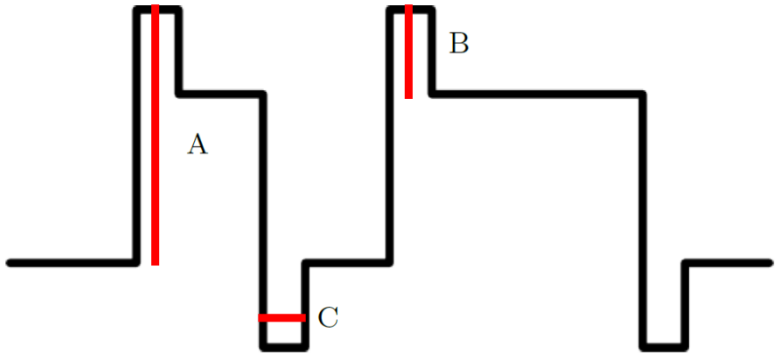
https://belle2.cc.kek.jp/svn/groups/pxdonline

Account: Same as for Redmine / Read-Only: standard BelleII username and password

Data Server (Measurements) – work in progress => MPP

Aurora Scan (1)

Data of the Sensor (DCD) is transferred via 1.6GBit/s links. The data is transmitted using the Xilinx Aurora protocol.



A: idac_cml_tx_**bias**

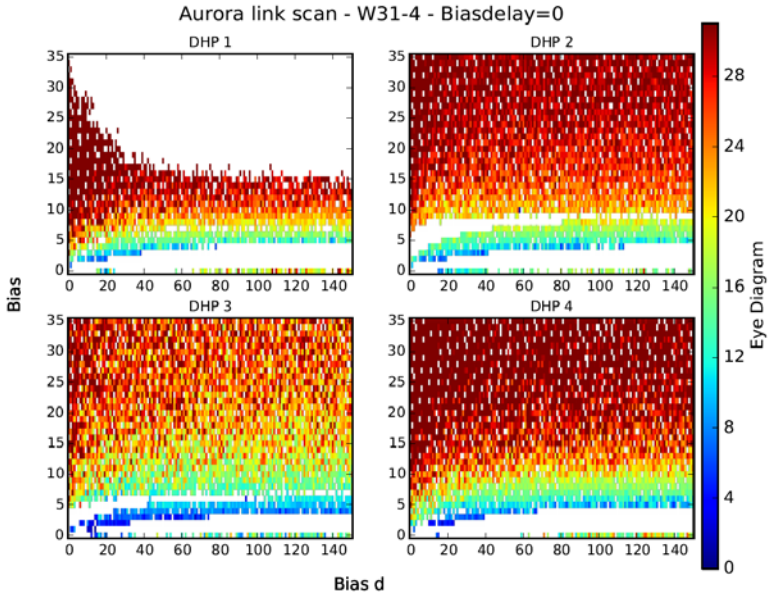
B: idaC_cml_tx_**bias_d**

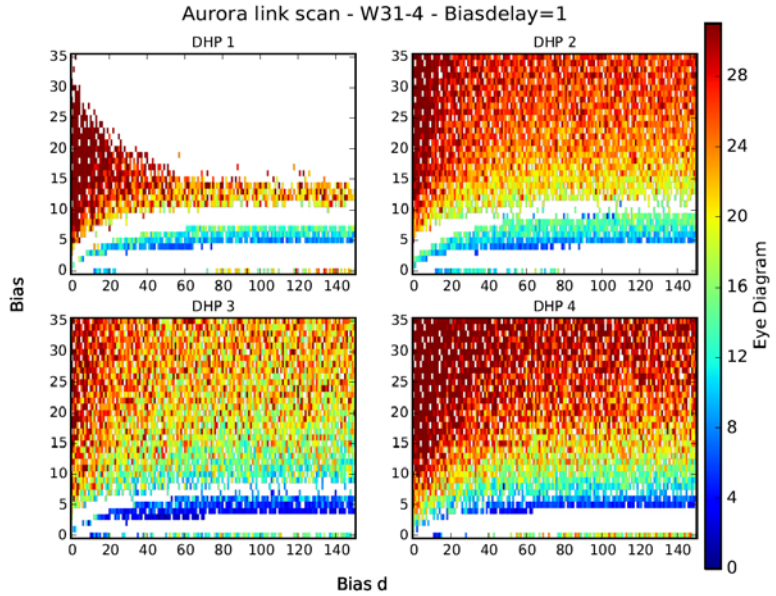
C: pll_cml_**dly**_sel

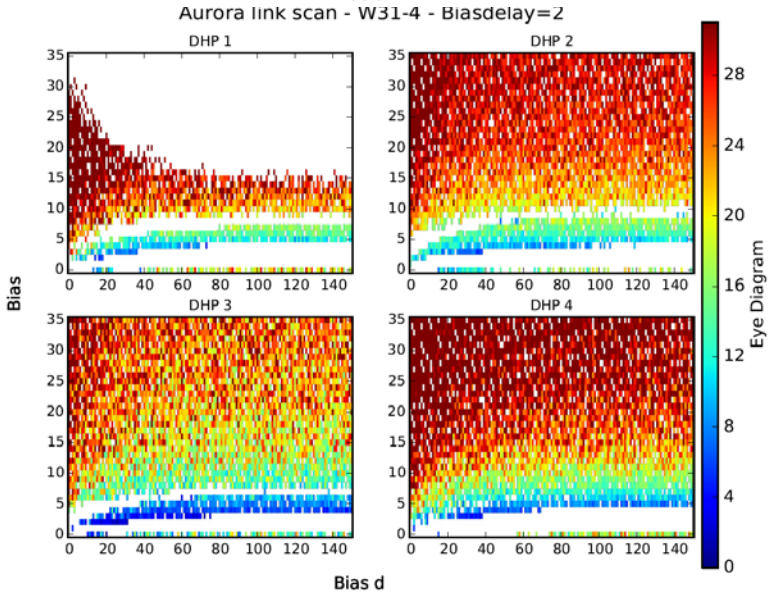
The pre emphasis is needed to compensate the attenuation of the high frequency component lost during data transmission.

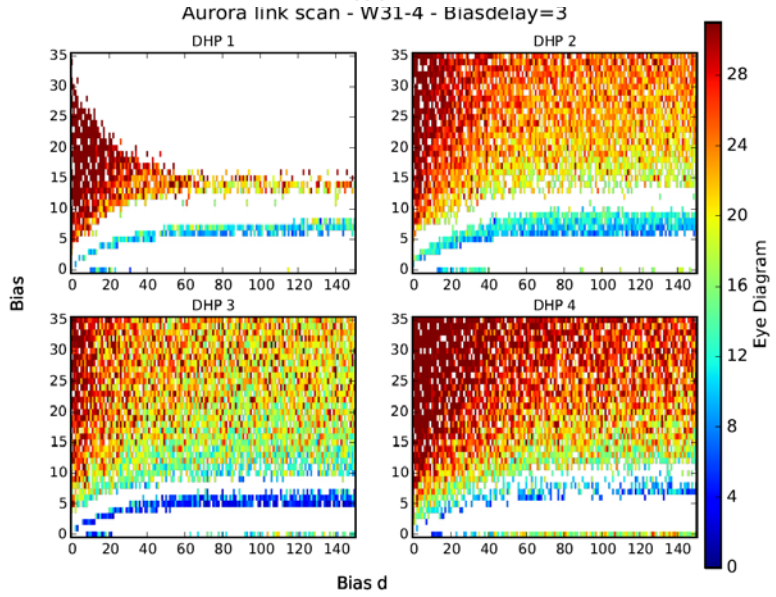
Aurora Scan (2) – W31-4 – Half Rate – pxdtest2

~/cs-studio/analysis/aurora_optimization/aurora_analyze.py

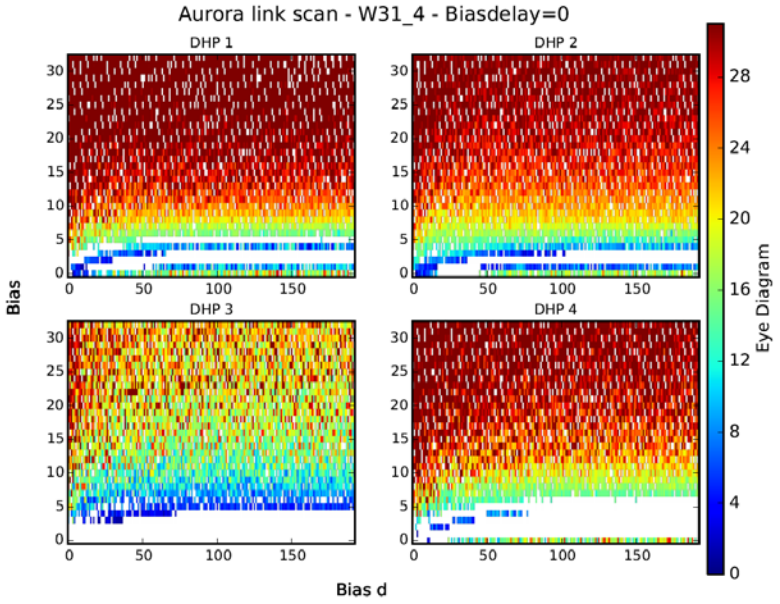


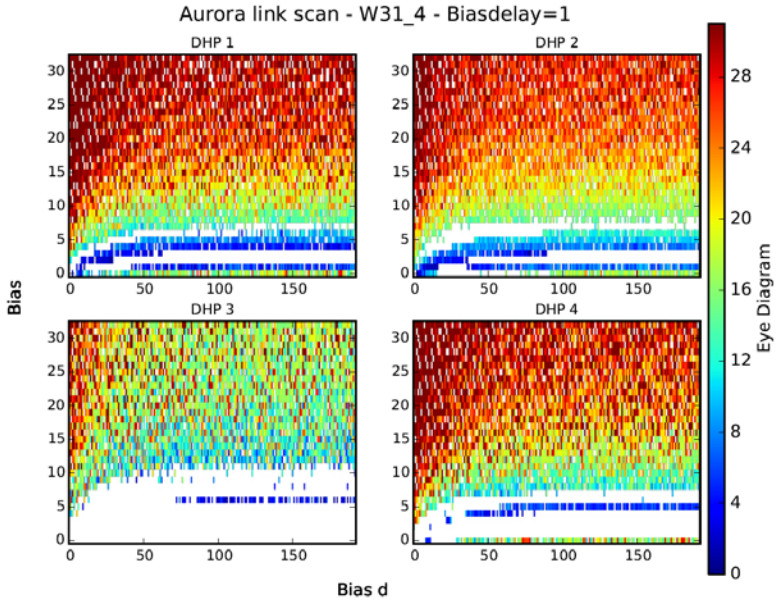


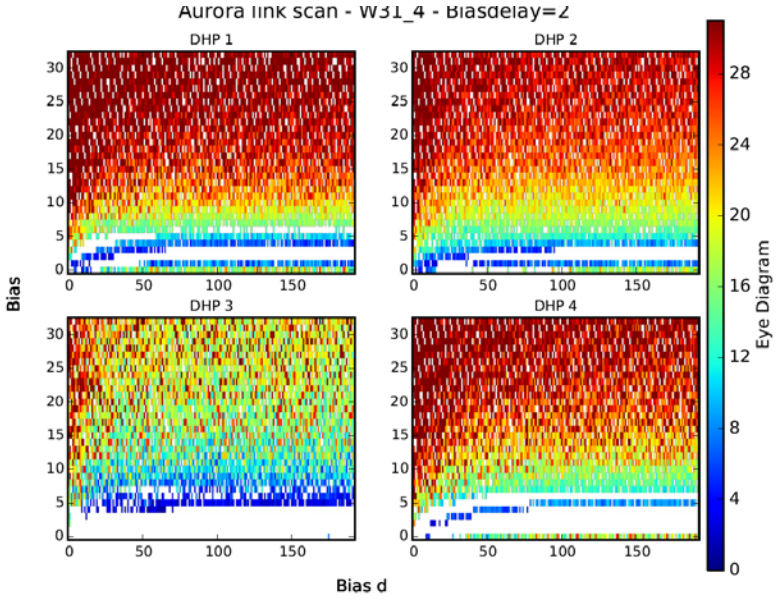


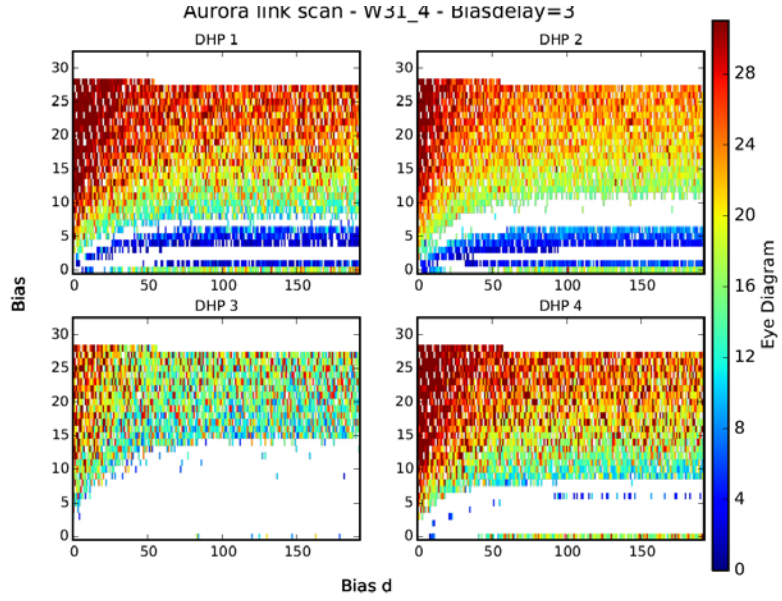


Aurora Scan (2) – W31-4 – Half Rate – pxdtest3



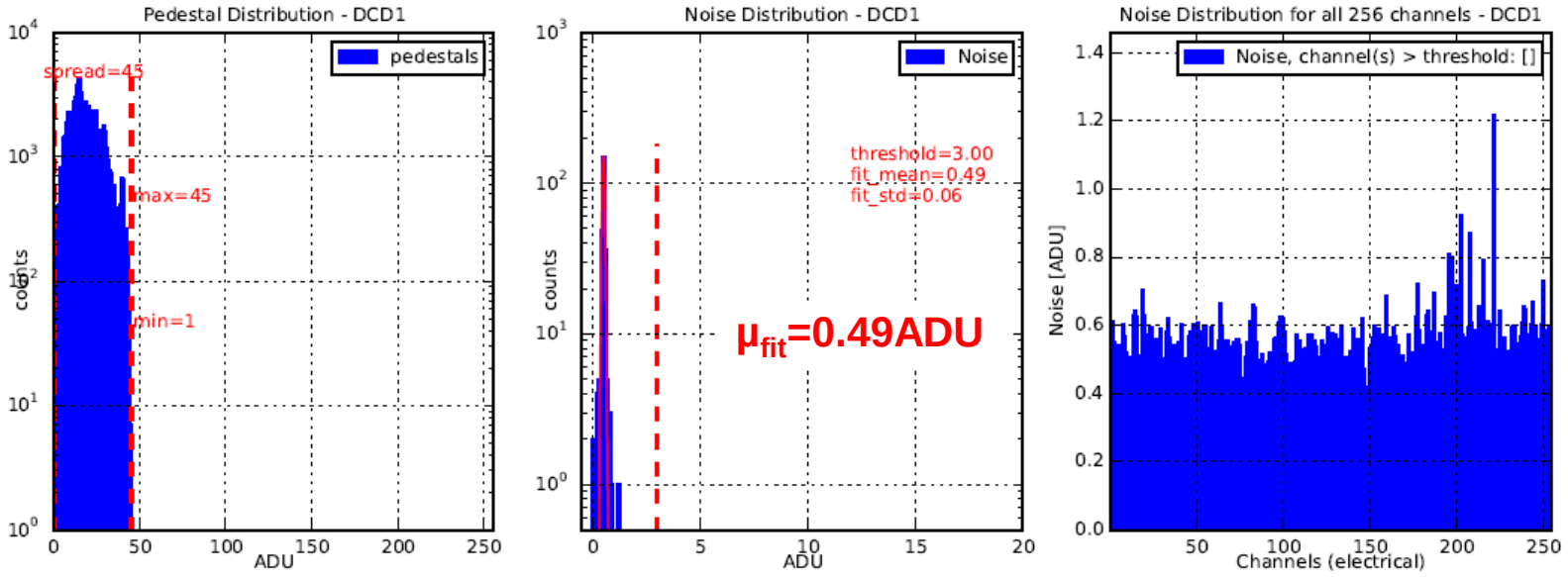




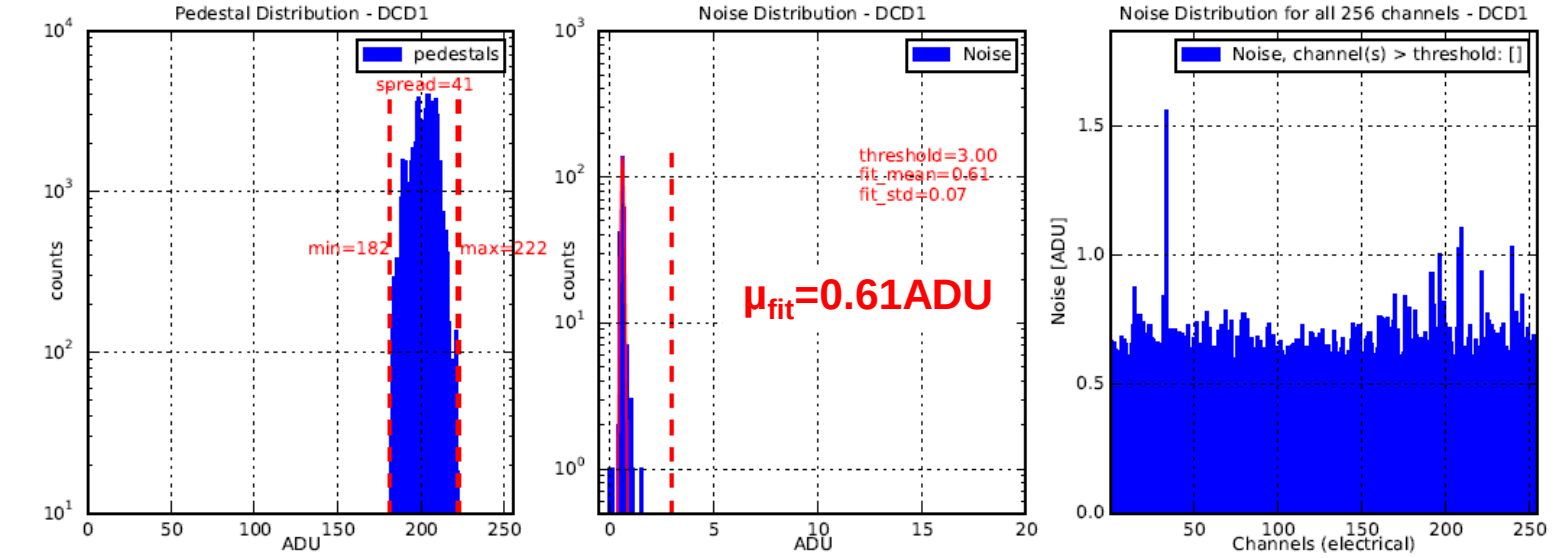


~/cs-studio/analysis/aurora_optimization/aurora_analyze.py

Noise measurements

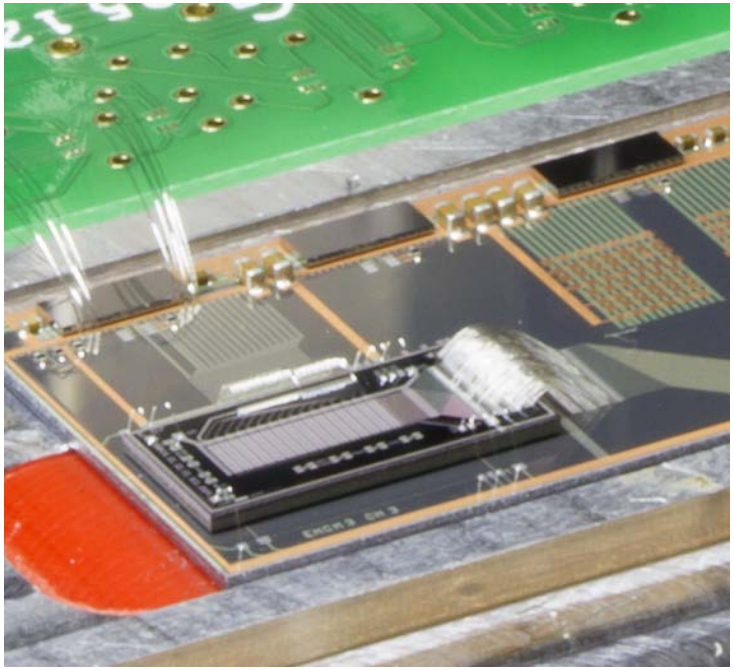


W31-3



~/cs-studio/analysis/plot_rawframe_data.py

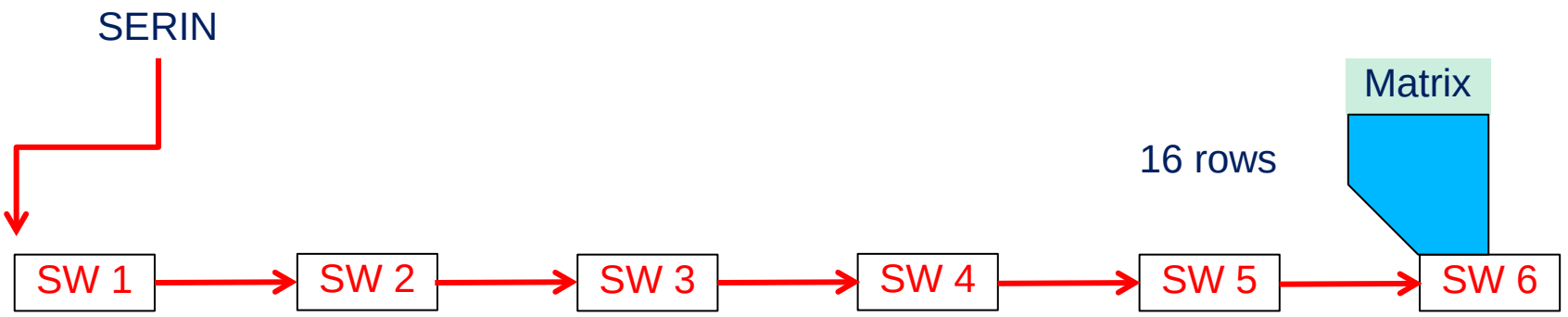
Matrix



EMCM W18-3

E07: ARR_128x16_ST_SD_SCG_Z075_TS
128 drains (electrical), 16 row (electrical), no capacitive coupled Cleargate, surrounding Cleargate, 75µm pixel size, Type save (referred to the p+ implant around the clear), 6µm gate length

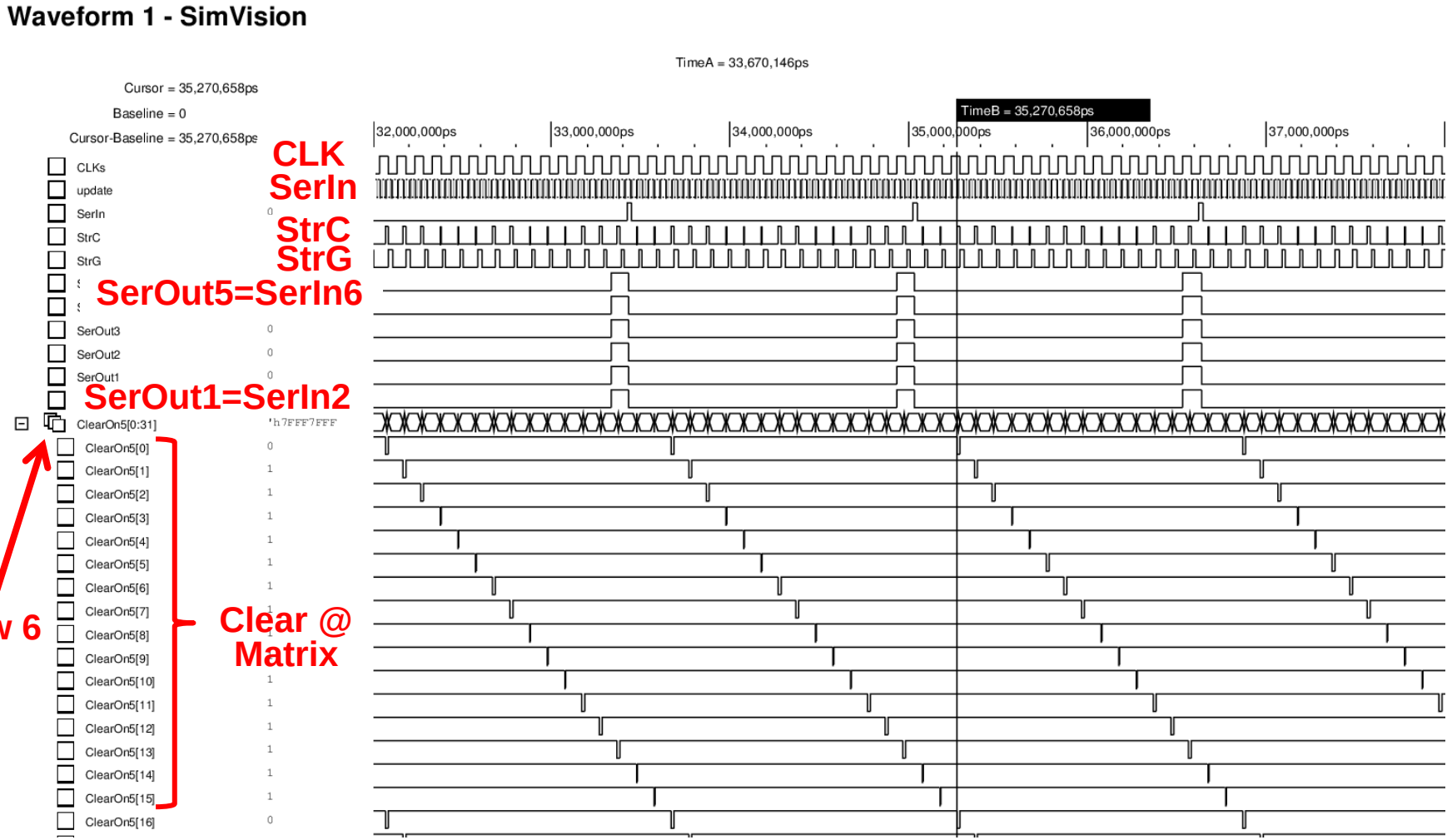
Switcher Sequence on EMCM



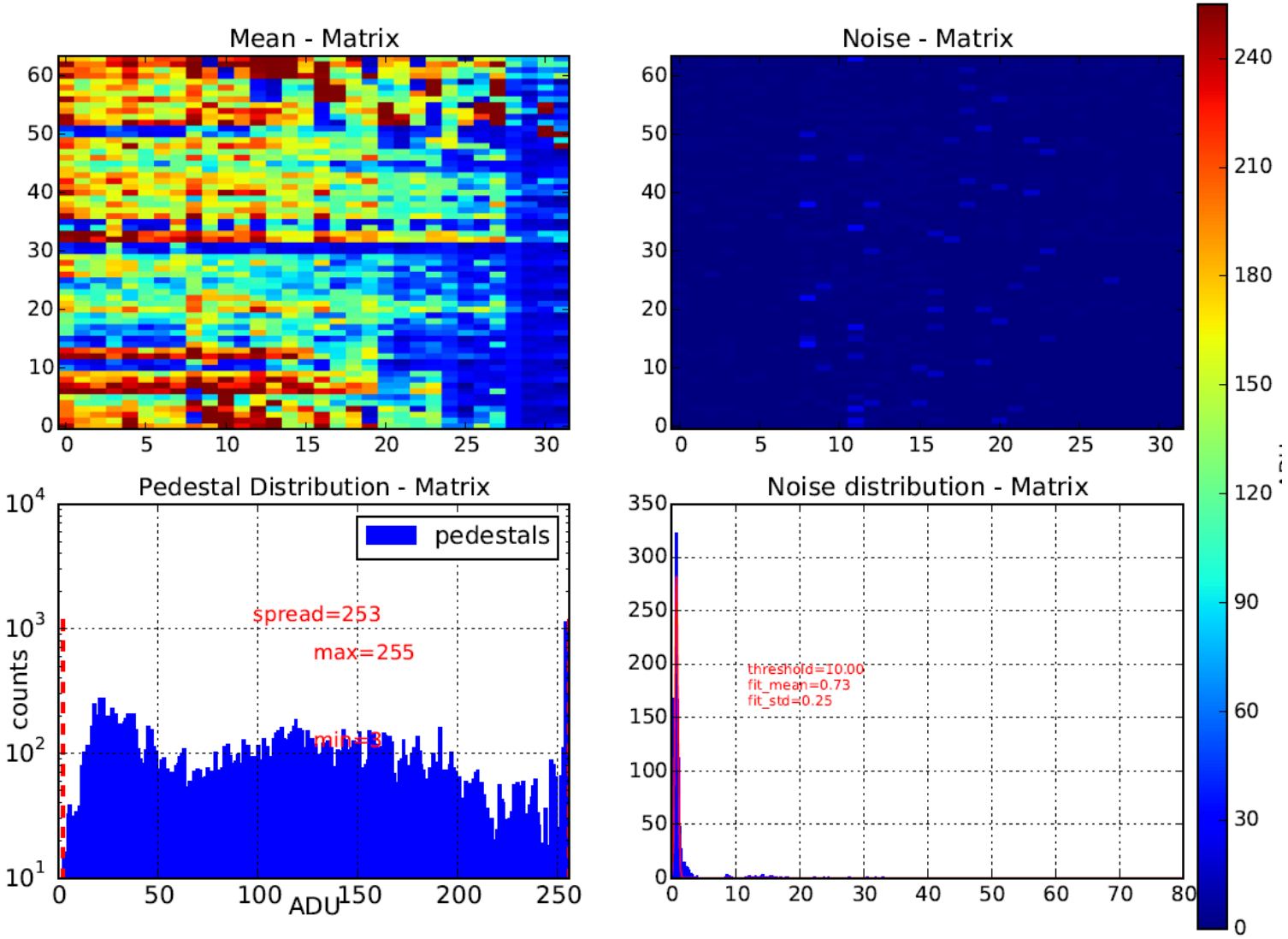
Matrix should be readout consecutively, i.e. 12 times within 192 rows in order to provide the DCD an input current

Switcher Sequence

Simulation of Switcher Signals @ EMCM



Preliminary Matrix (64x32) results



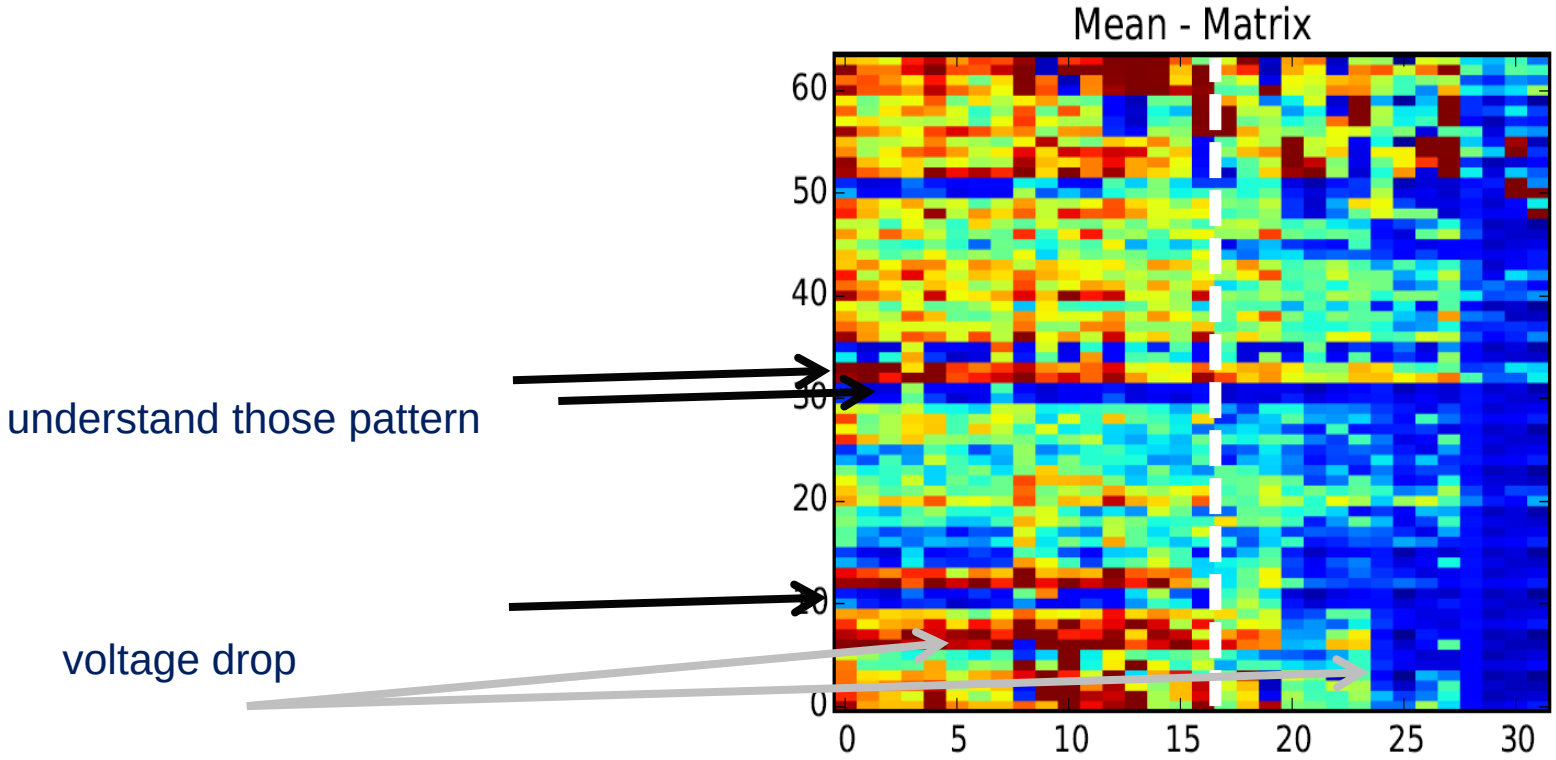
~/cs-studio/analysis/plot_rawframe_data.py -matrix

Preliminary Matrix (64x32) results

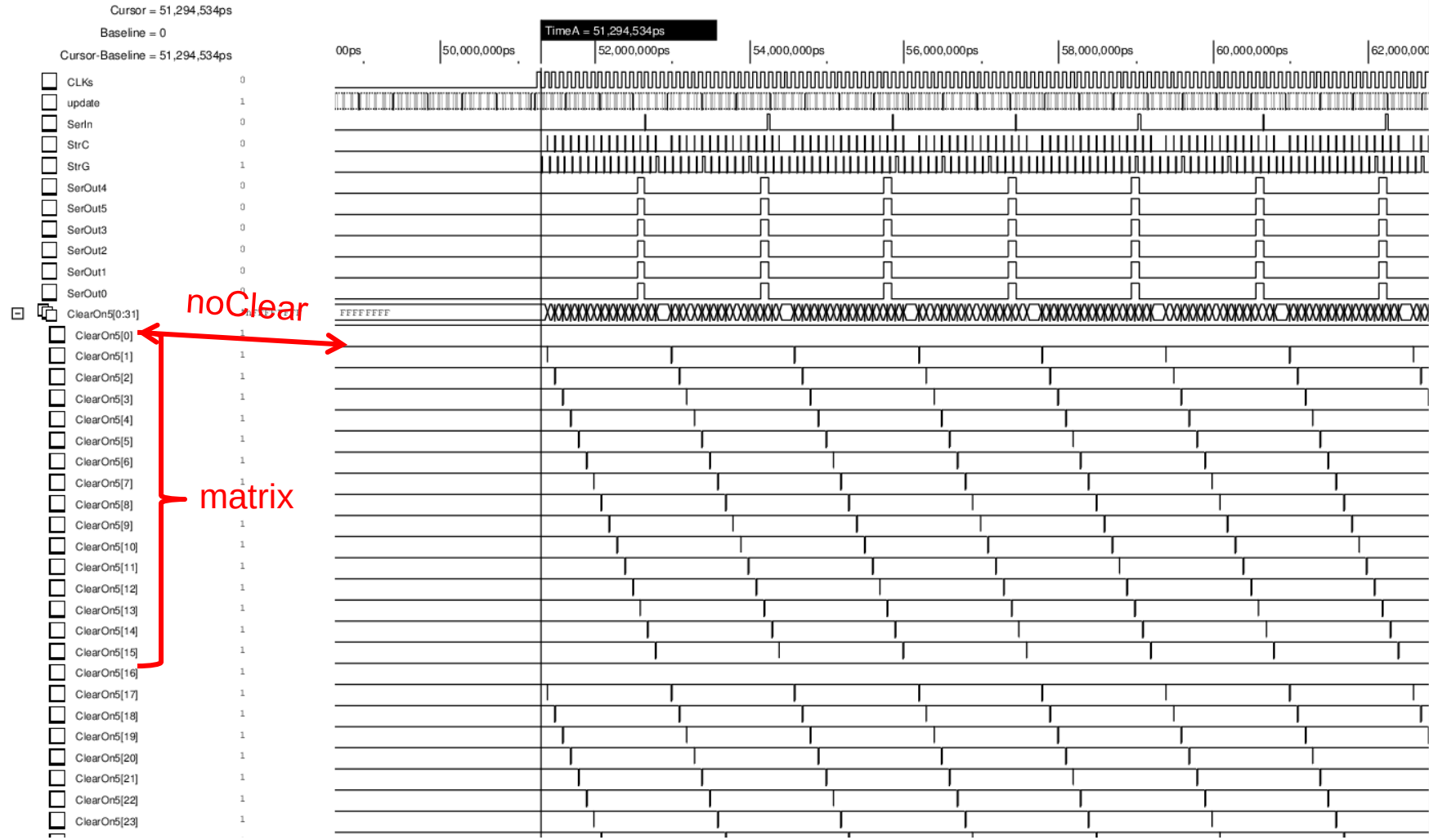
DCD			
Channels 0..63	Channels 63..127	Channels 128..191	Channels 191..255
	Hybrid 4.1		
		EMCM	

small matrix (64x32)

pixels has 16 rows, 128 drains (4-fold readout)



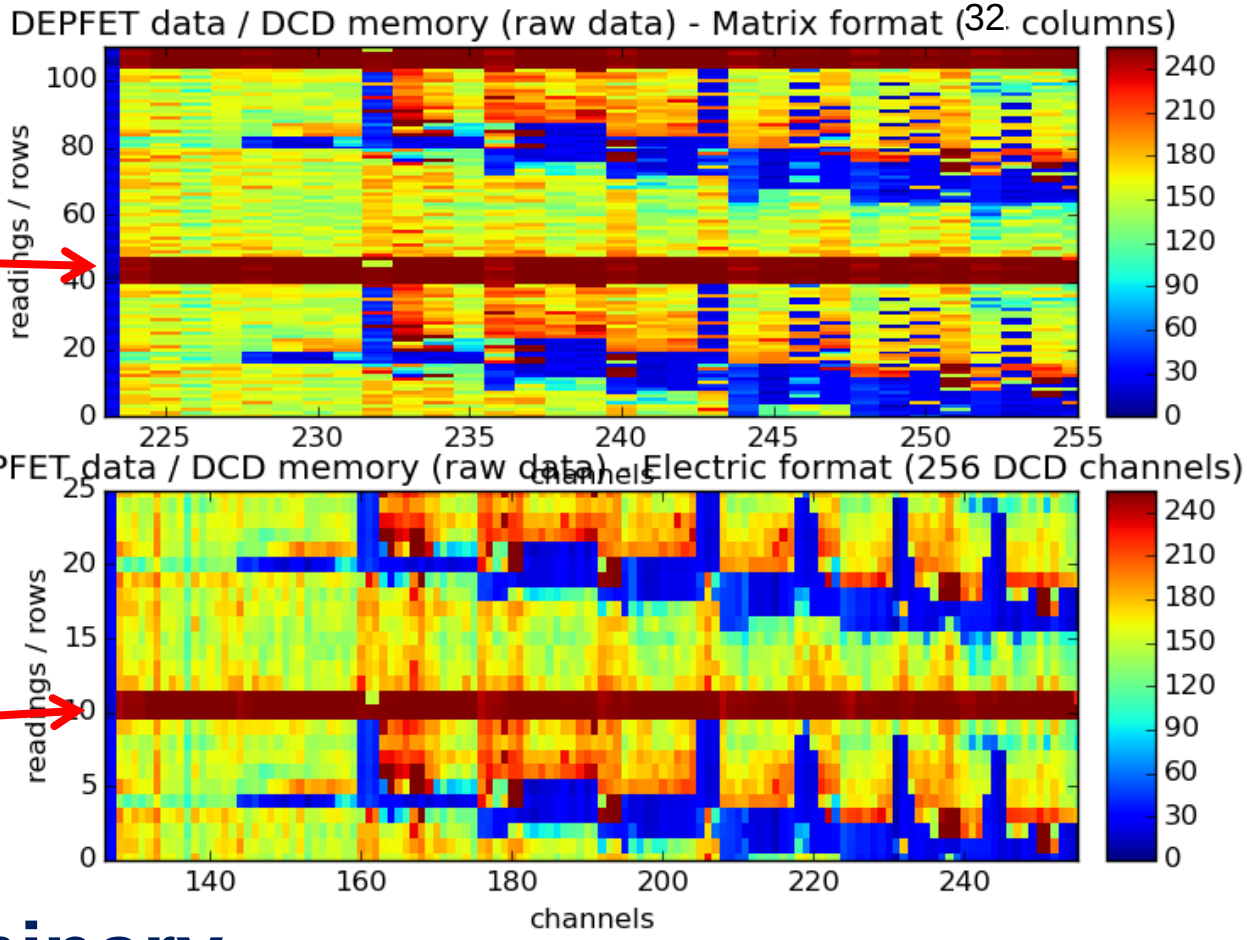
Switcher Sequence – row without clear



Consecutively Readout

Matrix is readout consecutively 12 times (frame readout time: **1,68µs**)

Switch off Clear in one row => DCD needs „recovery time“ (=> **+1**)



Row without clear **+ 1**

Row without clear **+ 1**

Preliminary

IPDAC (2bit Offset comp) & IPAddIn & VnSubIn

IPDAC is required to compensate the pedestal spread

IPDAC is set globally, 0x,1x,2x,3x is set for each pixel individually

- 0x IPDAC
- 1x IPDAC [0,60µA]
- 2x IPDAC [0,120µA]
- 3x IPDAC [0,180µA]

Cannot measure total strength of IPDAC (too strong, covers dynamic range multiple times)

Idea:

1) increase IPDAC to shift pedestals to the upper boundary (~250 ADU)

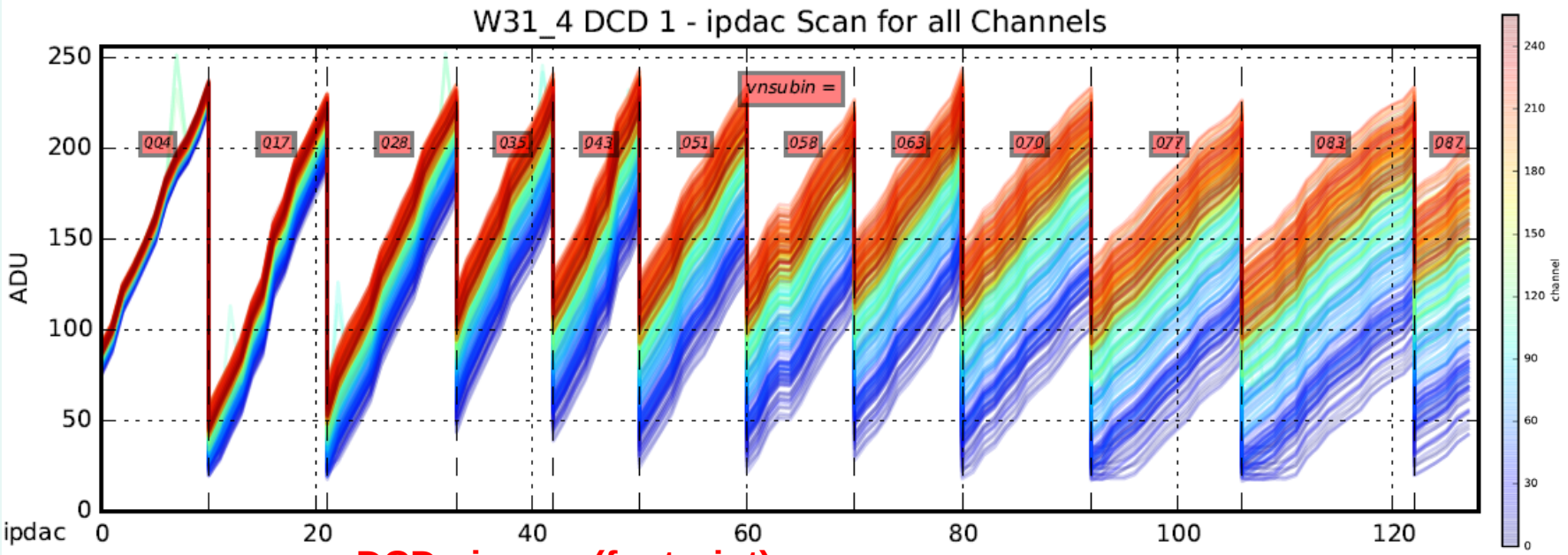
2) subtract current by increasing VNSubIn => pedestals will be shifted to (20ADU)

3) increase IPDAC to shift pedestals to upper boundary (~250ADU)

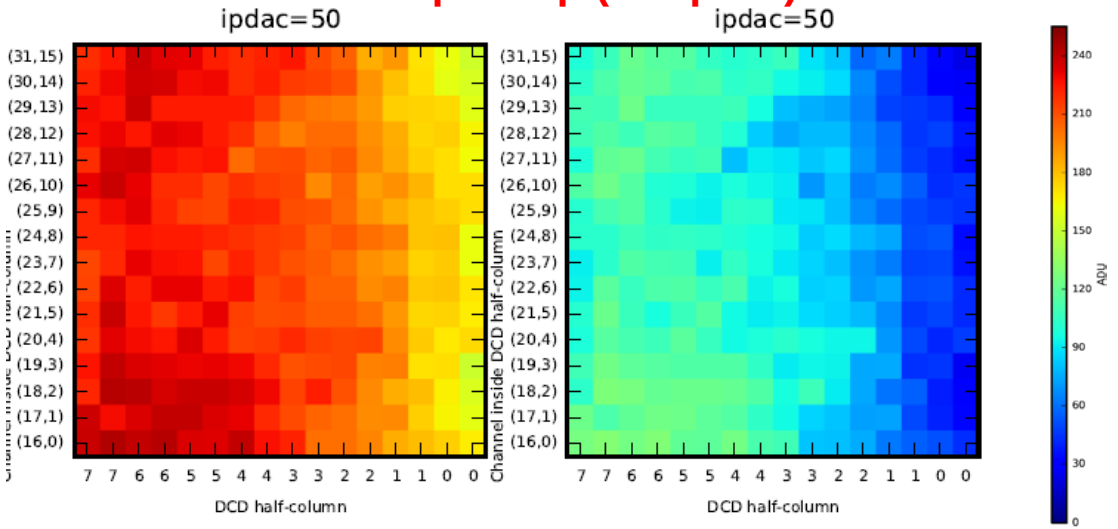
4) ….

IPDAC (2bit Offset comp) & IPAddIn & VnSubIn

~/cs-studio/analysis/cs_add_cs_sub/cs_add_cs_sub_analysis.py



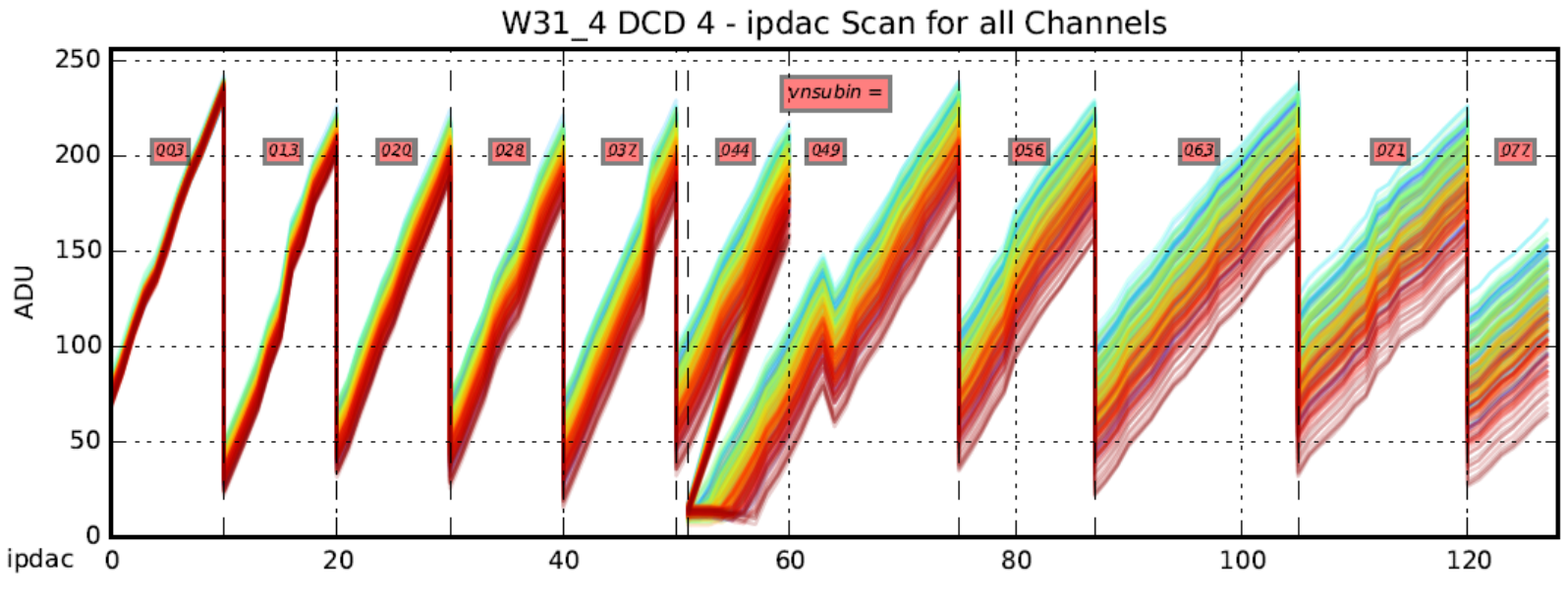
DCD pinmap (footprint)

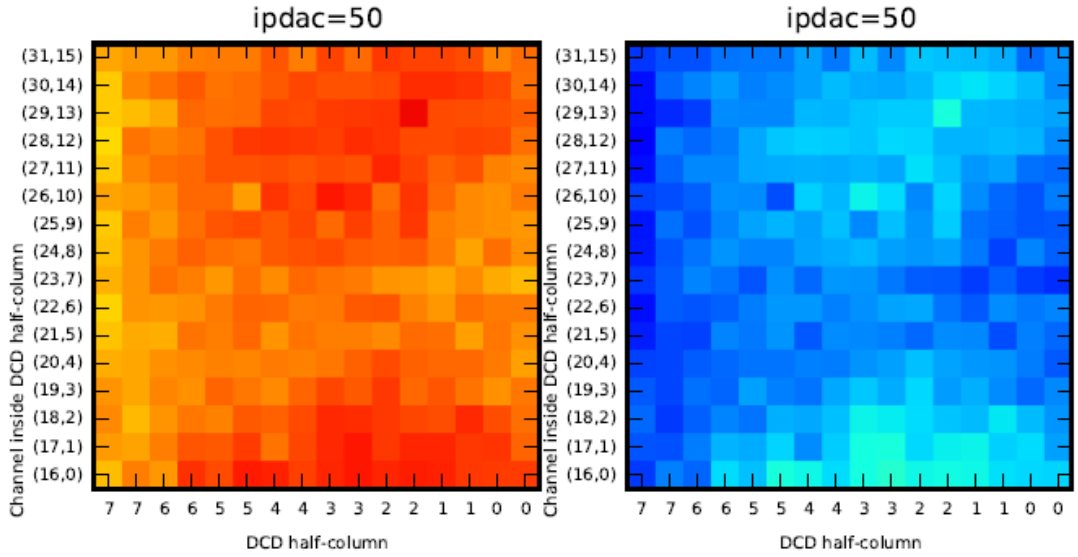


same behavior for IPDAC and IpAddIn

=> inhomogeneity in VNSubIn?

IPDAC (2bit Offset comp) & IPAddIn & VnSubIn

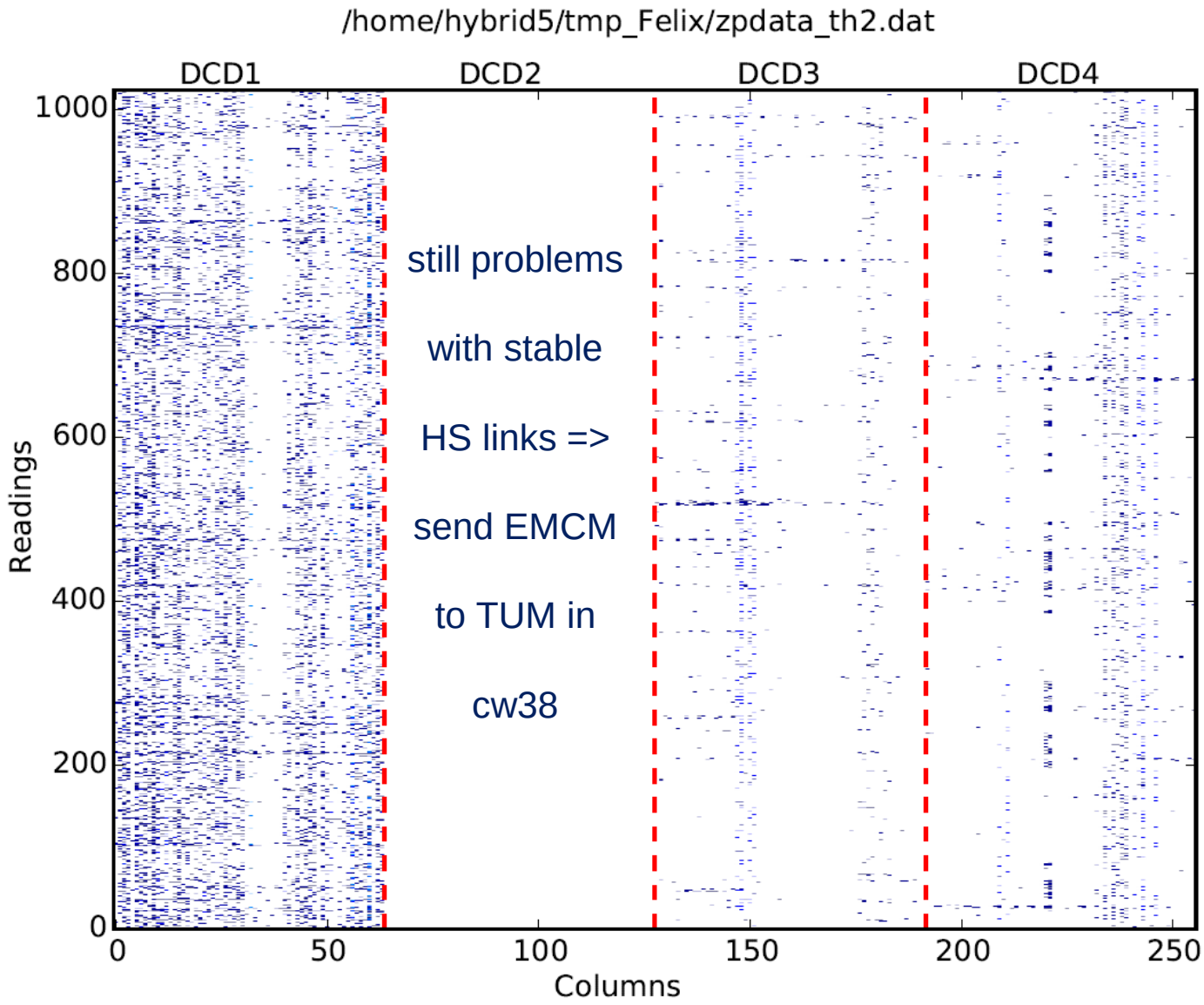




same behavior for IPDAC and IpAddIn => inhomogeneity in VNSubIn?

~/cs-studio/analysis/cs_add_cs_sub/cs_add_cs_sub_analysis.py

Zero Suppressed Readout



~/cs-studio/analysis/plot_zpframe_data.py

Outlook

Python:

Docstrings => Overview of existing functions, Create Overview

Optimize operation of matrix assembled on EMCM

DCDpp analogue common mode correction

Investigation of HS links (run 4 simultaneously)

Gated Mode Tests

Priority list:

https://docs.google.com/spreadsheets/d/1DINTXRg-sDK_V4NK_XbjK-bkuMY83rB6lhIniHfkV8A/edit#gid=1499142854

Expect Pilot runs (PXD9 & ASICs) mid of September

https://docs.google.com/spreadsheets/d/155aSvn3mvLV5qWFrh0GnLXhELrkM1Mf4Xqo_J7SGIs0/edit#gid=928068883