

# DHE, Back-end Electronics

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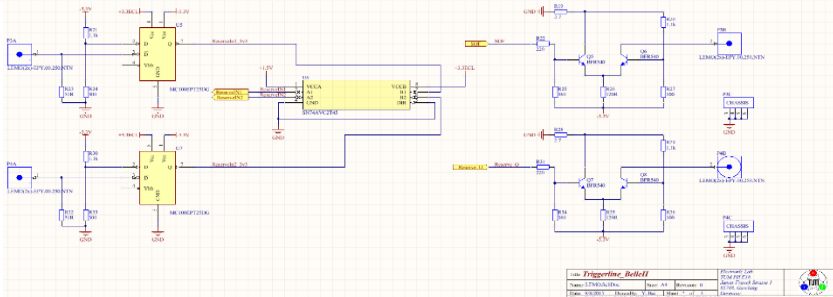


# Gated Mode Test Preparation

Firmware and software

Hardware and Test

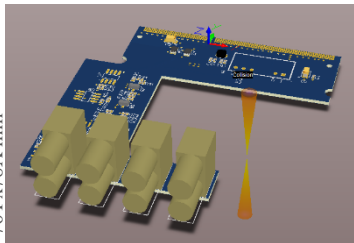
Summary

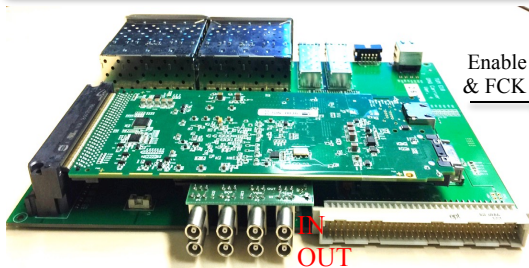


## LEMO Connector

- 4 input, 4 output
- NIM standard, 16mA 50 Ohm terminated
- 0V means logic 0
- -0.8V means logic 1

76Yx78X mm





## Memory Configuration

Trg Strobe	Trg	Veto	Laser
x	x	x	x
x	x	x	x
x	x	x	x
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮

⋮  
DHH

⋮  
DHPT

⋮  
Laser Control

## Sequencer Memory Block

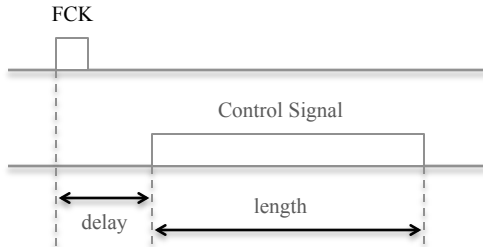
- Start signal from Lemo connector/TLU/IPbus
- x sequences configured via IPbus
- Trig, veto directly to DHPT
- Laser signal output via Lemo for controlling
- Further detail have to be discussed

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## 1. Configurable control signal for DHPT

- Memory dump, Veto, Trigger synchronized to FCK before Manchester encoding
- All signals have configurable delay and length
- Configured via IPbus

## 1. Firmware

- **DDR3 Memory has been included in the latest firmware version**

To buffer data before sending to UDP

For DHPT stress tests

- **Reading out of unique FPGA identifier (DNA, 56 bits)**

For DHH module identification

Accessible via IPbus, EPICS PVs

- **Dynamic reconfiguration of FPGA high speed serial link**

Switching of the DHPT data rate (full/half rate) without recompiling the FPGA program

Accessible via IPbus, EPICS PVs



## 2. Software

The functionality of the separate programs being moved to “devDHE” module (EPICS). The programs will not be maintained.

- Clock programming → PXD:H1032:clock\_frequency:set  
Possible value: 62.5Mhz, 65Mhz, 67.84Mhz, 71.2Mhz, 76.23Mhz, 127.21Mhz
- Software trigger  
Enable Software Trigger → PXD:H1032:ipbus\_trg\_en:S:set  
1 = activate; 0 = deactivate  
Set Frequency → PXD:H1032:trg\_ipbus\_freq:VALUE:set  
Set Trigger Number → PXD:H1032:nr\_of\_ipbus\_trg:VALUE:set  
0 = unlimited number of trigger  
Set Start Trigger Number → PXD:H1032:ipbus\_trg\_start\_nr:VALUE:set
- Data rate on DHPT → PXD:H1032:half\_rate:S:set  
0 = full rate; 1 = half rate



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## 1. Glenair 050-301-0X<sup>1</sup>

850nm, 100Mbps - 4.25Gbps

3.3V, 300mW Power consumption

Size 24x8x8 (mm)

TX (with blue stripe)



## 2. Avago AFBR-811FN1Z<sup>2</sup>

12 channels, 850nm, 10Gbps per channel

3.3V, 2.5V; 100mW per channel

Size 22x19x15 (mm)



	Glenair	Avago
Neutron	Passed	Passed
Gamma	Passed 230krad	Failed @ 90krad (approx. 9 years dose in Belle II)



- Meeting with Glenair on July 7-th

Change of package from wall mounted to cost efficient PCB mounted

Company has to integrate rad tolerant transmitters into new package

Delivery time is 11 weeks

TX (with blue stripe)



- Offer for 50 pcs + 20m of optical fiber cables: 50 k€
- Few details have to be clarified with company. We expect to order in 2 weeks.
- Repeat Gamma irradiation test



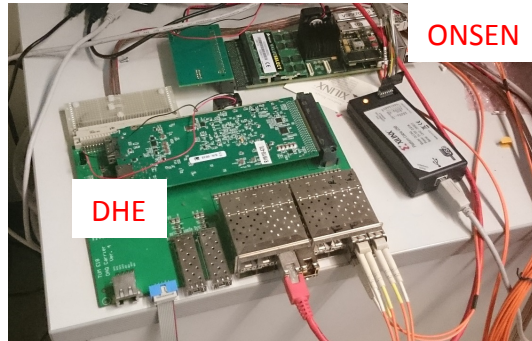
## Activity in June 2015

- DHC module was installed in Tsukuba hall with dedicated PC
- All components are integrated in DAQ environment
  - Ethernet access
  - IPbus
  - B2TT
- System is fully controllable remotely
- Still to be connected and tested with ONSEN





- 6 Gbps Aurora link works stably but still requires more reset attempts than 3Gbps => time out issues of Aurora protocol
- DHP/DHE/DHC data generator has been written to provide realistic system tests to check ONSEN data decoding and high rate event handling
- To be accomplished by end of September



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## New hardware for Gated mode ready

### Firmware

- Gated mode developed, details to be discussed
- FPGA DNA support
- Dynamic reconfiguration of FPGA

### Software

- Moving individual program functionality into EPICS
- Programming of the DHPT memory over EPICS array PV is under development

### Pocket DAQ Tests

- DHC has been installed in KEK
- Test of DHC – ONSSEN at TUM is in progress



Thank You for Your Attention!