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SuperKEKB Commissioning Detector
FANGS
Belle II Collaboration

FANGS

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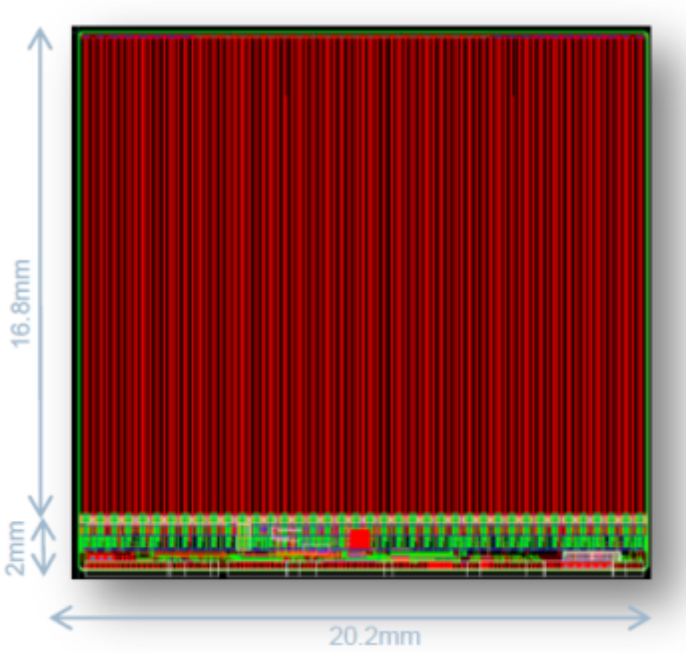
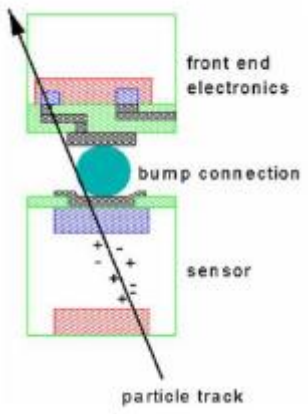
FANGS: FE-I4 ATLAS Near Gamma Sensors



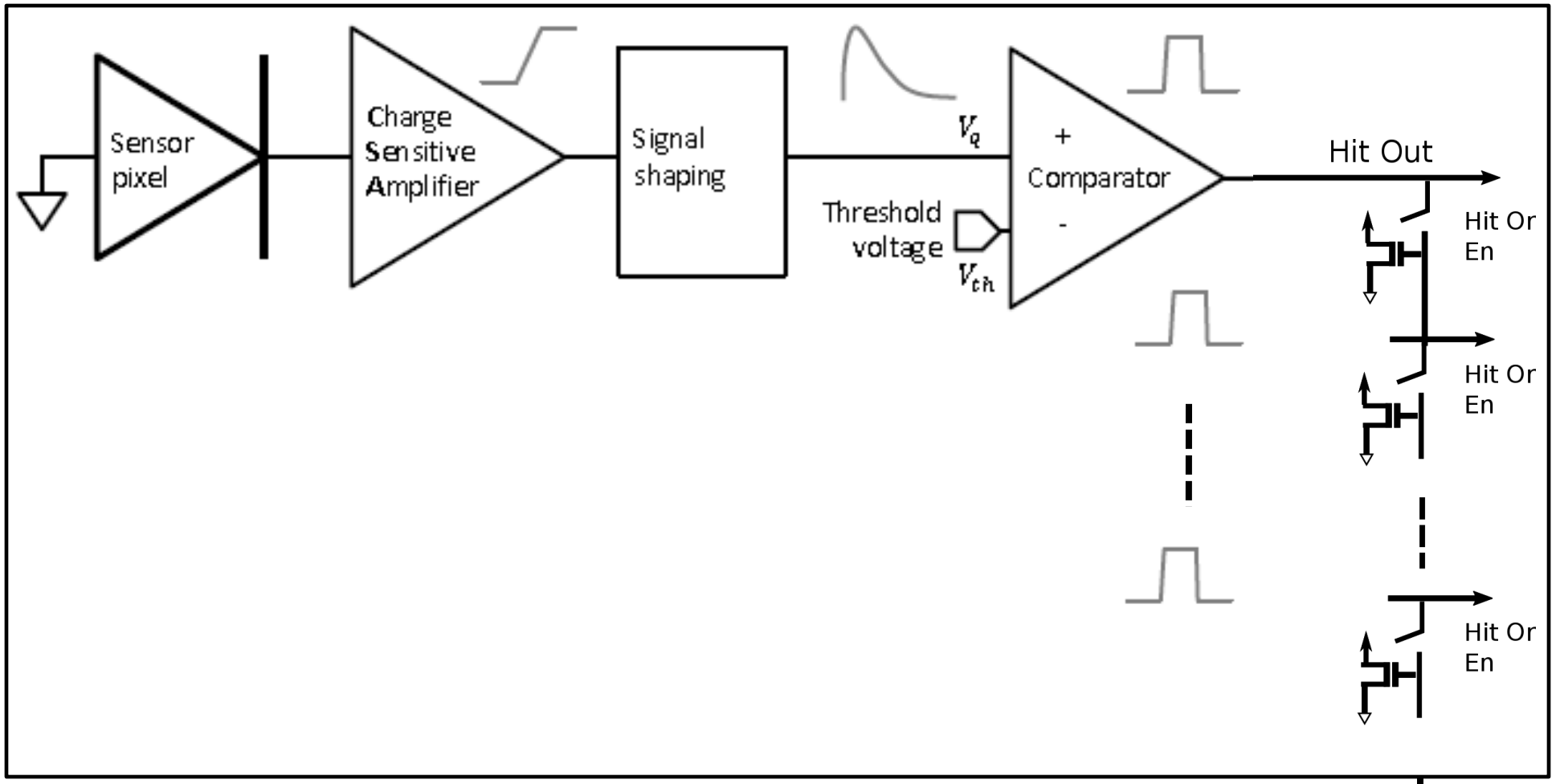


- FE-I4 read out chip:
  CMOS process: radiation hard
  Read out for 80x336 pixels (26880 pixels)
  Thickness : 150 µm
  Physical size : **21x19 mm²**

- Sensor:
  n-in-n planar
  Pitch=**50x250 µm²**
  Physical size=19x20 mm²

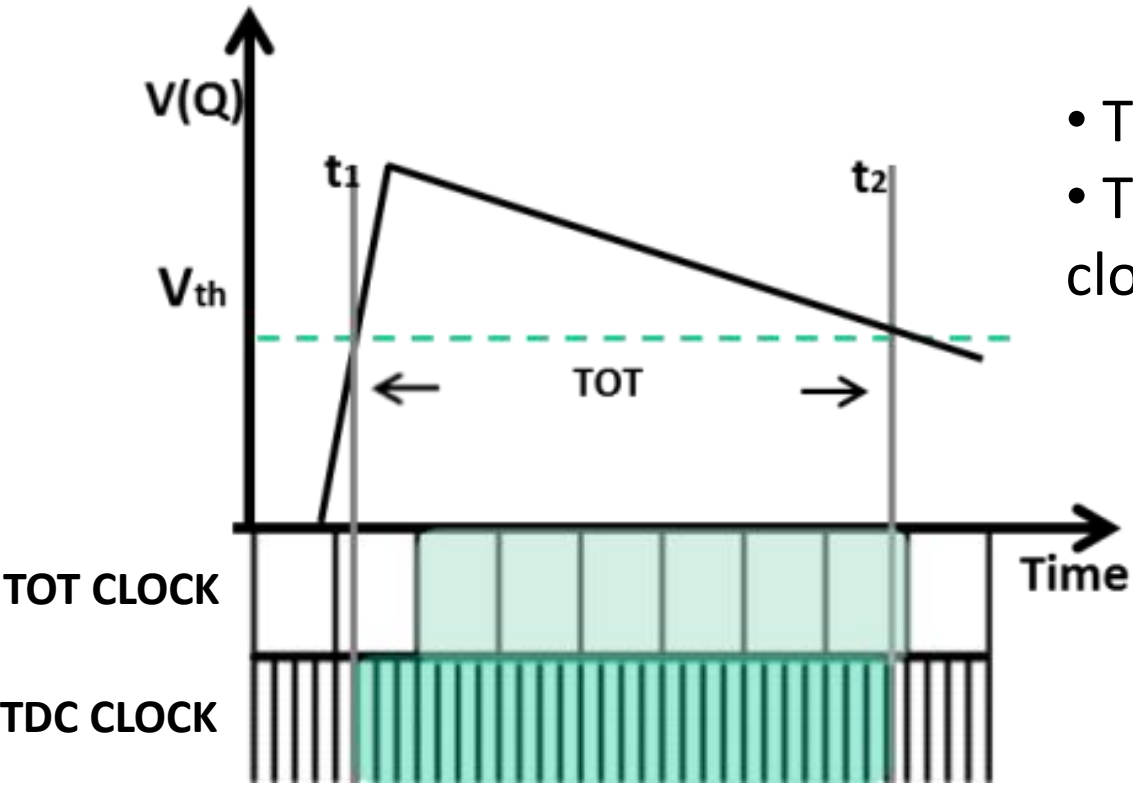
- **Background radiation measurements in Phase 2:**
  - Sensitive to full range of expected X rays
  - Measure high particle rates

Pixel Schematic



- Output for each pixel in ORed : Only highest fired pixel is read
- Hit Bus also used as self trigger

TDC Method



- TOT Method uses 40MHz clock:4 bit
- TDC Method uses FPGA's 640 MHz clock:16 bit

- Improved resolution
- Limited to one pixel per readout
- HitOr signal transmitted separately

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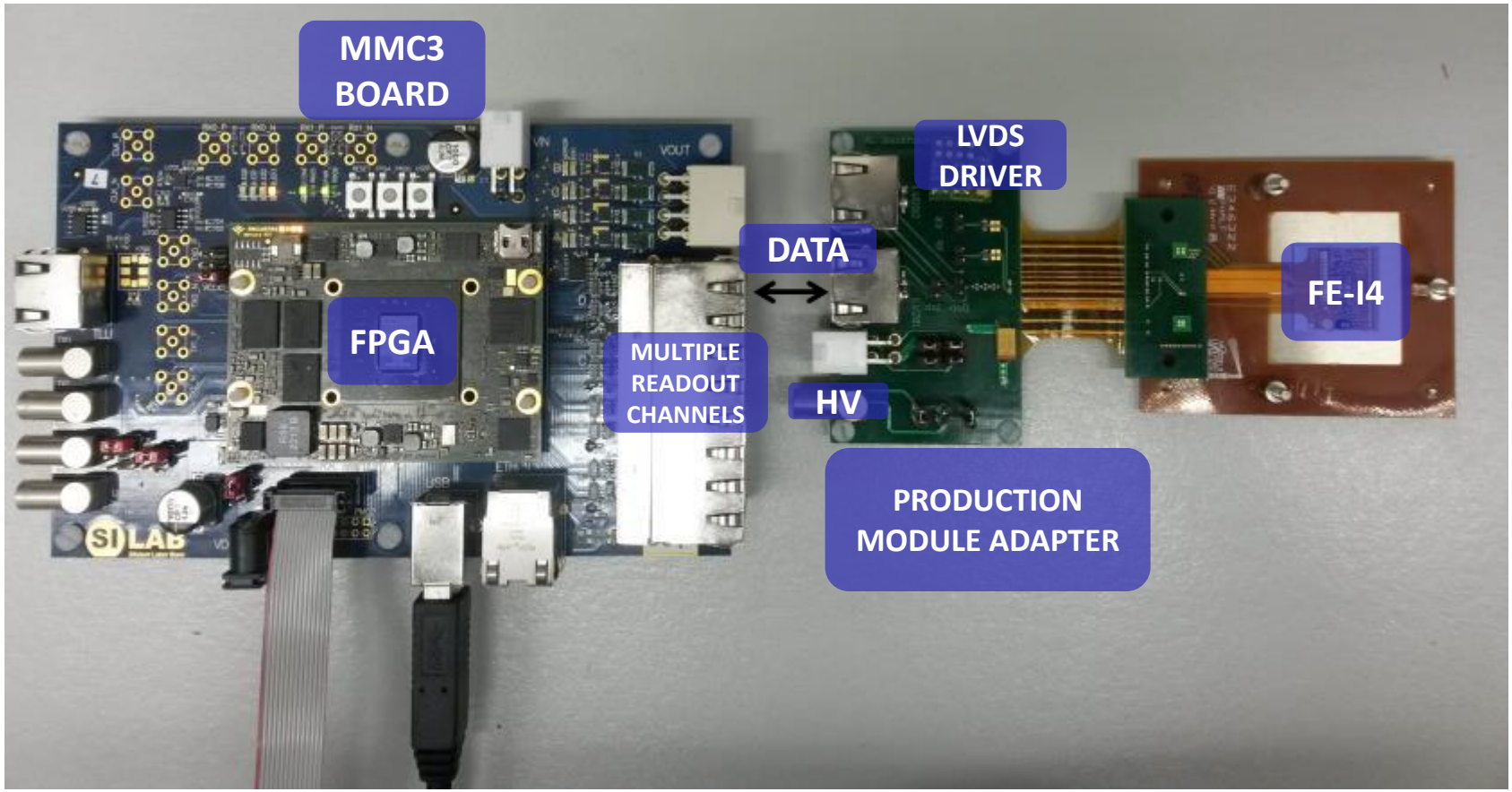
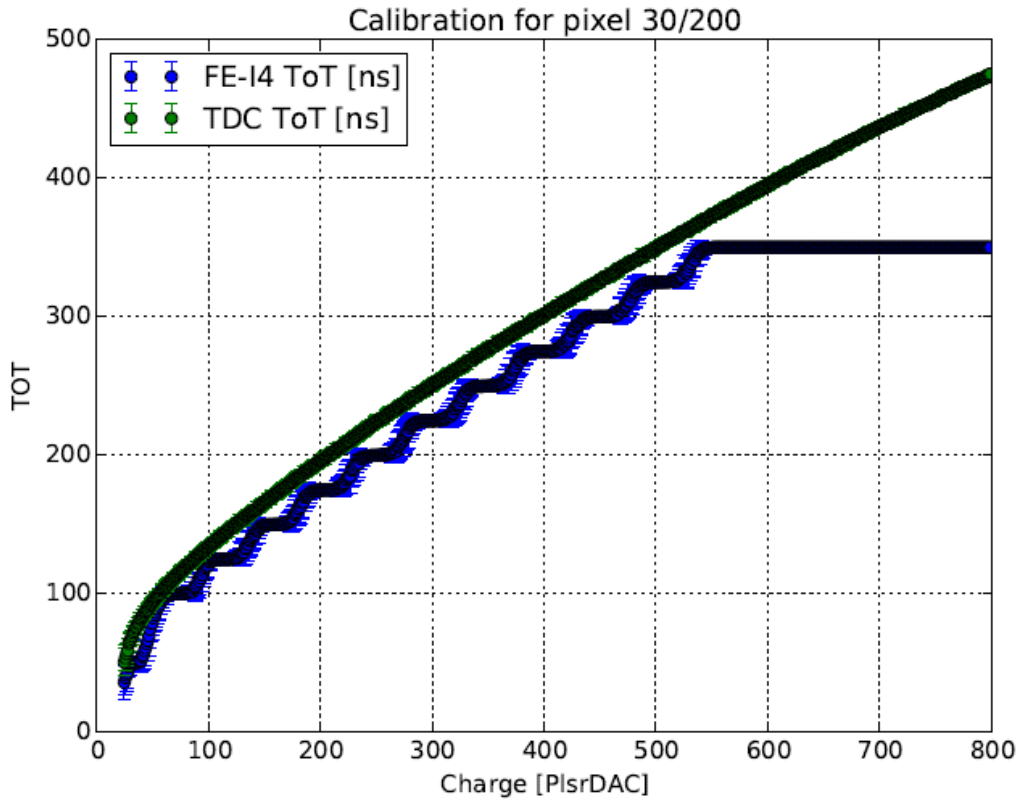
Experimental Setup



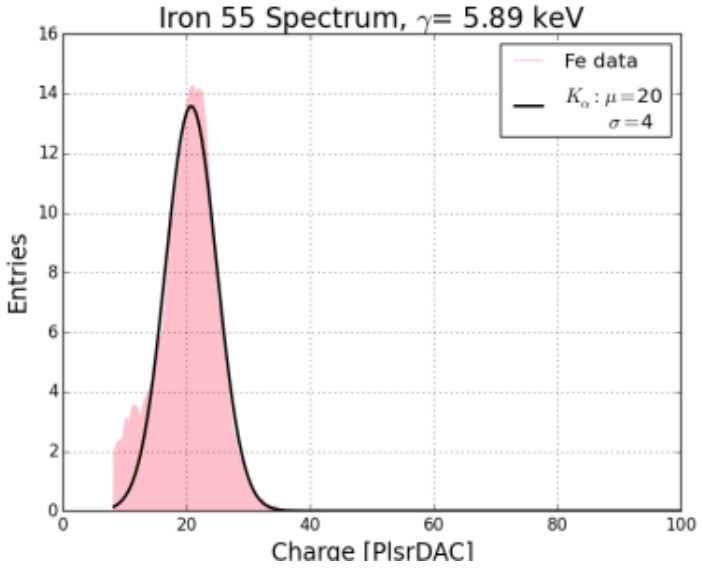
- MMC3: New data acquisition system for the BEAST experiment
  - Multiple FE read out in parallel
  - Faster FPGA; TDC Method may be improved
- Single ended HitOr signal converted to an LVDS signal.

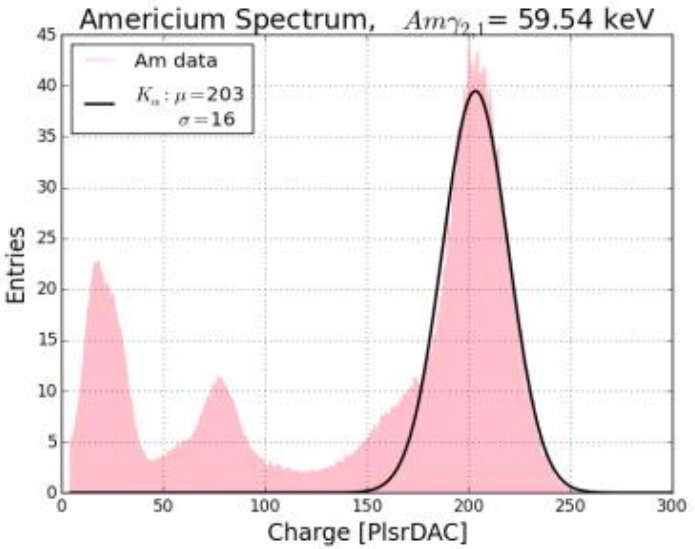
Pixel-per-pixel Calibration of Hit Or Signal

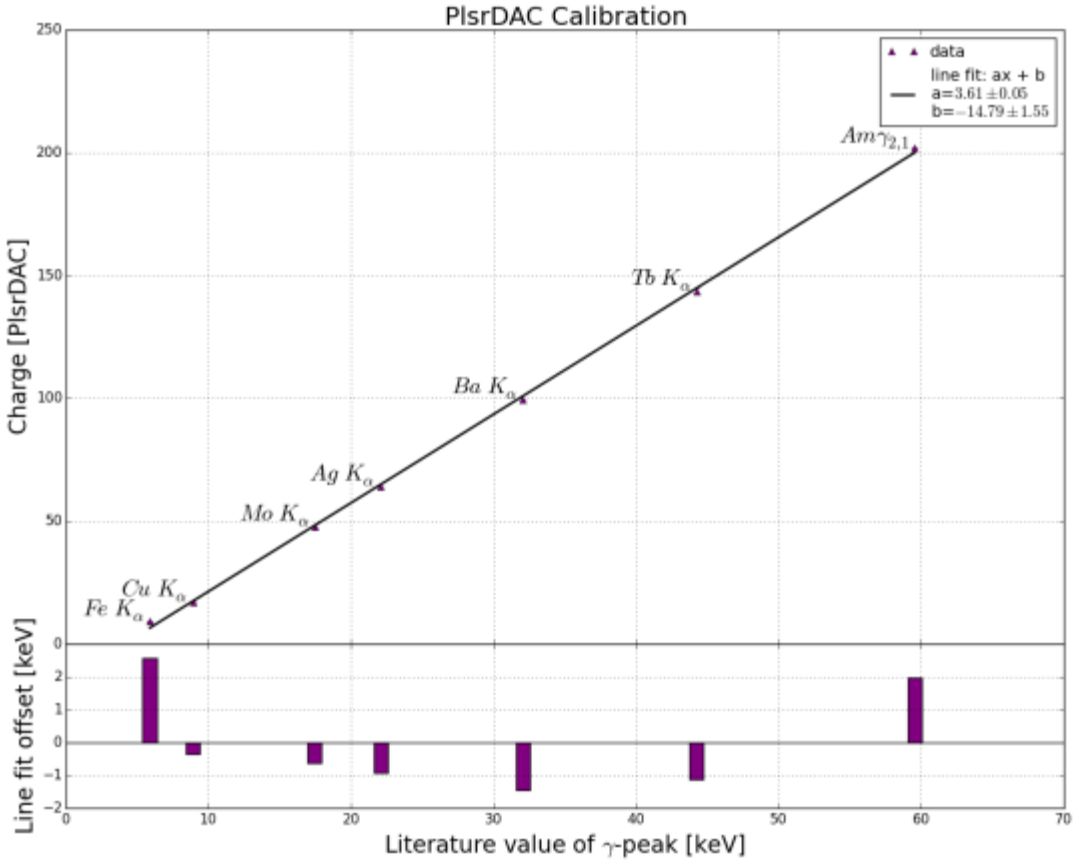


- Precise energy resolution requires pixel per pixel calibration
- Internal charge injection in units of PlsrDAC
- V_{th} and TDC as a function of charge different for each pixel.

Energy to PlsrDac Calibration

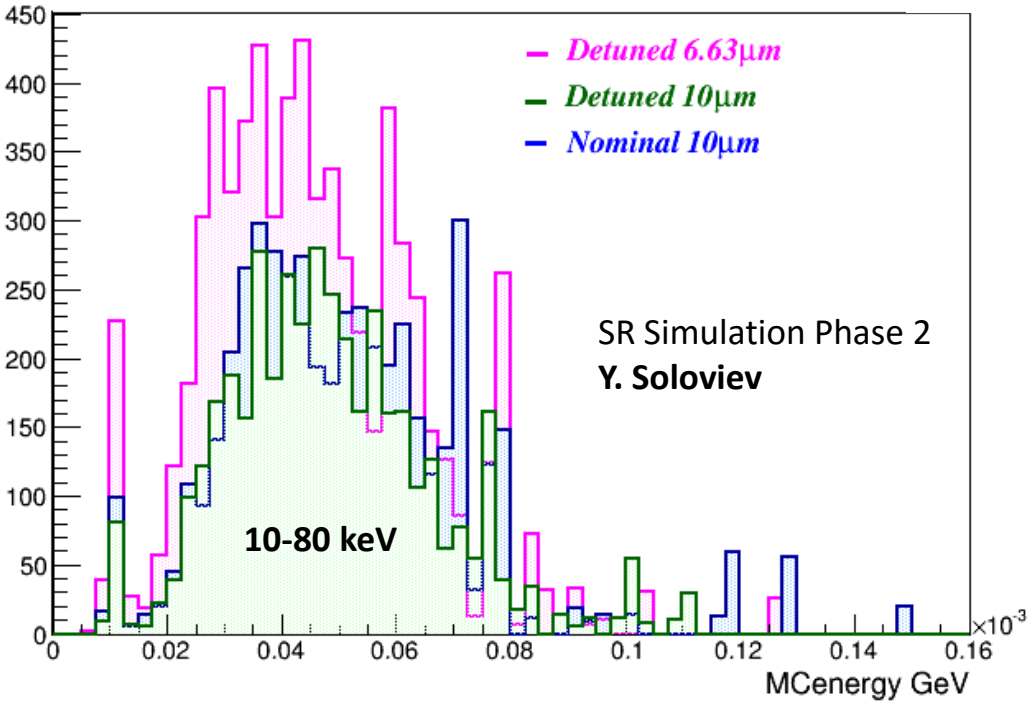


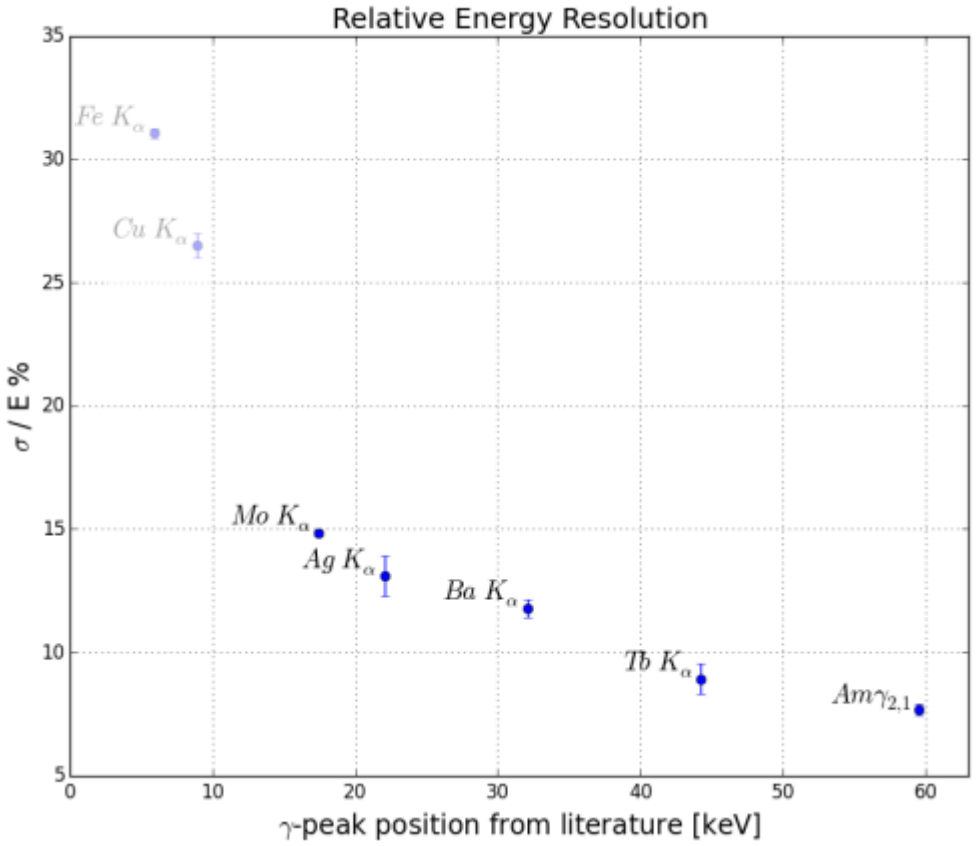




- Dynamic range 6-60 keV (wider possible)
  - Threshold of ~1000 electrons feasible

Energy Resolution



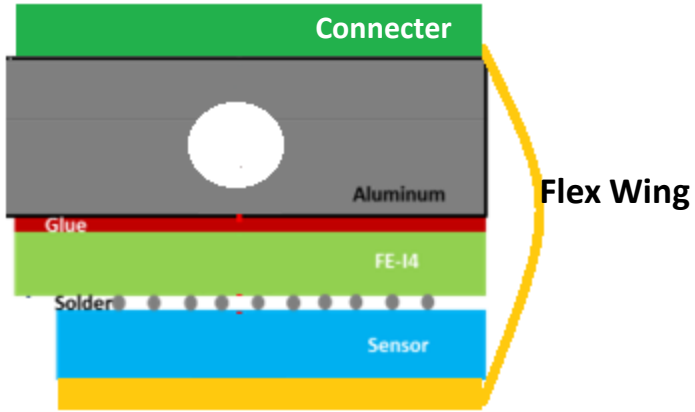


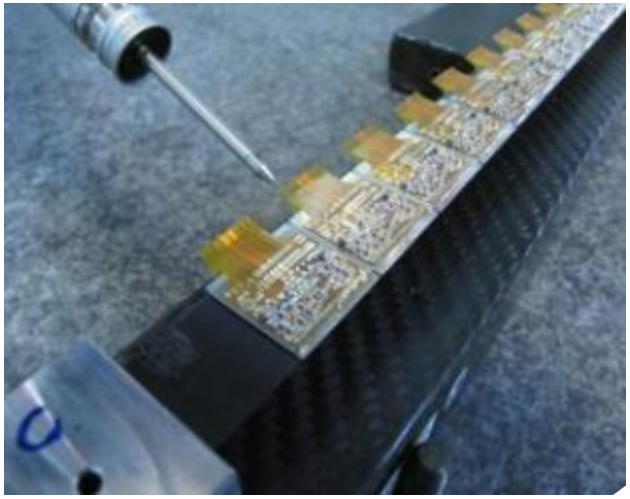
- Expected SR energies in Phase 2

- Adequate energy resolution in the expected range
- Better than 15 % above 10 keV

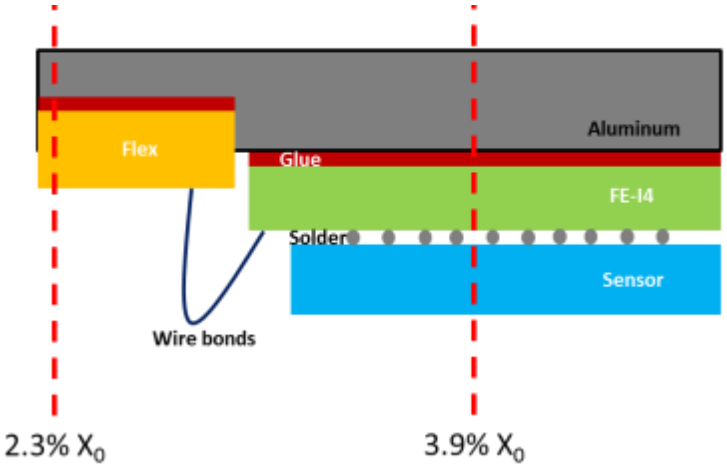
FANGS Stave Design Concept

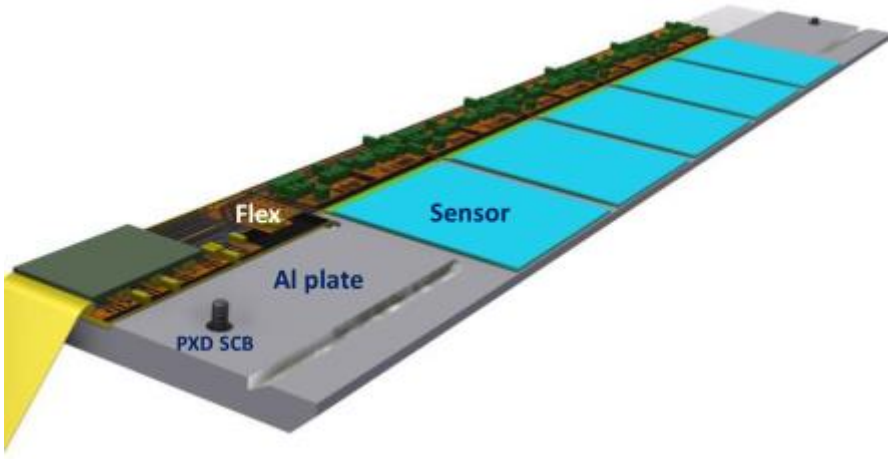
- Initial concept, following IBL stave design





- Revised design, adapted to BEAST needs





System Integration

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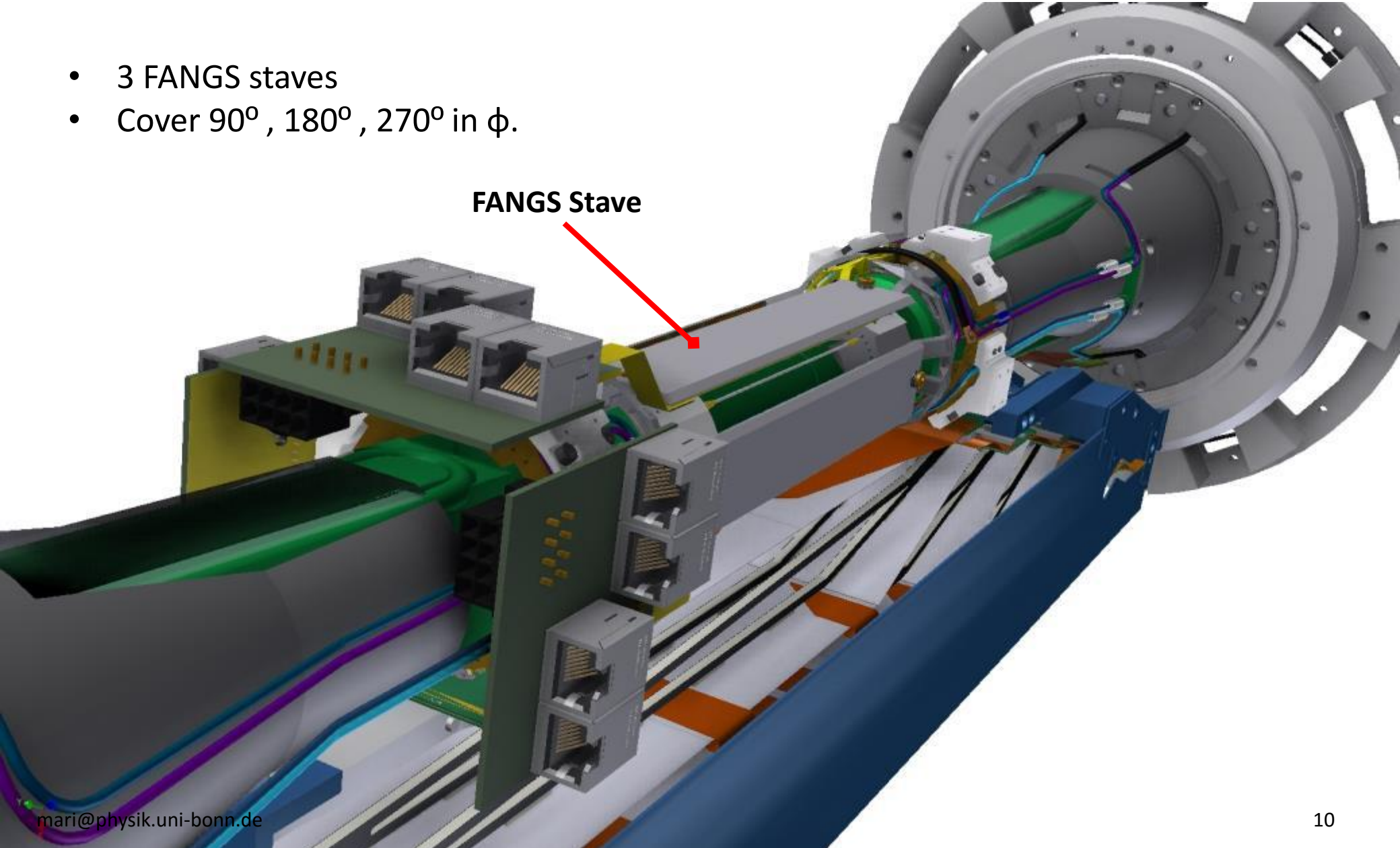
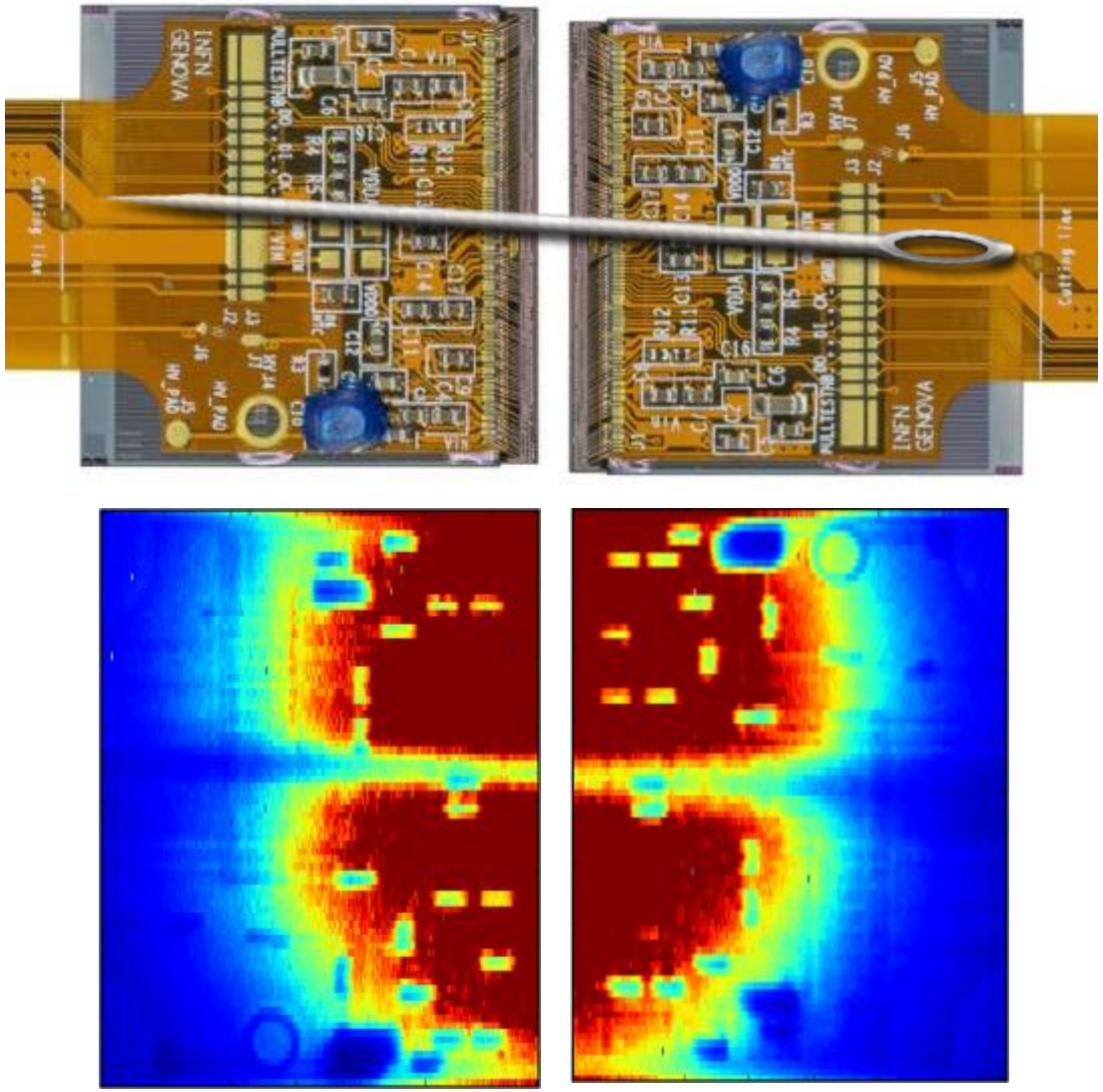
- 3 FANGS staves
- Cover 90^o , 180^o , 270^o in ϕ.

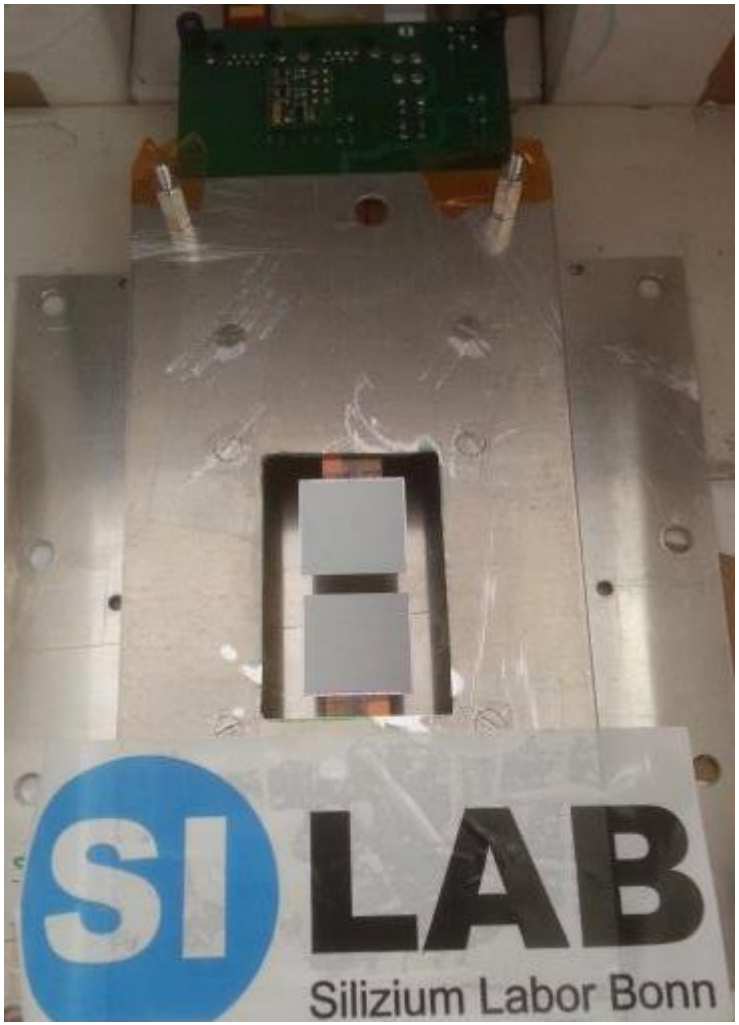


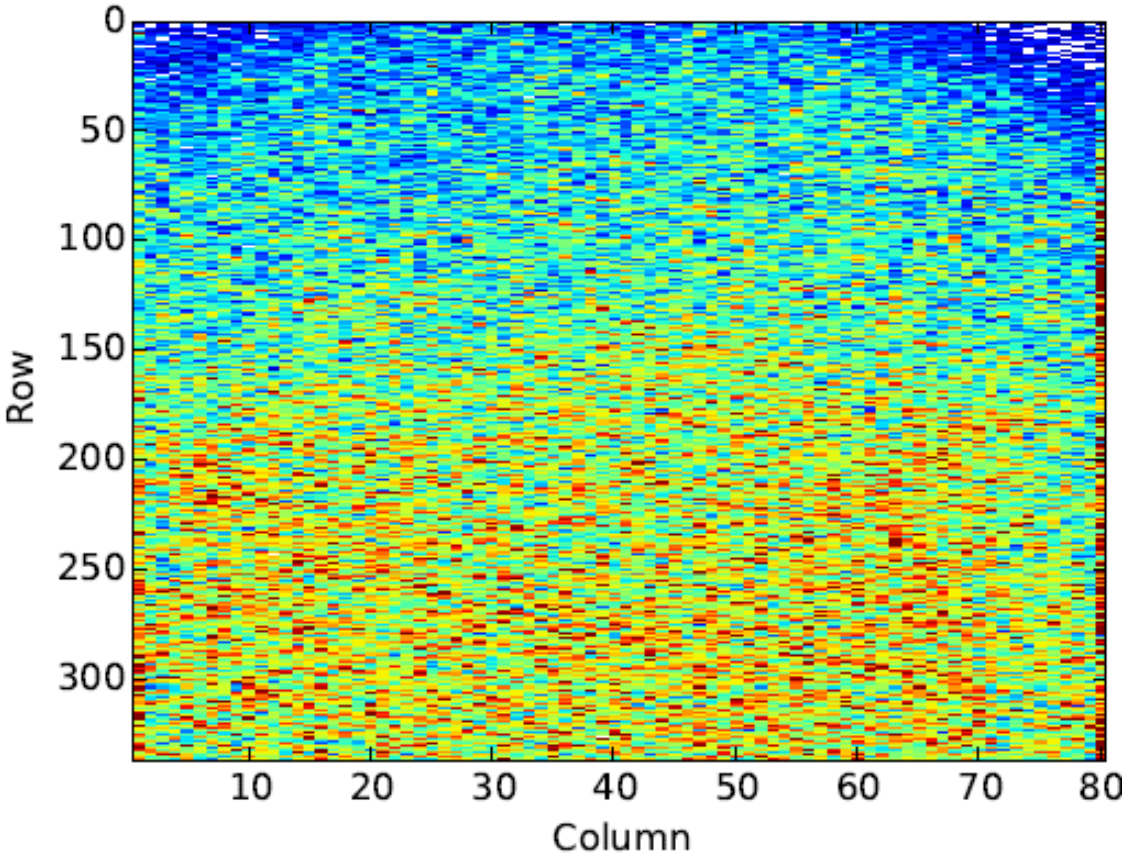
Multiple Chip Readout



- Hit map two FE under Sr90 illumination
- Multiple module parallel readout with MMC3
- Current stave design prompted by absorption of flex components

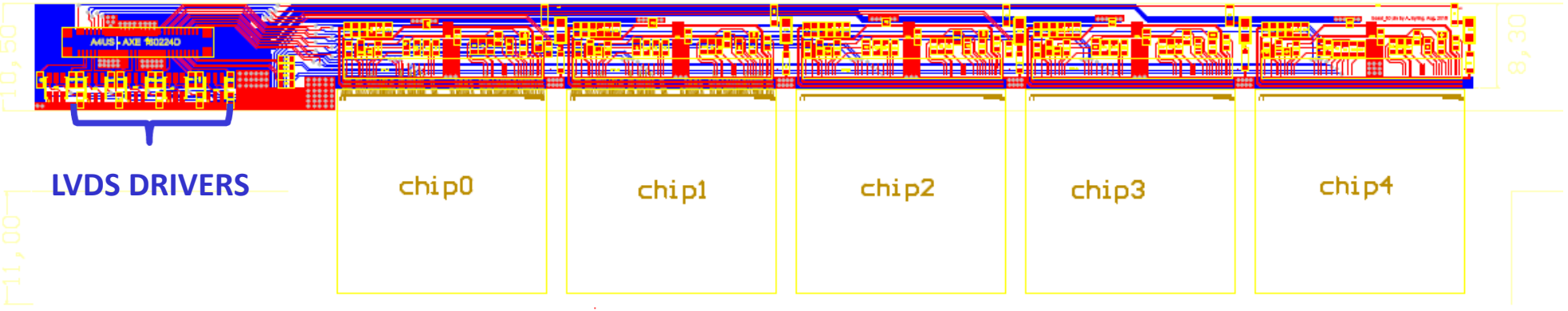
Backside Illumination





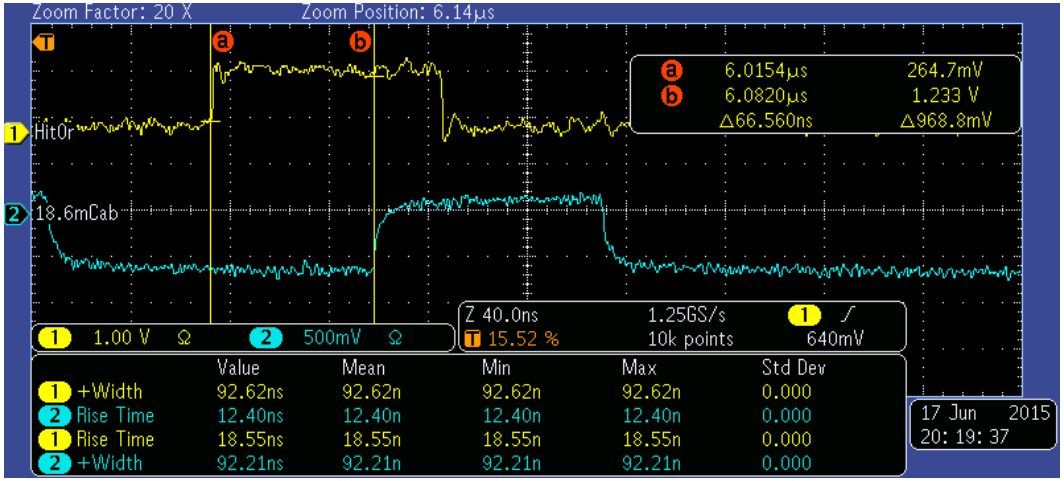
- Effect of components is eliminated by taking a source scan via backside (FE) illumination
- For BEAST, no material in front of the sensor; kapton running parallel to the modules

Kapton Design

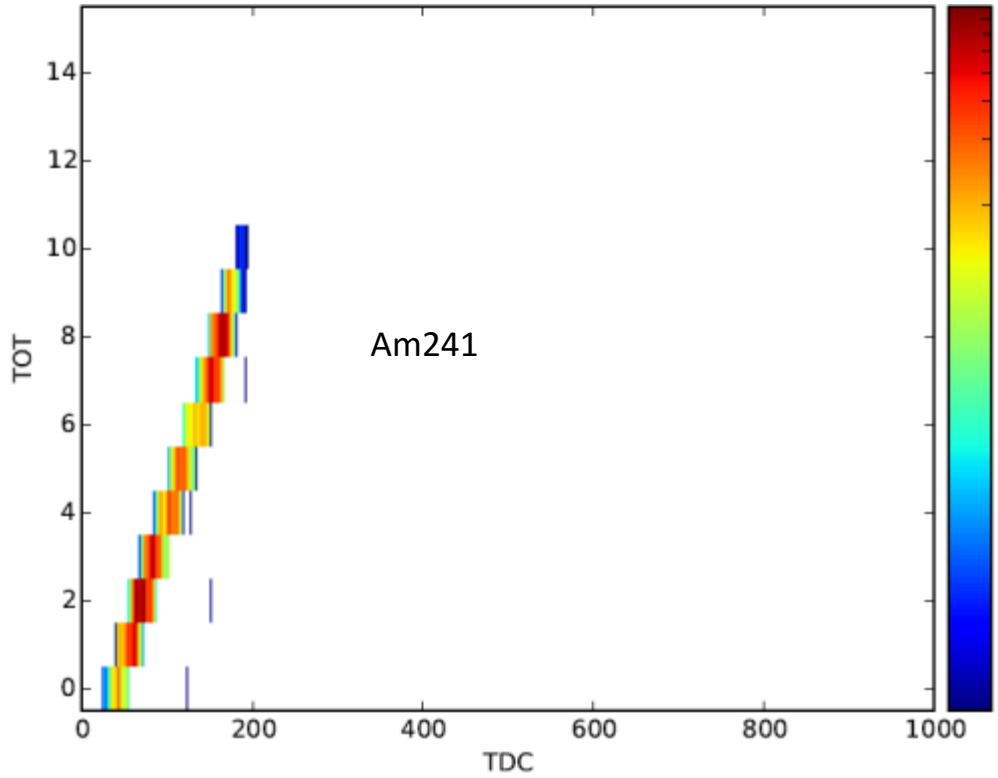


- Flex design for a single stave of 5 FE-I4 chips
- LVDS drivers converting single ended HitOr signal to differential signal for propagation over long cables
- Drivers positioned in backward direction shielded from radiation behind the PXD cooling block
- Radiation hardness to be investigated

Hit Or Delay and Signal Quality Measurements

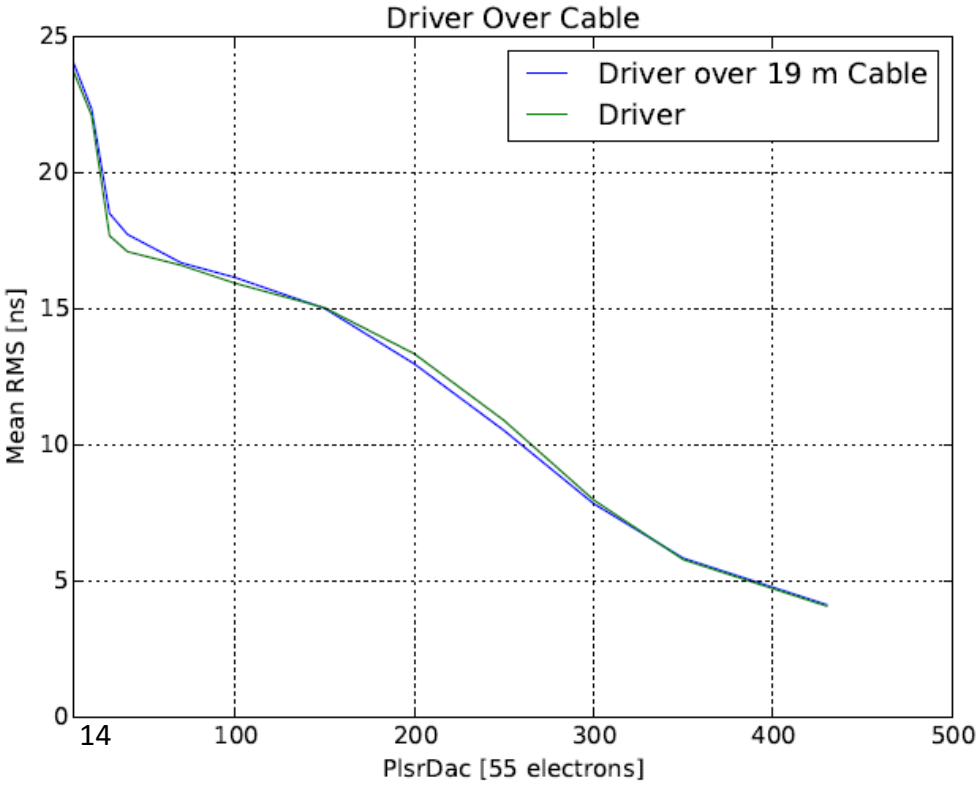


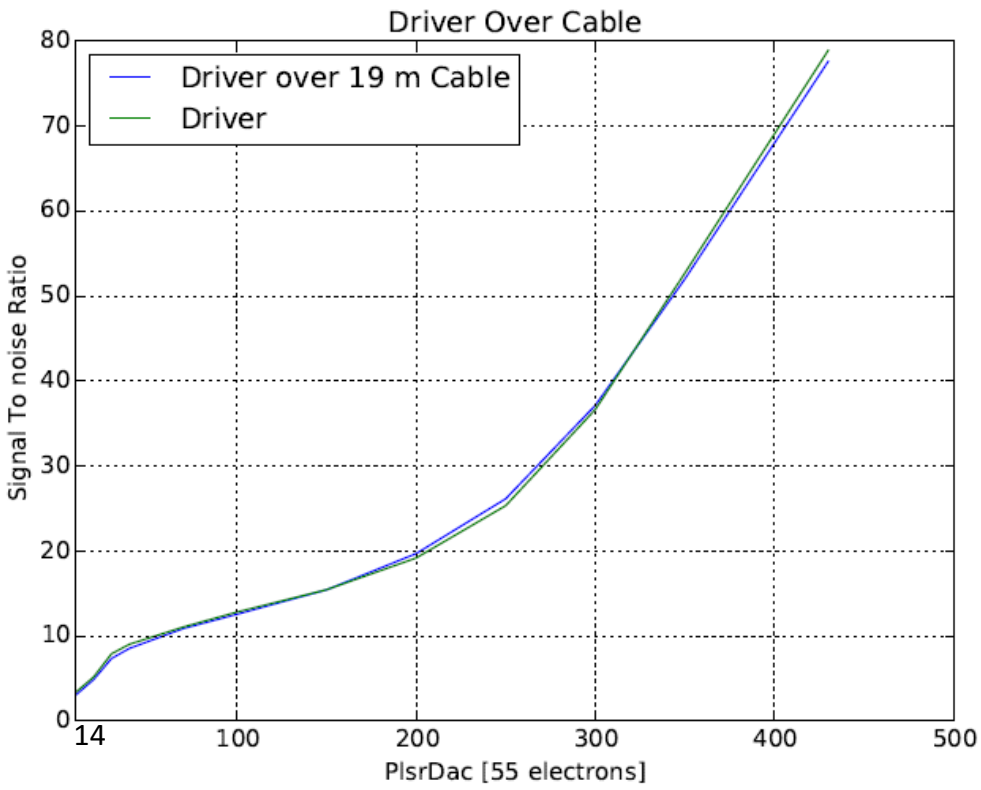
- Propagation delay of HitOr over a 19 m CAT 7
- Signal integrity maintained with delay of ~60 ns
- Improvement pulse shape under investigation



- TOT-TDC correlation with gamma source
- TDC values less that 45 (~10 PlsrDac) are not registered
- Experiment threshold is above device constraint

Signal Integrity





- Obtained during HitOr calibration; From n internal injections; 500 pixels
- Proper resolution at the expected experiment signals
- Signal integrity maintained over 19 m cable

Conclusion

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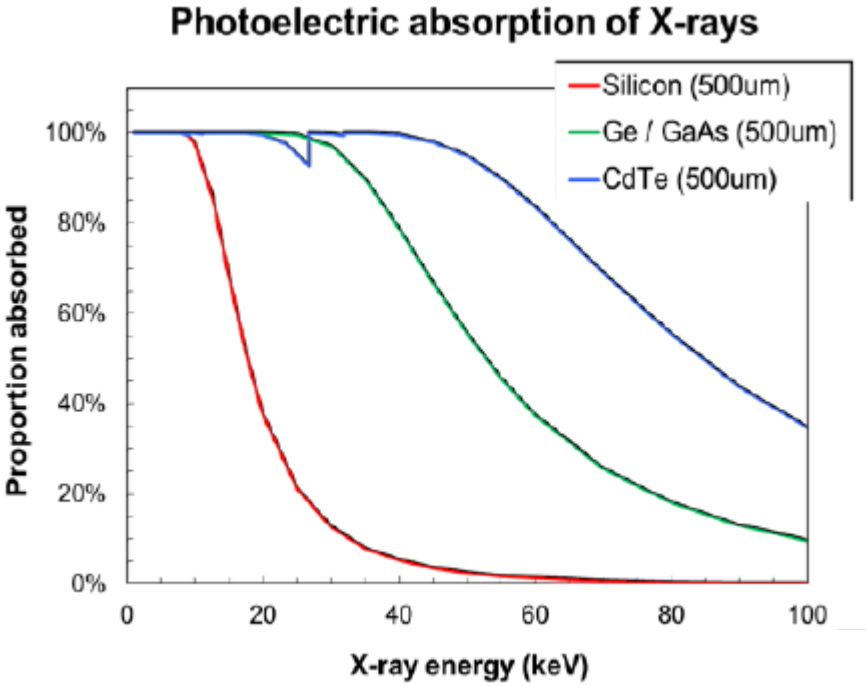
- Front end has been tuned to cover the expected energy range with sufficient **resolution** for Beast Phase 2
- **Multiple-FE DAQ** demonstrated
- **19 m long cables** tested
- Design of Kapton flex and intermediate boards is underway
- **Mechanical** concept and **cooling** management are finalized
- 30 hybrids (FE-I4 and planar sensor) have been prepared

Outlook

- Absorption coefficient (rate measurements)
- External trigger. Multiple module readout with TDC
- Temperature dependence of calibration, noise and energy resolution
- Radiation hardness flex electrical components
- More realistic environment: Spectrum with combined sources and continuum (X-ray machine at different voltages and filters)



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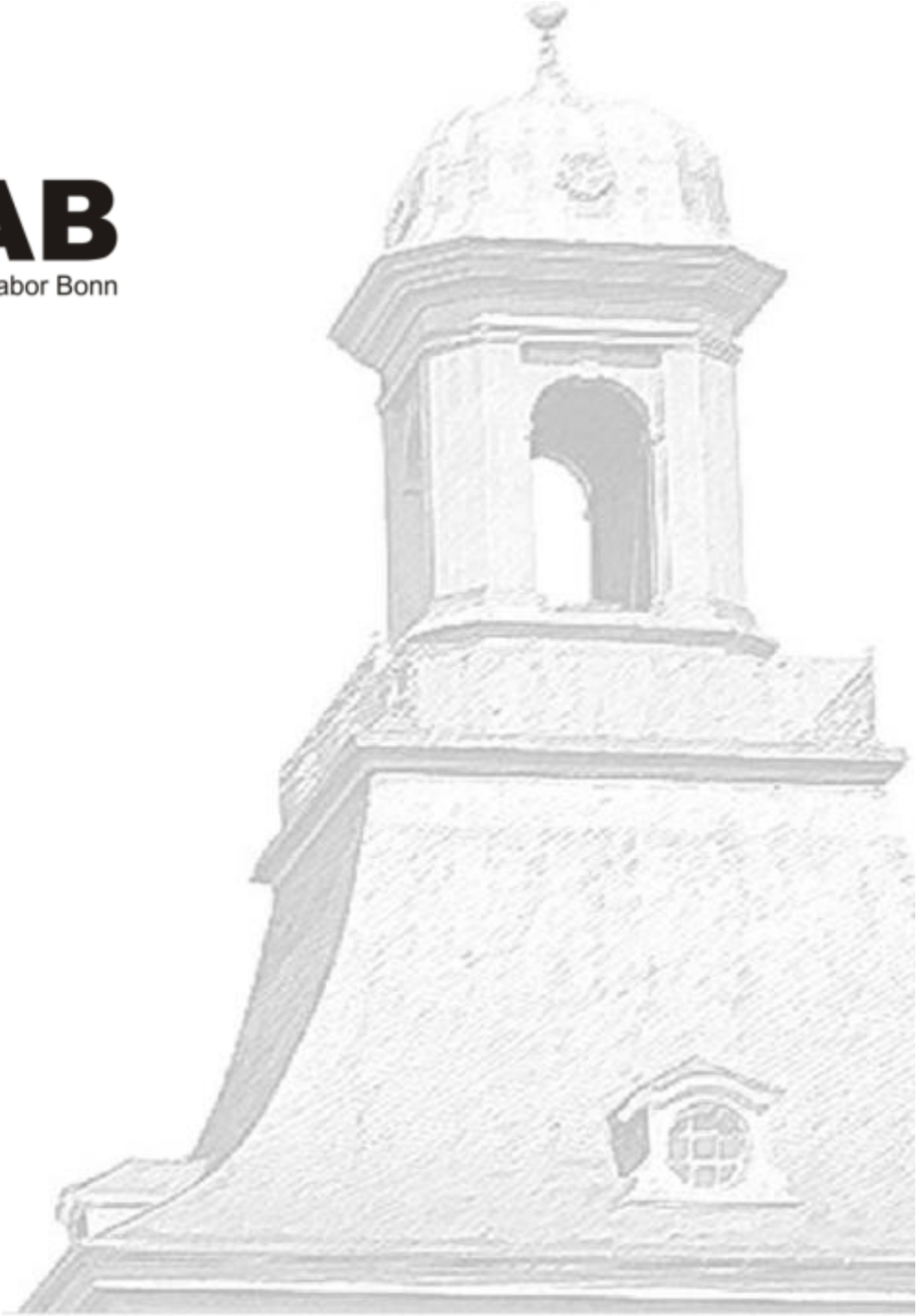

Thank you

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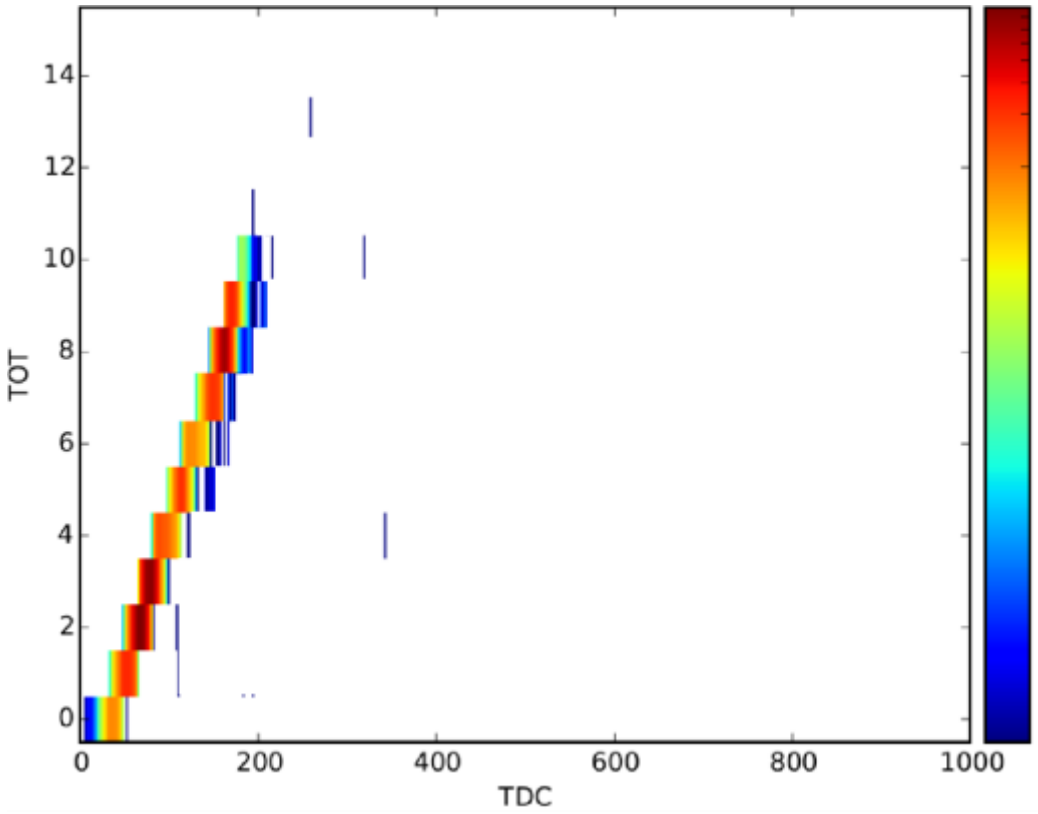
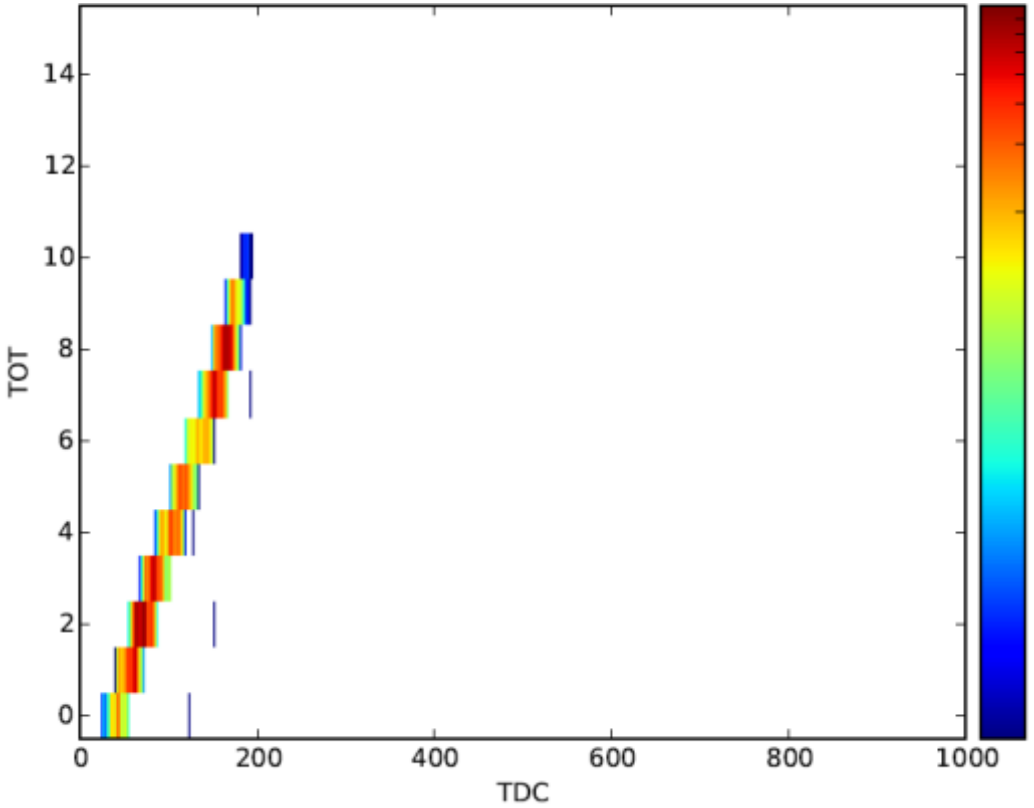
TDC TOT CORRELATION

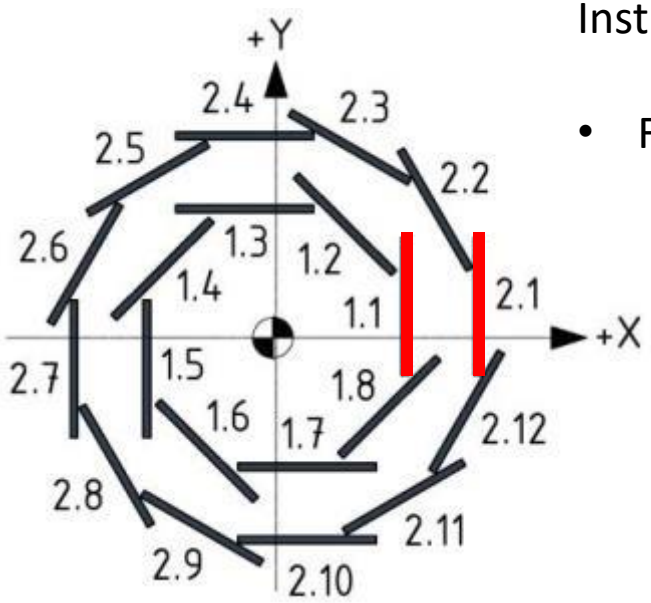




- Expected correlation with source scan

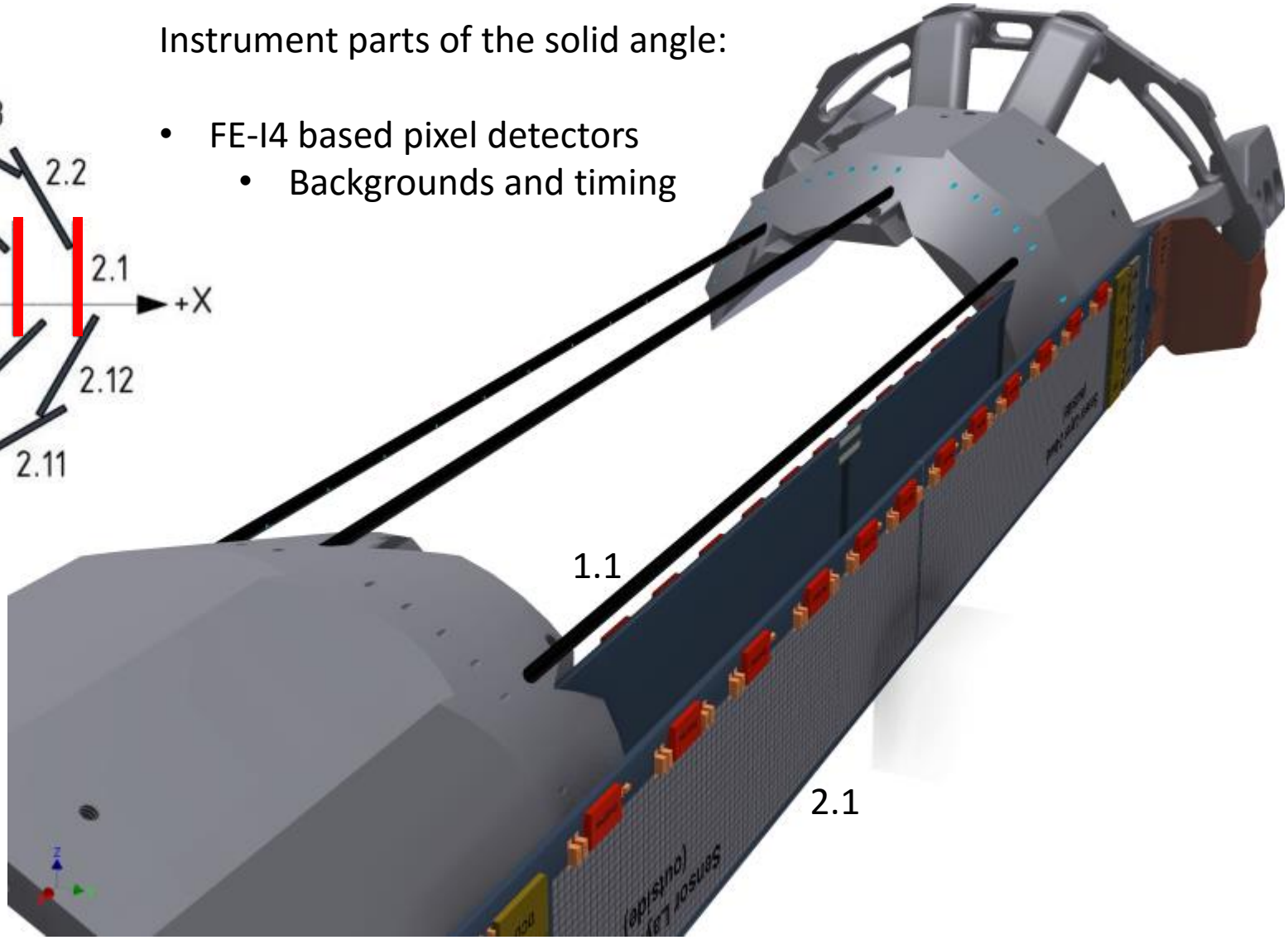
- Obtained correlation with HitOr passed over LVDS driver
- TDC values less that 45 (~10 Plsrdac) not registered.
- Lower limit set to ~ 550 electrons

Phase 2 PXD

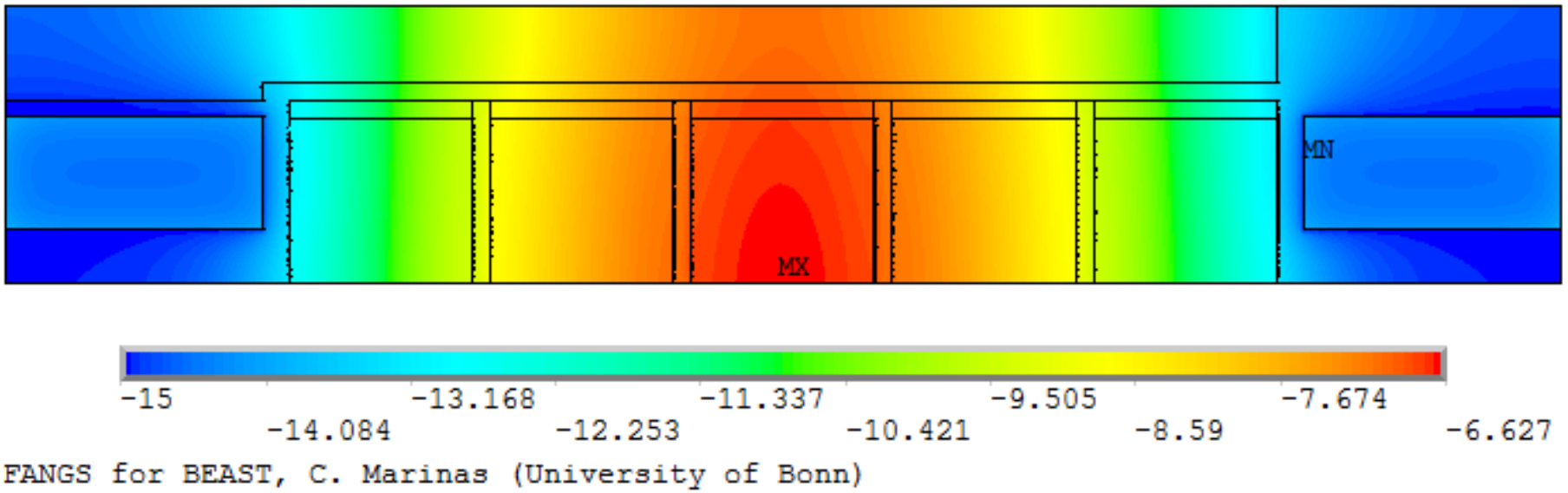


Instrument parts of the solid angle:

- FE-I4 based pixel detectors
  - Backgrounds and timing



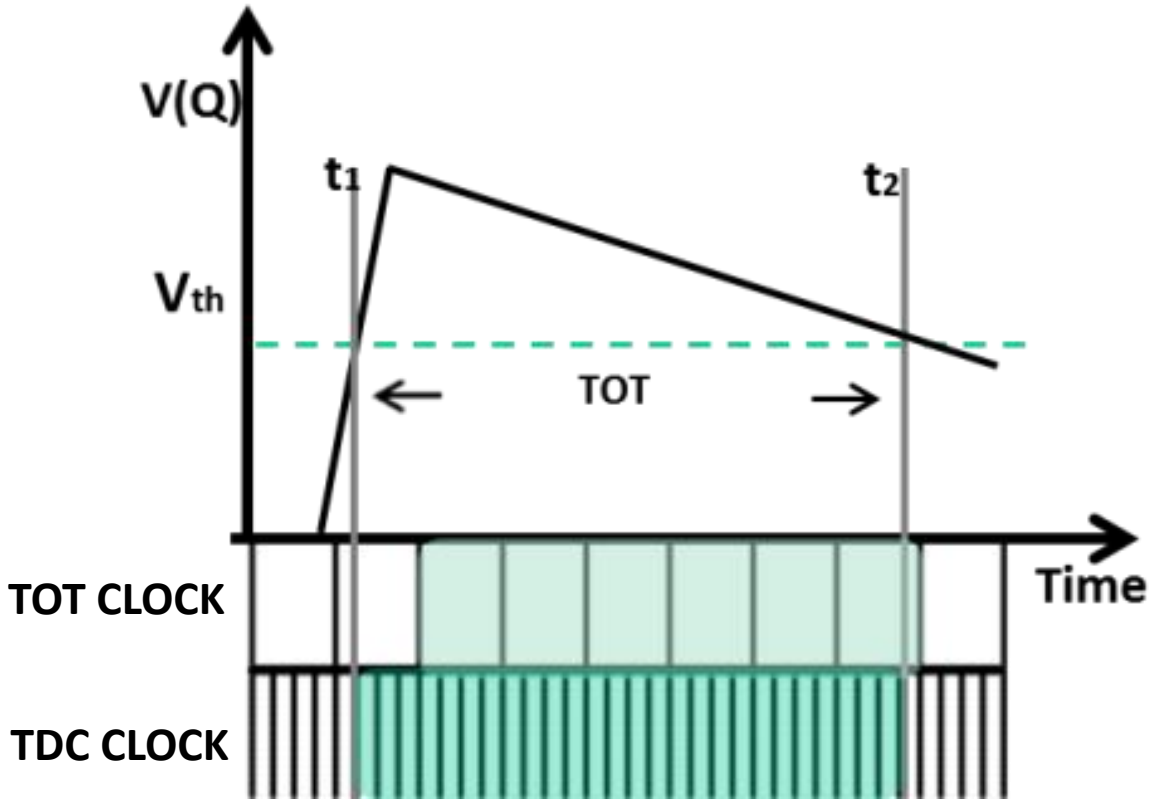
FEA of the FANGS Stave



- Maximum temperature = -4 ^{o}C
- Maximum ΔT within one sensor = 4 ^{o}C
- Power = 1.2 W each FE
- Cooling block = -15 ^{o}C
- Environment = 20 ^{o}C at 2 m/s

- Proper heat handling
- Low and flat temperature profile

TDC Method



System Integration

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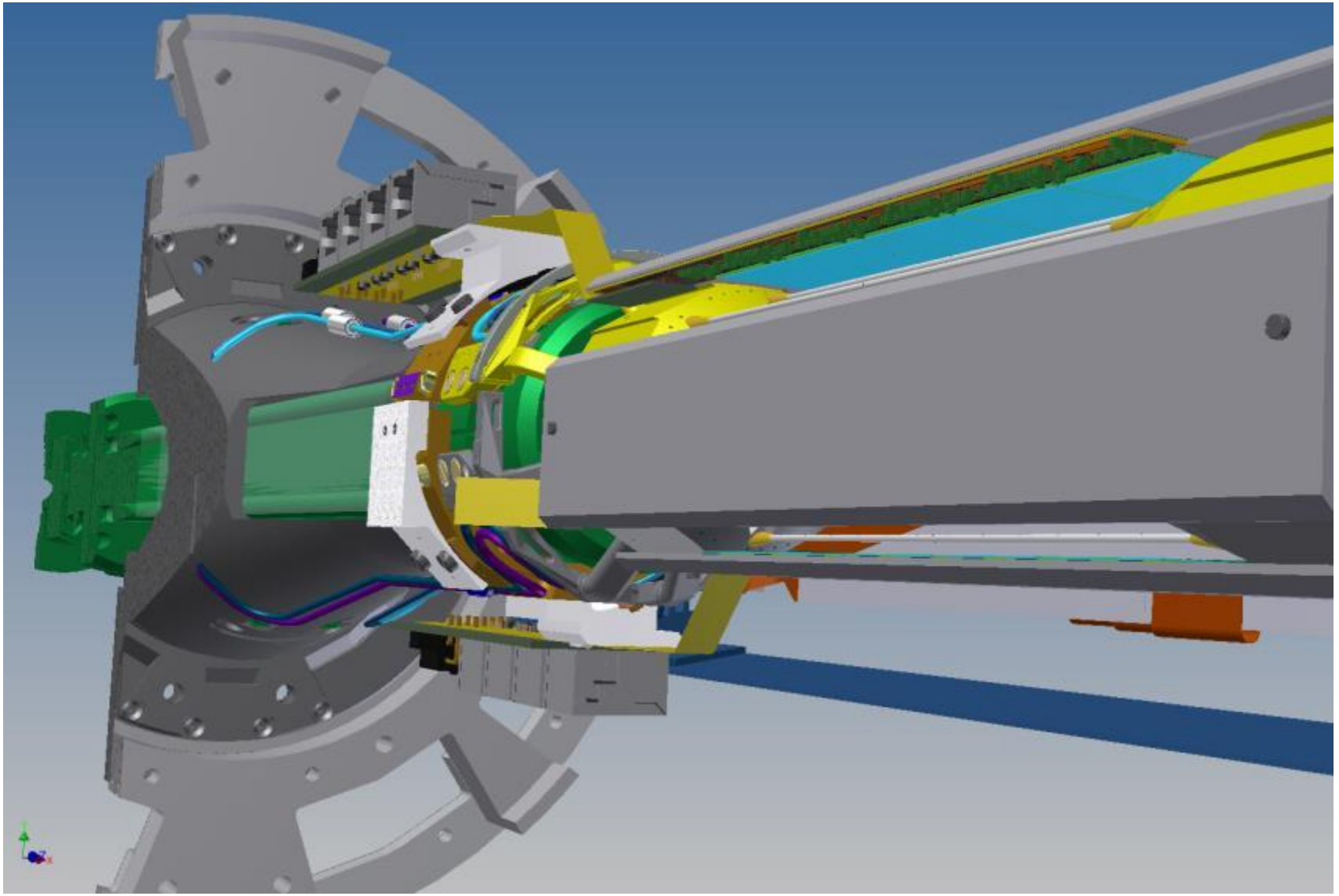
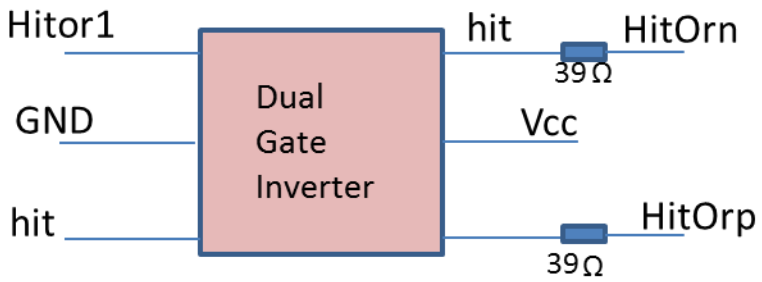
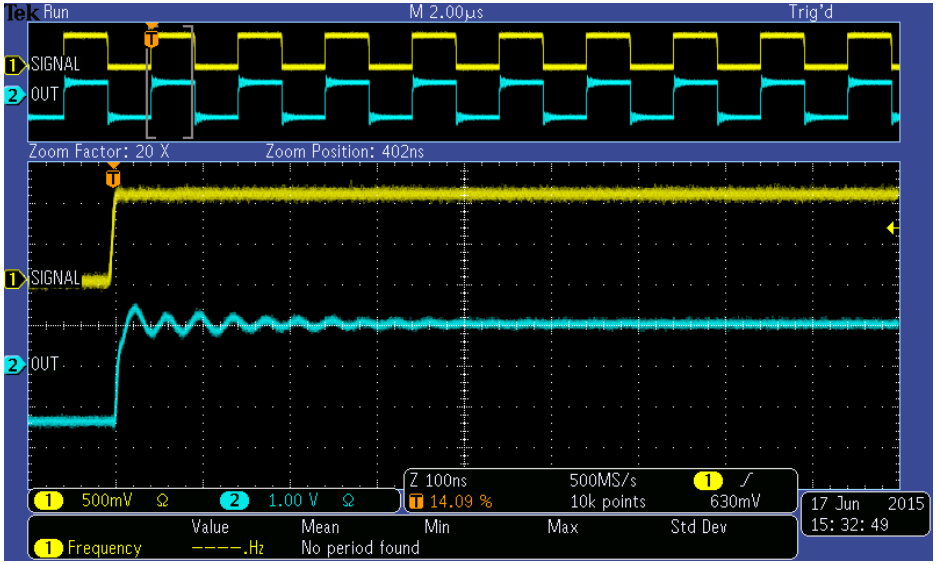
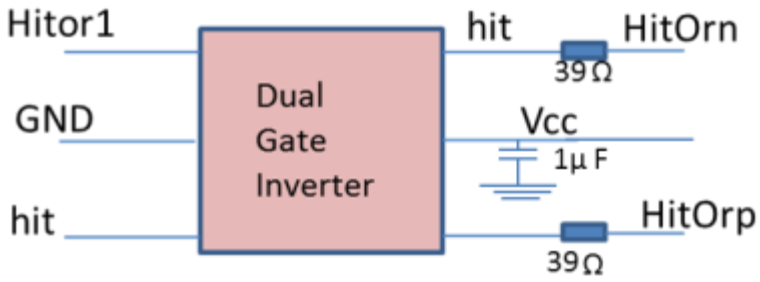


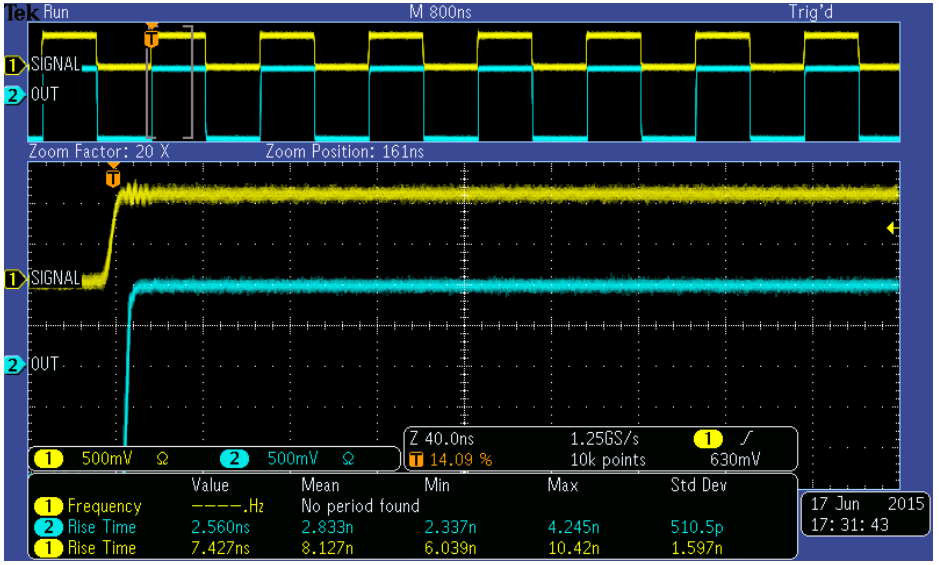
Test Kapton Flex Concept



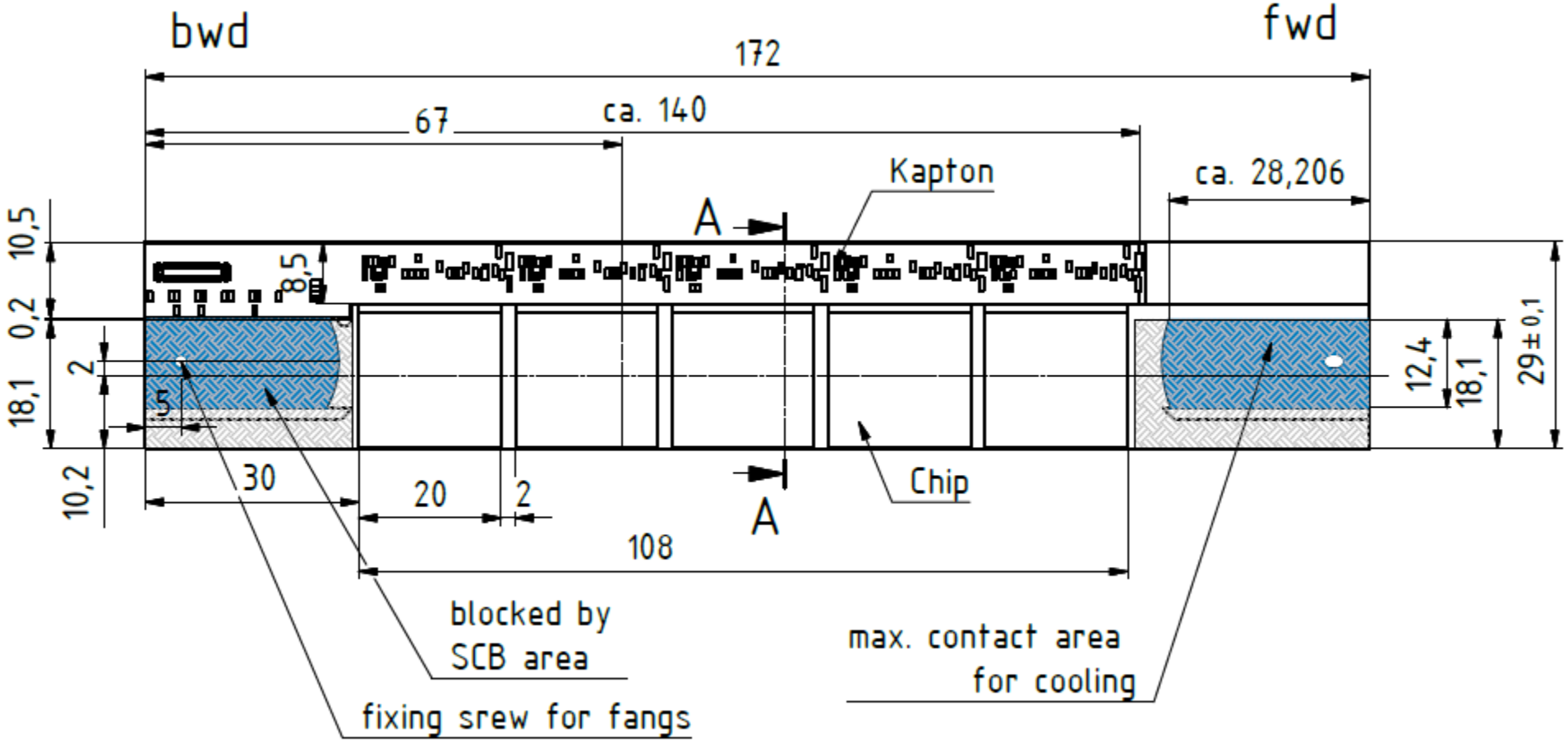


- Distortion observed at 1 MHz with final configuration
- Fixed after addition of one additional 1µF (0402) capacitor

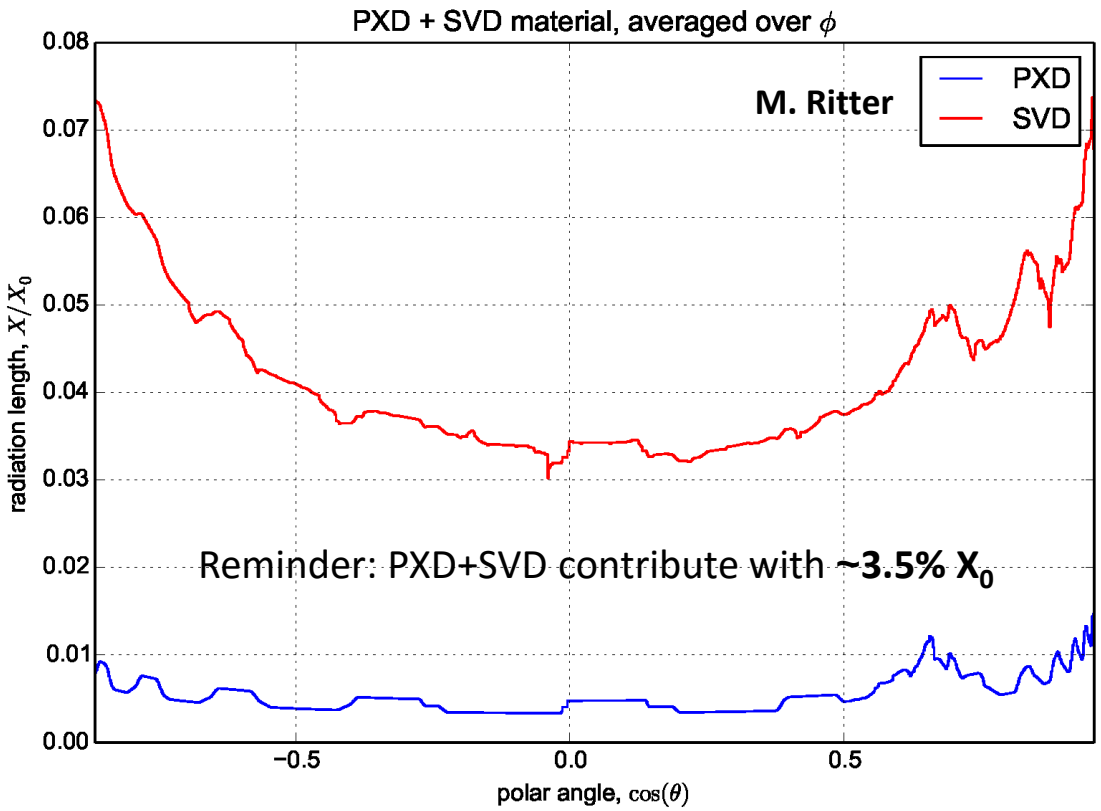




FANGS Stave Dimensions



Aluminum Stave Material Budget



- Low and flat material budget distribution
- No impact in outer detectors

- Support:
3 mm thick Aluminum → 3.4%X_0

- Glue:
50 µm thick Epoxy → 0.014%X_0

- FE-I4
150 µm thick Silicon → 0.16%X_0

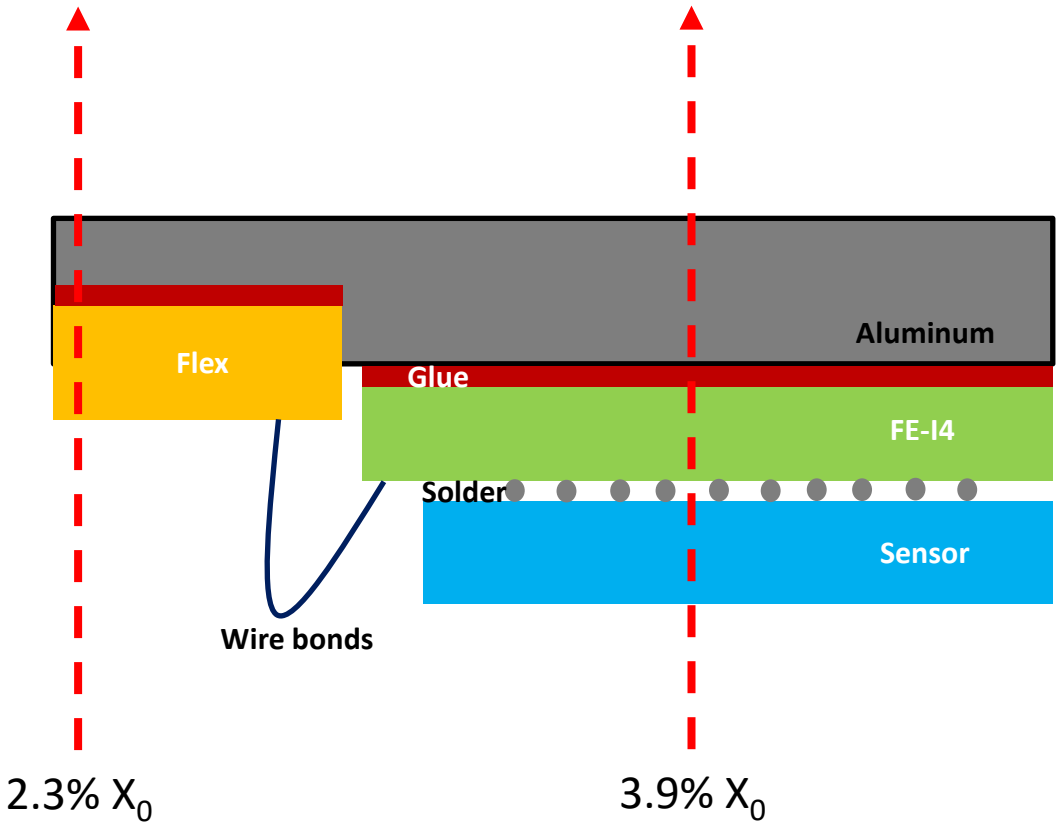
- Sensor:
200 µm thick Silicon → 0.21%X_0

- Solder balls
25 µm thick SnAg → 0.17%X_0 (3.3% of the area)

- Flex
66 µm thick polymide → 0.023%X_0
24 µm Cu (2 layers) → 0.17%X_0

$Total_{Max}$: 3.9% X_0

Aluminum Stave Material Budget



- Low and flat material budget distribution
- No impact in outer detectors

- Support:
3 mm thick Aluminum → 3.4%X_0

- Glue:
50 µm thick Epoxy → 0.014%X_0

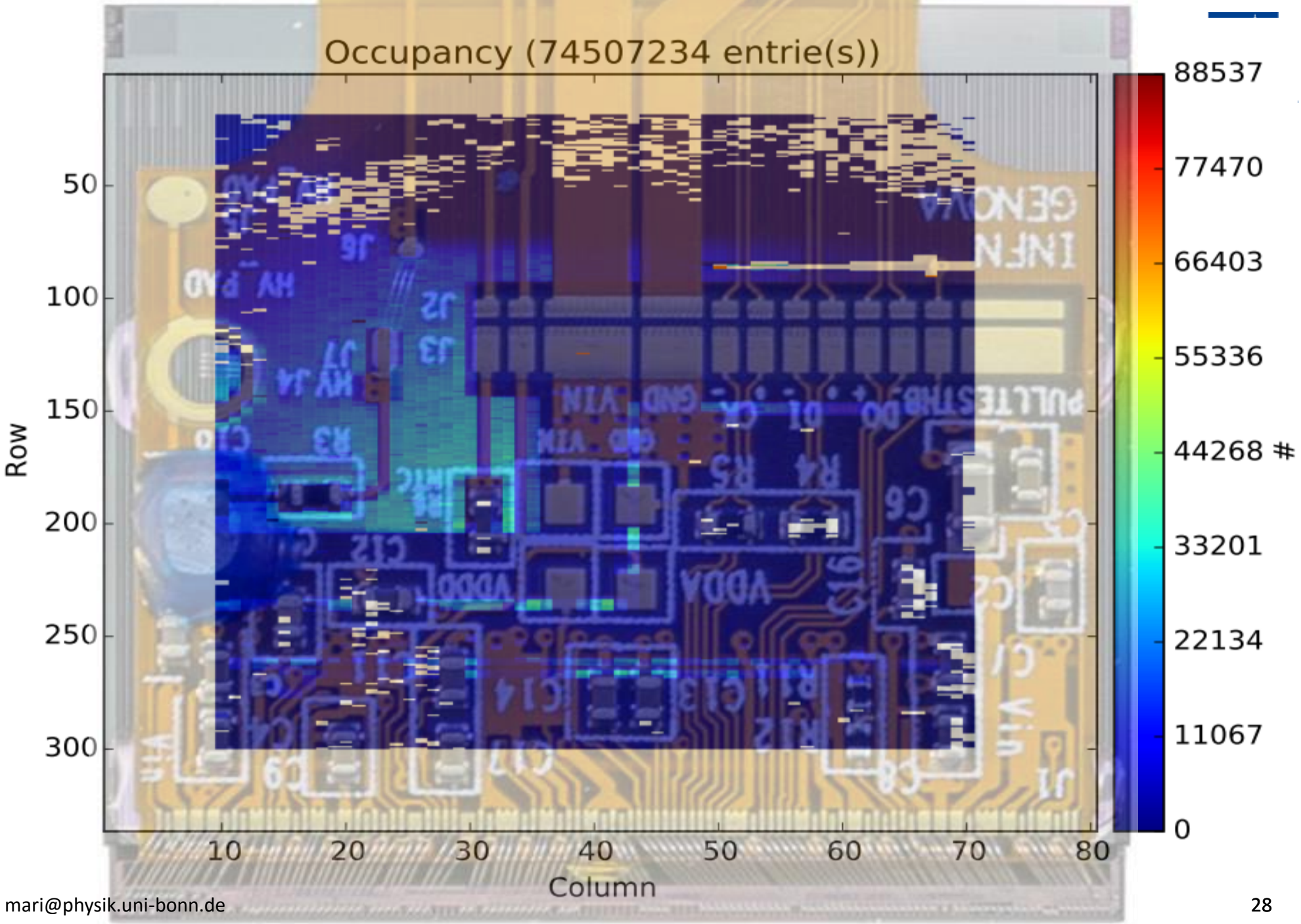
- FE-I4
150 µm thick Silicon → 0.16%X_0

- Sensor:
200 µm thick Silicon → 0.21%X_0

- Solder balls
25 µm thick SnAg → 0.17%X_0 (3.3% of the area)

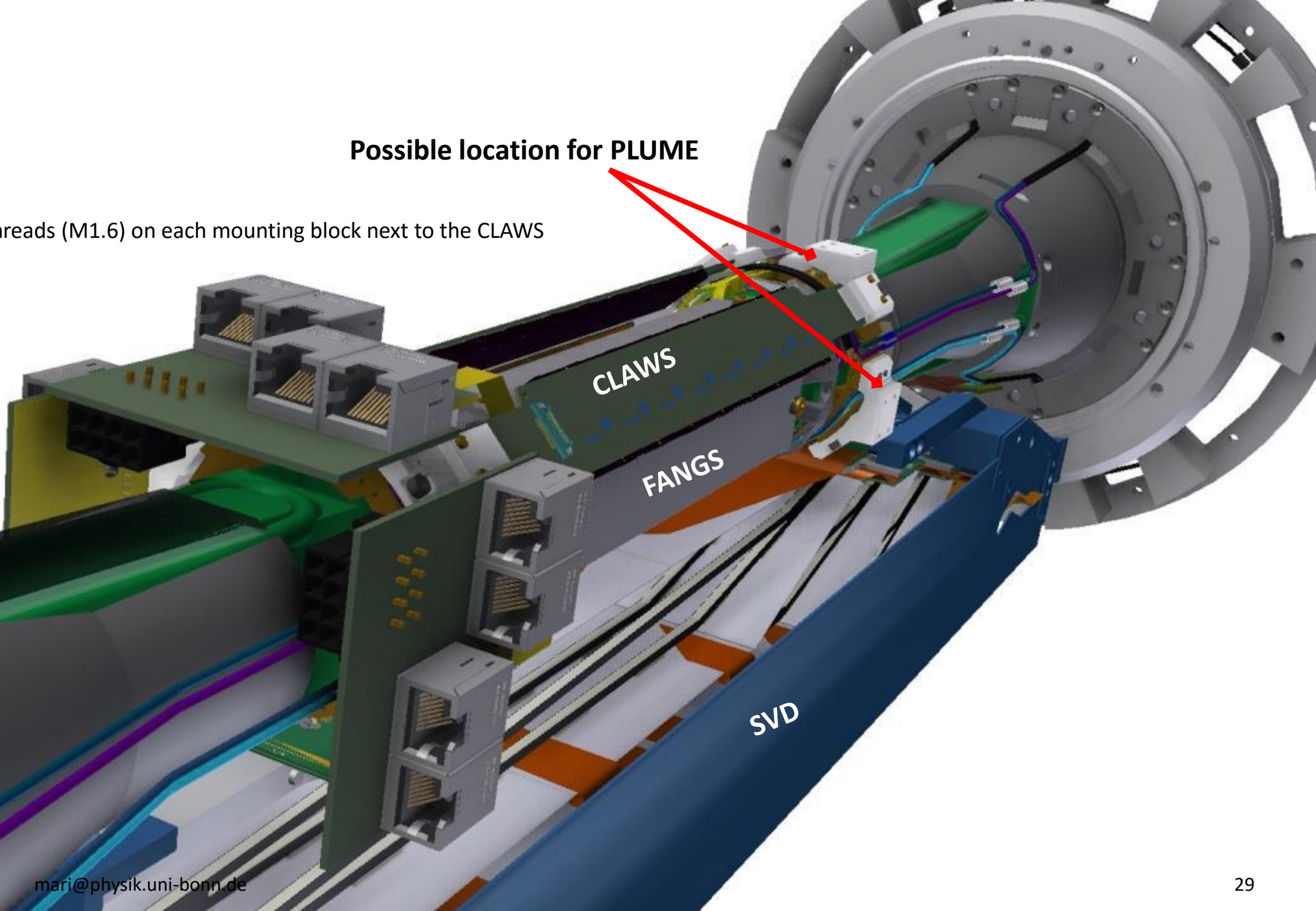
- Flex
100 µm thick polymide → 0.035%X_0
70 µm Cu (2 layers) → 0.50%X_0
50 µm thick Epoxy → 0.014%X_0

$Total_{Max}$: 3.9% X_0


Occupancy (74507234 entrie(s))
Row
50
100
150
200
250
300
10
20
30
40
50
60
70
80
Column
88537
77470
66403
55336
44268 #
33201
22134
11067
0

Possible location for PLUME

hreads (M1.6) on each mounting block next to the CLAWS



System Integration

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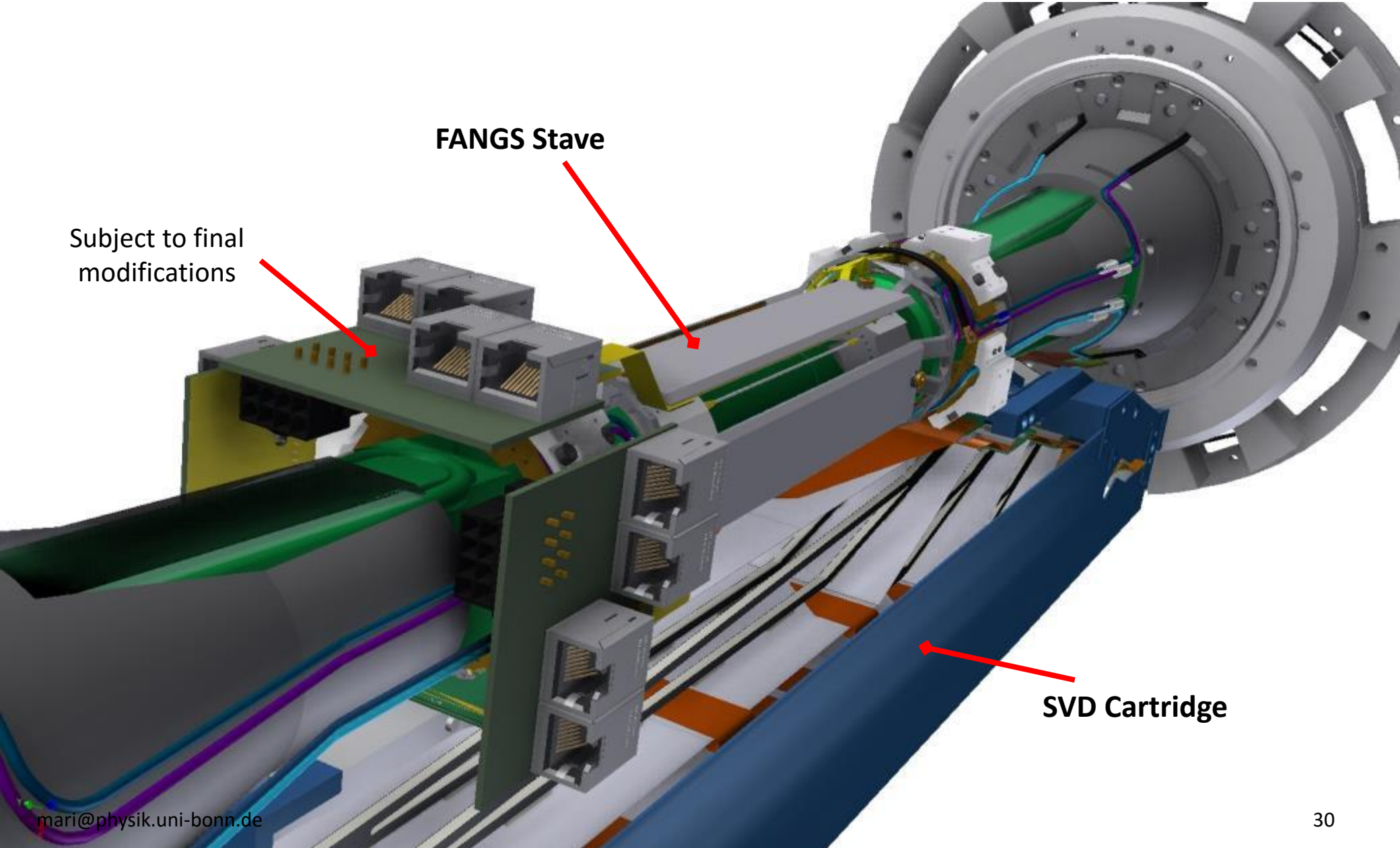

System Integration

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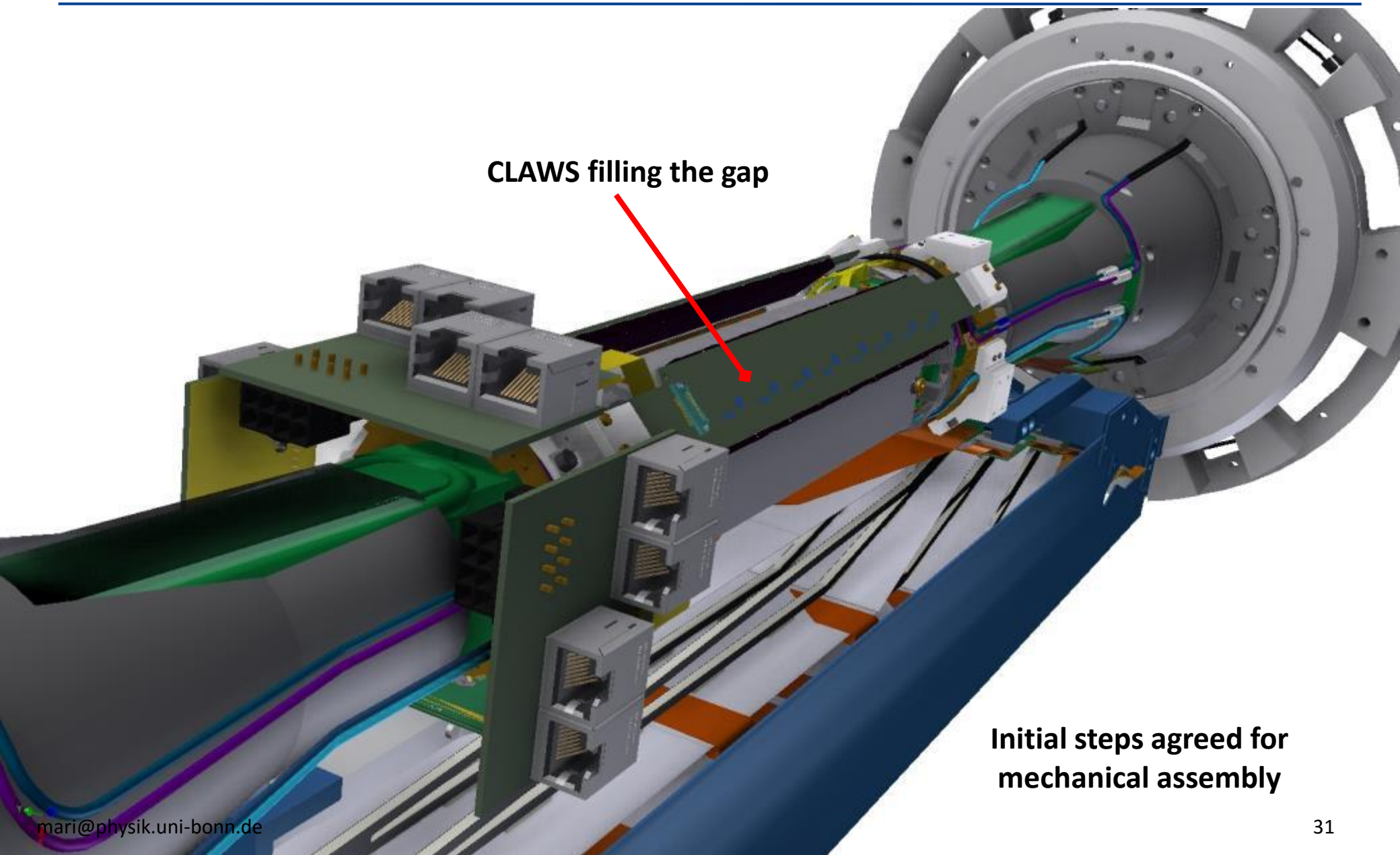

Initial steps agreed for mechanical assembly

System Integration

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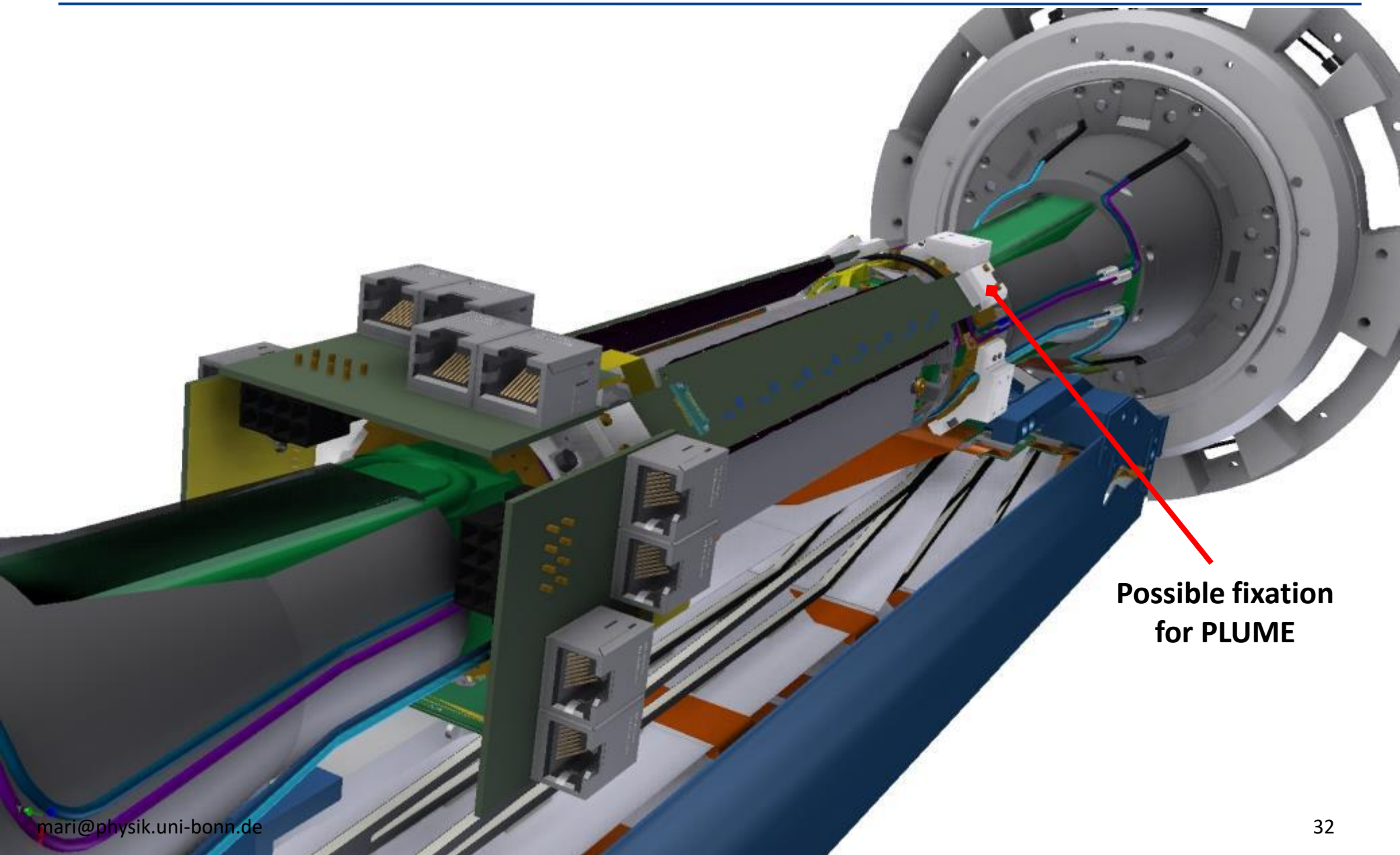
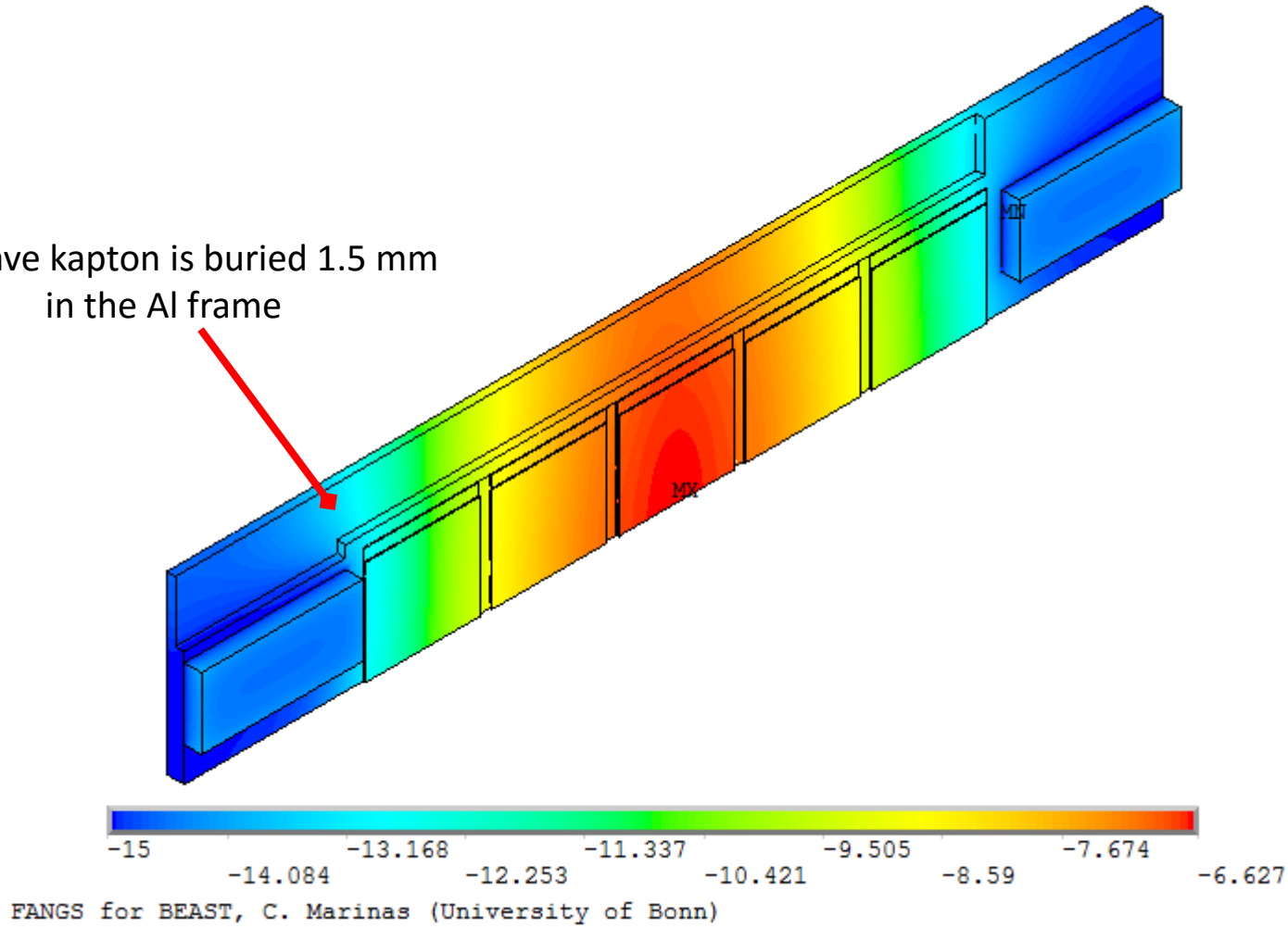
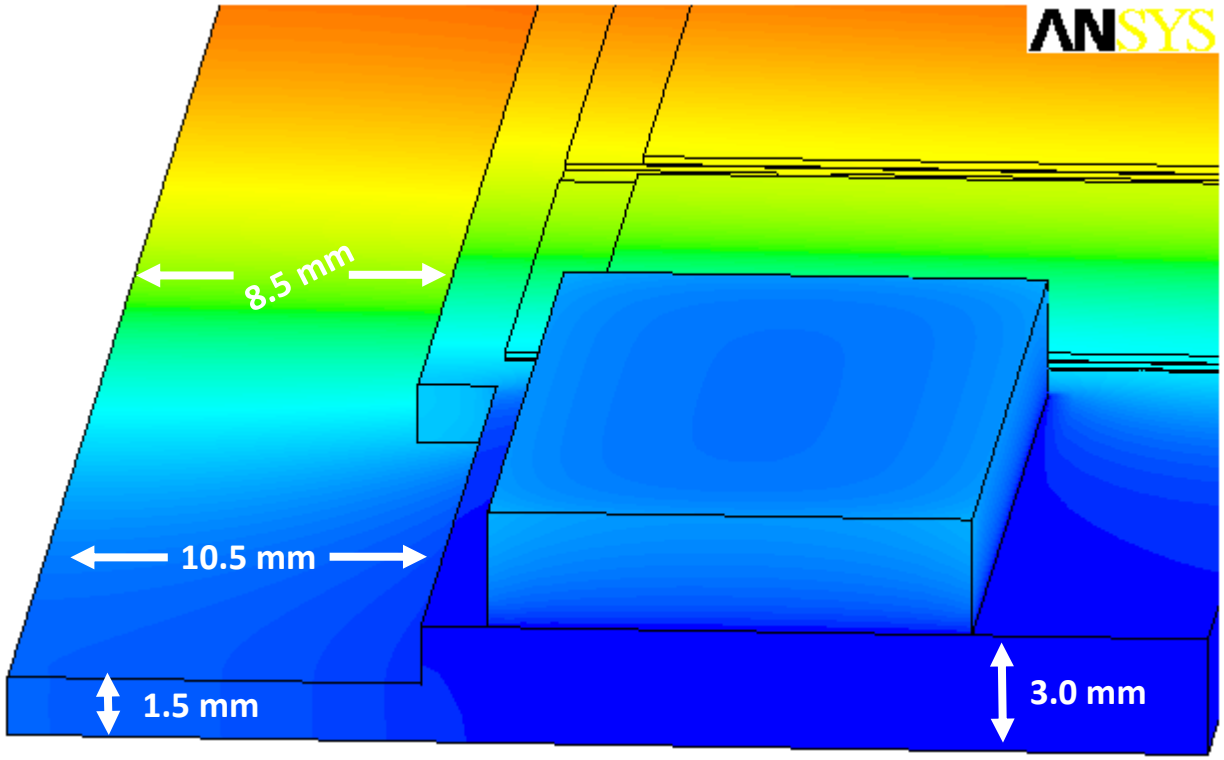


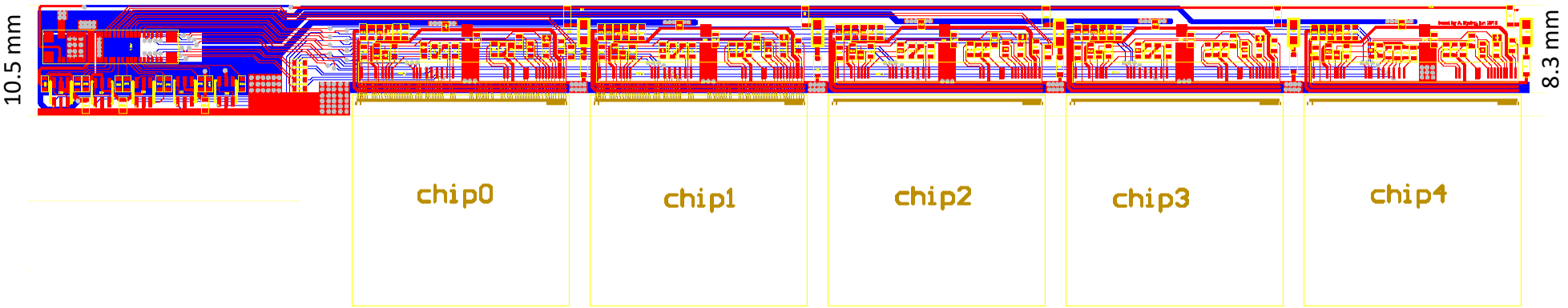
The stave kapton is buried 1.5 mm in the Al frame




ANSYS
8.5 mm
10.5 mm
1.5 mm
3.0 mm

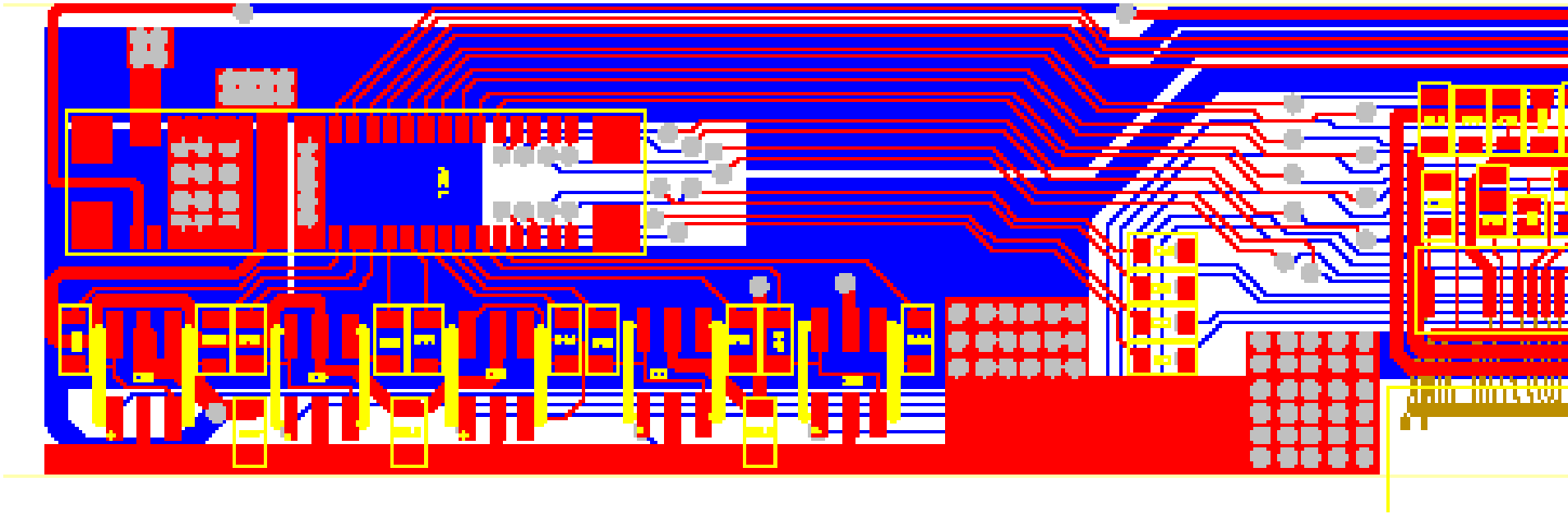
Stave Dimensions: Connector Side

60 pin connector size: 13.8 mm (L) x 2.2 mm (W) x 1.5 mm (T)
LVDS inverter size: 2.15 mm (L) x 1.4 mm (W) x 1.1 mm (T)
0402 2.2 uF capacitor size: 1 mm (L) x 0.5 mm (W) x 0.56 mm (T)

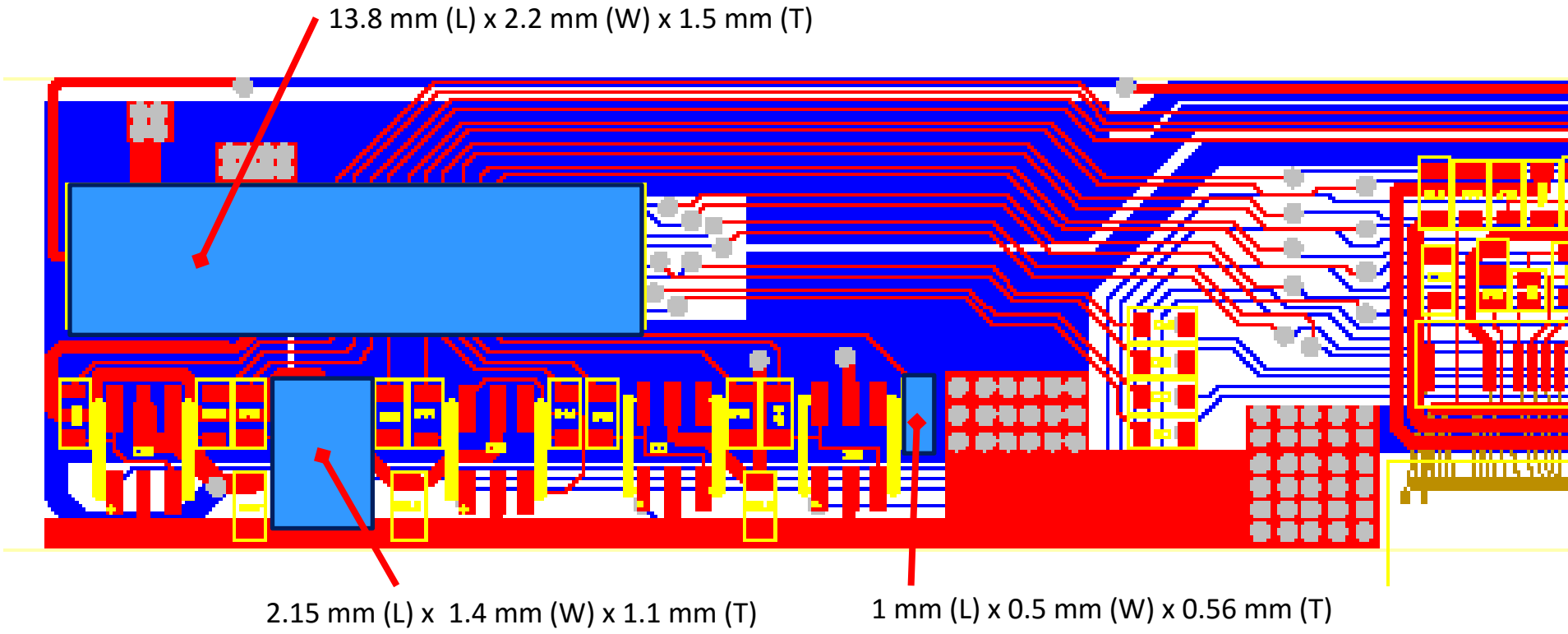


Stave Dimensions: Connector Side

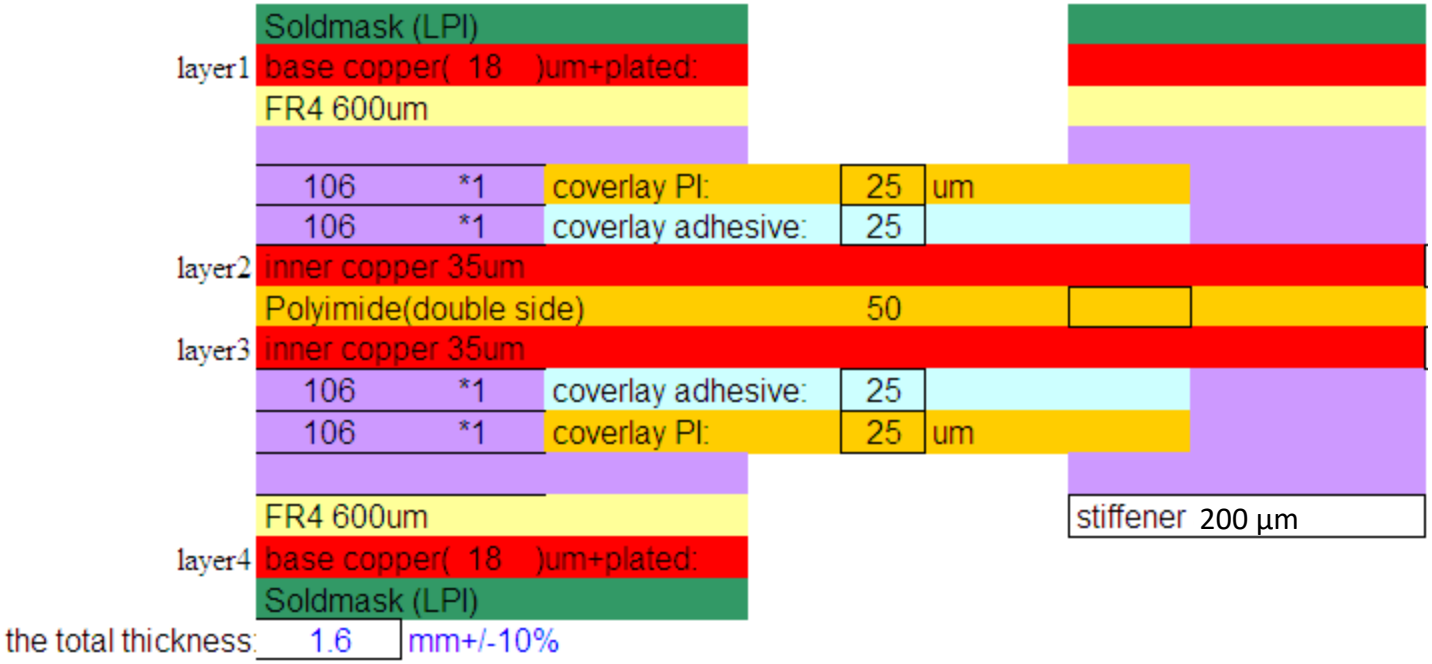
60 pin connector size: 13.8 mm (L) x 2.2 mm (W) x 1.5 mm (T)
LVDS inverter size: 2.15 mm (L) x 1.4 mm (W) x 1.1 mm (T)
0402 2.2 uF capacitor size: 1 mm (L) x 0.5 mm (W) x 0.56 mm (T)



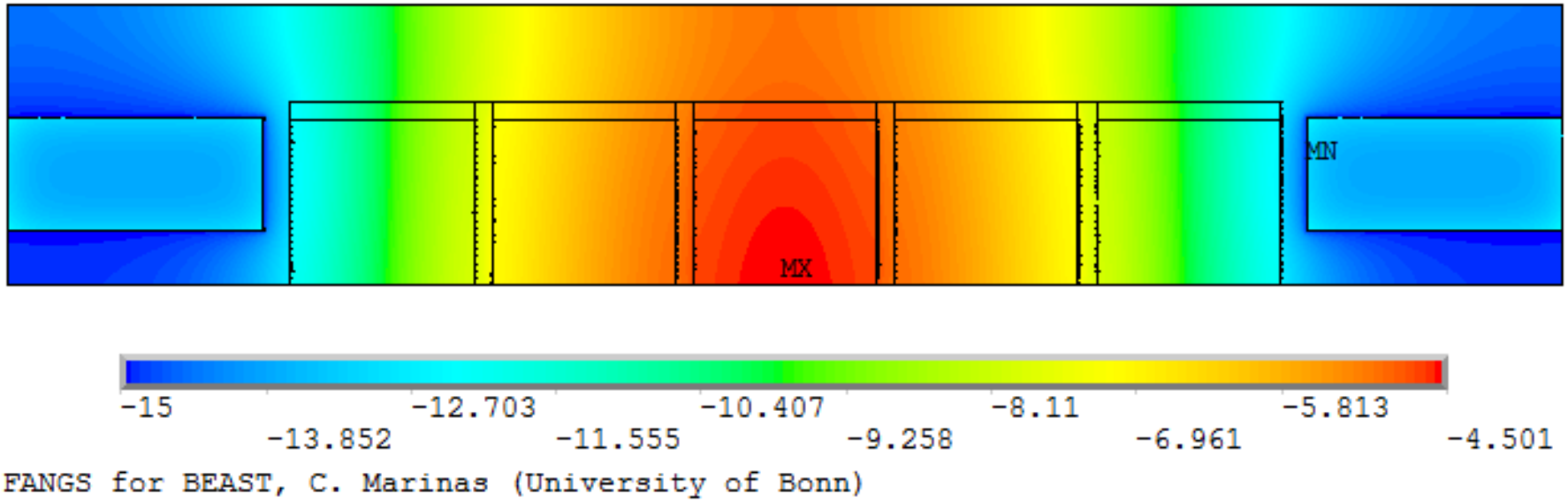
Stave Dimensions: Connector Side



Intermediate Kapton Thickness

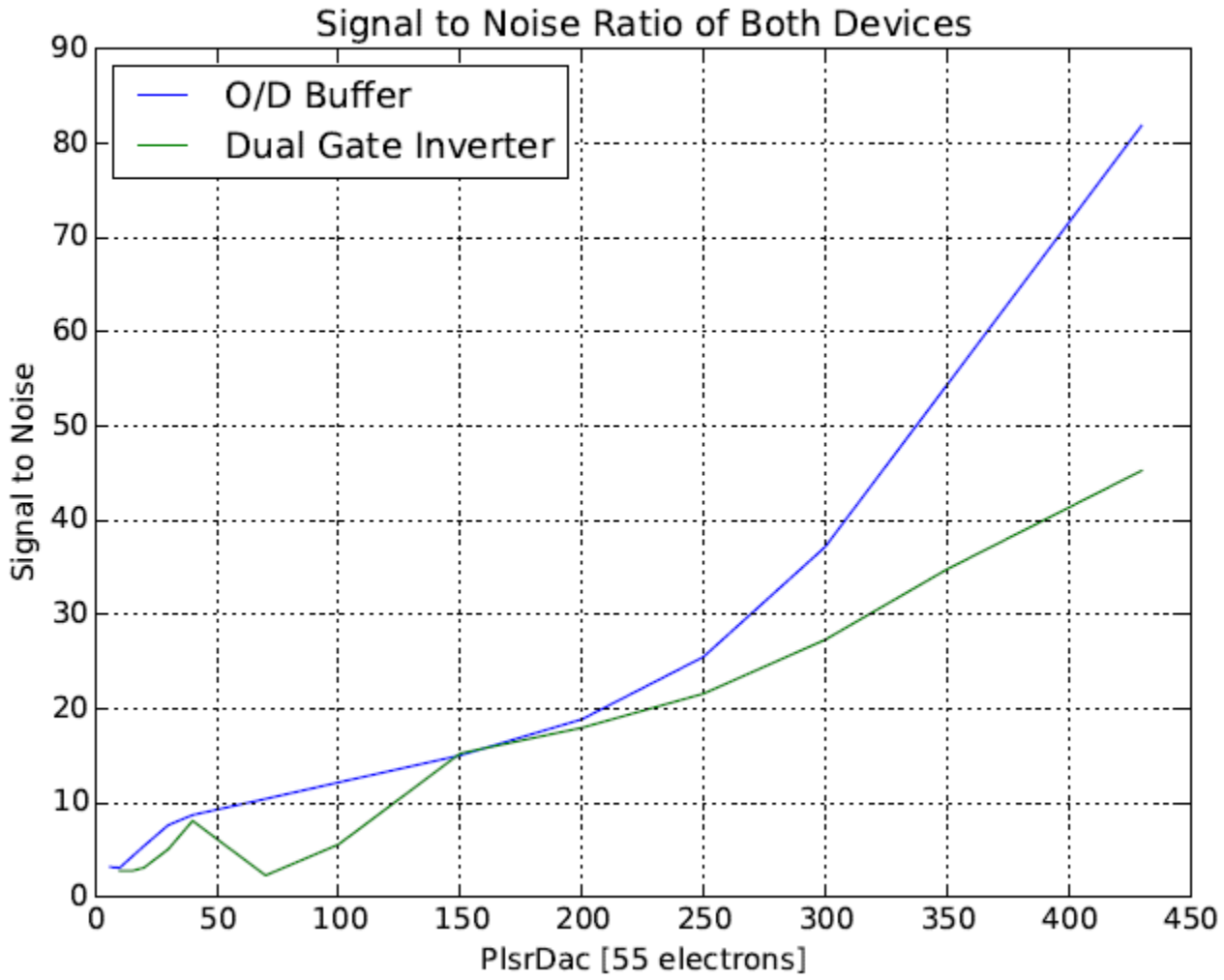


FEA of the FANGS Stave



- Maximum temperature = -4 ^{o}C
- Maximum ΔT within one sensor = 4 ^{o}C
- Power = 1.2 W each FE
- Cooling block = -15 ^{o}C
- Environment = 20 ^{o}C at 2 m/s

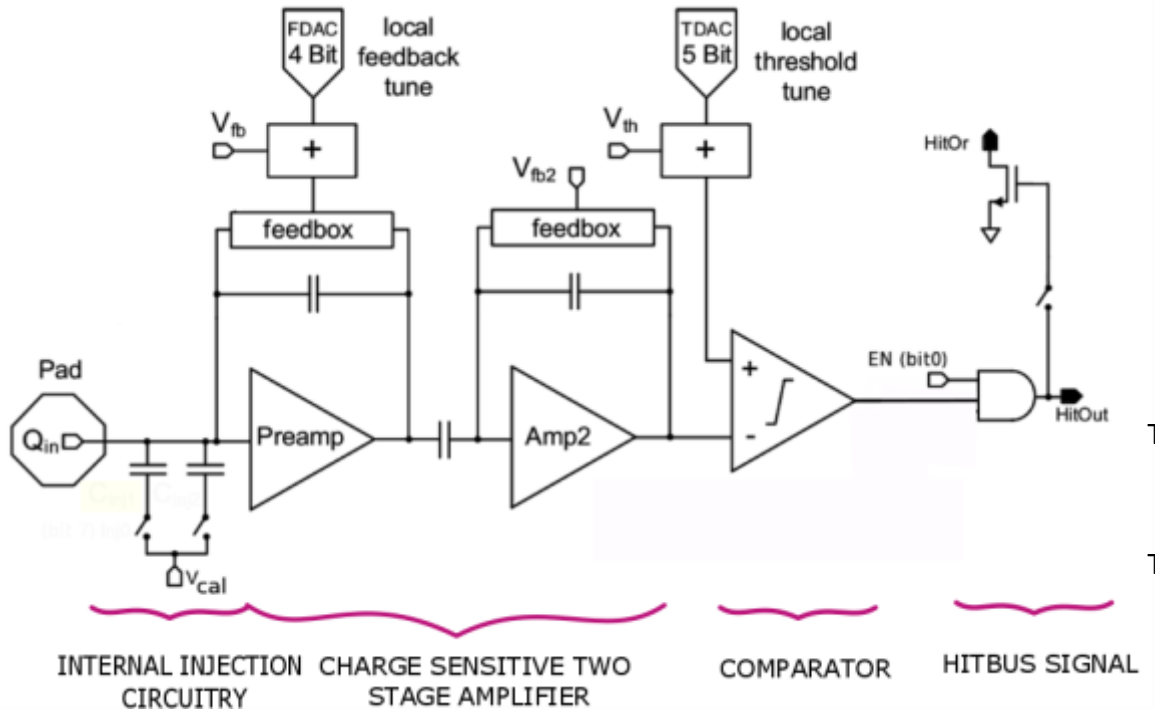
- Proper heat handling
- Low and flat temperature profile

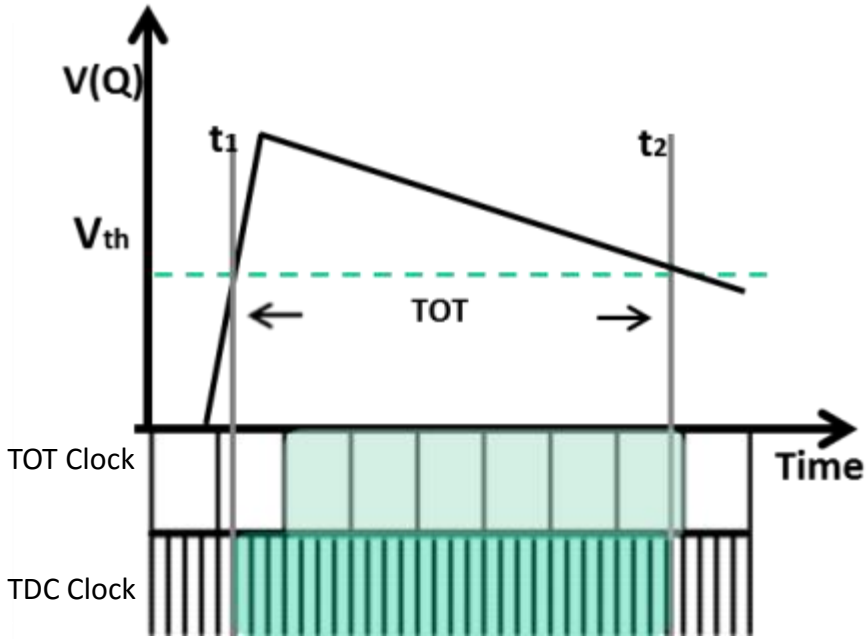

Signal to Noise Ratio of Both Devices
O/D Buffer
Dual Gate Inverter
Signal to Noise
PlsrDac [55 electrons]
0
10
20
30
40
50
60
70
80
90
0
50
100
150
200
250
300
350
400
450

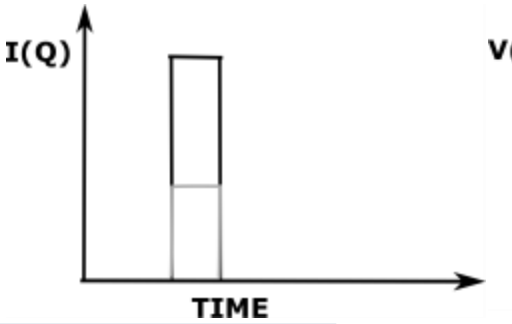
TDC Method

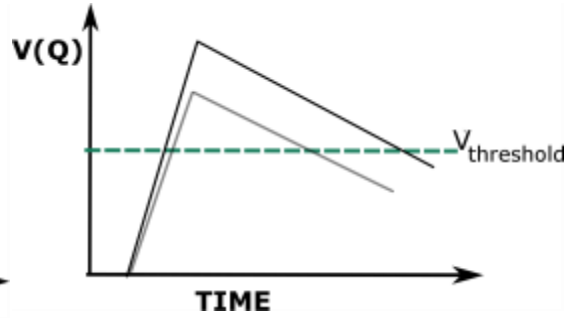
- Upper limit of Yuri Soloviev simulation: 120 KHz
- (6*2)cm^2 = 12
- 5 fe-i4: (0.202 * 0.188)cm^2 = 0.1898 cm^2
- Rate per unit area: 10 KHz/cm^2 : 400 MHz hits/cm^2/s
- But for TDC method, reduced to: one pixel per read out:
- 80*336=26880 pixels/chip
- Assuming:

TDC Method









TOT method previously used with 40 MHz clock
TDC method uses a 640 MHz clock from external FPGA
→ Finer sampling and better energy resolution