ONSEN: Hardware/Firmware Status and Test Plans

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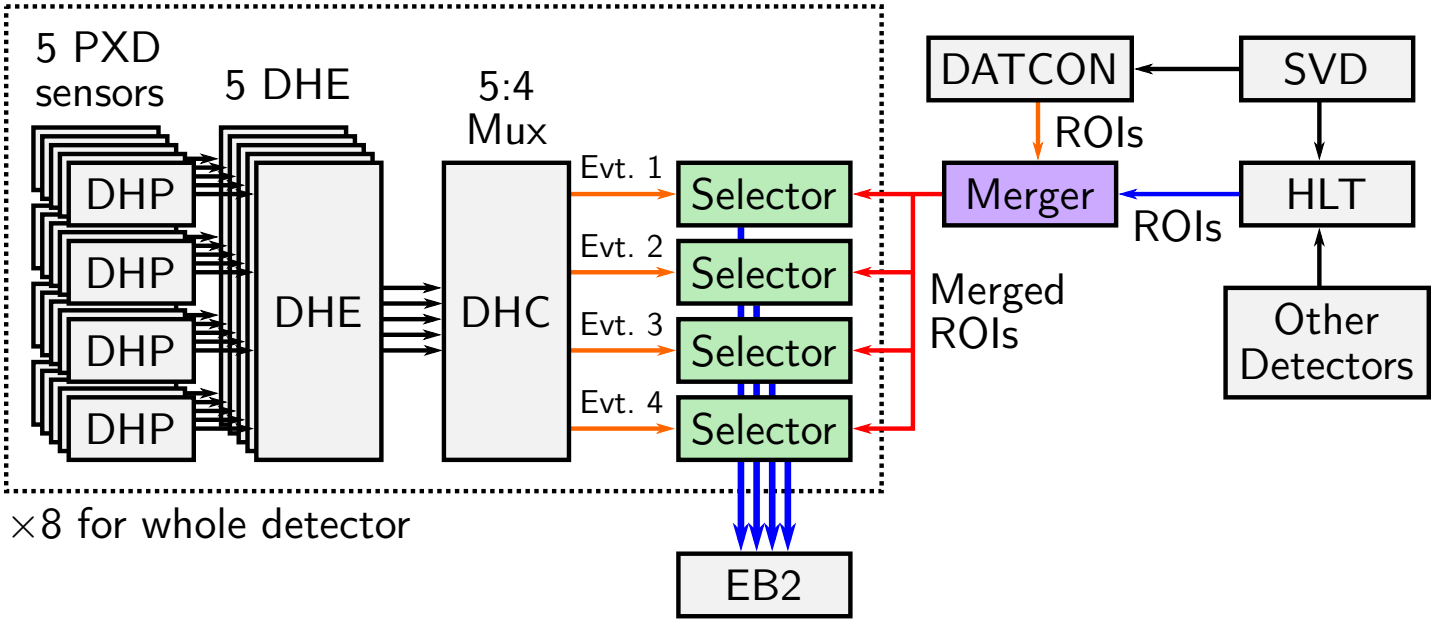
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Belle II

Outline

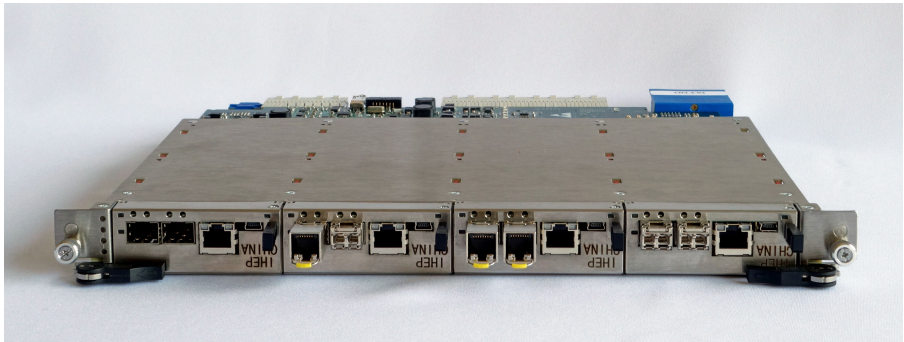
The ONSEN Data Reduction System for the PXD



1. ONSEN Selectors buffer complete PXD data output ($\sim 20\,\mathrm{GB/s}$)
2. ONSEN Merger buffers ROIs generated by DATCON
3. When HLT decision and ROIs for an event arrive, Merger combines HLT ROIs with DATCON ROIs
4. Selectors discard PXD data for HLT-rejected events
5. For other events, Selectors filter PXD data according to merged ROIs
6. Selectors send filtered PXD data to Event Builder 2

ONSEN Setup for Belle II: ATCA Boards and Shelf

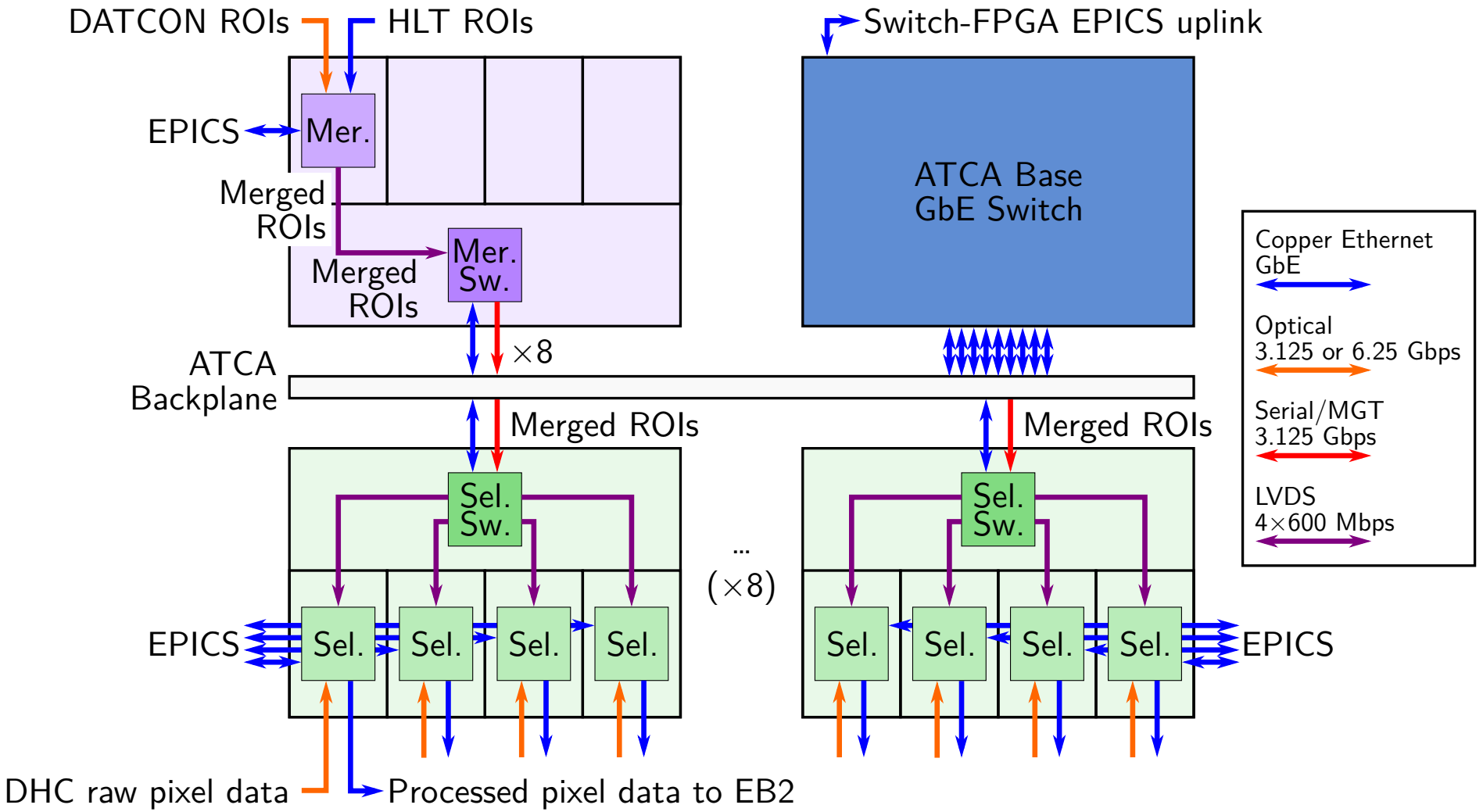
- ONSEN uses 9 ATCA carrier boards with 33 AMC cards



1	2	3	4	5	6	7	8	9	10	11	12	13	14
M		S A0	S E0	S A1	S E1	ATCA Base GbE Switch		S A2	S E2	S A3	S E3		
		S B0	S F0	S B1	S F1			S B2	S F2	S B3	S F3		
		S C0	S G0	S C1	S G1			S C2	S G2	S C3	S G3		
		S D0	S H0	S D1	S H1			S D2	S H2	S D3	S H3		

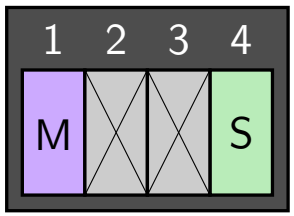
- 1 Merger node (**M**)
- 32 Selector nodes (**S**) for PXD regions A–H and event numbers 0–3

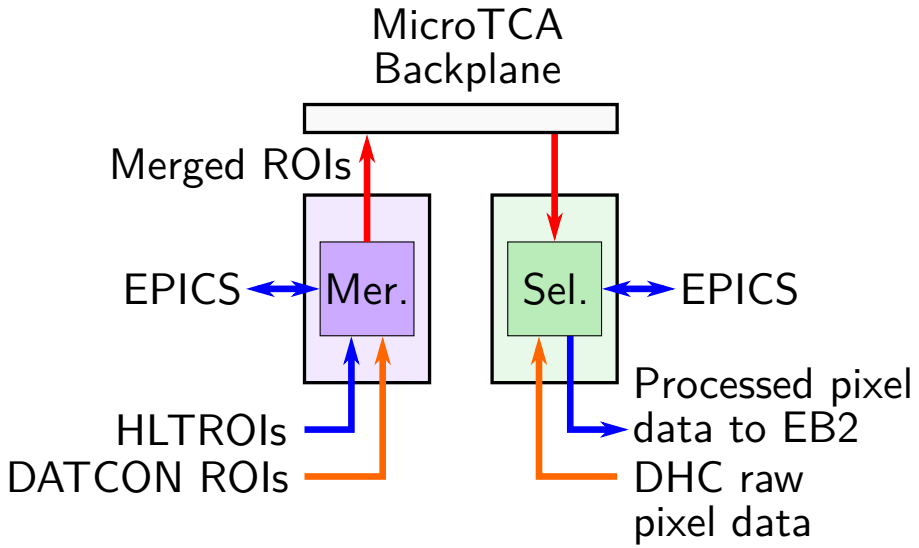
ONSEN Setup for Belle II: Module Interconnection



- 4 types of FPGA firmware required:
  1×Merger, 1×Merger-Switch, 8×Selector-Switch, 32×Selector

ONSEN Test Setup: Pocket ONSEN



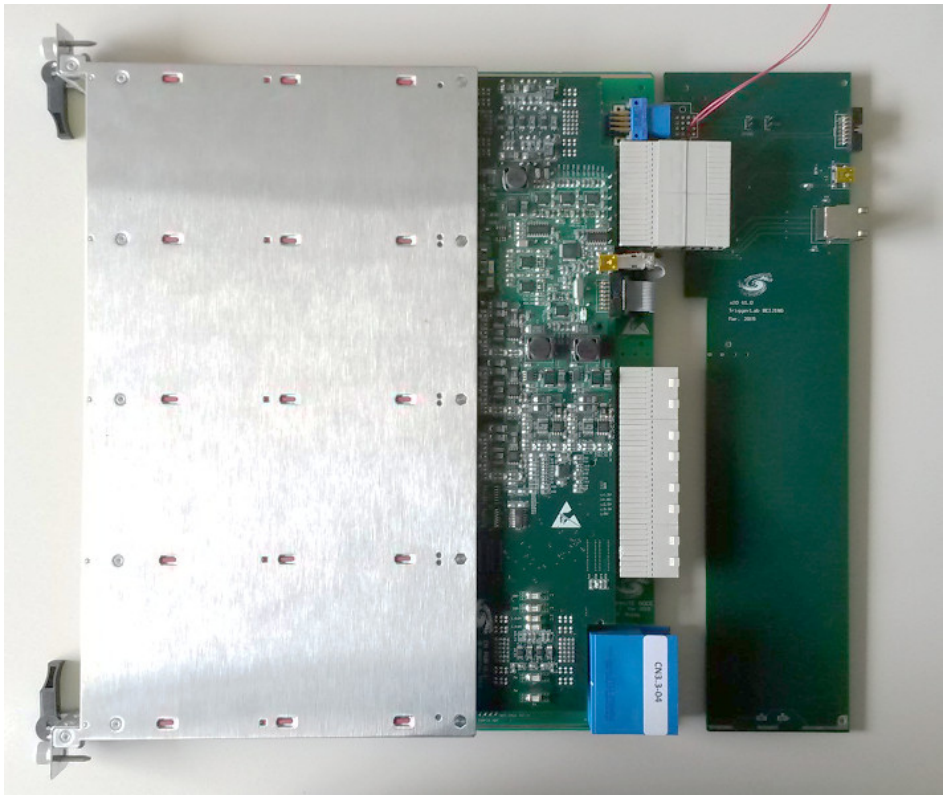


- Alternative setup with a MicroTCA shelf instead of the full ATCA system
- Allows tests of Merger/Selector AMC firmware without ATCA carrier and backplane routing
- Up to 3 Selectors
- Used during DESY test in January 2014

Hardware Status: Final AMC Version, xFP v4.0

- Fixes voltage issue
- From 4 SFP to 2 SFP+
- All components tested OK $\rightarrow$ will be used for ONSEN

Hardware Status: Final Carrier Board Version, CNCB v3.3



- LVDS links to AMC cards and backplane were fixed
- All components tested OK $\rightarrow$ will be used for ONSEN
- New RTM allows rear access to Ethernet, USB, JTAG
- New power supply version is needed due to IPMI issues

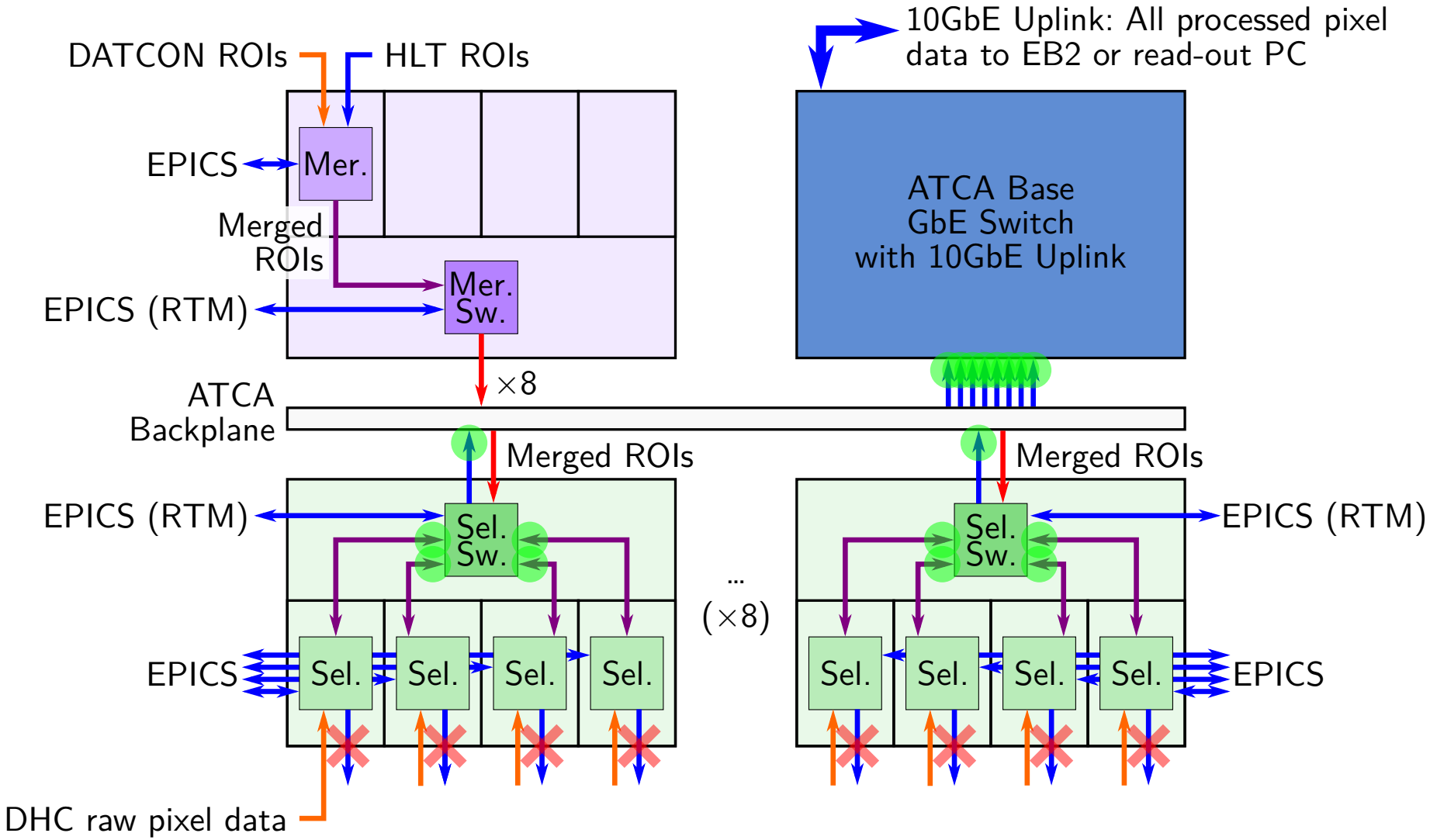
Firmware Status for Merger and Selector AMC cards

- Merger/Selector FPGA firmware in Pocket ONSEN were stable during DESY test in January 2014
- Problem between ONSEN and EB2 was discovered during the DESY test (event number mismatch)
- ONSEN output was changed to a new data format to avoid this problem
- New format was implemented in Selectors and BASF2
- Additional smaller firmware changes were made:
  - Reduction of FPGA resource utilization by FPGA projects
  - Internal buffer size and data format for memory management changed
  - Several fixes for smaller bugs of the ROI filter core
- Merger-Switch and Selector-Switch firmware are not yet ready

Possible Changes for Data Output Path

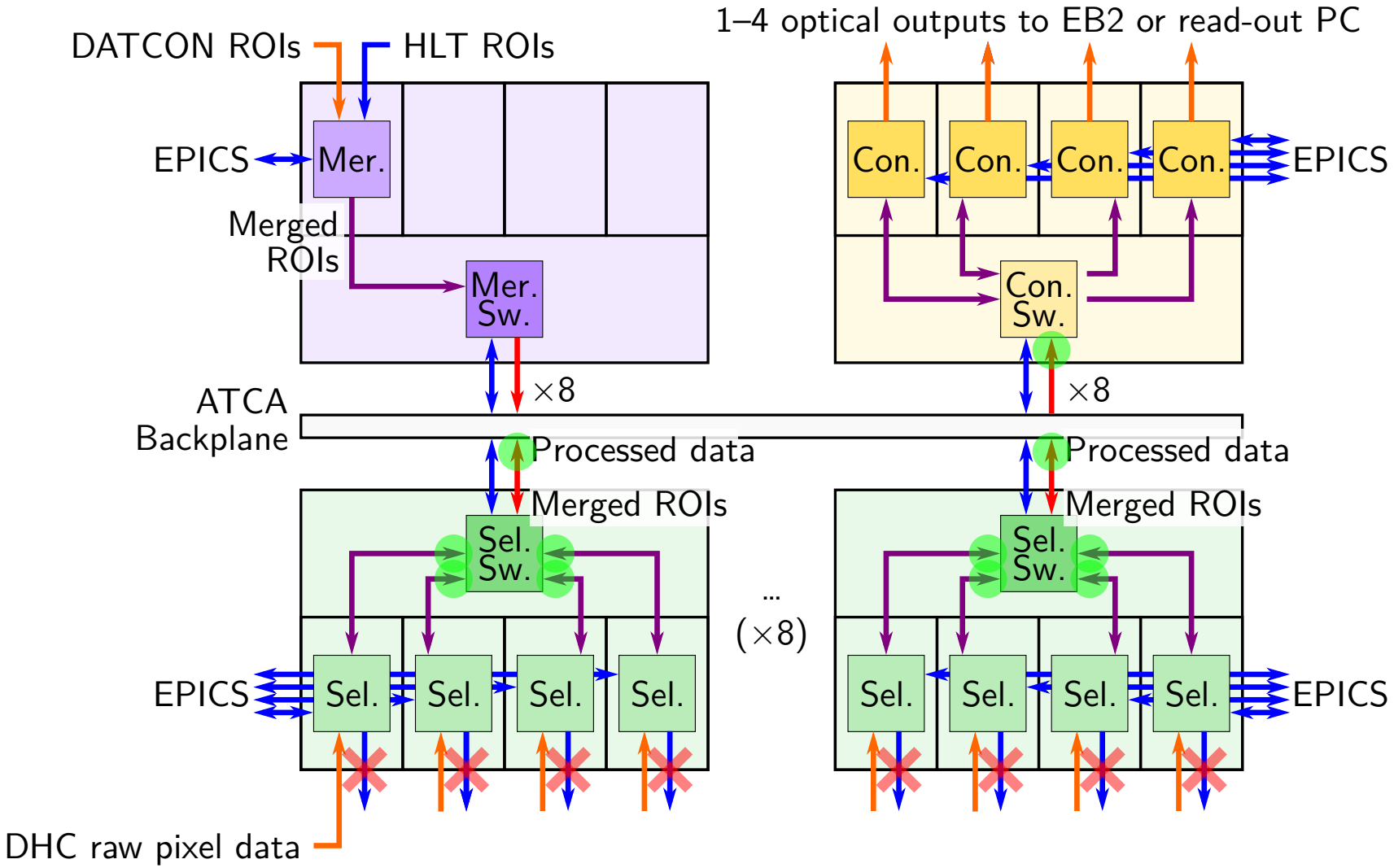
- Motivation: currently 32 (large) SiTCP cores in the Selectors for output to EB2 $\rightarrow$ 32 GbE links for $< 700\,\mathrm{MB/s}$
- In each FPGA, SiTCP covers $\sim 20\,\%$ of slices
- OK for current firmwares, but for possible future changes/upgrades, reduction of firmware size is desirable
- To remove SiTCP from Selector nodes:
  - Combine data from 4 Selectors on the Switch FPGA
  - Send out combined data using the ATCA backplane
- Option 1: Selector board $\rightarrow$ ATCA Ethernet Switch $\rightarrow$ EB2
- Option 2: Selector board $\rightarrow$ new ONSEN Concentrator board $\rightarrow$ Read-out PC $\rightarrow$ EB2

Possible Changes for Data Output Path: Option 1



- Possible issue: switch bandwidth
- Feasibility will be investigated in the next months

Possible Changes for Data Output Path: Option 2



- Completely removes dependence on SiTCP
- More firmware developments and hardware required

Migration to the Cluster Format

- In the future, data format from DHC to ONSEN will be changed from zero-suppressed DHP format to cluster format
- Firmware side: Cluster processing is implemented in the Selector nodes (ROI filter core by D. Münchow)
- Not tested yet with DHC data
- Will not be used in the 2016 DESY test
- Software side (BASF2): Decoding/unpacking of clusters and DQM module implemented by K. Lautenbach
- Decoder performance: 3250 events/s on 1 CPU@1.6 GHz. Events with 20 clusters per trigger and per half-module (7 pixels per cluster in V-shape).

Cluster data format integration

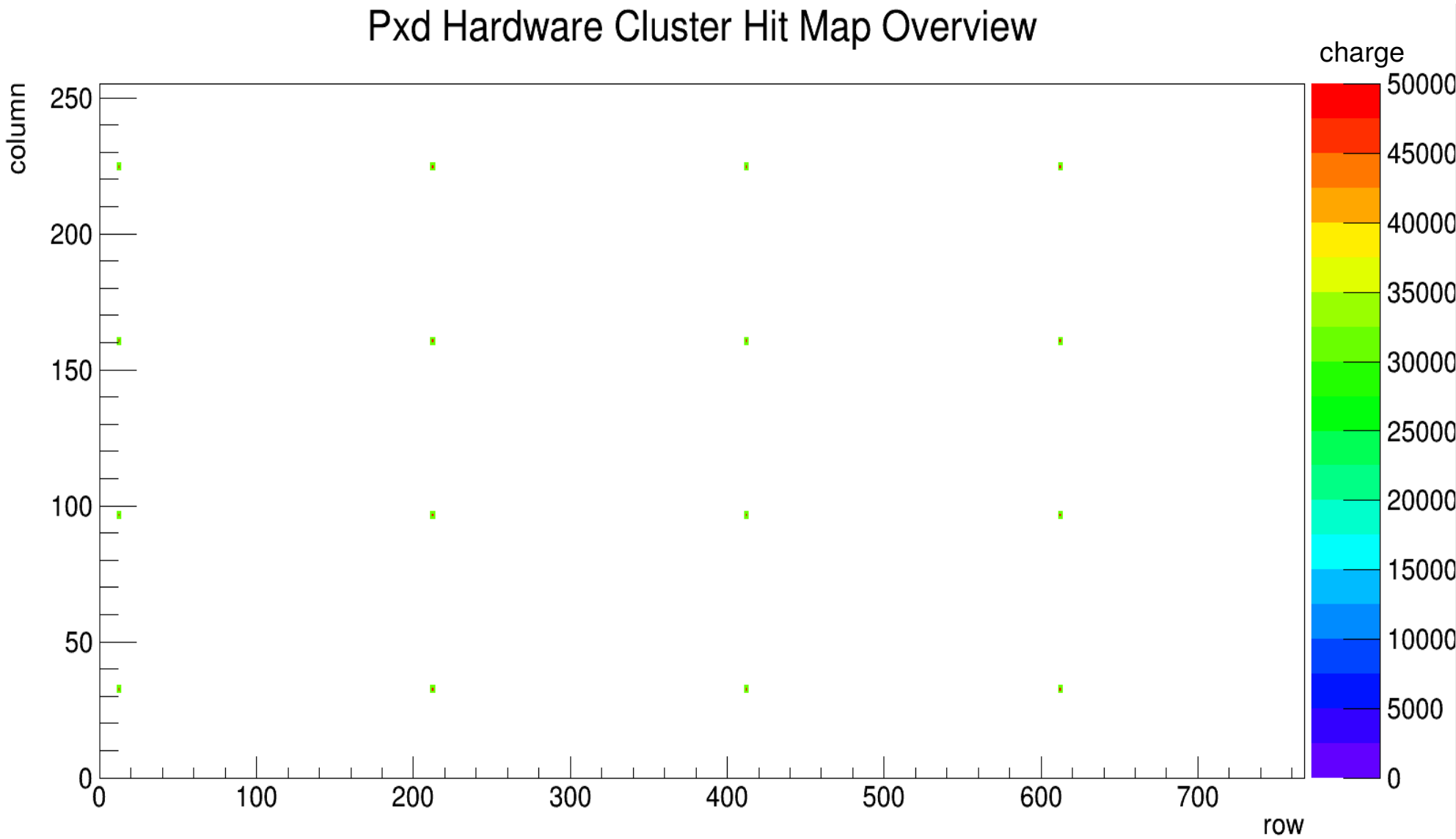
- Cluster data format was integrated in basf2
  - → PXDRawCluster class, saves length and packed information
  - → PXDHardwareCluster class, saves unpacked cluster information
    - → row, column, adc of each pixel in cluster
    - → VXD ID of the cluster
    - → seed pixel address and charge
    - → total cluster charge

- PXDUnpacker unpacks Data to PXDRawCluster

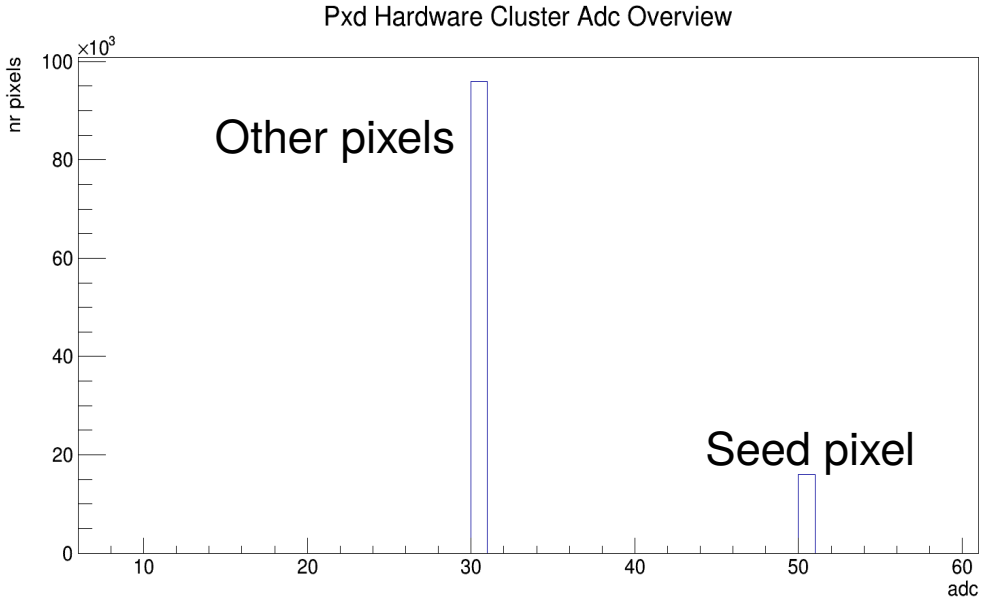
- PXDHardwareClusterUnpacker unpacks PXDRawCluster to PXDHardwareCluster

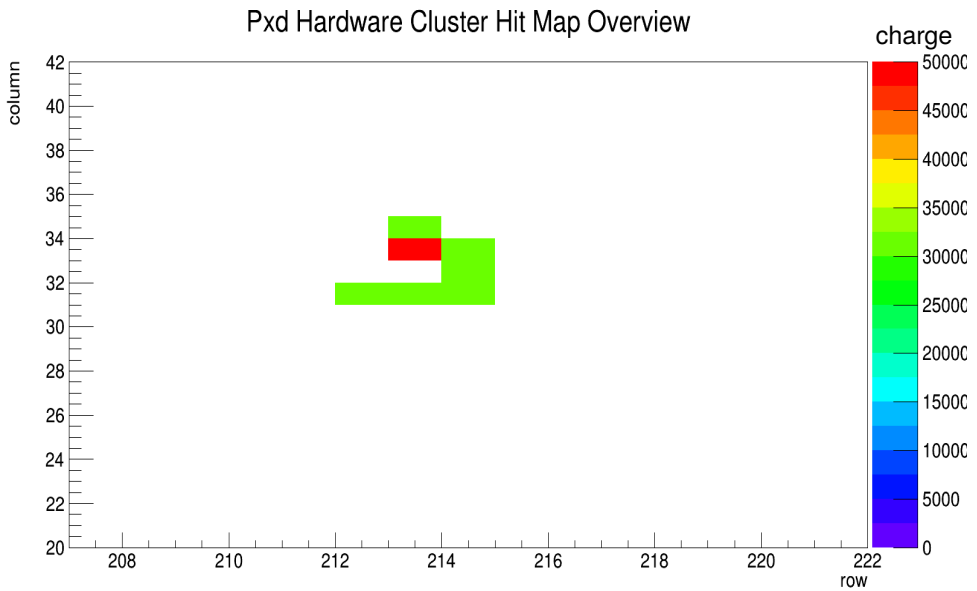
- DQM module to monitor the unpacking process was integrated (PXDHardwareClusterDQM)
  - → monitors cluter per half ladder
  - → cluster packet size
  - → pixel in cluster
  - → cluster hit and adc map
  - → total cluster charge and seed pixel charge

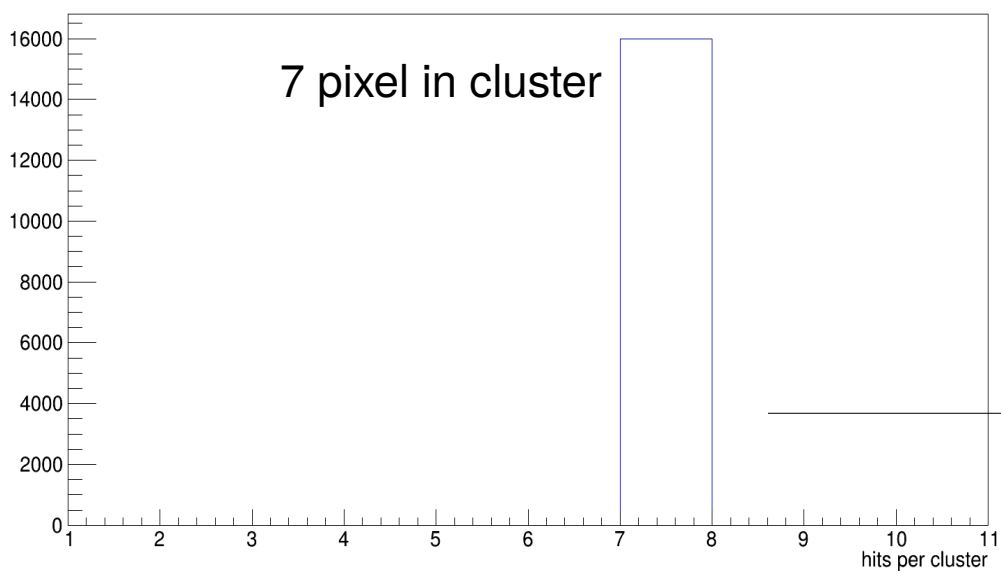
Cluster data format integration

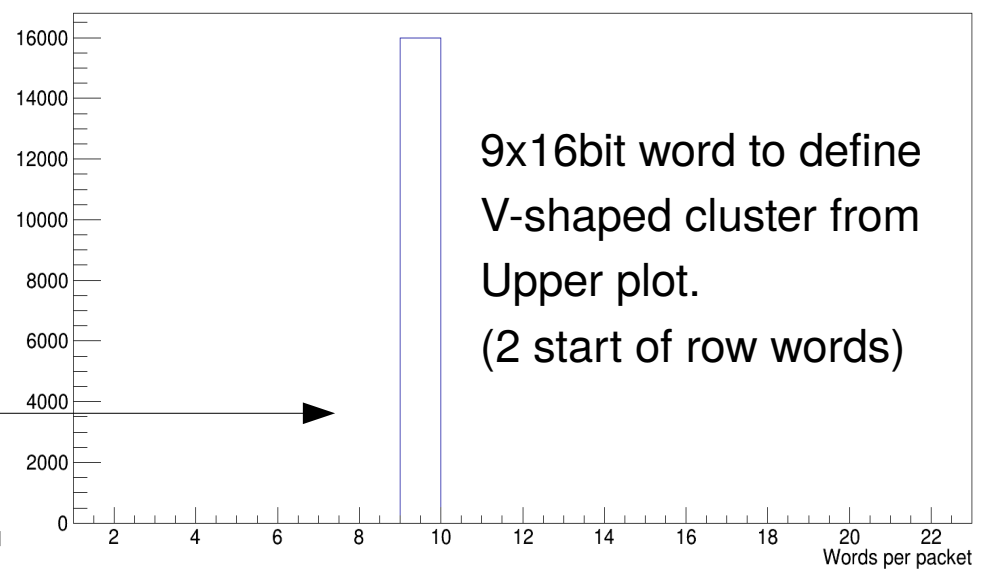


Cluster data format integration









9x16bit word to define V-shaped cluster from Upper plot.
(2 start of row words)

Remaining Issues

- Carrier boards must be integrated into the system's data flow
- Cluster data format must be fully included and tested
- Recurring issue during tests: Sudden drop of data rate from $\sim 100\,\mathrm{MB/s}$ to below $1\,\mathrm{MB/s}$
  $\rightarrow$ Possible issue with arbitration of memory-controller access; will be investigated in the next months

Rate Test at KEK in October 2015

- Test of the PXD read-out chain: DHC $\rightarrow$ ONSEN ($\leftarrow$ HLT) $\rightarrow$ EB2
- Participants from Gießen: Dennis Getzkow and Klemens Lautenbach
- DHC and Pocket ONSEN system are already at KEK, but not connected
- Artificial triggers will be generated and distributed with B2TT/FTSW
- DHC will produce pseudo-random pixel data
- Limits for trigger rate, data rate, event size, etc. will be probed
- Results will be shown at the B2GM

DESY Test in April (?) 2016

- ONSEN setup will be carrier-board based, *not* Pocket ONSEN like in the 2014 DESY test
- 2 carrier boards, 1 Merger AMC, up to 4 Selector AMCs
- ATCA shelf might be a 2-slot "pizza box" shelf

- Allows to test ROI distribution over the ATCA backplane for the first time
- Requires some more firmware work, but no show-stoppers foreseen
- No cluster format, otherwise firmware is more-or-less final

ONSEN Commissioning at KEK

- New hardware ordered: Two carrier boards and 8 AMC cards for each Gießen and KEK
- I will work at KEK for a year starting from November, starting with ONSEN setup when the first hardware arrives
- After functionality of the carrier-board architecture is verified, the remaining ONSEN hardware will be ordered
- ONSEN setup at KEK will be finished at the end of 2016
- ONSEN will be present and ready for VXD commissioning
- In parallel, a Pocket ONSEN system can be set up for BEAST II phase 2 PXD read-out