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Hybrid 5 Testing

8th Belle II VXD workshop
9th-11th September 2015, Trieste

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Hybrid 5 Testing

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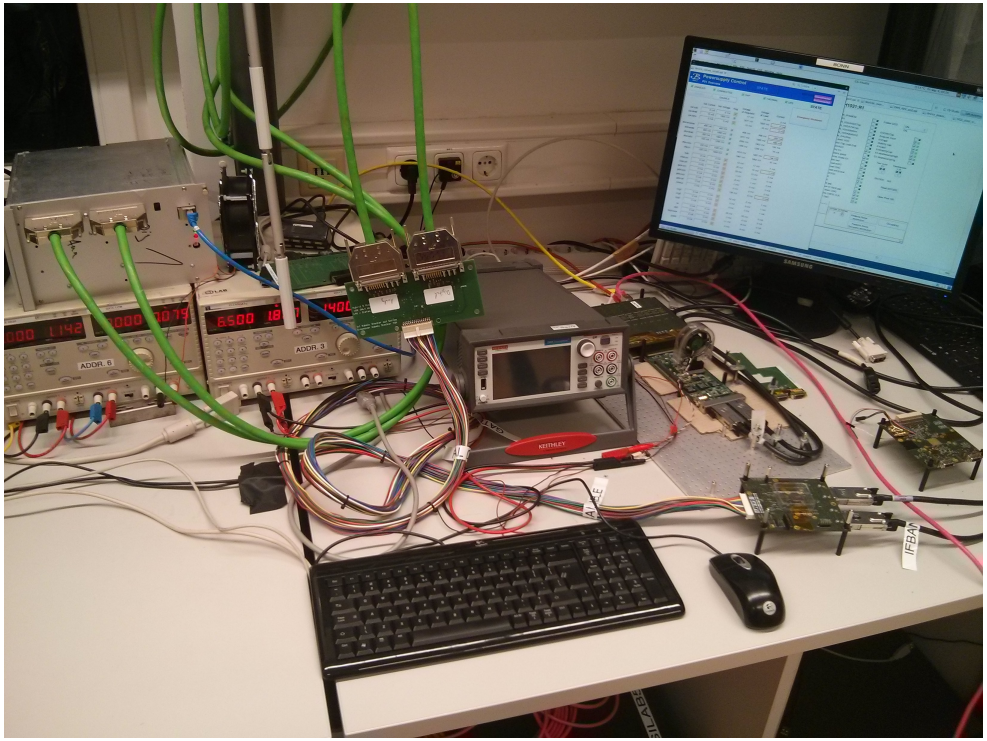
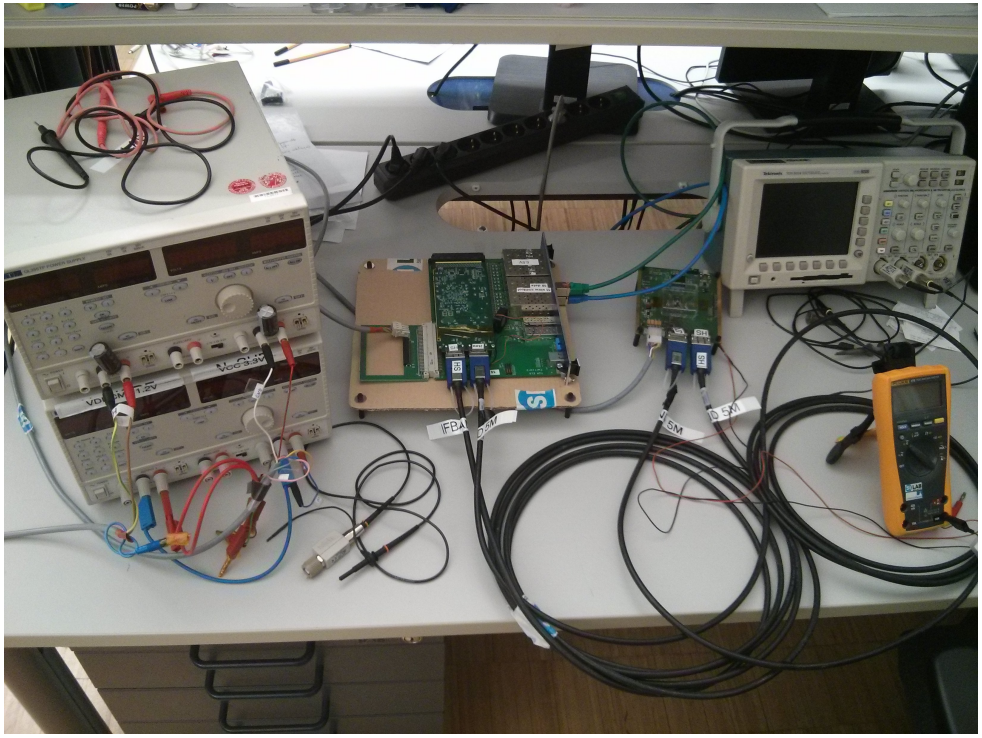
- Setup and stock in Bonn
- DHP <-> DCD communication
- DHE current source for ADC testing
- DHP memory dump bug
- Future plans

Setups in Bonn

- Setup 1:
  DHH and PS
  for Hybrid 5 testing

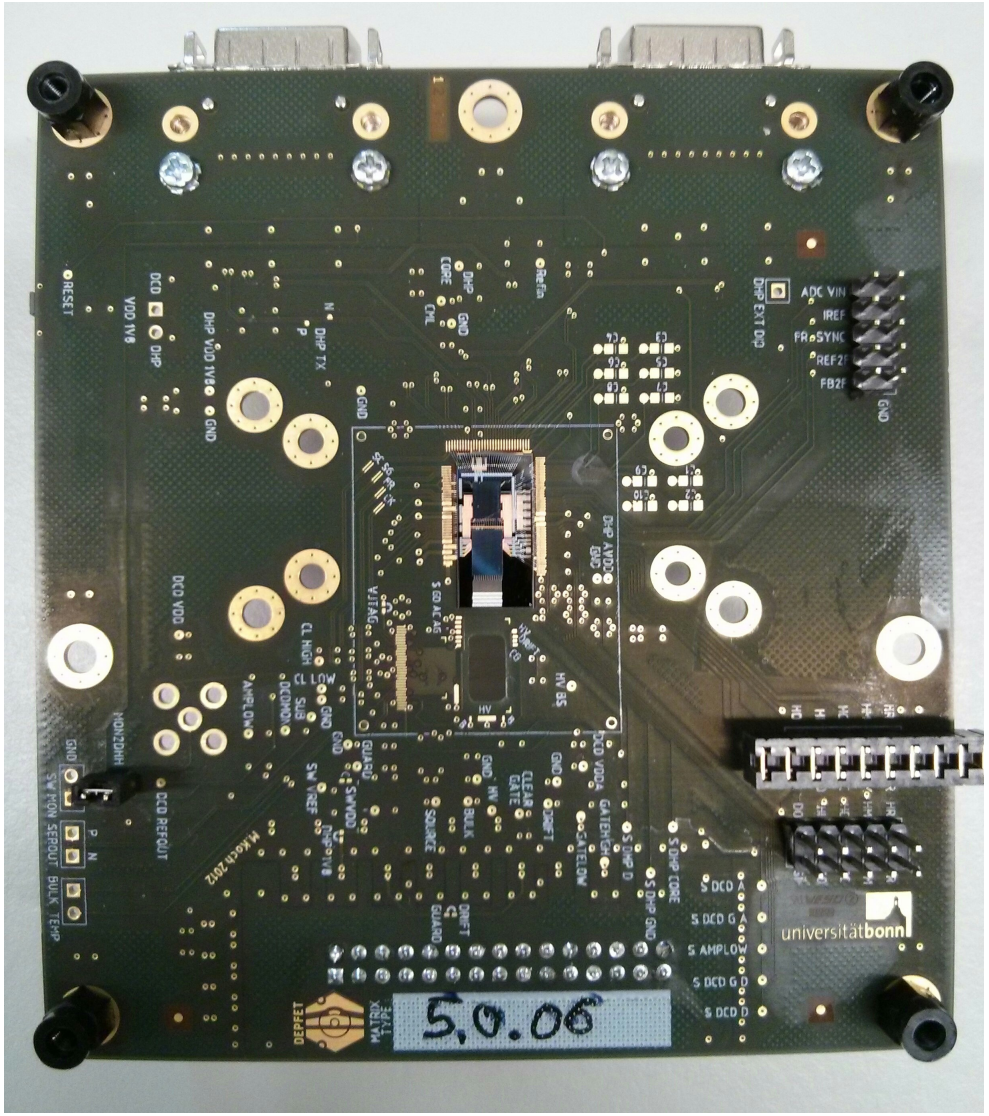


- Setup 2:
  DHH
  for debug card (bonded DHP + FPGA)
  or needle card (contacted DHP + FPGA)

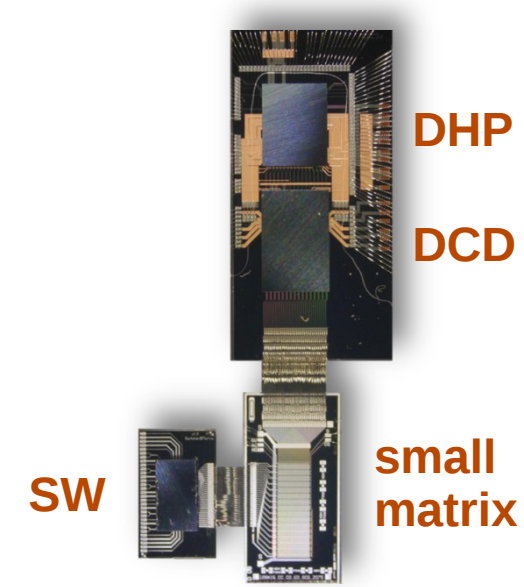


- Third setup coming up with DHH and PS for Hybrid 6 testing

The Hybrid 5



[Hybrid 5.0.06]



- Can be equipped with
  1 DHP, 1 DCD, 1 switcher and 1 small matrix
- ASICs are bump-bonded to wirebond adapters
- Connection via 2 Infiniband cables and one multipole power connection

Hybrid 5 Stock and Status

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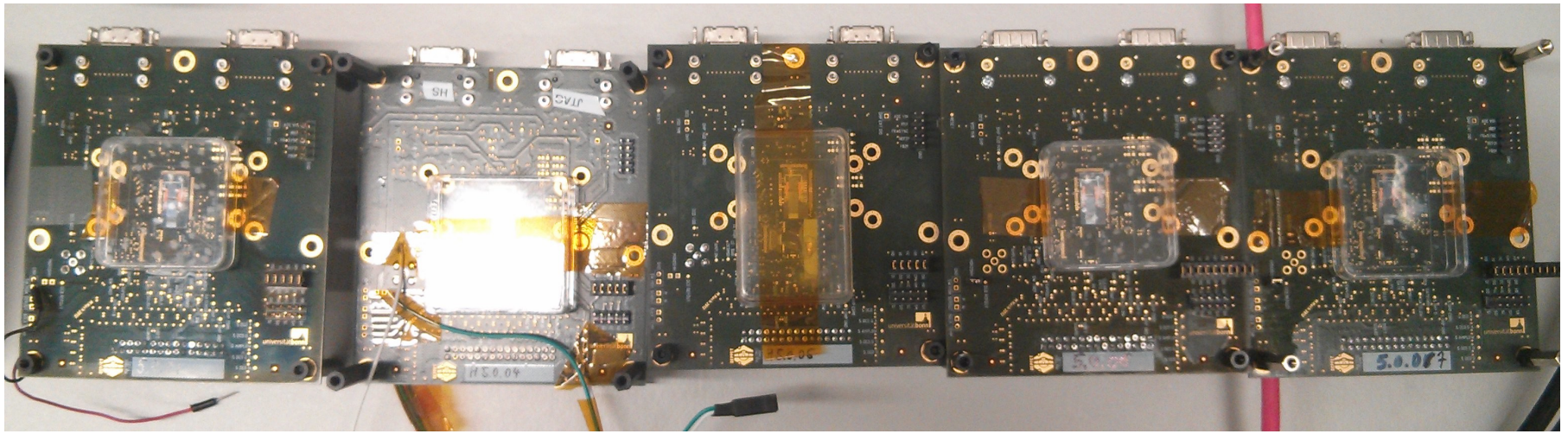
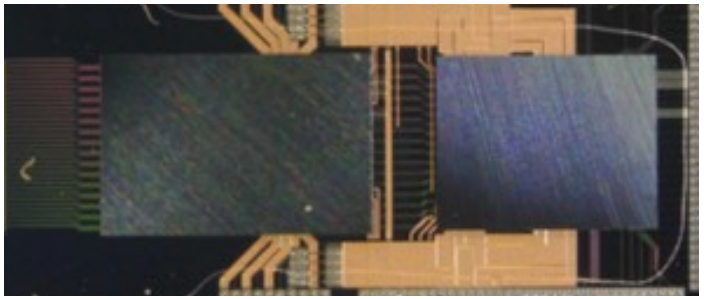
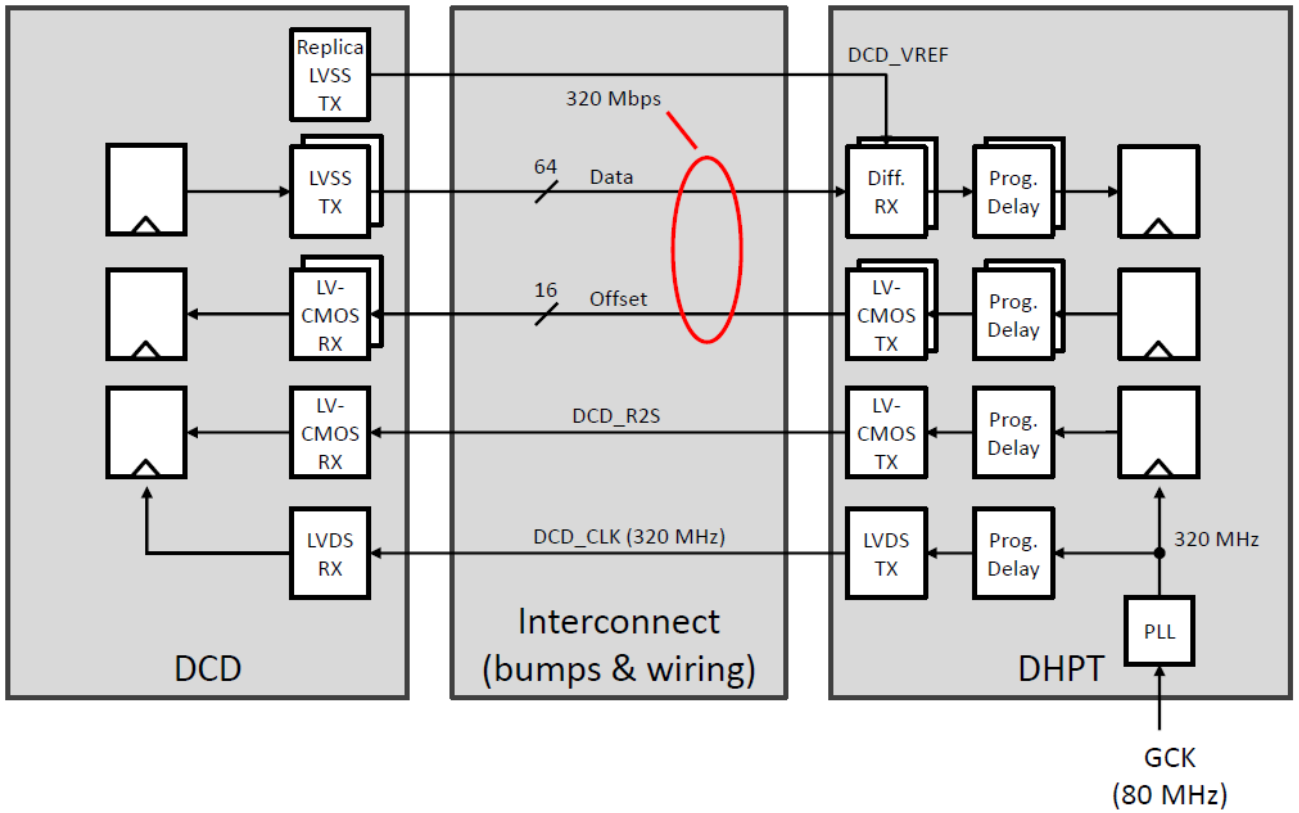
- 2 functioning Hybrid 5 assemblies in Bonn (H5.0.06, H5.0.07)
- 20 new PCBs are ordered and will be equipped with passives in Munich
- ASICs, matrices and wirebond adapters:
  - 22 DHPT1.0 (8 tested and okay)
  - 1 DCDBpp
  - 3 SwitcherB1.8G
  - Wirebond adapters for DHP and DCD
  - 2 small PXD9 Belle II type matrices



DCD – DHP Communication

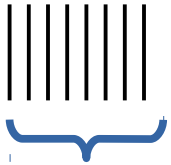




- General reference clock (GCK) ~ 80 MHz (76.3 MHz) supplied to DHP
- PLL produces 320 MHz clock for signal transmission DCD ↔ DHP
- Programmable delay in DHP for every transmission line
- All delay registers 4 bit → 16 settings

DCD – DHP Communication: Test Pattern

- 64 data lines between one ASIC pair arranged into 8 buses with 8 links each

64 links =  x 8 ; 8 bit bus transfers one 8 bit ADC value per clock cycle

, 32 clock cycles needed to transfer all 256 ADC channels of the DCD

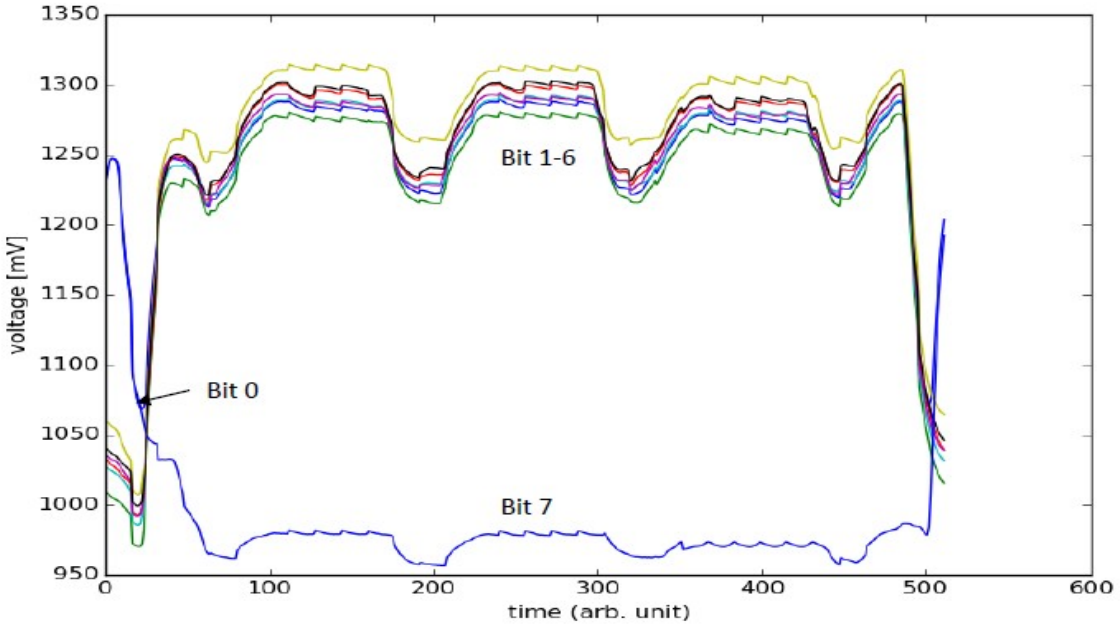
8 bit bus

- For testing of the DCD – DHP communication a test pattern is generated by the DCD
- Unchangeable 32 byte sequence:

ADC Index	29	30	31	0	1	2	3	…	29	30	31	0
MSB	0	0	0	1	0	0	0	…	0	0	0	1
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
LSB	1	1	0	1	0	1	1	…	1	1	0	1
Value	**127**	**127**	**0**	**-127**	**0**	**127**	**127**	…	**127**	**127**	**0**	**-127**

DCD – DHP Communication: Test Pattern

- Reference voltage V_{ref} can be overwritten on Hybrid 5
  → crude measurement of signal possible by scanning V_{ref} and delay



ADC Index	29	30	31	0	1	2	3	…	29	30	31	0
MSB	0	0	0	1	0	0	0	…	0	0	0	1
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
LSB	1	1	0	1	0	1	1	…	1	1	0	1
Value	**127**	**127**	**0**	**-127**	**0**	**127**	**127**	…	**127**	**127**	**0**	**-127**

DCD – DHP Communication: Test pattern

- Reference voltage V_{ref} can be overwritten on Hybrid 5
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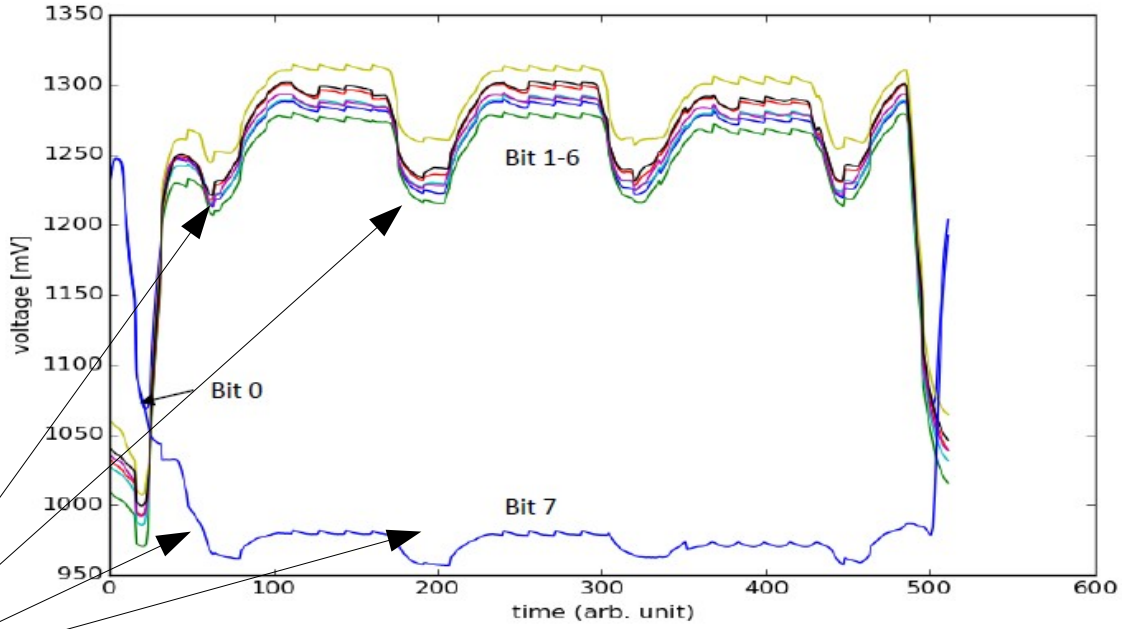
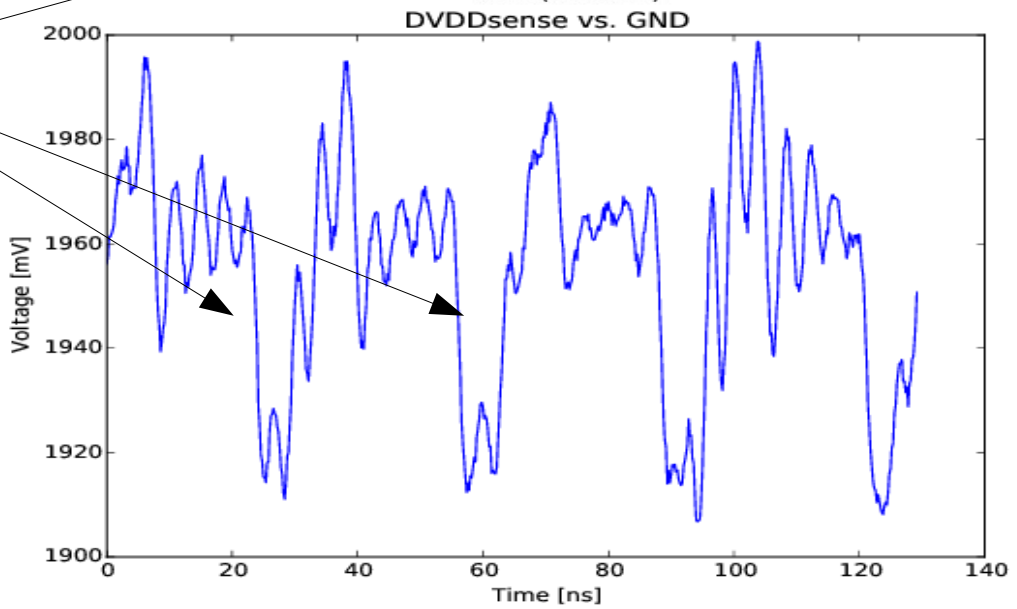
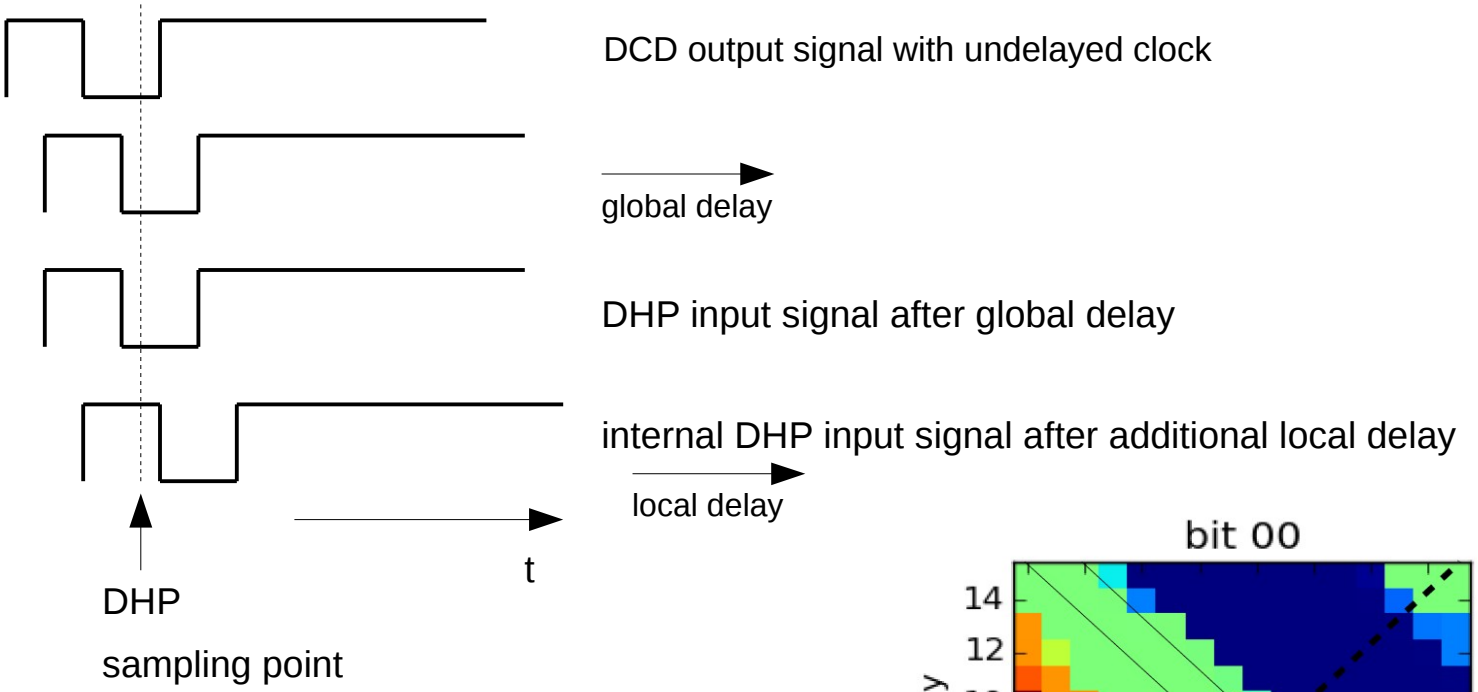


- Structure of one voltage drop per 2 GCK cycles also visible in sensed digital supply voltage of DCD

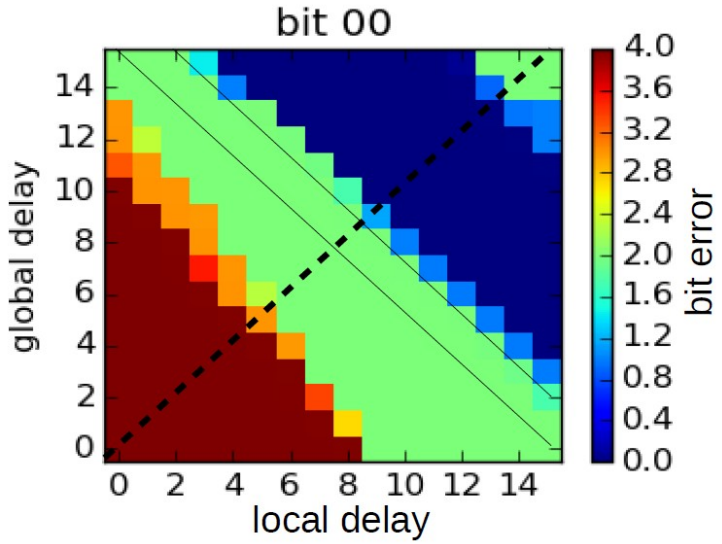


DCD – DHP Communication: Data Line Delays

- Delays shift DCD output and DHP sampling times



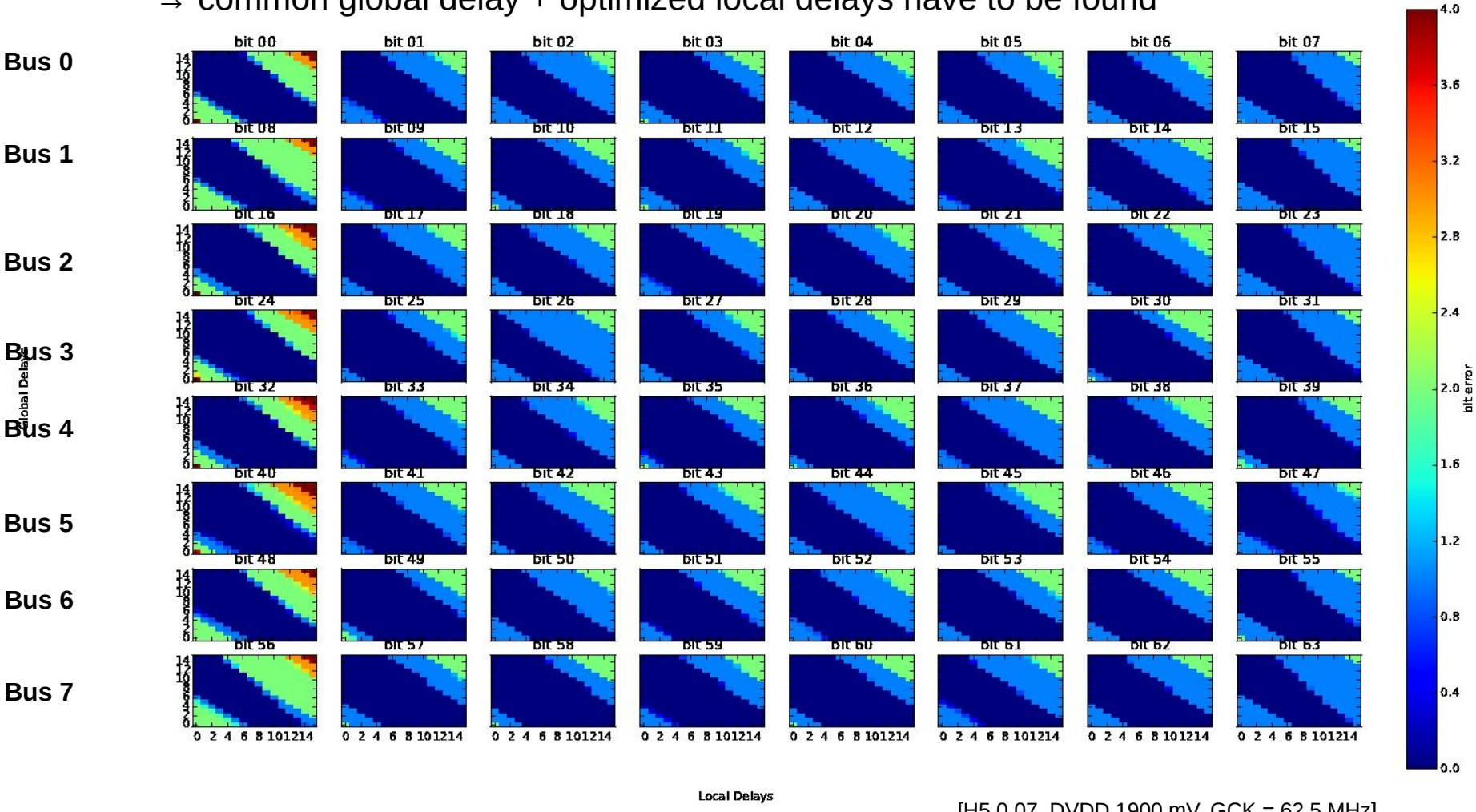
- Signal is scanned over delay settings and compared to testpattern



Delay Space per Data Line

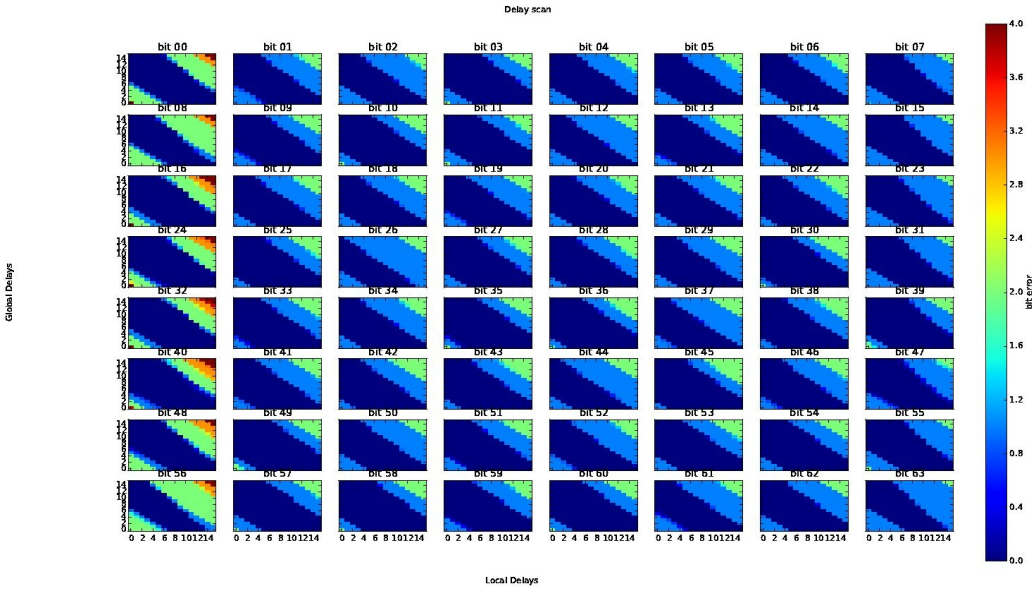
- One “zero bit error” band per link

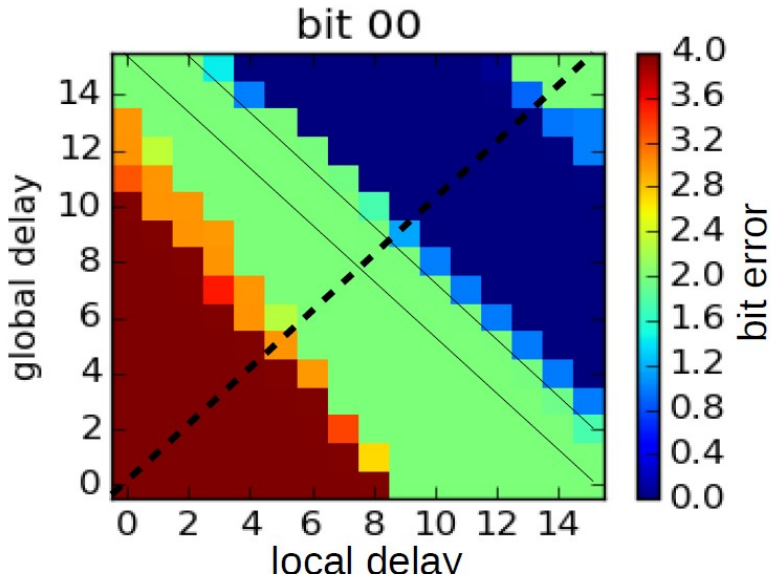
  → common global delay + optimized local delays have to be found



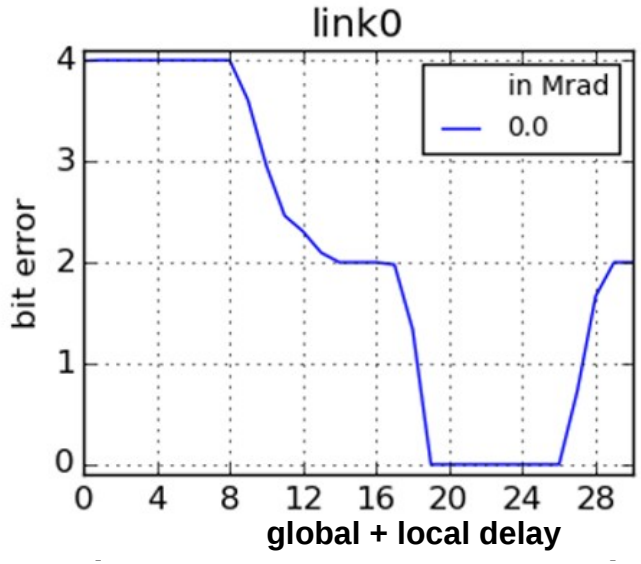
[H5.0.07, DVDD 1900 mV, GCK = 62.5 MHz]

Delay Space per Data Line



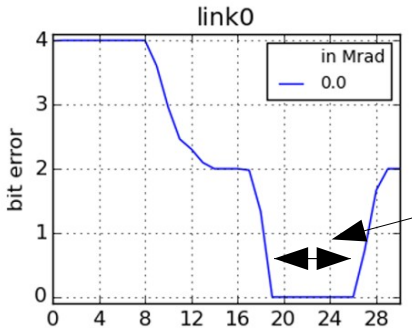


- Global and local setting add the same amount of delay
- “Delay tolerance” measured for each line
- Size of tolerance determined by duty cycle distortion and fall/rise times
  → signal size, DHP input capacitances
- Measure of data link quality



Delay Tolerance Depending on Clock Speed

- Delay measurements for 7 EMCM ASIC pairs were extensively analyzed by Philipp and Benjamin (Göttingen) and the link performance was categorized according to delay tolerance:



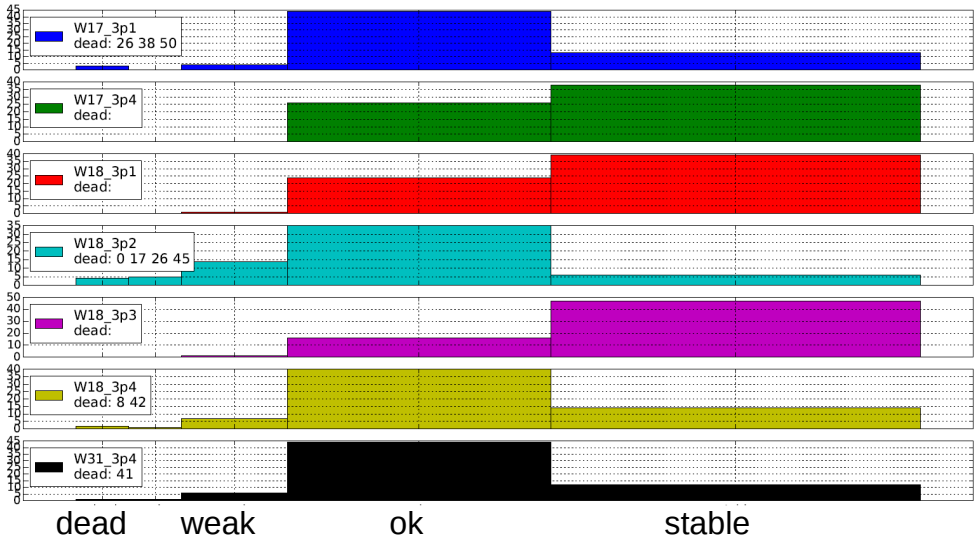
delay tolerance

0 = dead

1-2 = weak

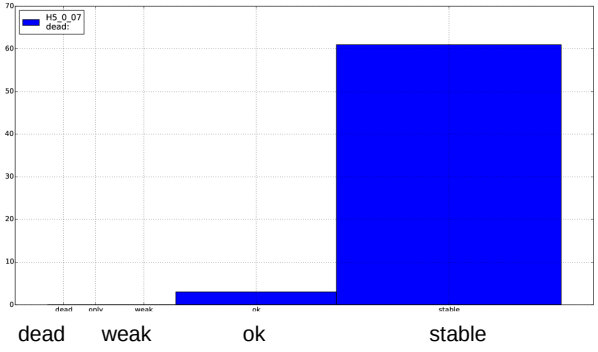
3-7 = ok

8-15 = stable

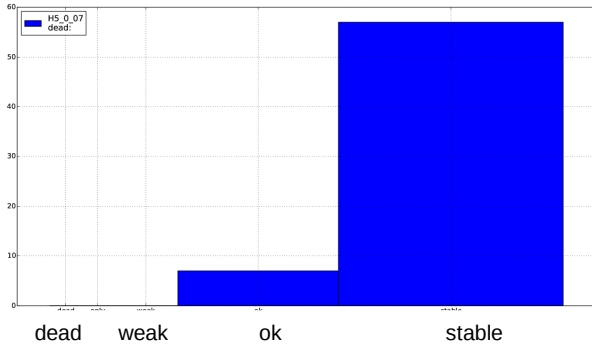


Hybrid5.0.07:

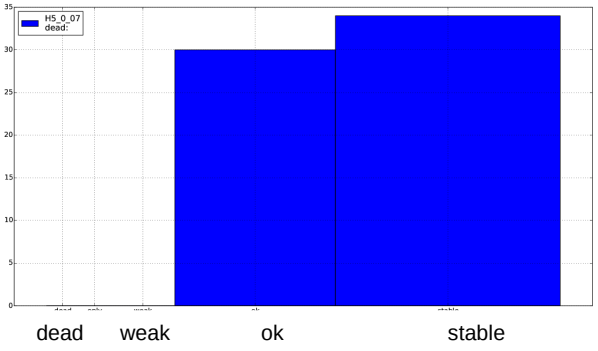
GCK 62.5 MHz



GCK 67.8 MHz

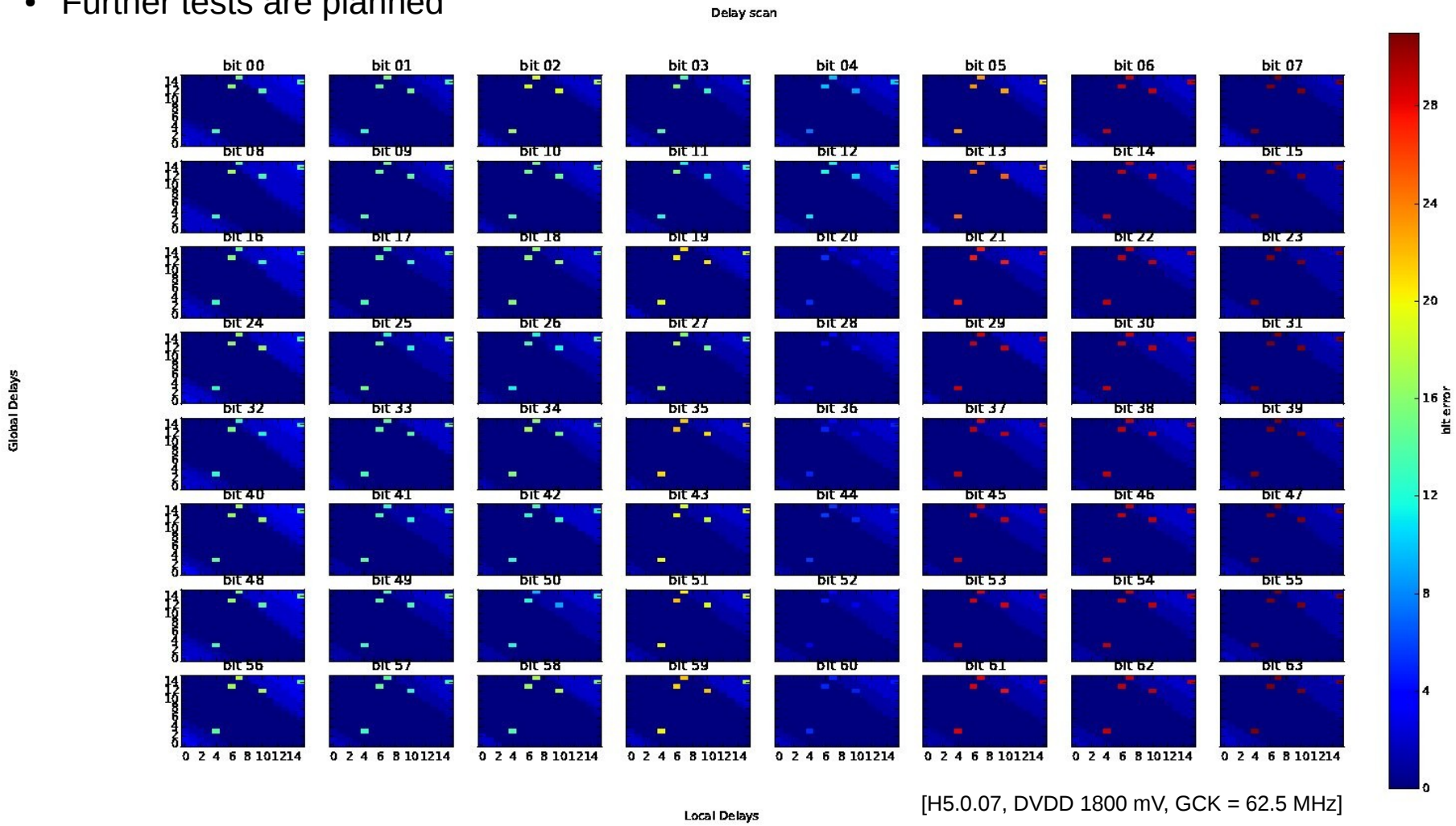


GCK 76.3 MHz



Other Parameters Influencing DCD ↔ DHP Com.

- Digital DCD supply voltage plays a role in stability of data transmission
- Further tests are planned

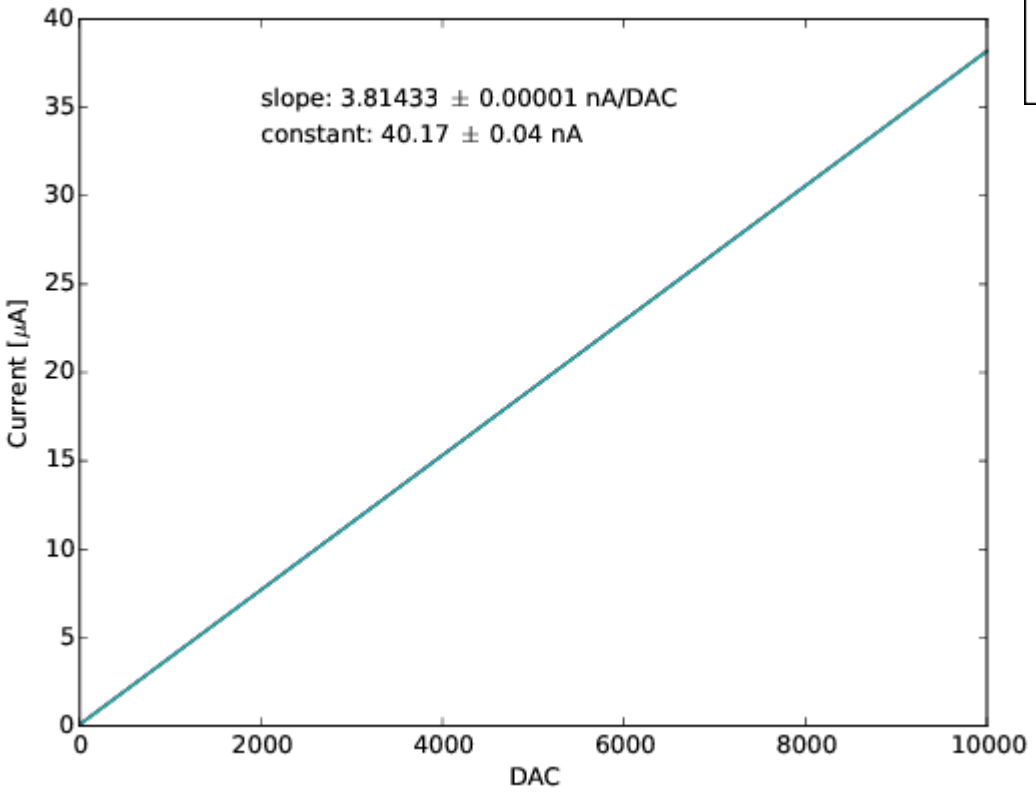


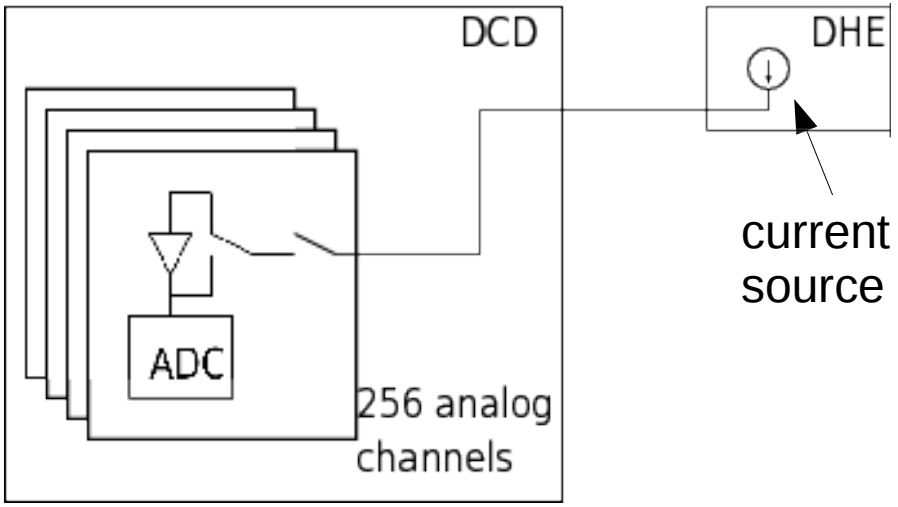
[H5.0.07, DVDD 1800 mV, GCK = 62.5 MHz]

ADC Characterization – DHE Current Source

- External current source on DHE was put into operation and characterized

DHE v1.0 add-on current source

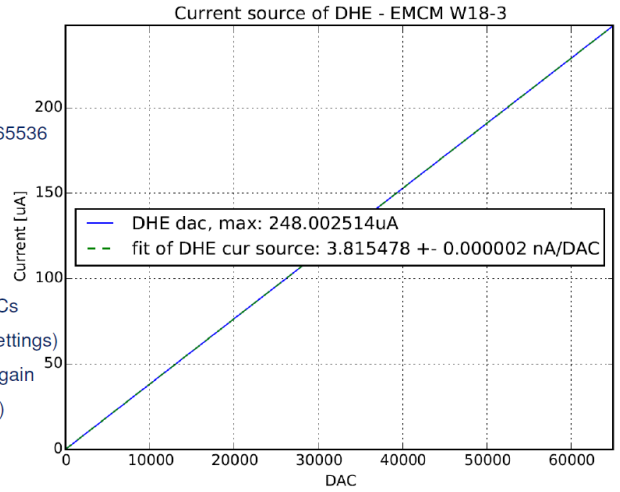




for comparison:

DHHv3.2 Internal Current Source

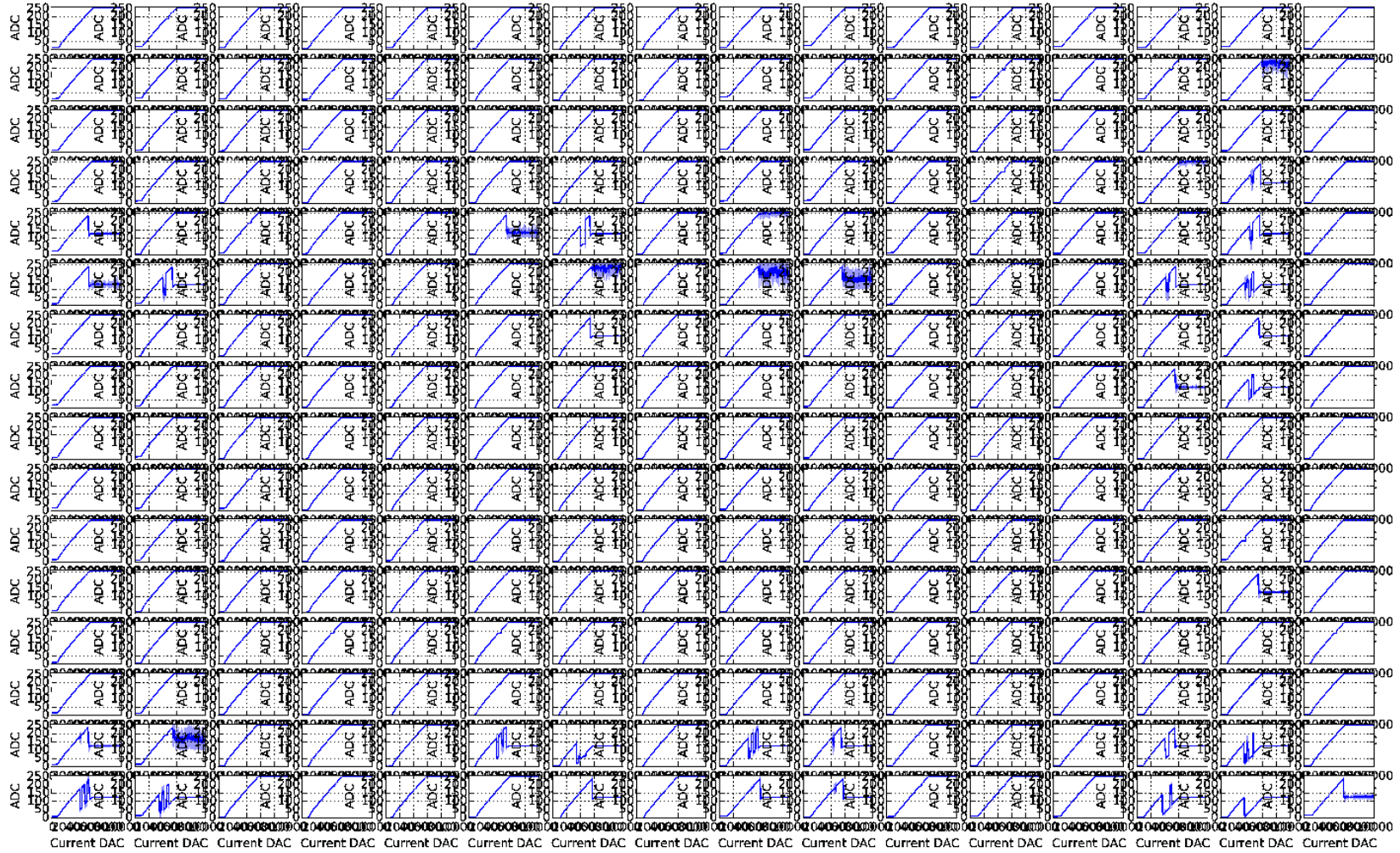
- linear
- low noise
- 248μA in 65536 steps
- 16-35 DACs (current settings) per ADU (gain G=1, G=4)



11.05.2015 Felix Müller, 19th DEPFET workshop

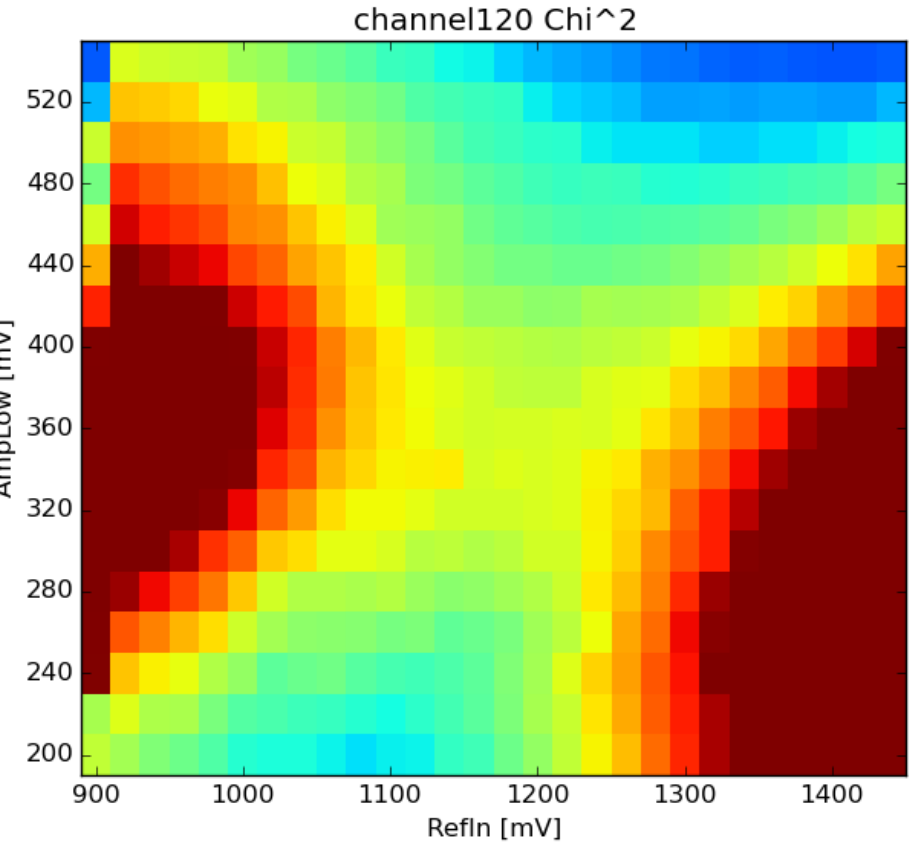
ADC Characterization – DHE Current Source

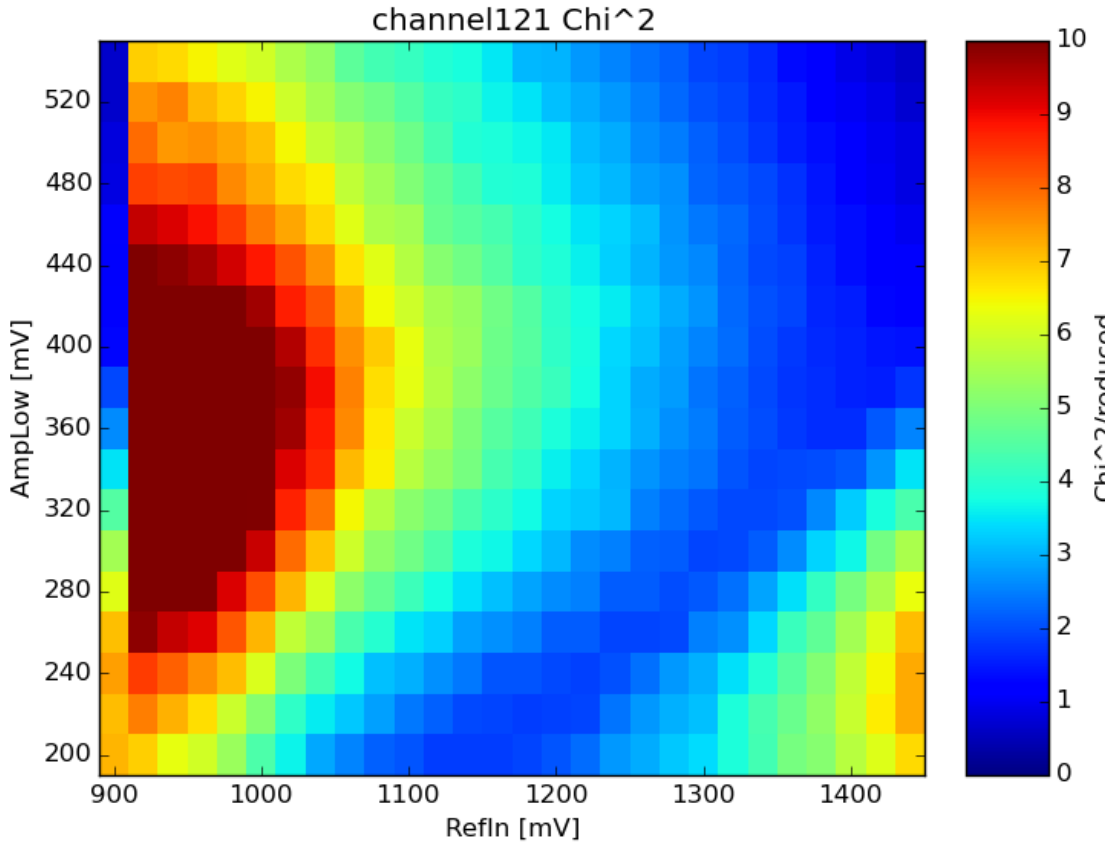
- First ADC curves successfully measured with DHE source last week
- Plan: characterization of all Hybrid 5 DCDs during the coming weeks



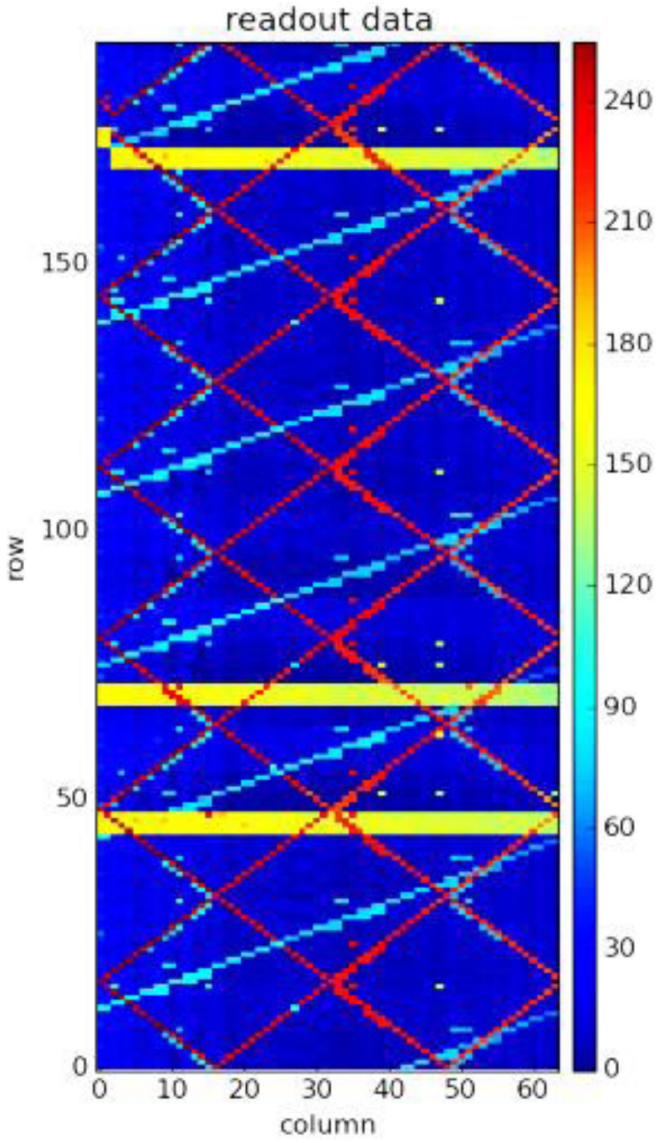
ADC Characterization – DHE Current Source

- Refin and AmpLow optimization
- Most impacting DACs in DCD

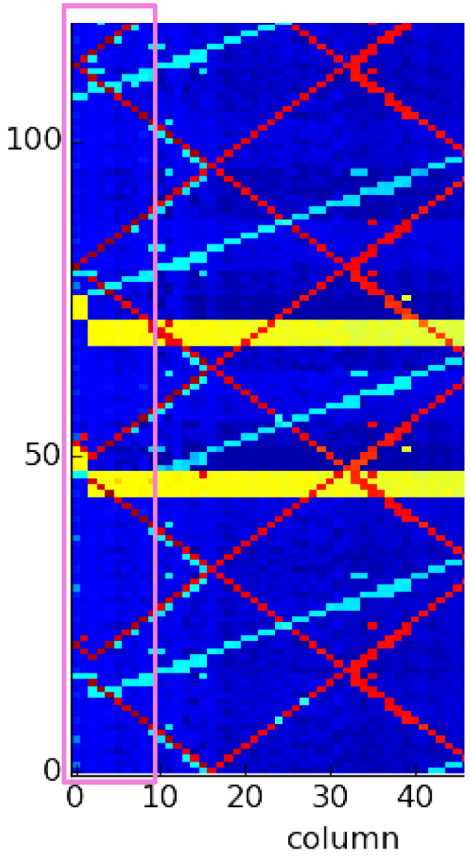




DHPT Memory Dump Issue



- Florian's talk at 19th international DEPFET workshop
- Testing offset upload to DCD
- Noticed randomly occuring shift of pixels in first two columns by one gate (4 rows, 32 dcd_clk cycles)



- Possible interfaces of this problem occuring:
  - DHP upload of offset values
  - DCD → DHP communication
  - DHP → DHE communication

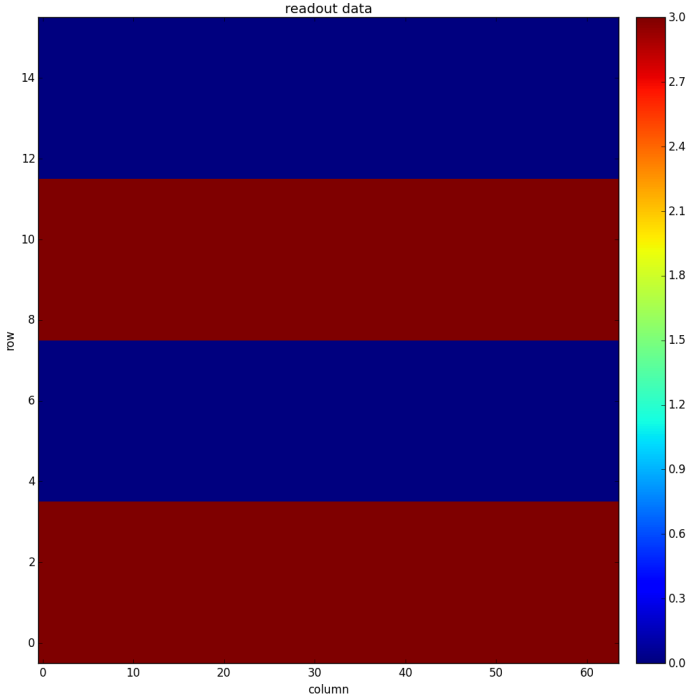
DHPT Memory Dump Issue

- Problem isolated by enabling test mode in DHP

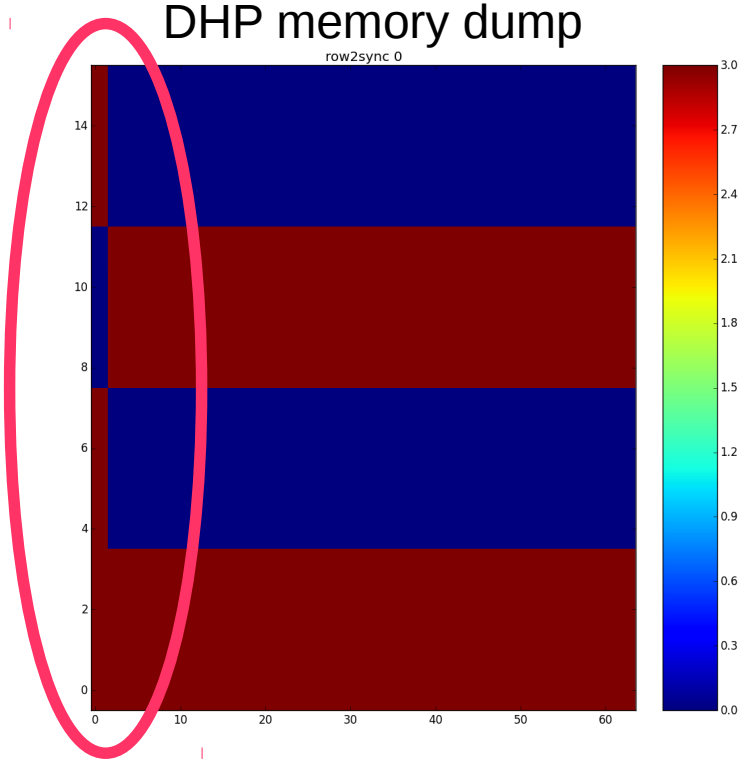
  i.e. raw data memory is not overwritten by fresh DCD data
- 1. write test pattern via JTAG directly into DHP memory

  2. read out a regular memory dump
- Problem can be reliably reproduced → no DCD ↔ DHP communication problem

JTAG readout



DHP memory dump



DHPT Memory Dump Issue

Characterization of effect:

- Occurs very often for DHE half rate mode
- At full rate (regular speed): effect occurs << 0.5% of readouts
- Effect has been verified in simulations of designers to originate from DHP memory dump readout
  -> Bug in DHP

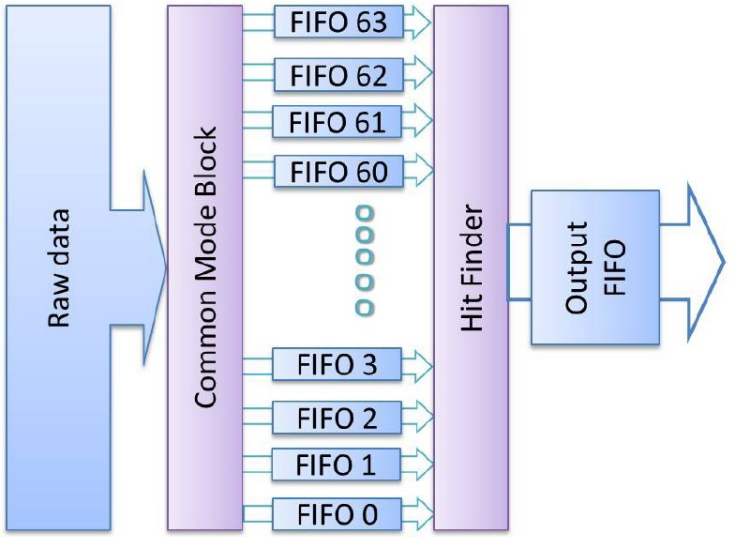
Impact on experiment:

- For standard data taking in the experiment zero suppressed data are read out → no effect
- For pedestal measurement the memory dump is used
  - Happens only every couple of minutes
  - Effect is local in the first couple of pixel columns
    → Possible solution: since on short timescales stable pedestals are expected look for shift/doubling/outliers in successive frames and discard faulty ones

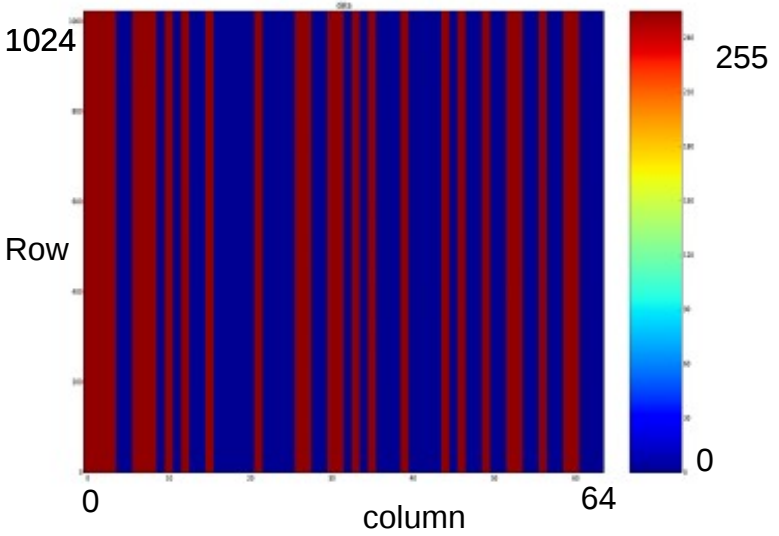
→ The bug is understood, not critical and no measures are taken to fix it
-> For list of changes in DHPT1.1 see talk by Carlos about the ASICs (before lunch)

DHP High Occupancy Testing

- System is specified to work without loss for occupancies < 3%
- DHP readout was tested for particular controlled scenario, i.e. all hits in the same columns

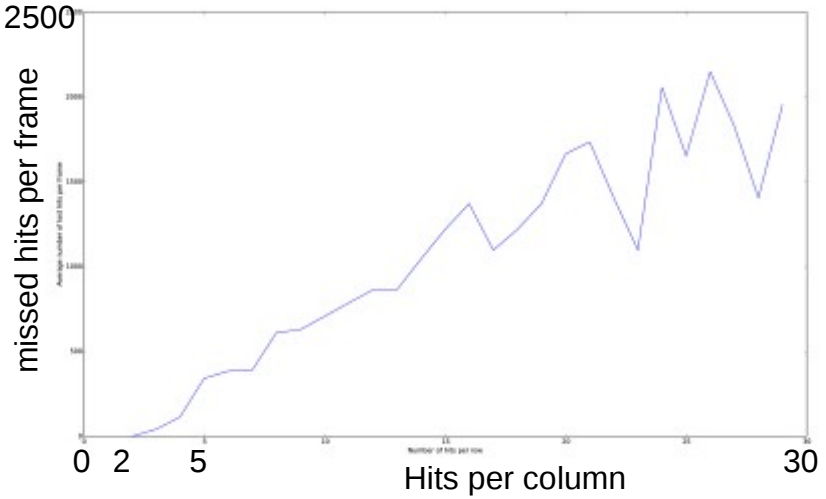


test frame:



- Buffer 1 column FIFOs 256 bytes deep
- Two columns completely filled

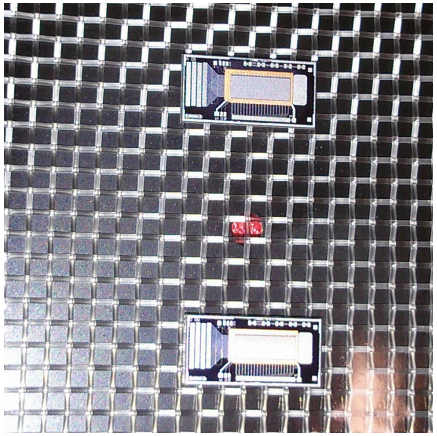
  → 3.1 % occupancy, no lost hits
- Further tests with random data/high bursts

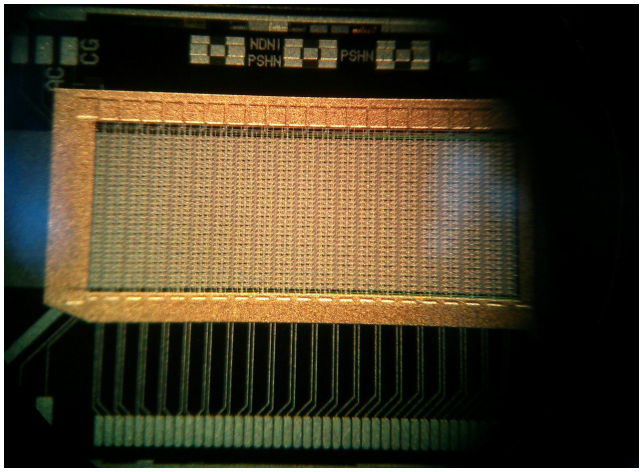


Summary and Outlook

- Characterization of Hybrid 5 boards will proceed
  - DCD ↔ DHP communication
  - ADC parameters of DCDs

- Two small PXD 9 matrices will be attached to Hybrid 5 boards and tested to be used at the upcoming November beam test at DESY





- DHP accordance to occupancy specification is being tested
- Uncritical bug in memory dump of DHP discovered

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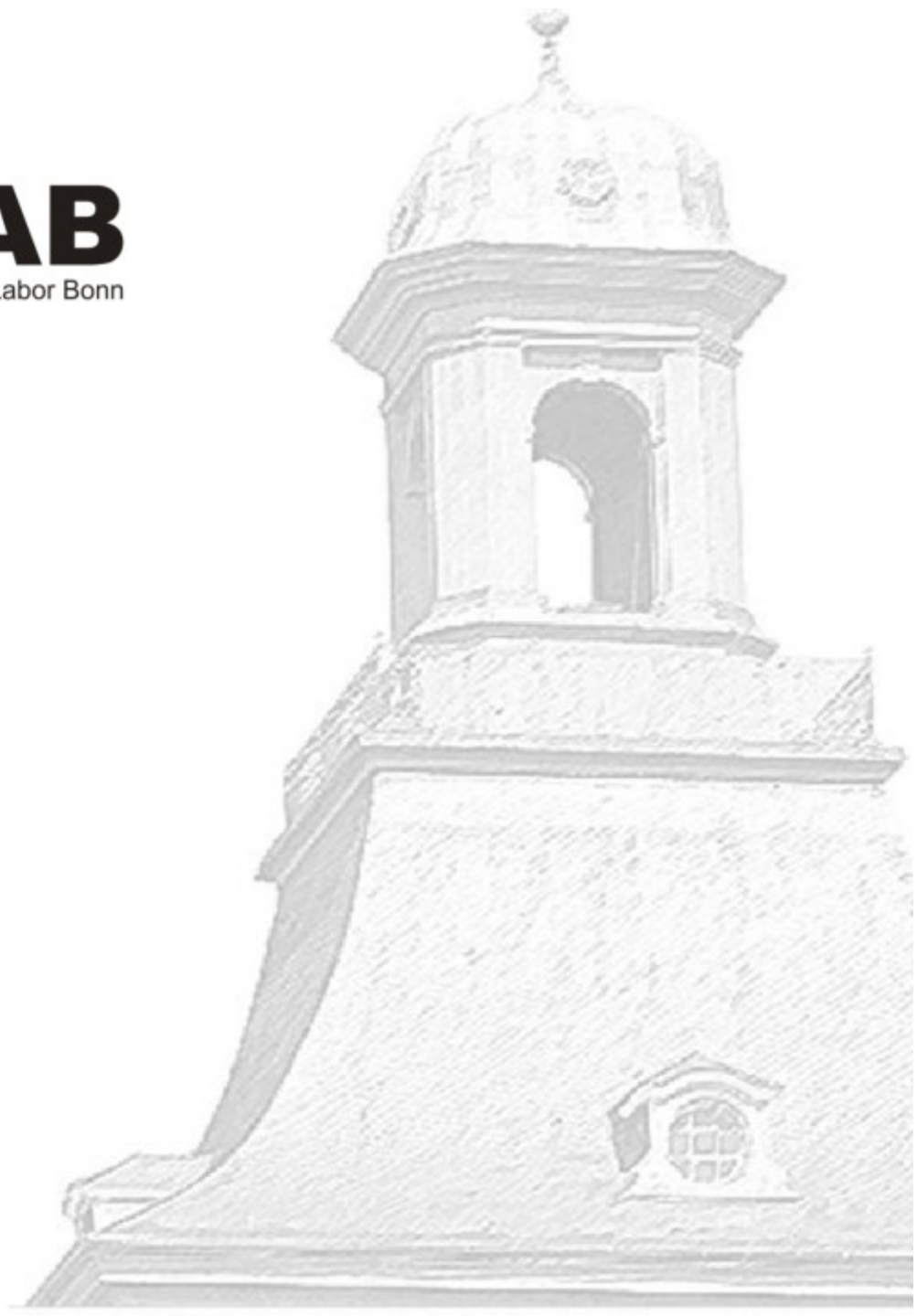
SI LAB
Silizium Labor Bonn

Thank you



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DHE Half Rate Mode

- half rate DHP ↔ DHE communication

  → DHP doubles all output bits, DHE running at effectively half frequency