IFIC
INSTITUTO DE FÍSICA CORPUSCULAR

Probe Card Status.

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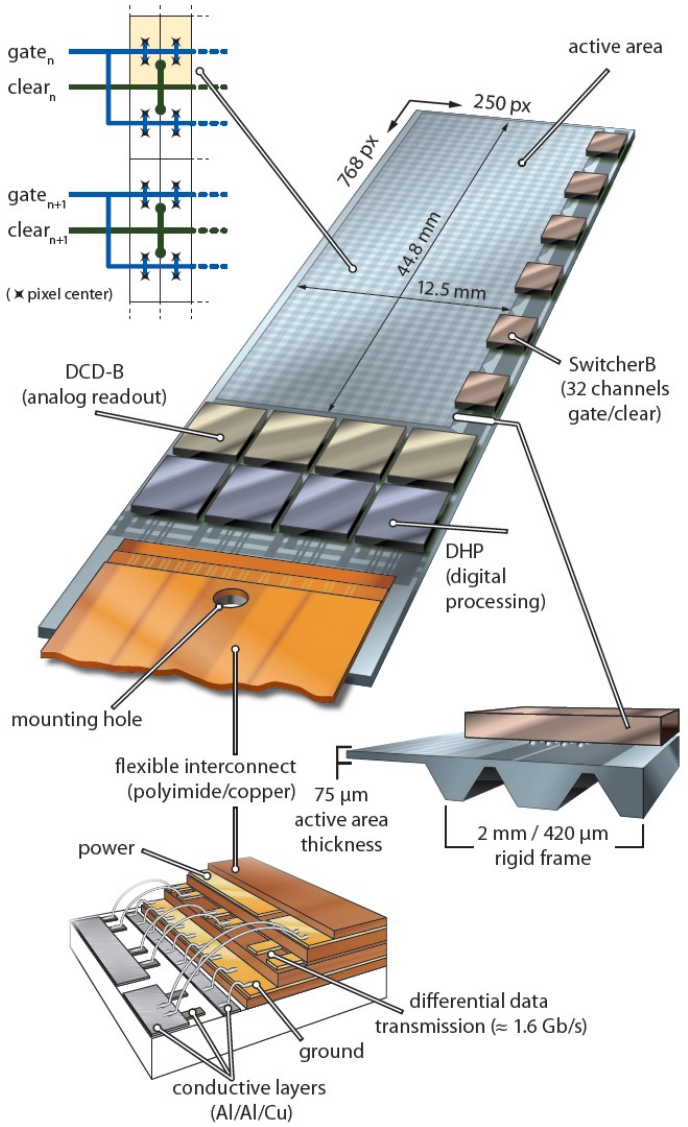
DEPFET pre-test

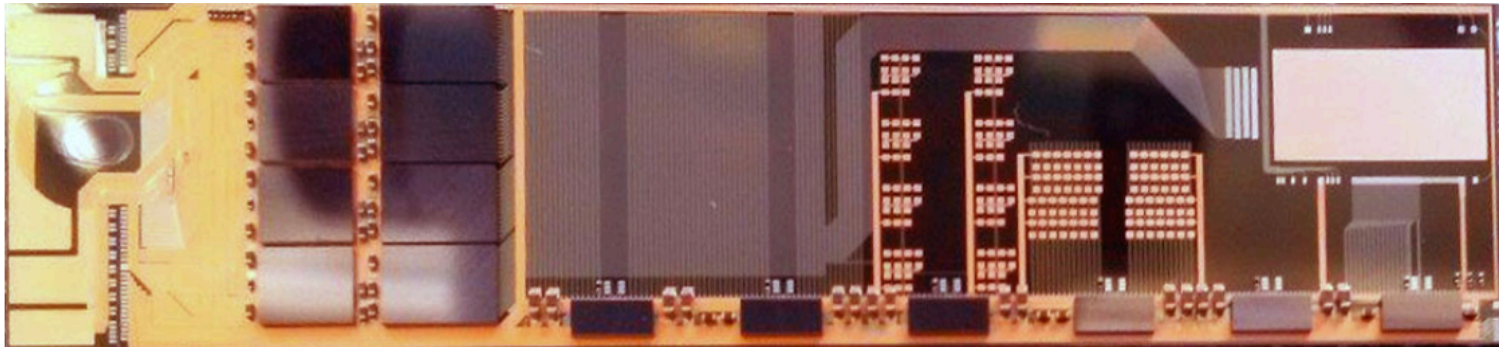
- The DEPFET modules, full assembled, will include the "kapton" cable attached.
- After attaching the "kapton" cable, reworking may be impossible.
- The idea is to pre-test the modules before attaching it.
- A needle card is required.



EMCM

EMCM (electrical module without active area):

- A probe-card for the EMCM has been build.
- The results prove that testing with a needle-card is feasible.
- The EMCM pad layout is similar, but not equal to the final modules, a new needle card design is required.



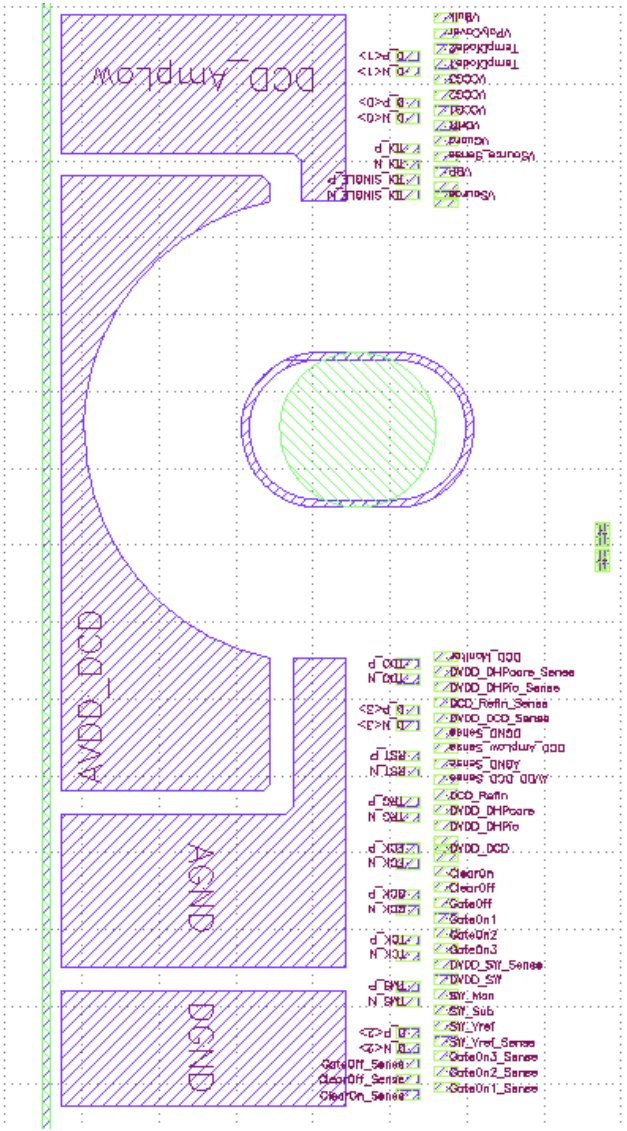
Needle Card

Pad distribution EMCM

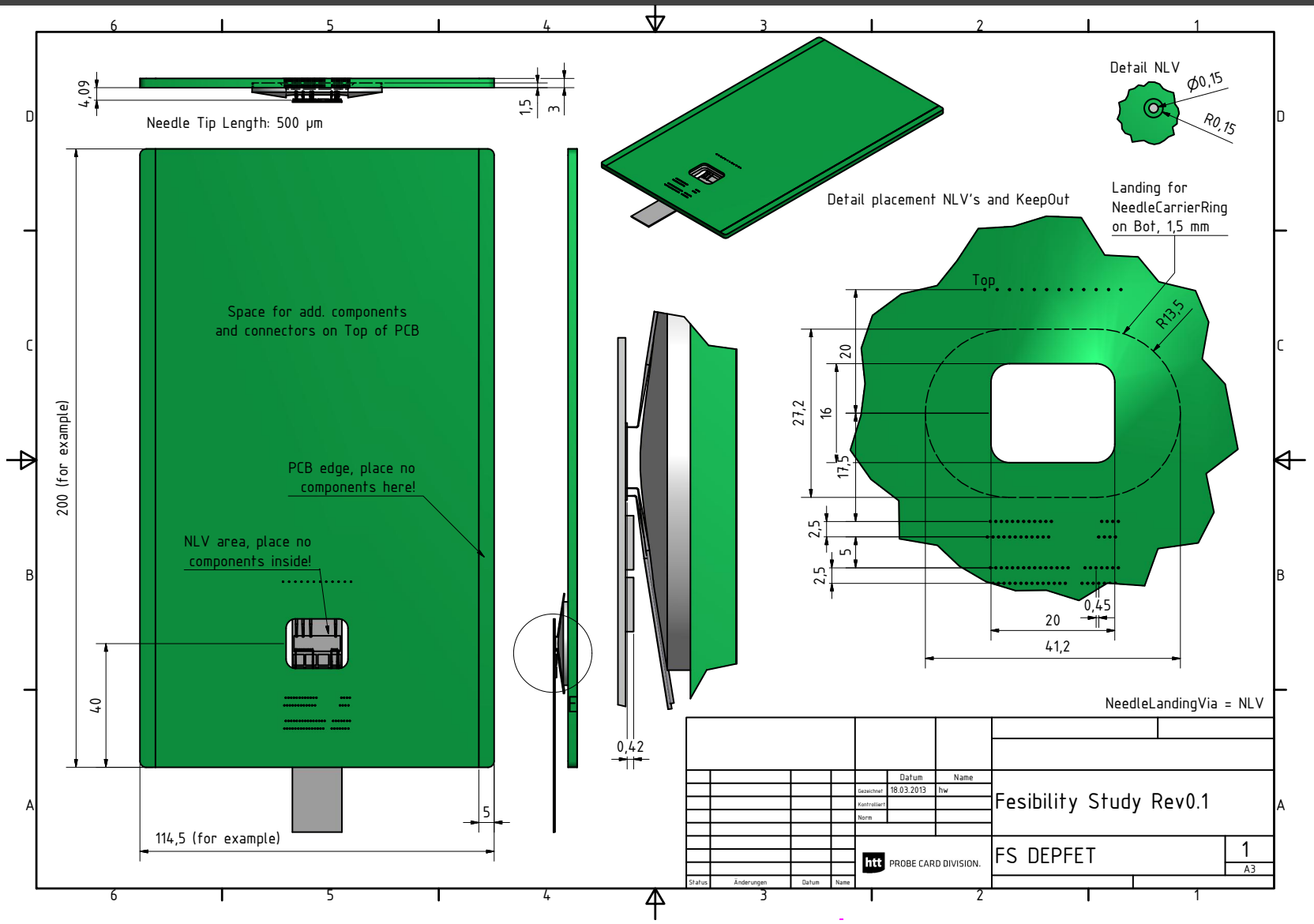
- 73 small aluminium pads, 4 big copper pads.
- 8 pads for high speed differential lines.

Solutions:

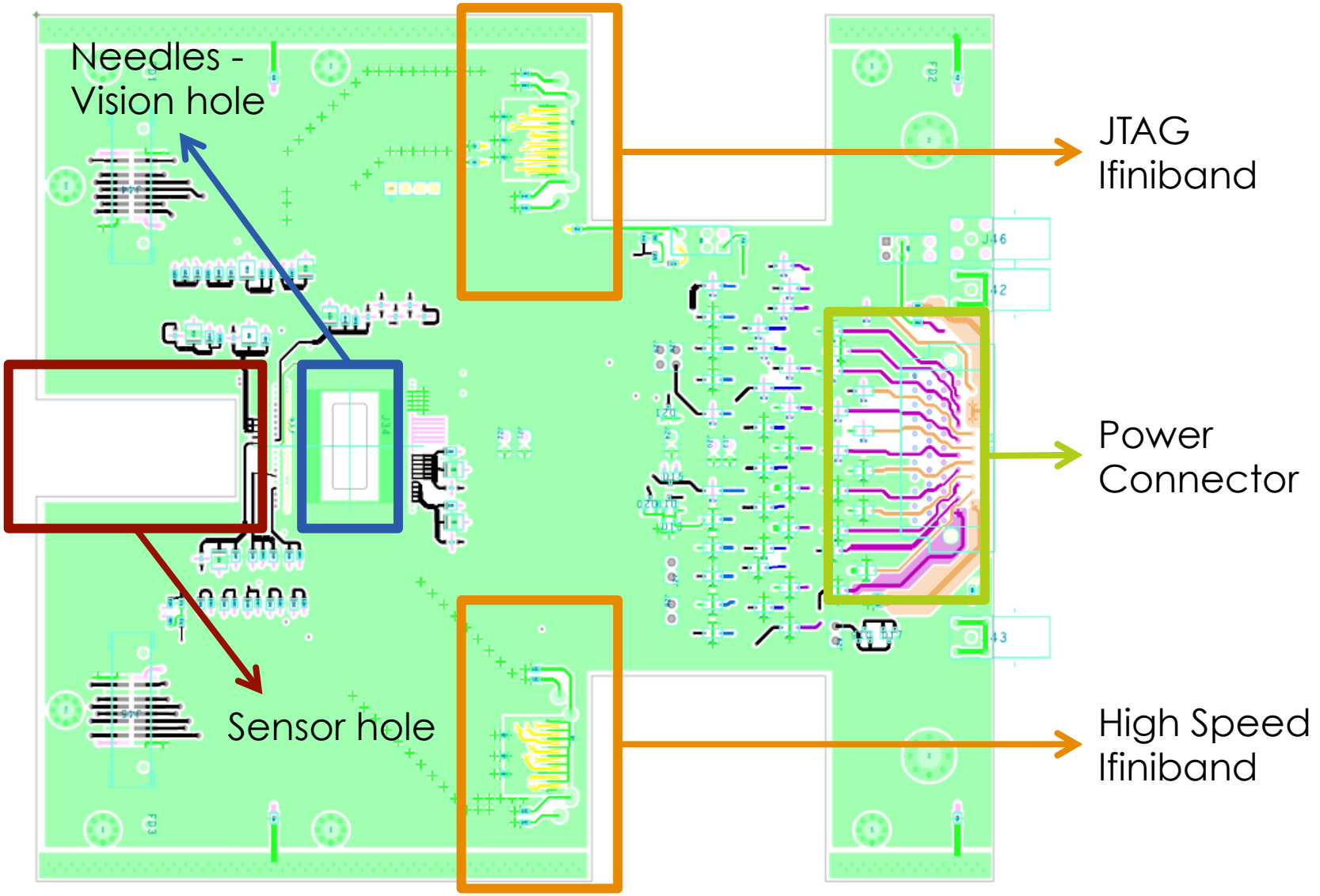
- 114 needles were required (multiple needles in the big pads).
- PCB size was limited by connectors (Power + Infiniband).
- Design priority: rather simple and passive PCB, minimizing the path length of the high speed signals



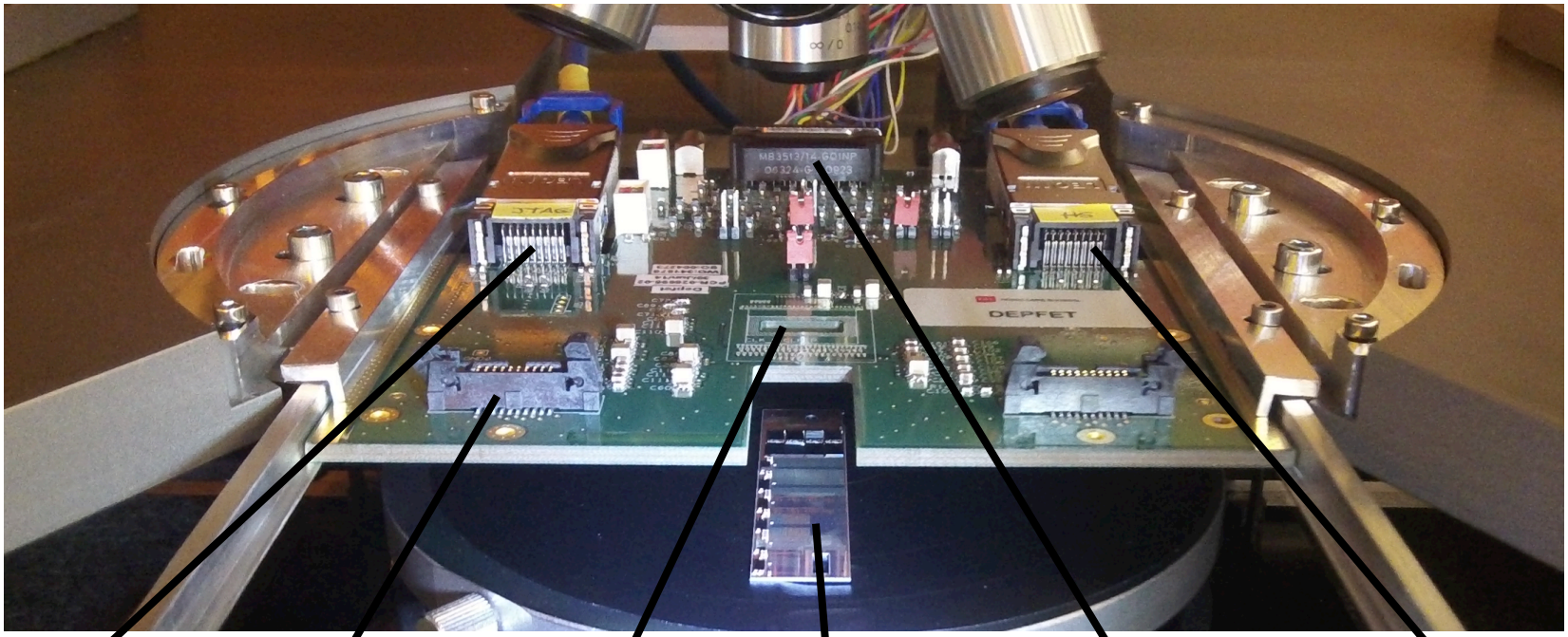
HTT Solution v1.0



Final Design



Needle Card



JTAG Ifiniband

Voltages Monitor – Not Used

Needles hole

EMCM W17-4

Power Connector

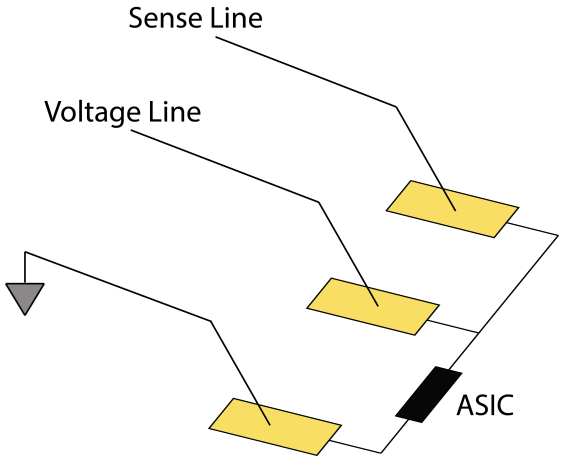
High Speed Ifiniband

Needle Card Test & Performance

- Voltages applied and current consumptions measured.
- Slow control and boundary scan.
- High speed link stability.

Voltages and Current Consumptions

- Planarity test (needles – pads).
- Test with a non populated EMCM (Voltage connections sensed).
- Simulation of a problem in a sense line needle.
- Test with populated EMCM – Check of the current consumption values.



Name:	R_{val} (Ω):	V_{appl} (V)	V_{reg} (V)	V_{ASIC} (V)	C (mA)
DHP core	12	1.62	1.88	1.74	145
DHP core	12	1.2	1.43	1.32	111
DHP core	2	1.62	2.1	1.64	489
DHP core	2	1.2	1.6	1.23	370
DHP io	12	1.8	2.04	1.9	157
DHP io	2	1.8	2.2	1.77	535
DCD DVDD	12	1.8	2.02	1.9	160
DCD DVDD	2	1.8	2.16	1.77	535
Source	390	7	7.2	7.25	18
Source	290	7	7.28	7.25	26
DCD AVDD	82	1.9	2.16	2.15	27
DCD AVDD	12	1.9	2.21	2.1	175
DCD AVDD	2	1.9	2.38	2.0	610

Table 1: Values measured with sensed lines connected.

Name:	R_{val} (Ω):	V_{appl} (V)	V_{reg} (V)	V_{ASIC} (V)	C (mA)
DHP core	12	1.62	2.16	1.99	165
DHP core	12	1.2	1.64	1.52	127
DHP core	2	1.62	2.16	1.65	500
DHP core	2	1.2	1.64	1.26	391
DHP io	12	1.8	2.37	2.2	180
DHP io	2	1.8	2.35	1.86	562
DCD DVDD	12	1.8	2.37	2.24	185
DCD DVDD	2	1.8	2.37	1.94	587
Source	390	7	8.79	8.7	22
Source	290	7	8.1	8.1	27 (limit)
DCD AVDD	82	1.9	2.62	2.59	34
DCD AVDD	12	1.9	2.6	2.49	206
DCD AVDD	2	1.9	2.6	2.2	665

Table 2: Values measured without sensed lines.

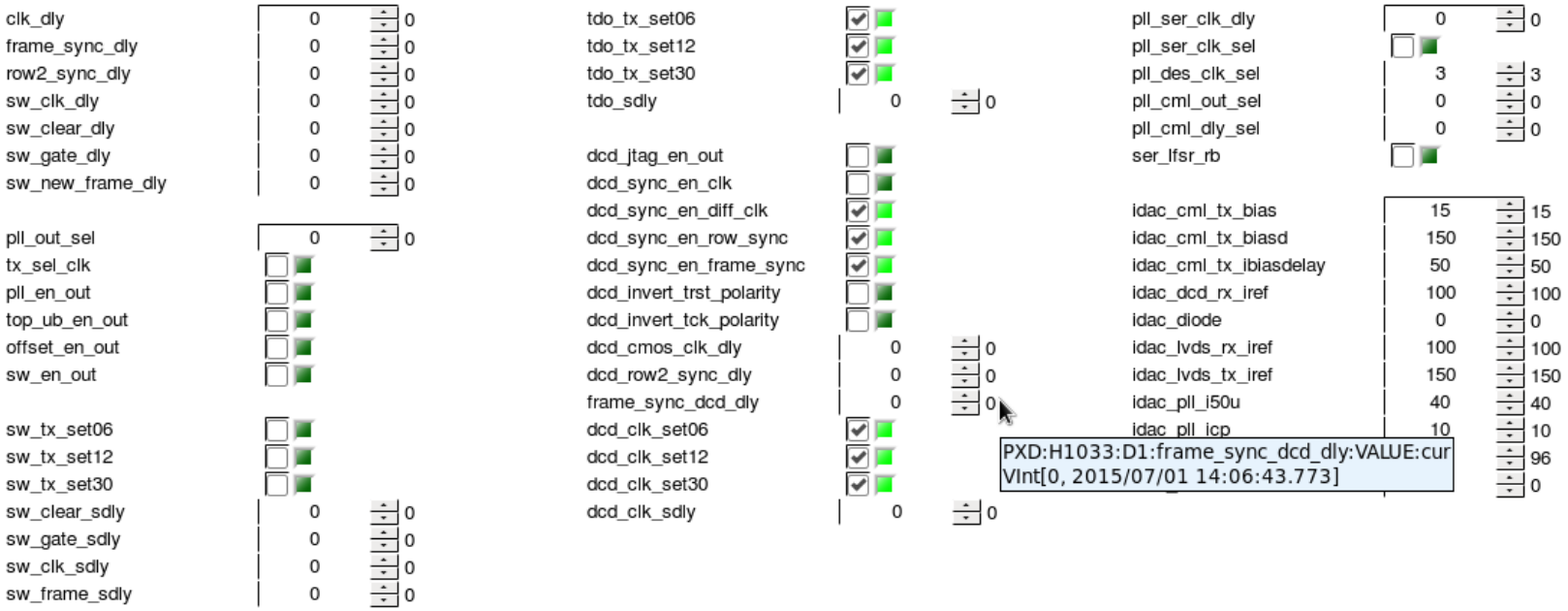
Voltages and Current Consumptions

- Planarity test (needles – pads).
- Test with a non populated EMCM (Voltage connections sensed).
- Simulation of a problem in a sense line needle.
- Test with populated EMCM – Check of the current consumption values.

min.	Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
0 mV	0 mV	0 mV		-130 mV	-139 mV	2 mA	sw-sub
0 mV	1800 mV	2000 mV		2296 mV	1799 mV	27 mA	sw-dvdd
0 mV	0 mV	0 mV		-918 mV	1399 mV	-2 mA	sw-refin
0 mV	400 mV	500 mV		545 mV	405 mV	0 mA	dcd-amplow
0 mV	1900 mV	2000 mV		2016 mV	1897 mV	41 mA	dcd-avdd
0 mV	1800 mV	2000 mV		2615 mV	1796 mV	303 mA	dcd-dvdd
0 mV	1200 mV	1300 mV		1262 mV	1202 mV	1 mA	dcd-refin
0 mV	1200 mV	1640 mV		2015 mV	1200 mV	252 mA	dhp-core
0 mV	1800 mV	2000 mV		2732 mV	1801 mV	180 mA	dhp-io
0 mV	0 mV	10000 mV		4 mV	-6 mV	-1 mA	bulk
0 mV	0 mV	22000 mV		-11 mV	28 mV	-1 mA	clear-on
0 mV	0 mV	20000 mV		-21 mV	27 mV	0 mA	clear-off
-4000 mV	0 mV	3000 mV		1 mV	4 mV	0 mA	gate-on1
-4000 mV	0 mV	3000 mV		-3 mV	1 mV	0 mA	gate-on2
-4000 mV	0 mV	3000 mV		0 mV	1 mV	0 mA	gate-on3
0 mV	0 mV	6000 mV		-244 mV	-2 mV	-1 mA	gate-off
0 mV	0 mV	7000 mV		375 mV	-38 mV	3 mA	source

Slow Control and Boundary Scan.

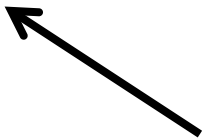
- Using the automatic configuration script, configure the chips.
- Change, write & read some parameters via JTAG i.e: pll_ser_clk_sel (1➔3).
- Infrastructure test.
- Interconnection test.



Boundary Scan – EMCM W17-4

- Measurements with the hardware provided by Goepel

```
================================================================================
6/15/2015 3:53:14 PM  UUT: EMCM-P6-1   Start Test: Infrastructure
================================================================================
Testing boundary register SWITCHER_5 ...Ok
Testing boundary register SWITCHER_4 ...Ok
Testing boundary register SWITCHER_3 ...Ok
Testing boundary register SWITCHER_2 ...Ok
Testing boundary register SWITCHER_1 ...Ok
Testing boundary register SWITCHER_0 ...Ok
Testing boundary register DCD3 ...Ok
Testing boundary register DHP3 ...Ok
Testing boundary register DCD2 ...Ok
Testing boundary register DHP2 ...Ok
Testing boundary register DCD1 ...Ok
Testing boundary register DHP1 ...Ok
Testing boundary register DCD0 ...Ok
Testing boundary register DHP0 ...Ok
================================================================================
3:53:14 PM  P A S S  Elapsed Time  00:00:00.111
================================================================================
```



Infrastructure test PASS

Boundary Scan – EMCM W17-4

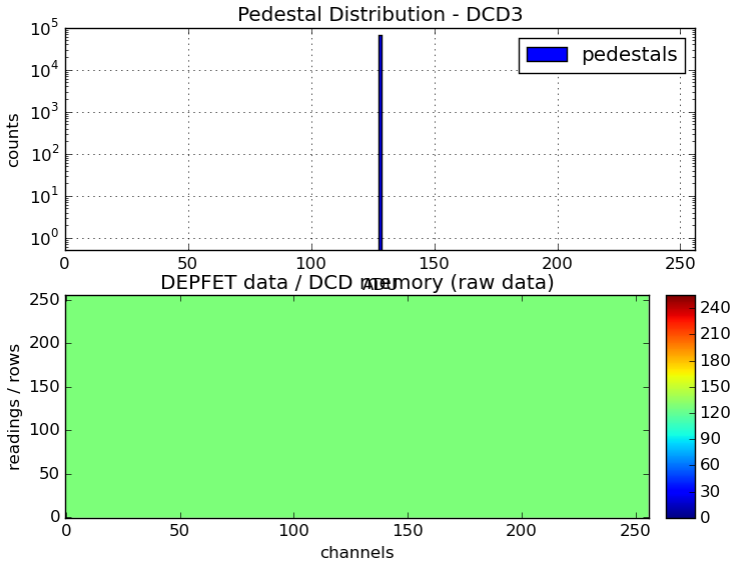
```
================================================================================
6/15/2015 3:54:33 PM  UUT: EMCM-P6-1   Start Test: Interconnection
================================================================================
DHP2:DI0_0(#28)      EH ML
DHP2:DI0_1(#20)      EH ML
DHP2:DI0_2(#16)      EH ML
DHP2:DI0_3(#24)      EH ML
DHP2:DI0_4(#30)      EH ML
DHP2:DI0_5(#22)      EH ML
DHP2:DI0_6(#18)      EH ML
DHP2:DI0_7(#26)      EH ML
DHP2:DI1_0(#27)      EH ML
…
…
…
- 1- Line NET0141_0 defective:
-73-       1. pin <: OUT DCD2:DO7_7(#P79)     {BScan     } DCD_FOOTPRINT              NET0141_0
-73-       2. pin >: In  DHP2:DI7_7(#99)      {BScan     } DHP10_FOOTPRINT            NET0141_0
- 8-    Stuck at Low of the line

-24- Test step table of the line NET0141_0:
-25-        Expected                    H L L L H L H L H L L H H L H L H L H H
-28-        Measured <Stuck at low>
-30-      Output pin  DCD2:DO7_7(#P79)  H L L L H L H L H L L H H L H L H L H H
-31-       Input pin   DHP2:DI7_7(#99) >L L L L>L L>L L>L L L>L>L L>L L>L L>L>L
…
…
…

================================================================================
3:54:35 PM  F A I L  Elapsed Time  00:00:01.702
================================================================================
```

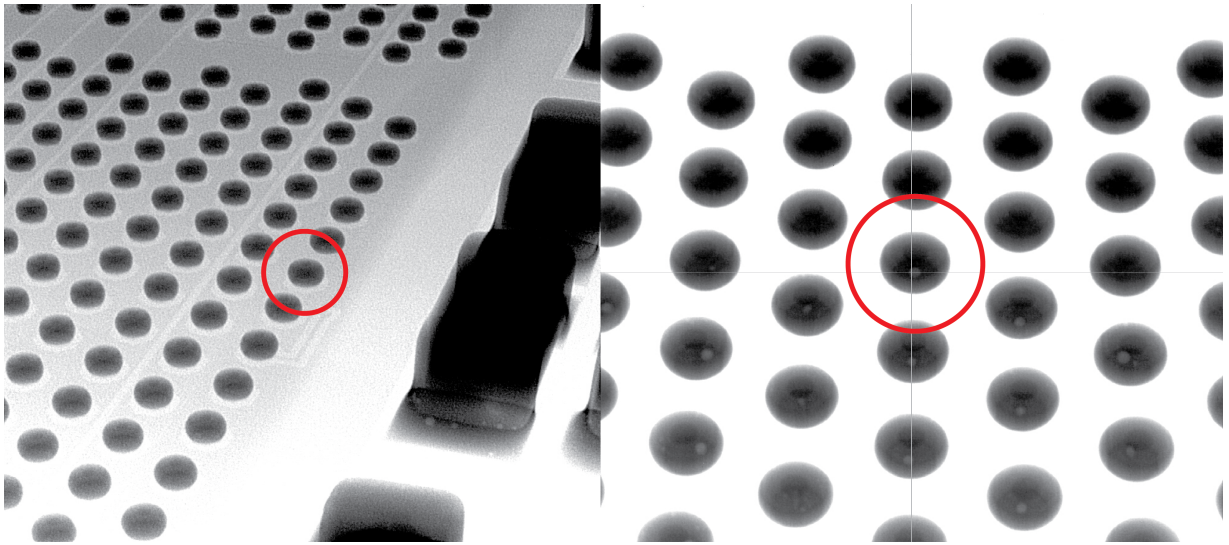
Fault found in all digital connection between DCD2 and DHP2

Stuck in low level.

Boundary Scan – EMCM W17-4

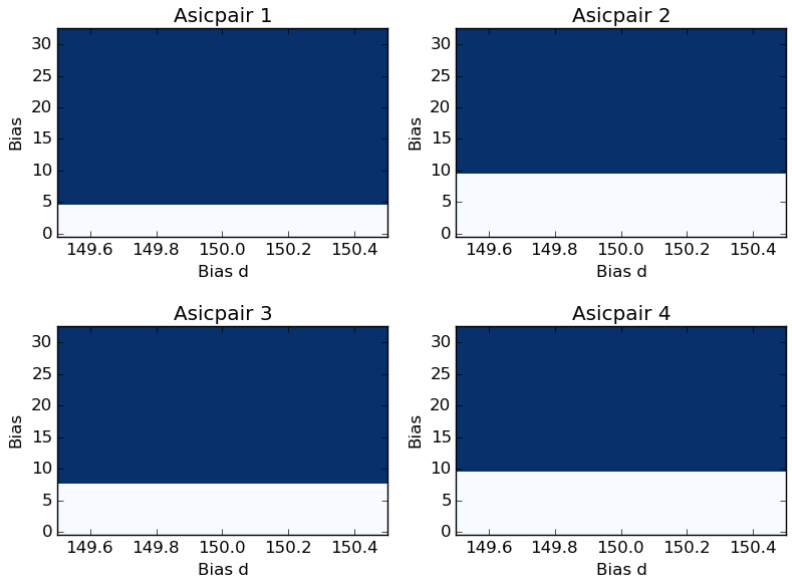
- Problem also detected reading out data
- Reason for this massive fault – problem in the reference voltage.
- X-Ray test does not show any problem with the bumps involved.





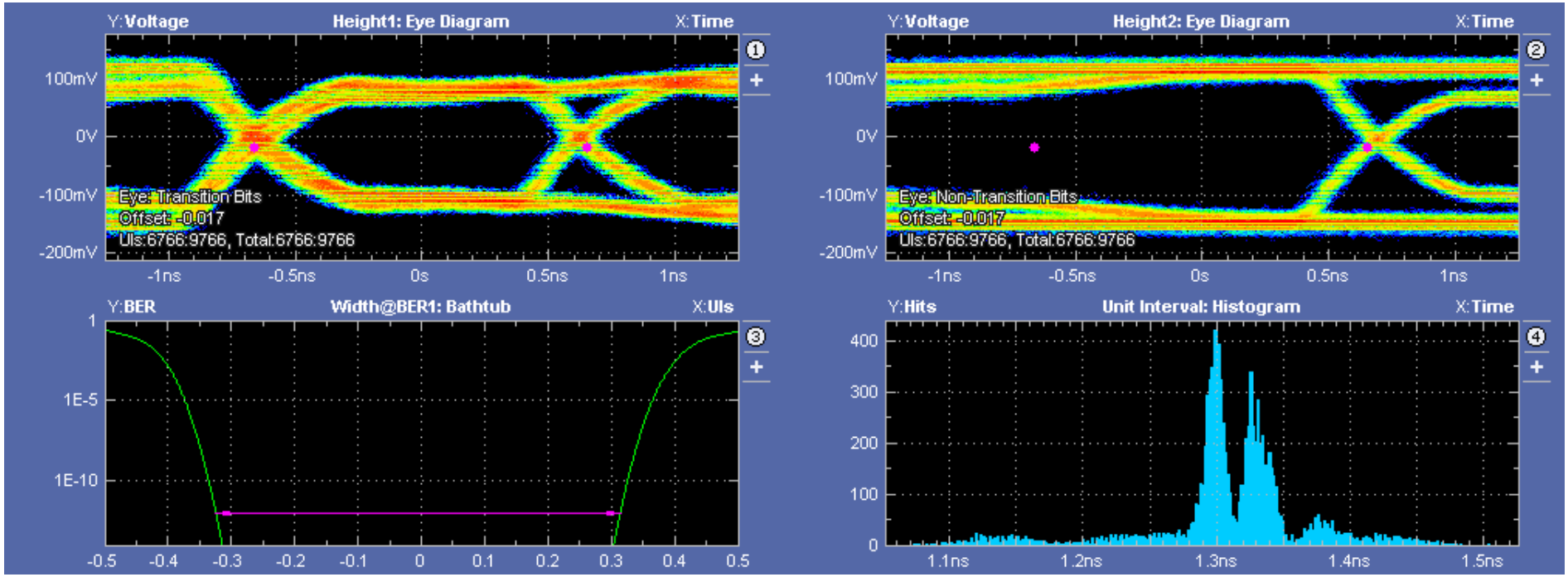
High Speed Link Stability (Half Rate).

- Test the High Speed link stability with the DHE software.
- Measure the eye diagram.
- Test the High Speed link stability with the random pattern.
- Readout Data.



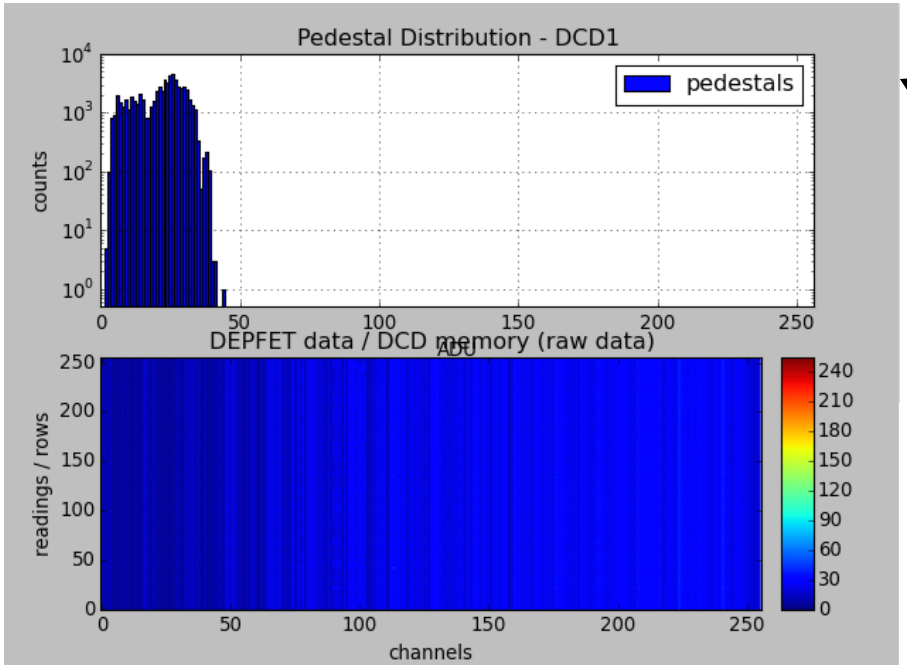
Script to optimize the HSL – blue region means the link is up.

High Speed Link Stability.

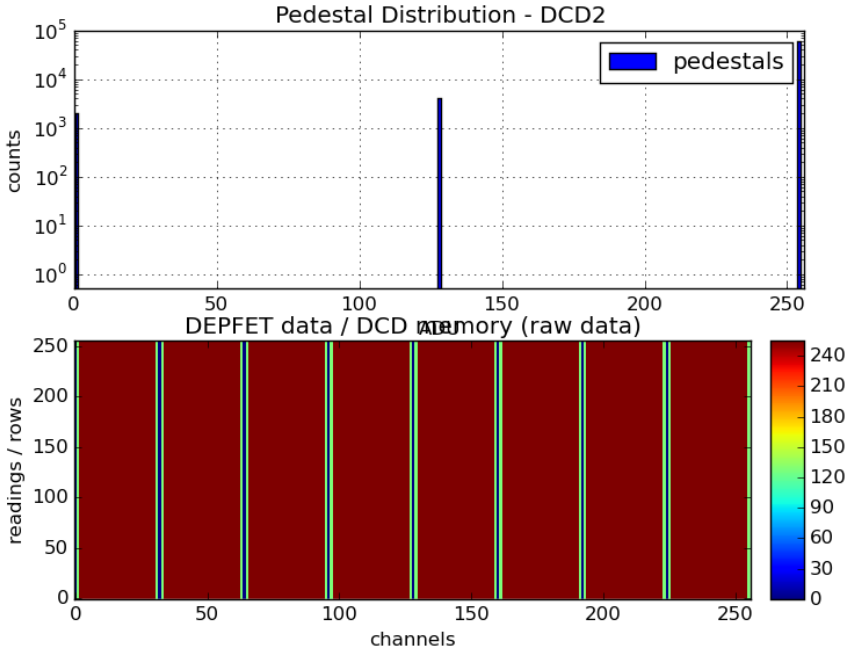


HSL Eye Diagram at Half Rate – DHP 0

Reading out Data



Pedestals read out form DCD1



Delay Settings Optimization Results

Needle Card

- If the contact between the needles and the module is good enough, there is any problem to operate the module, even to get stable high speed links.

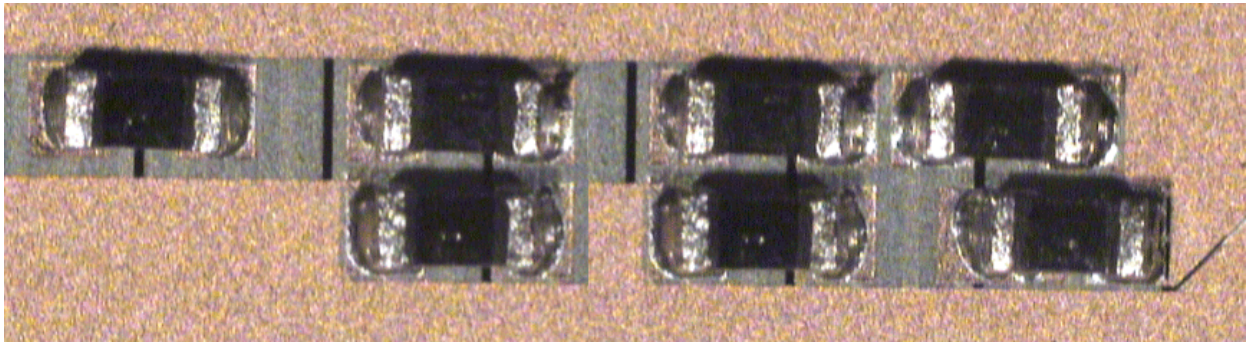
Based on the results…

Based on the results a preliminary testing protocol can be proposed:

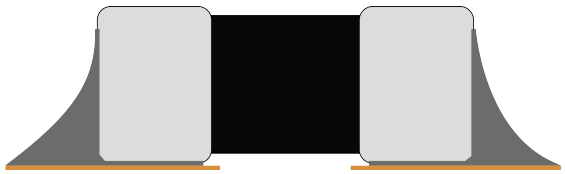
- Visual Inspection.
- Check of Voltages & Currents
- Chip Configuration: JTAG Write & Read
- Boundary Scan
- High Speed Link Stability
- Delays & Test Injection
- Check of Voltages & Currents (DCDB Analogic Part)
- Read DCDB Pedestals
- Check of Voltages & Currents (Matrix)
- Read Matrix Pedestals
- Modification of Switcher Sequence: Matrix Saturation

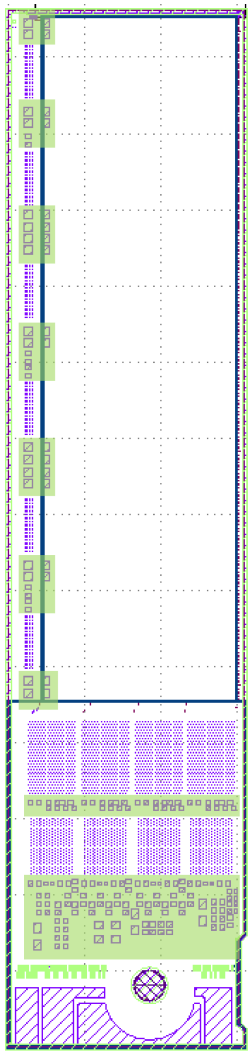
Testing Protocol

Visual Inspection



- Visual Inspection over SMDs and the rest of the components.
- Tested:
  - Visual quality of the SMDs soldering.
  - Any visual inconvenience in the module.

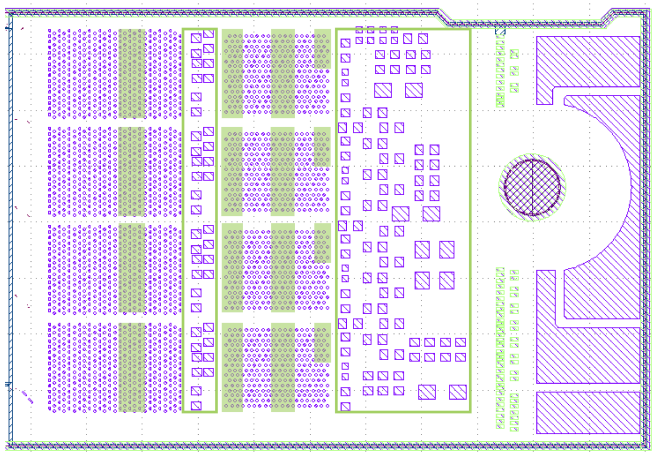




Testing Protocol

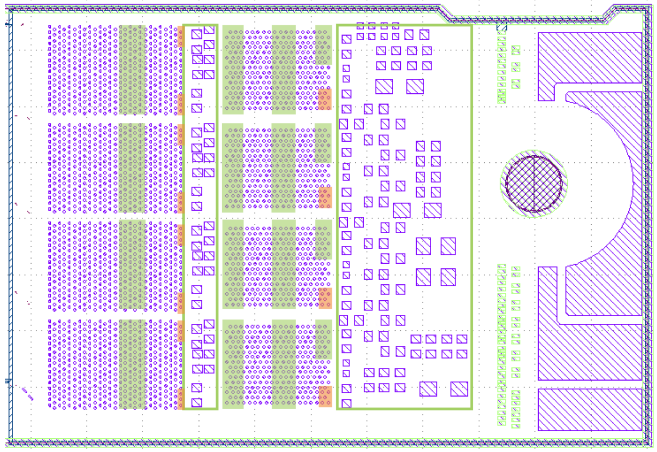
Check of Voltages & Currents

- Tested:
  - Proper connection between the ASICs and the Power Supply
  - Expected current consumption ➔ Normal behaviour of the ASICs



Chip Configuration: JTAG Write & Read

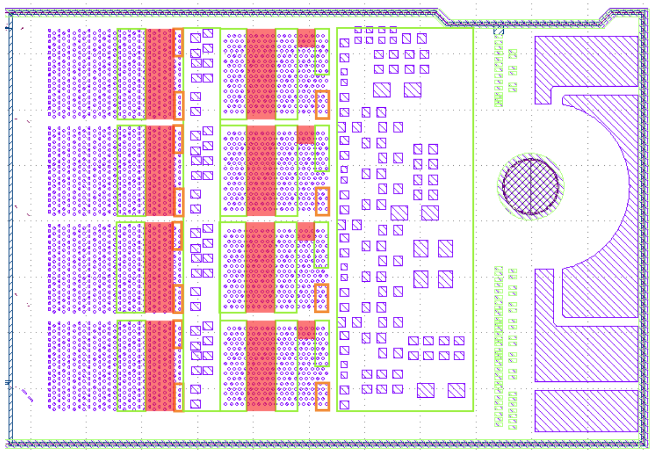
- Use the automatic configuration script & Change, Write & Read some parameters
- Tested:
  - Proper slow control connection.
  - Proper ASICs response



Testing Protocol

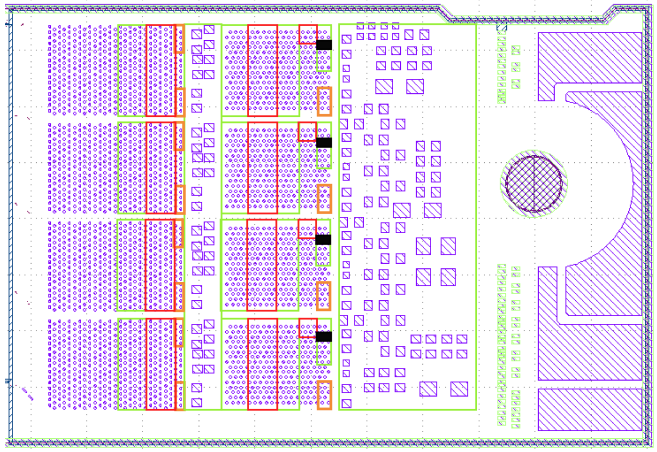
Boundary Scan

- Tested:
  - Proper boundary cell structure, chip ID & communication with JTAG controller
  - Check of the digital connections between boundary cells.



High Speed Link Stability

- DHE software to establish the links
- IBERT & Random pattern to debug
- Tested:
  - Quality of the data transfer connection



Testing Protocol

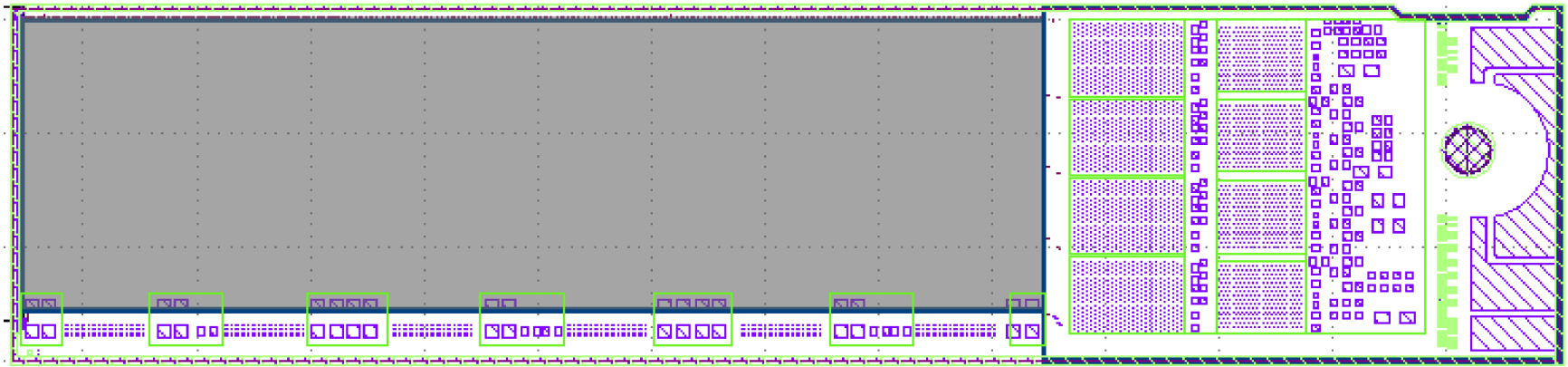
Delays & Test Injection

- Use the delays optimization script
- Quality of the data transferred using the Injection Pattern

Check of Voltages & Currents (DCDB Analogic Part)

Read DCDB Pedestals

Check of Voltages & Currents (Matrix)

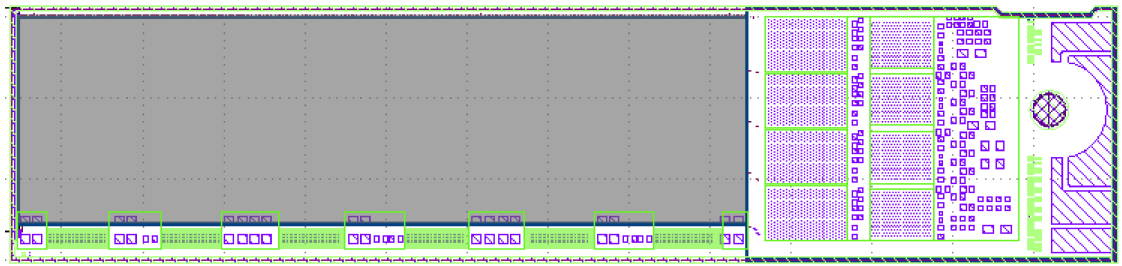


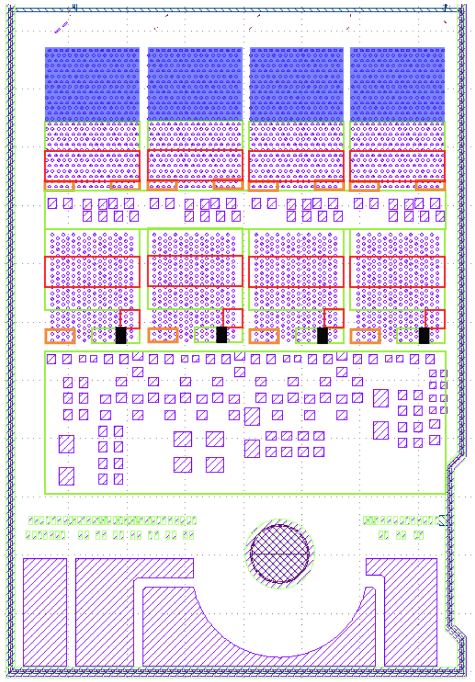
Testing Protocol

Read Matrix Pedestals

Modification of Switcher Sequence: Matrix Saturation

- Change the Switcher sequence, removing clean process to saturate the matrix
- Tested:
  - Response of the matrix
  - Proper operation of the Switcher





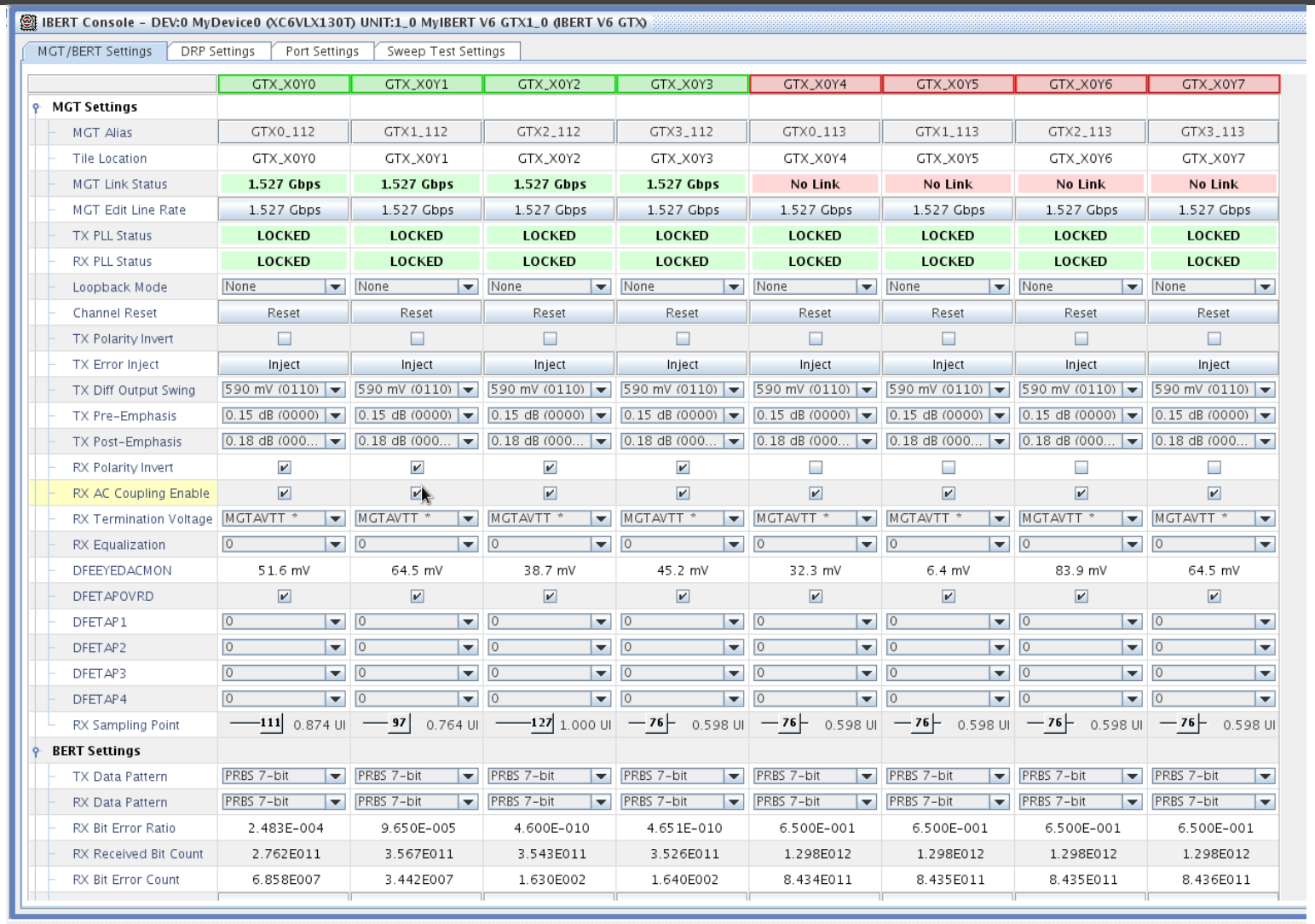
Summary

- The pre-test of the modules, with the needle card, is an important step to ensure the viability of the rework in case of ASIC problems.
- The test performed with the needle card prove the feasibility of this kind of test.
- With this testing protocol, all the ASIC aspects are covert.
- The needle card should be redesign to be adapted to the new pad distribution and to improve some details.

IMPORTANT REQUEST: To be able to debug the testing protocol and the new needle card, and practice before the final production process. AT LEAST, ONE MODULE OF THE PILOT RUN SHOULD BE ASSEMBLED AND FULL POPULATED WITHOUT ATTACHING THE KAPTON CABLE.

BACKUP

High Speed Link Stability



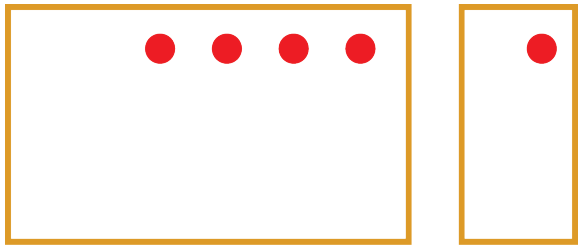
	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Settings								
MGT Alias	GTX0_112	GTX1_112	GTX2_112	GTX3_112	GTX0_113	GTX1_113	GTX2_113	GTX3_113
Tile Location	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Link Status	**1.527 Gbps**	**1.527 Gbps**	**1.527 Gbps**	**1.527 Gbps**	**No Link**	**No Link**	**No Link**	**No Link**
MGT Edit Line Rate	1.527 Gbps	1.527 Gbps	1.527 Gbps	1.527 Gbps	1.527 Gbps	1.527 Gbps	1.527 Gbps	1.527 Gbps
TX PLL Status	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**
RX PLL Status	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**	**LOCKED**
Loopback Mode	None	None	None	None	None	None	None	None
Channel Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
TX Polarity Invert	☐	☐	☐	☐	☐	☐	☐	☐
TX Error Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	590 mV (0110)	590 mV (0110)	590 mV (0110)	590 mV (0110)	590 mV (0110)	590 mV (0110)	590 mV (0110)	590 mV (0110)
TX Pre-Emphasis	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)
TX Post-Emphasis	0.18 dB (000...	0.18 dB (000...	0.18 dB (000...	0.18 dB (000...	0.18 dB (000...	0.18 dB (000...	0.18 dB (000...	0.18 dB (000...
RX Polarity Invert	☑	☑	☑	☑	☐	☐	☐	☐
RX AC Coupling Enable	☑	☑	☑	☑	☑	☑	☑	☑
RX Termination Voltage	MGTAVTT *	MGTAVTT *	MGTAVTT *	MGTAVTT *	MGTAVTT *	MGTAVTT *	MGTAVTT *	MGTAVTT *
RX Equalization	0	0	0	0	0	0	0	0
DFEEYEDACMON	51.6 mV	64.5 mV	38.7 mV	45.2 mV	32.3 mV	6.4 mV	83.9 mV	64.5 mV
DFETAPOVRD	☑	☑	☑	☑	☑	☑	☑	☑
DFETAP1	0	0	0	0	0	0	0	0
DFETAP2	0	0	0	0	0	0	0	0
DFETAP3	0	0	0	0	0	0	0	0
DFETAP4	0	0	0	0	0	0	0	0
RX Sampling Point	111 0.874 UI	97 0.764 UI	127 1.000 UI	76 0.598 UI	76 0.598 UI	76 0.598 UI	76 0.598 UI	76 0.598 UI
BERT Settings								
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	2.483E-004	9.650E-005	4.600E-010	4.651E-010	6.500E-001	6.500E-001	6.500E-001	6.500E-001
RX Received Bit Count	2.762E011	3.567E011	3.543E011	3.526E011	1.298E012	1.298E012	1.298E012	1.298E012
RX Bit Error Count	6.858E007	3.442E007	1.630E002	1.640E002	8.434E011	8.435E011	8.435E011	8.436E011

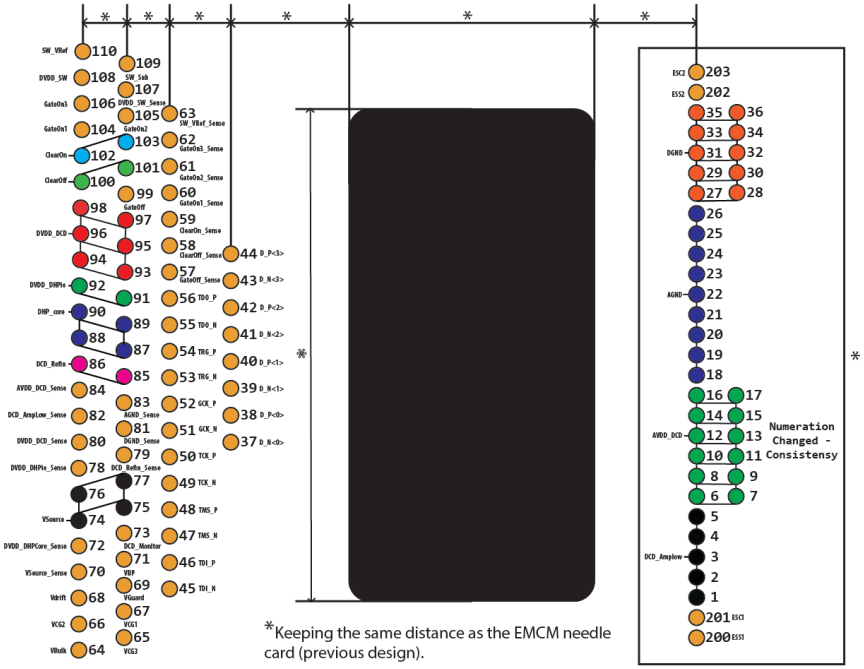
HSL Stability with the Random Pattern – IBERT Software

New Needle Card

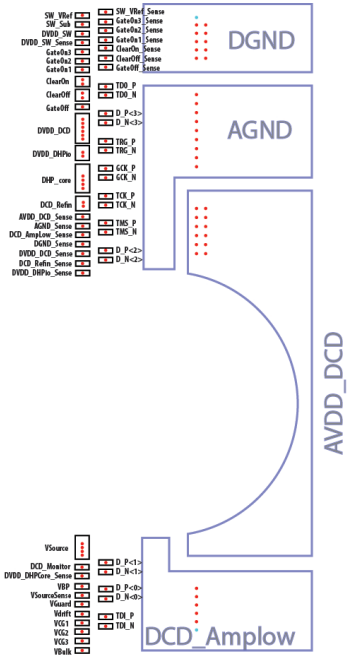
Needle card for the final modules ➔ a new design is required.

- High Speed Link optimization
  - Reduce length of HSL needles
  - Thicker needles
- To reduce the damage – new needle contact distribution
- Limitation of the maximum voltage applied – protection diodes.

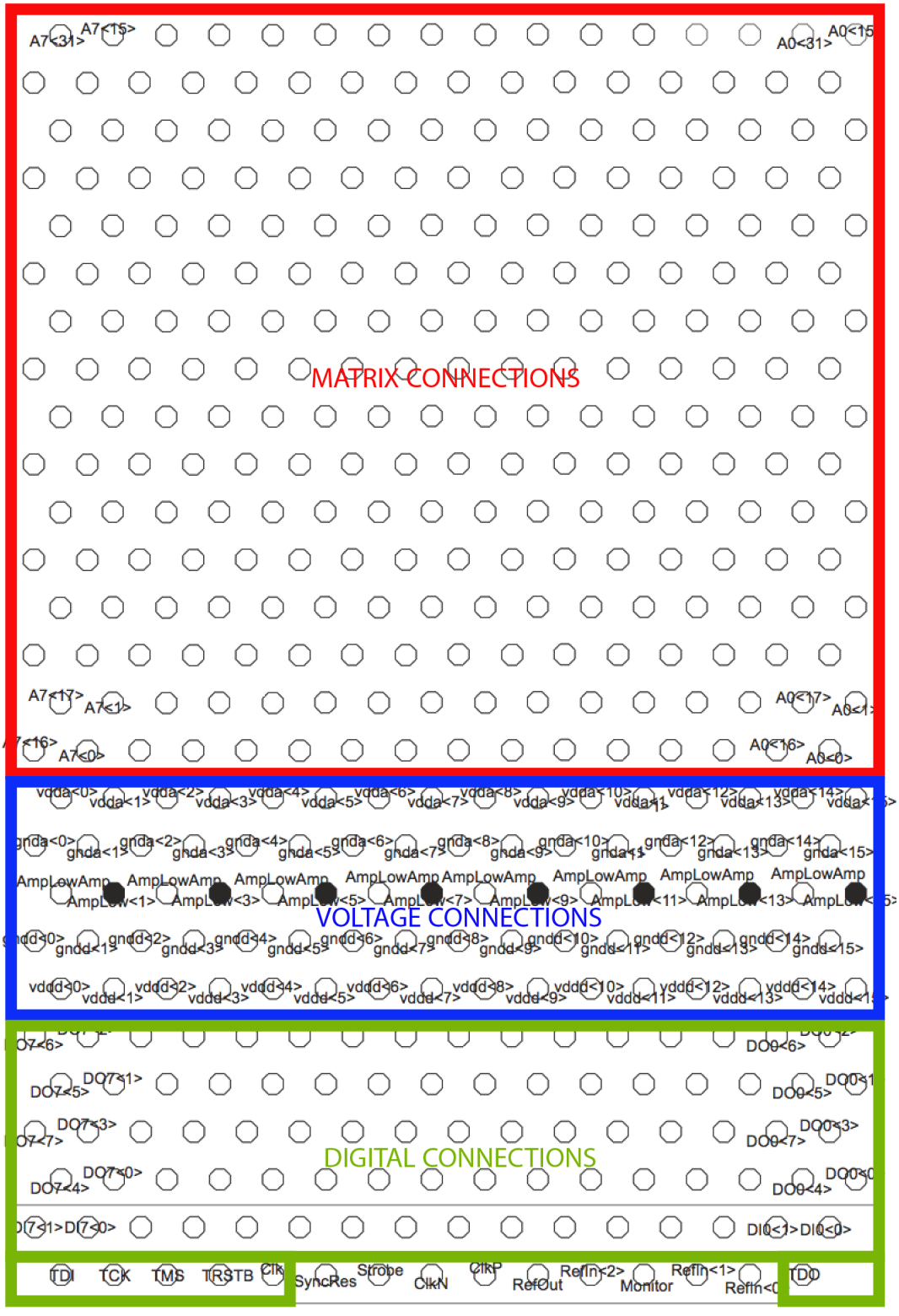




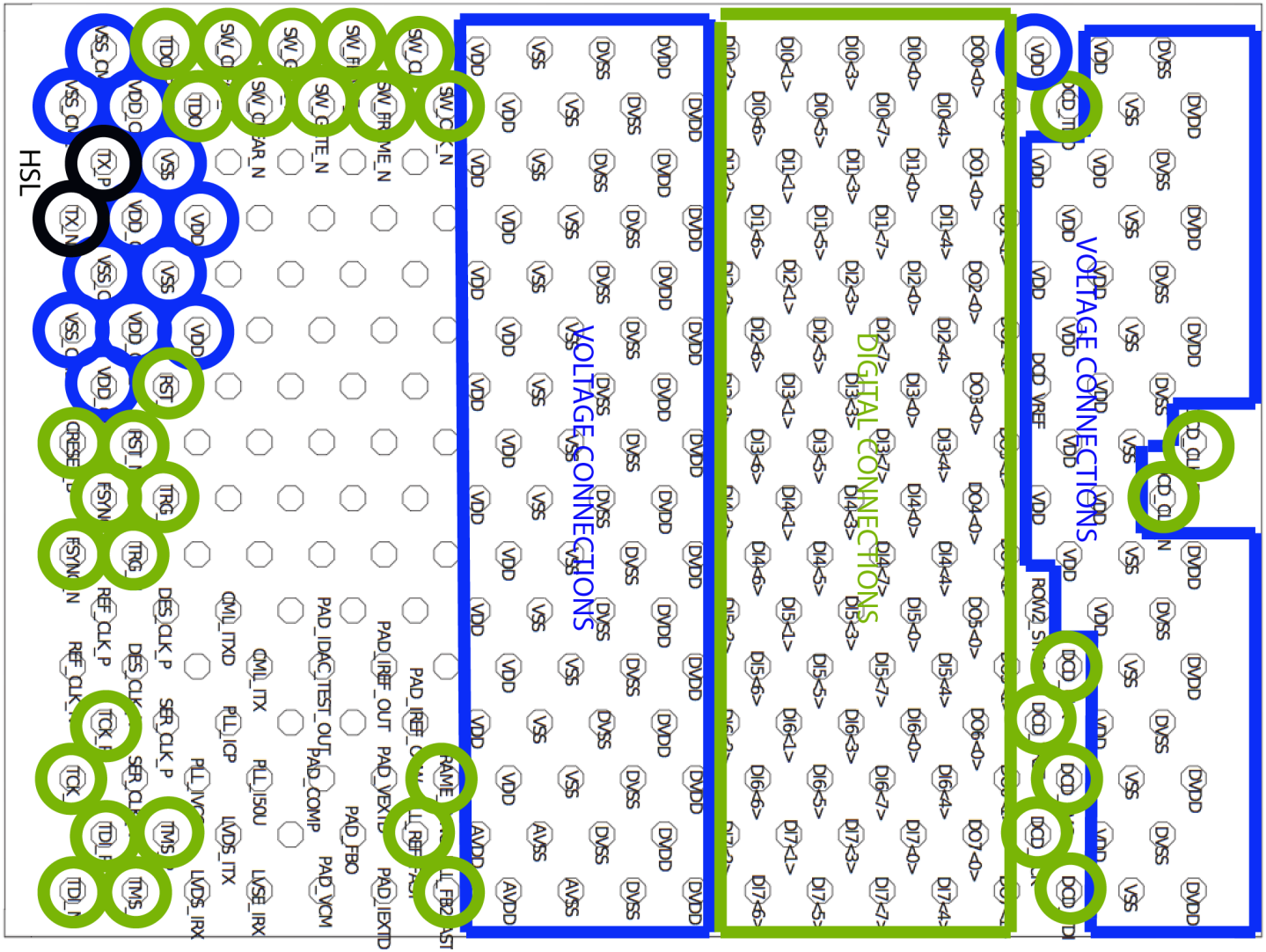
*Keeping the same distance as the EMCM needle card (previous design).



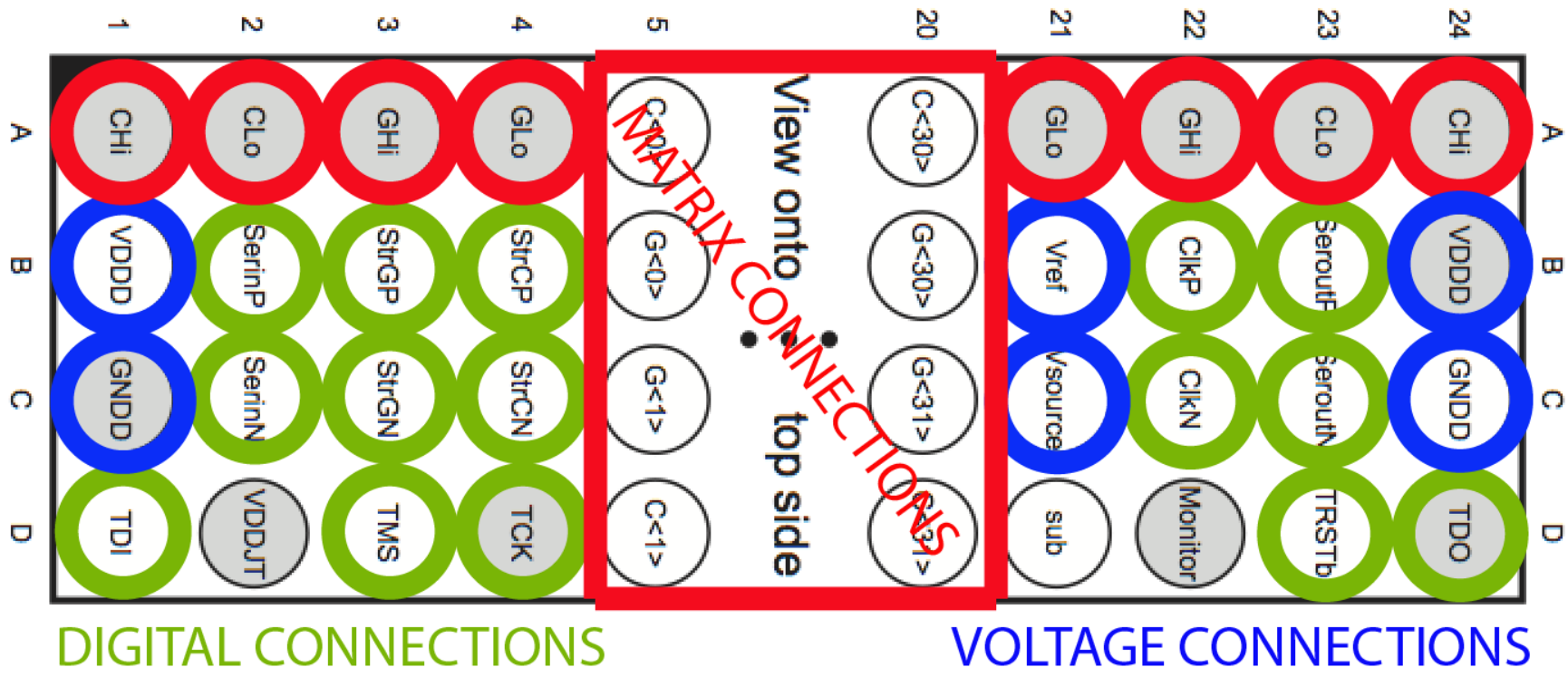
Backup


MATRIX CONNECTIONS
VOLTAGE CONNECTIONS
DIGITAL CONNECTIONS
TDI
TCK
TMS
TRSTB
Clk
SyncRes
Strobe
ClkN
ClkP
RefOut
Refin<2>
Monitor
Refin<1>
TDO

Backup


VOLTAGE CONNECTIONS
DIGITAL CONNECTIONS
VOLTAGE CONNECTIONS
HSL

Backup


1
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4
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23
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A
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C
D
CHi
CLo
GHi
GLo
VDDD
GNDD
SerinP
SerinN
StrGP
StrGN
StrCP
StrCN
VDDJT
TDI
TMS
TCK
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G<0>
G<1>
C<1>
C<30>
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G<31>
C<31>
Vref
Vsource
ClkP
ClkN
SeroutP
SeroutN
Monitor
sub
TRSTb
TDO
View onto top side
MATRIX CONNECTIONS
DIGITAL CONNECTIONS
VOLTAGE CONNECTIONS