Testing of PXD9 sensors from W30

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Paola Avella, Daniel Klose, Christian Koffmane, Jelena Ninkovic, Rainer H. Richter
for the MPP/HLL team

Outline

- Testing summary
- Pilot run wafer status after Al2 and Cu
- Summary of available PXD9 small matrices
- Yield outcome from pre-tests and metallization tests on small matrices
- Results from full scan on F00/W30
- Conclusions and future developments

Summary of testing of PXD9 wafers

- **First phase:** testing after Al1 @ probe station

  possible to measure shorts between metal lines, health of diodes, punch through voltage on long matrices and DEPFET characteristics on test structures

- **Second phase:** testing after Al2 @ probe station equipped with switching system and probe card

  characterization of DEPFETs with info on:
  - Yield outcome of the metal system: shorts among neighbour drain lines and discontinuities in drain lines
  - Pedestal spread from a set of pixels (typically 1000)
  - Threshold voltage from a set of pixels (typically 1000)

- **Third phase:** testing after Cu @ flying needle prober (atg tester)

  final health check on the periphery of each half ladder (End Of Stave + Balcony) looking for inter and intra-level shorts and discontinuities

Status of pilot run wafers after tests on Al1/Al2

Yield in %

	W30	W35	W36
IF	75	100	100
OF1	100	100	100
OF2	100	100	100
OB1	99.8	99.4	0
OB2	99.6	0	99.8
IB	100	0	100
Tot	**95.7**	**66.6**	**83.3**

Wafer grading

W30	W35	W36
3	2	2
0	2	2
2	2	2
2	2	4
2	4	2
2	4	2

- The yield info combines results from pre-tests (i.e. All Clear vs Source) and results from Al2 characterization. *Shorts in poly1/poly2 are not reported in the table.*
- The wafer grading info refers to the full characterization performed up to the second metal (i.e. Al2) of the PXD half ladder metallization. *Shorts in poly1/poly2 are included.*
- **0** = no faults; **1** = pixel level faults; **2** = row/column level faults; **3** = high impact faults; **4** = lethal faults; **5** = to be clarified.

Status of pilot run wafers after tests on Cu

Yield in %

	W30	W35	W36
IF	0	100	100
OF1	100	100	100
OF2	100	100	100
OB1	99.8	99.4	0
OB2	99.6	0	99.8
IB	100	0	100
Tot	**95.7**	**66.6**	**83.3**

Wafer grading

W30	W35	W36
4	2	2
0	2	2
2	2	2
2	2	4
2	4	2
2	4	2

- IF/W30 resulted affected by the handling damage: despite a still (partially) operational matrix, lethal shorts in the periphery were introduced.
- OF1/W30 has no defects (platinum chip), OF2 and OB2 have one short in the poly layers (golden chips), OB1 and IB present multiple (i.e. ≥ 2) shorts in the poly layers (silver chips).
- **0** = no faults; **1** = pixel level faults; **2** = row/column level faults; **3** = high impact faults; **4** = lethal faults; **5** = to be clarified.

PXD9 small matrices of W30

L (μm)	Z (μm)	#	Design	Chips
3	55	1	STD	A00
3.5	55	3	STD	A01, E02, N01
4	55	2	STD	A04, L00
4.5	55	2	STD	A07, F02
5	55	3	STD	A02, A05, F00
5	60	5	STD	A03, A06, I02, L02, N03
5	70	4	STD	B00, B02, I00, N04
5	85	5	STD	C00, C02, J00, M02, N06
5.4	75	3	SCG	E00, G02, J02
6	55	3	STD	D00, G00, H02
TOT		**31**		

Four additional small matrices with ILC design omitted as not relevant to the Belle II community.

PXD9 small matrices of W30

L (μm)	Z (μm)	#	Design	Chips
3	55	1	STD	A00
3.5	55	3	STD	A01, E02, N01
4	55	2	STD	A04, L00
4.5	55	2	STD	A07, F02
5	55	3	STD	A02, A05, F00
5	60	5	STD	A03, A06, I02, L02, N03
5	70	4	STD	B00, B02, I00, N04
5	85	5	STD	C00, C02, J00, M02, N06
5.4	75	3	SCG	E00, G02, J02
6	55	3	STD	D00, G00, H02
TOT		31		

Needs further inspection

Destroyed during optical inspection

Affected by bugs in the layout

The remaining (15) matrices passed the pre-test phase showing total absence of poly1/poly2 shorts.

Four additional small matrices with ILC design omitted as not relevant to the Belle II community.

Yield outcome of PXD9 small matrices of W30

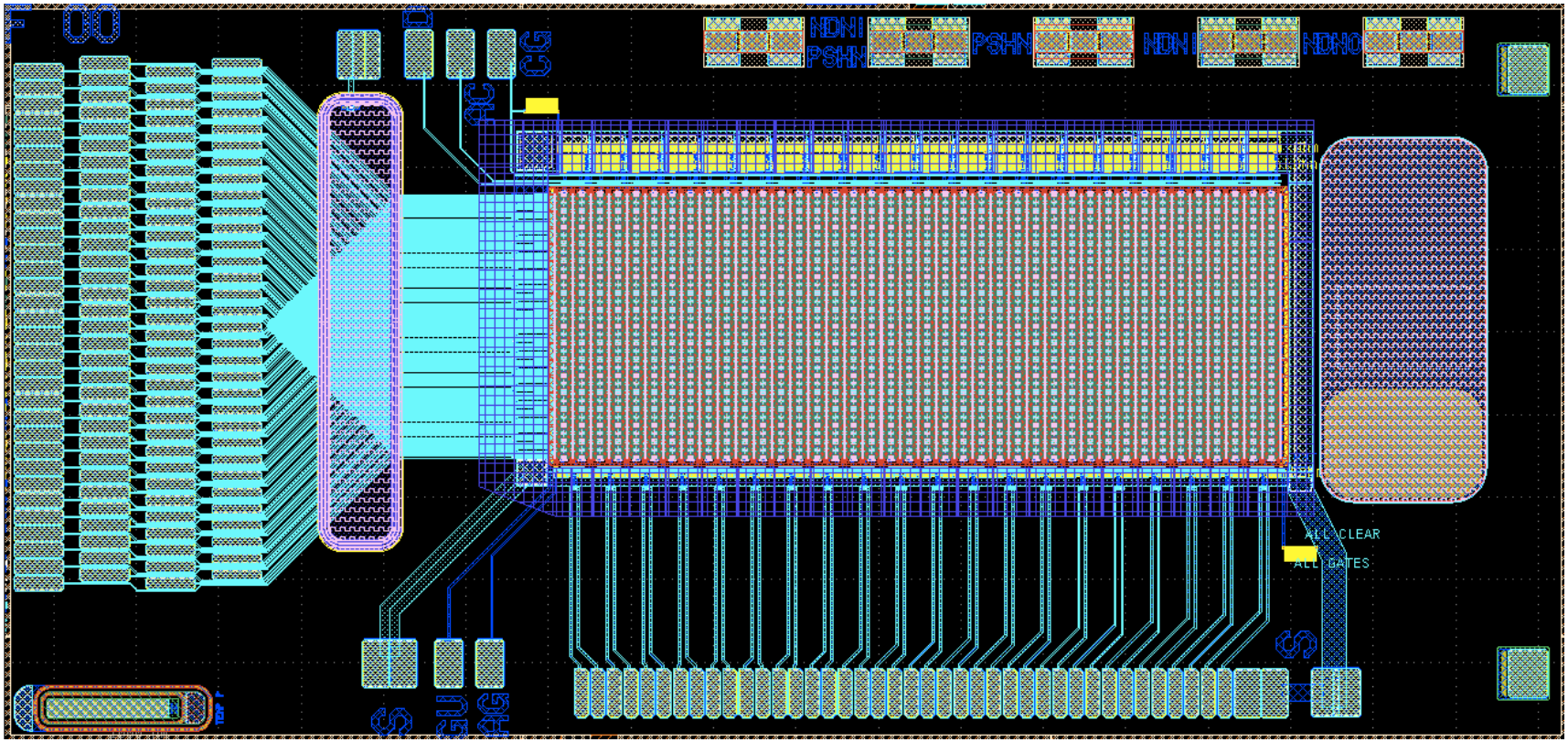
- **Chips:** 6 matrices, **with Z55 and L5 and L6** were selected for test of the metal system
- **Instrumentation:** probe station PA200 equipped with semi-automatic probe head and Keithley SCS 4200.
- **Test:** measurement of transfer characteristics at the last gate row, to understand how many discontinuities in the drain lines and stringers among neighbour drain lines are present.
- F00 was selected to perform a full matrix scan

	Chip	opens	shorts	$\langle I_{ds} \rangle$ (μm)	δi_{ds} (%)	V_{th} (μm)	Status
L5	A02	0	0	-120.19 ± 0.01	8.42 ± 0.02	0.14 ± 0.04	Hybrid 5/ Bonn?
L5	A05	0	0	-120.44 ± 0.01	10.61 ± 0.02	0.11 ± 0.04	Hybrid 5/ Bonn
L5	F00	0	0	-107.76 ± 0.01	13.06 ± 0.03	0.03 ± 0.04	EMCM/ Munich
L6	D00	0	0	-72.90 ± 0.01	13.53 ± 0.03	-0.25 ± 0.03	Hybrid 5/ Bonn
L6	G00	0	0	-72.07 ± 0.01	8.85 ± 0.03	-0.24 ± 0.03	tbd
L6	H02	1	10	-72.76 ± 0.01	7.98 ± 0.03	-0.23 ± 0.03	tbd

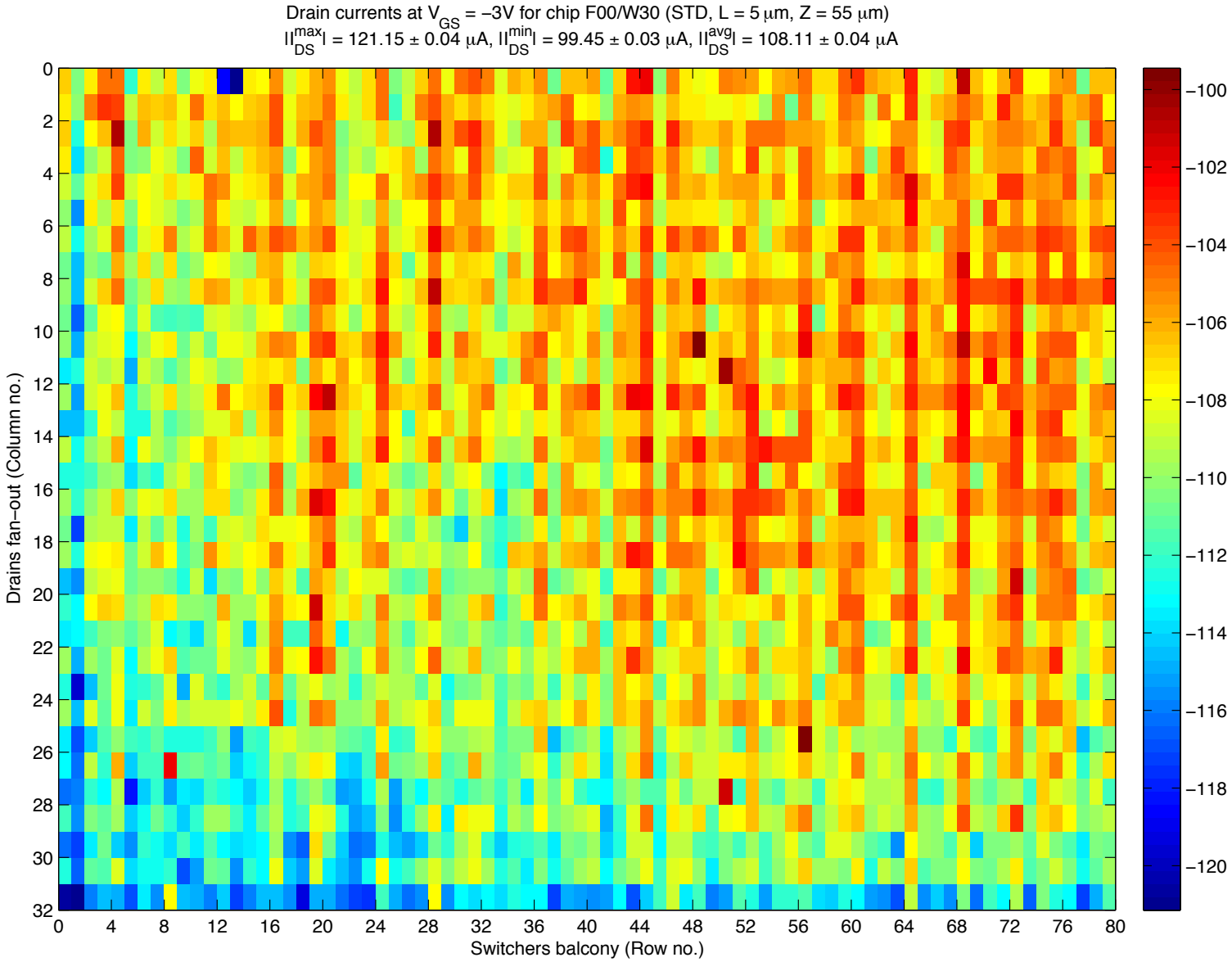
*the values reported in the table refer to measurements on the last gate row, i.e. involve a total of 128 pixels.

Small matrix F00/W30

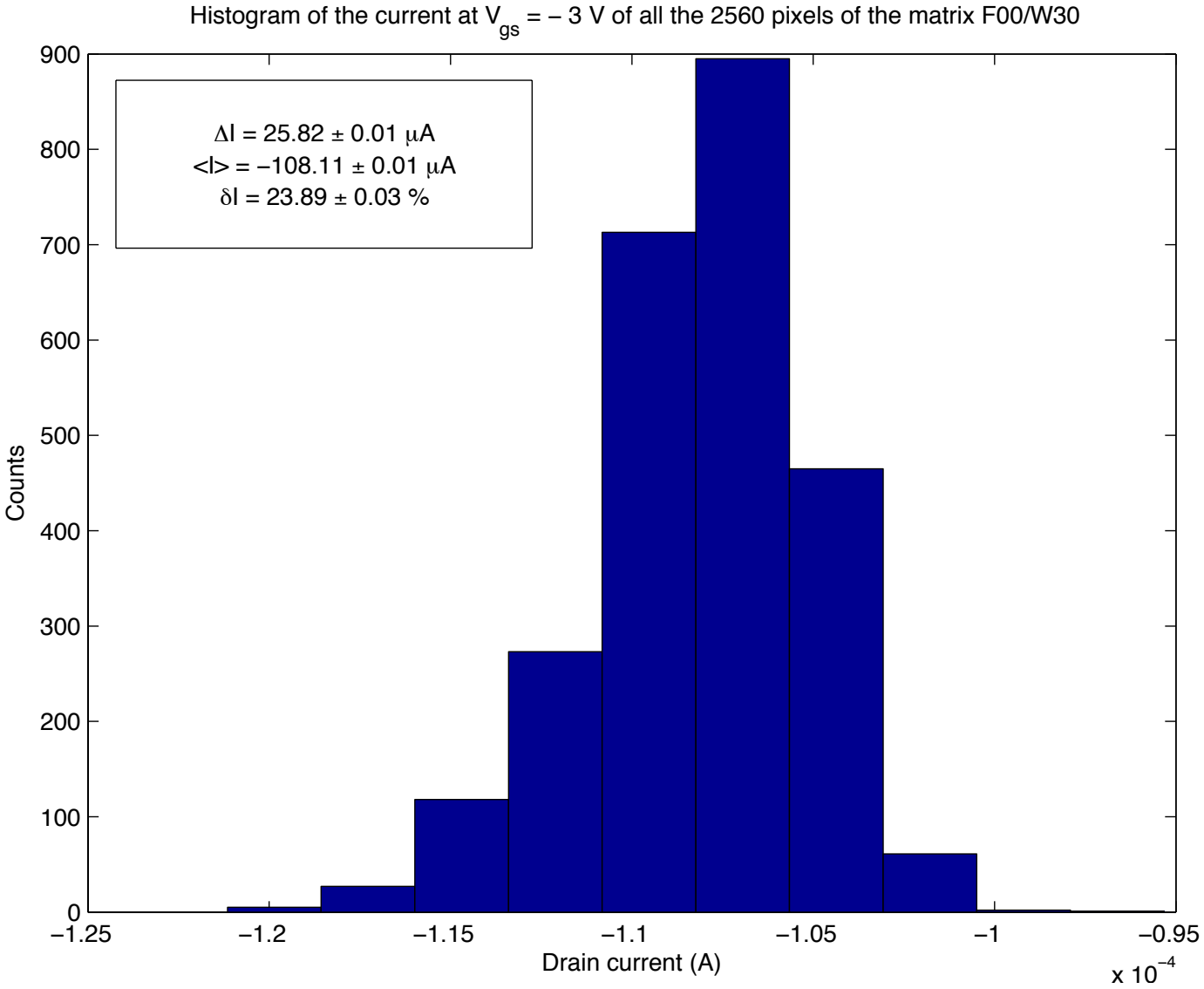
- 128 drain lines
- 20 gate rows
- 2560 total pixels



Map of small matrix F00/W30



Spread of F00/W30

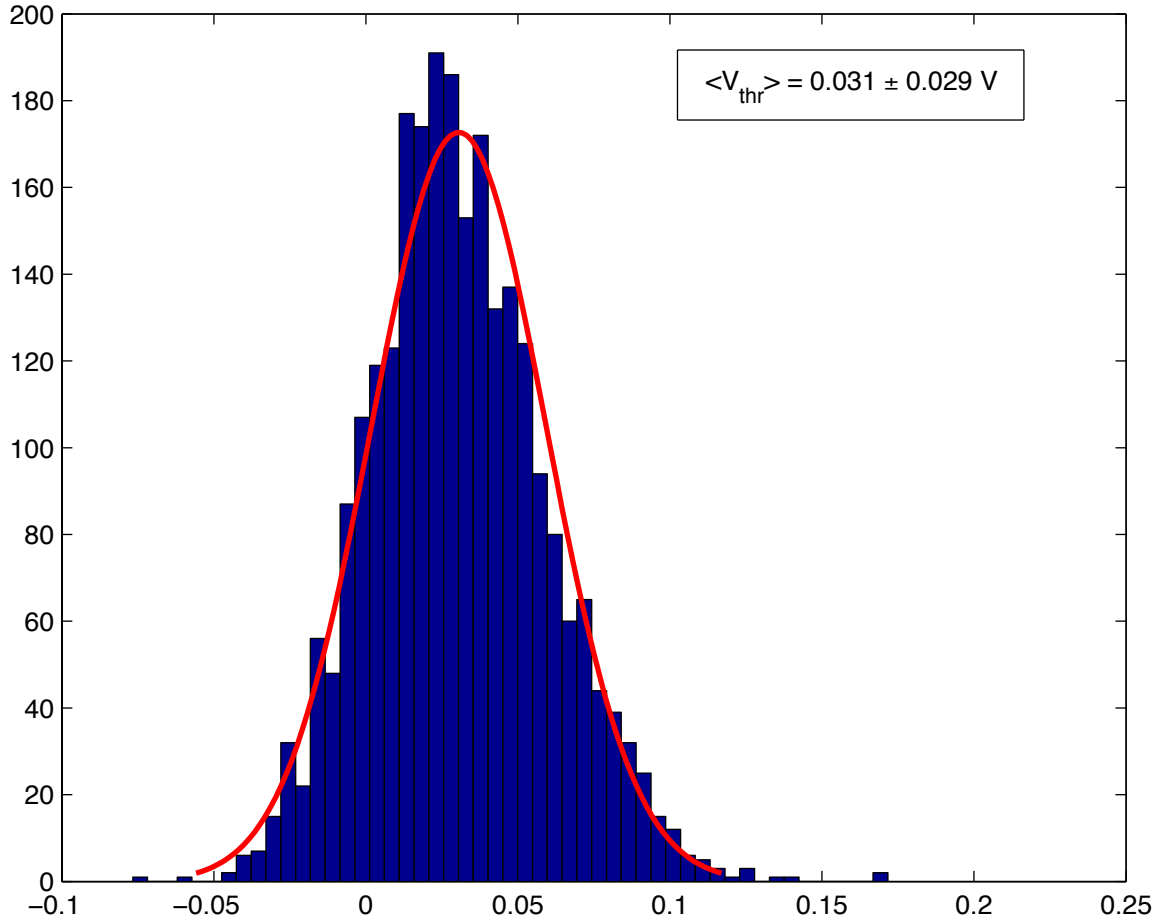


$$\Delta I = \left| I_{\max} \right| - \left| I_{\min} \right|$$

$$< I >= \left. \frac{\sum_{i=1}^{N} I_{ds}^{i}}{N} \right|_{N=2560}$$

$$\delta I = \frac{\Delta I}{< I >} \cdot 100$$

Threshold voltage of F00/W30



$$\sqrt{I_{DS}} = a + b \cdot V_{GS}$$

$$V_{thr} = -\frac{a}{b}$$

$$< V_{thr} >= \left. \frac{\sum_{i=1}^{N} V_{thr}^{i}}{N} \right|_{N=2560}$$

Conclusions and future developments

- The three phases of wafer level testing of PXD9 were completed for W30, with the outcome of five good half ladders (one of which classified as grade 0) and one faulty chip.

- Pre-tests to qualify the status of 31 small matrices with various technology parameters have given the result of 15 healthy chips.

- Small matrices with Z55 and L5 and L6 have been selected for metal system yield verification, with the result that all, but one (H02), are faults free

- The chip F00 has been selected for full matrix test: it shows a quite uniform distribution of the currents, a percentage spread of 24% and uniform threshold voltage of 0.03 V.

- More chips to follow next autumn…

Thank you for your attention!