Boundary Scan Test of the Belle II Pixel Vertex Detector

Triest 10.09.2015

8th Belle II VXD Workshop

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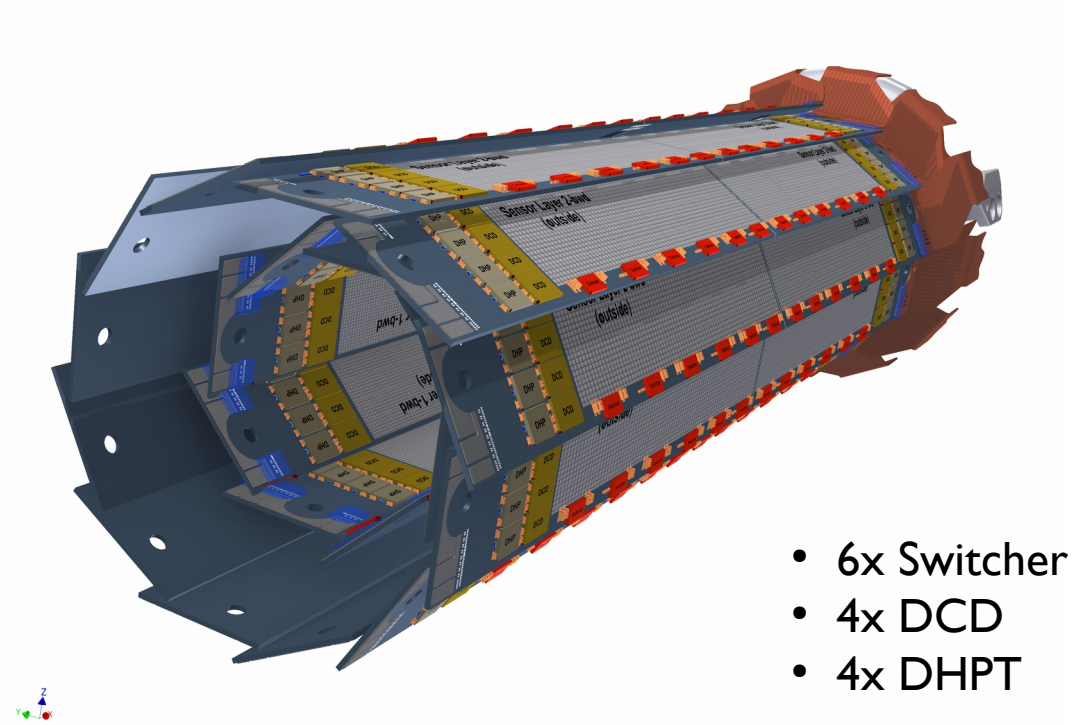
PXD bump bonds



ASIC	Pins
Switcher	96
DCD	431
DHPT	255

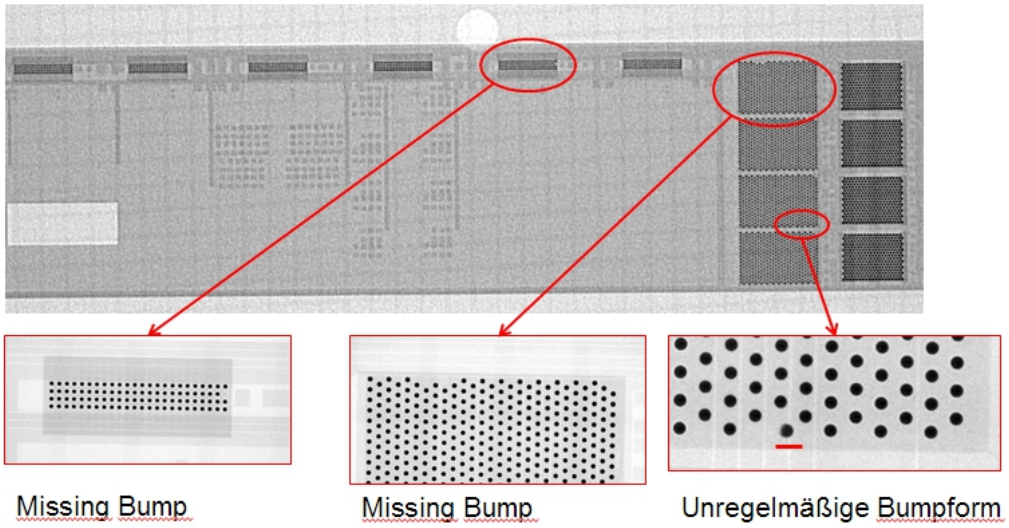
- 6x Switcher
- 4x DCD
- 4x DHPT

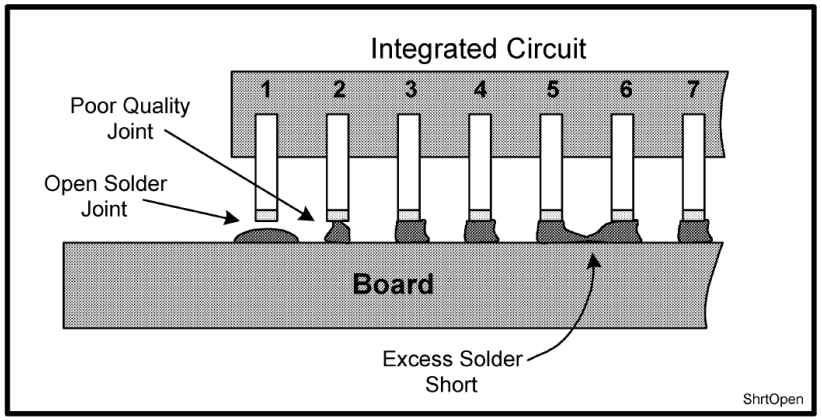
} 3320 for each half ladder

→ 132.800 bump bonded ASIC pins

PXD bump bonds

X-Ray W17-4

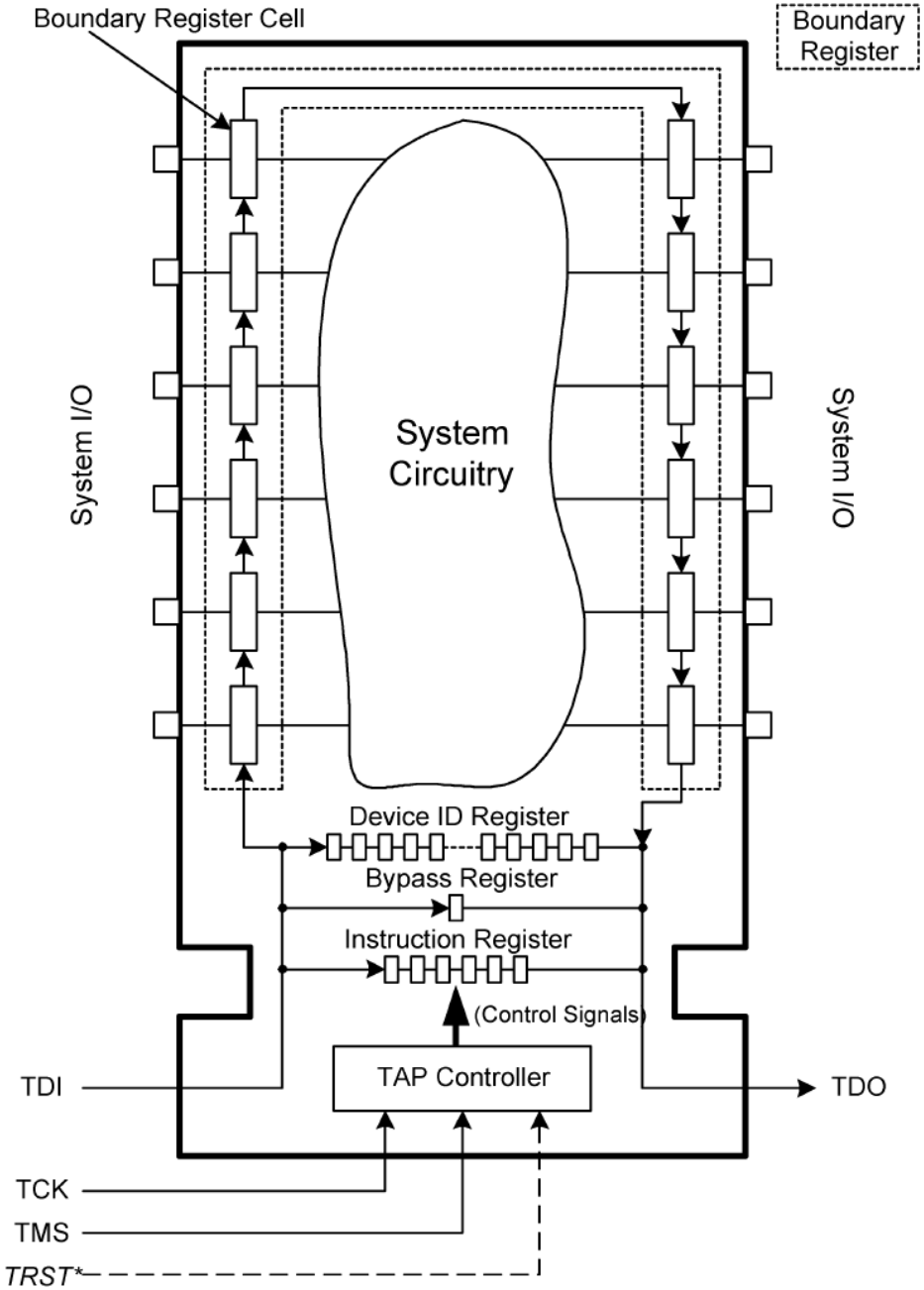




Fraunhofer IZM

e.g. DCD chip bump pitch:
200µm in y and 180µm in x

not accessible for a probe station with needles



JTAG

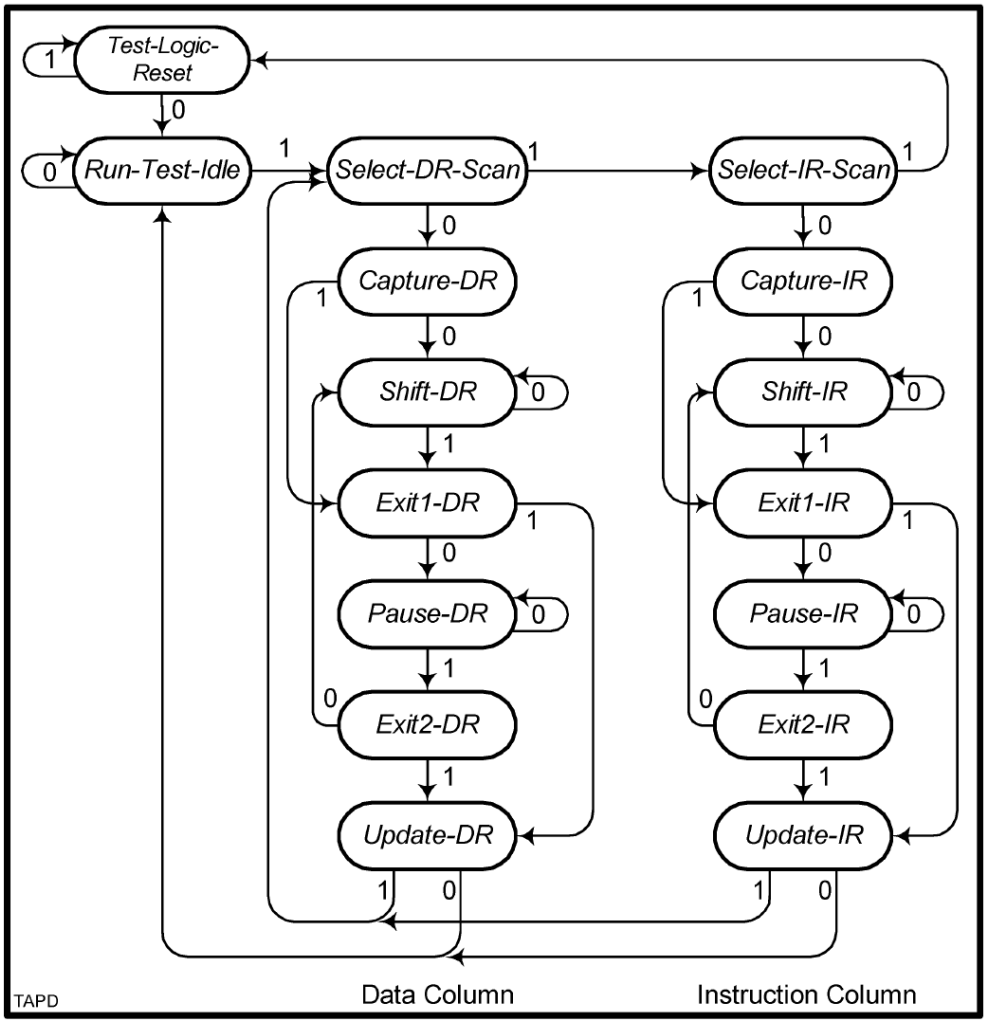
IEEE Std. 1149.1
Joint Test Action Group (JTAG)

additional boundary-scan cells (BSC) at the I/Os of an IC

four additional I/O ports
Test Access Port (TAP)

TCK	test clock
TMS	test mode select
TDI	test data input
TDO	test data output
(TRST	test reset)

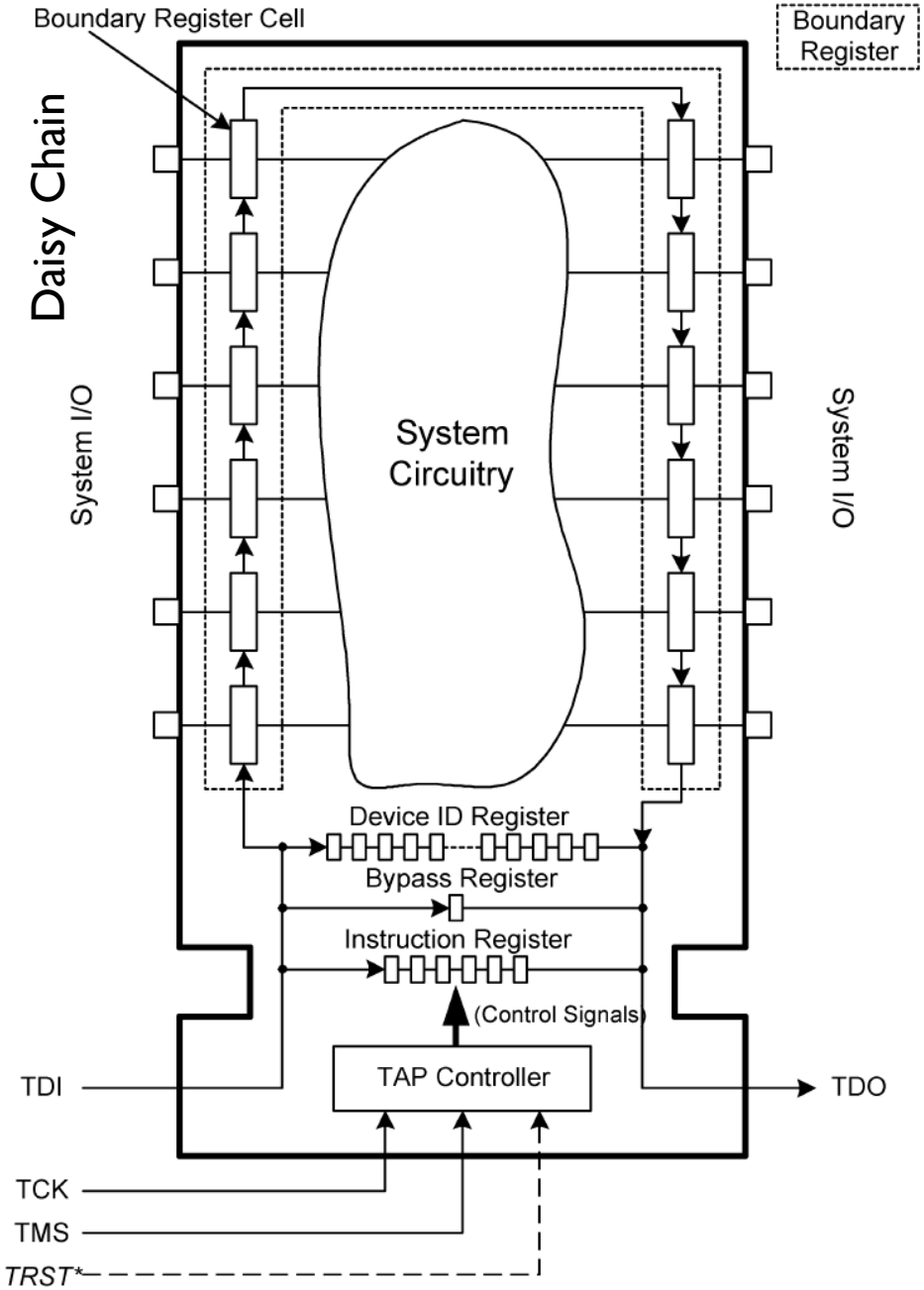
TAP controller



state transition diagram of the TAP controller (Test Access Port)

16 state machine

controlled by TCK and TMS



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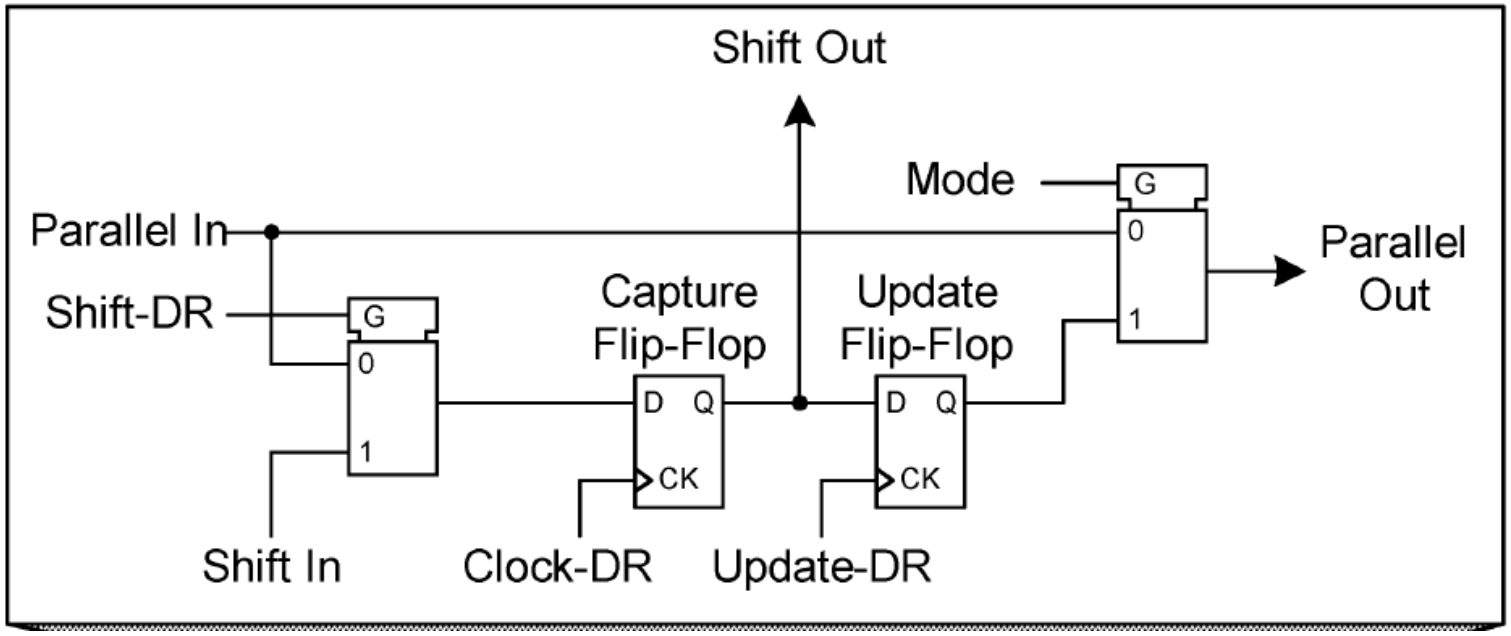
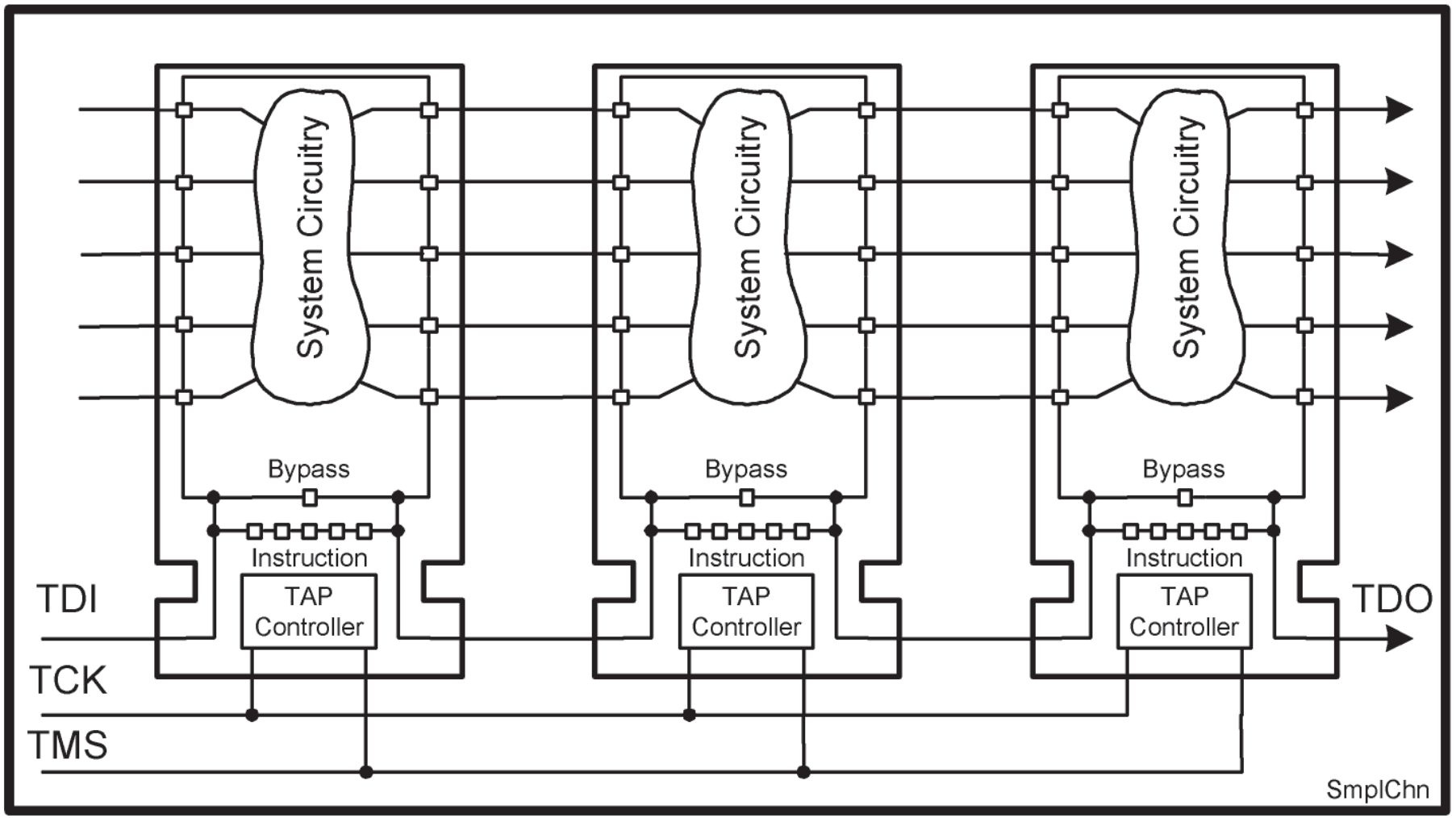
Boundary Register Cell

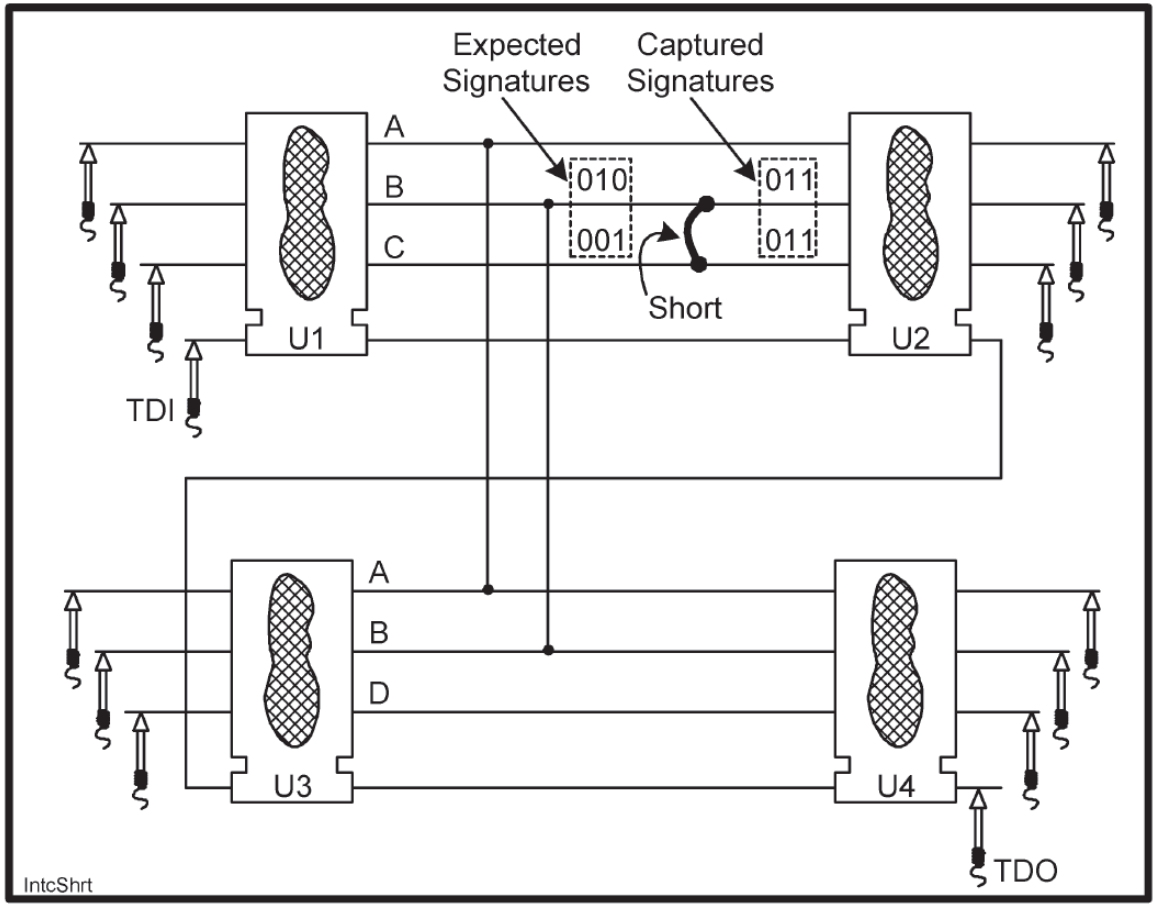


two multiplexer
two flip-flops

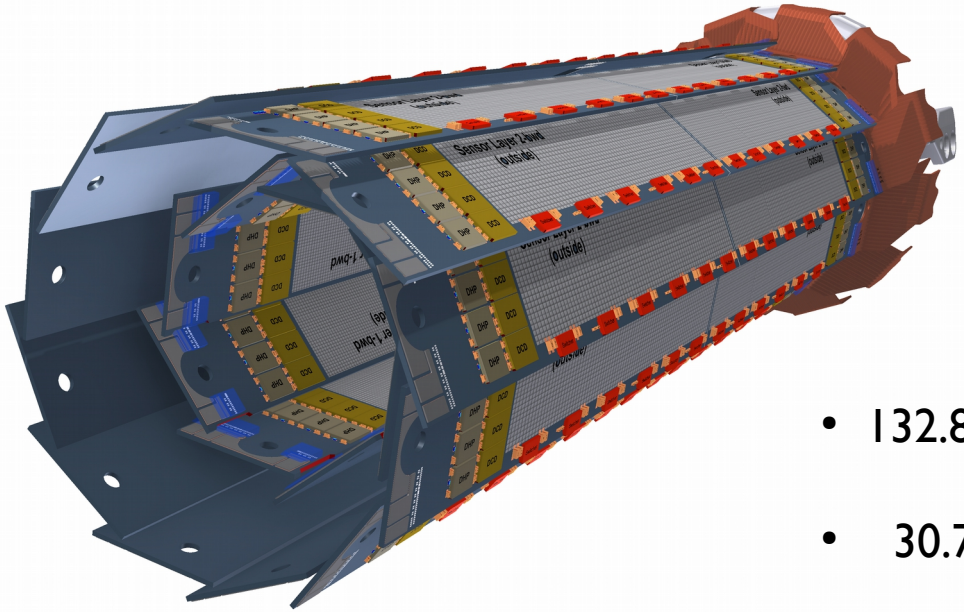
Chain of Boundary Scan ICs



Interconnect Test



PXD bump bonds



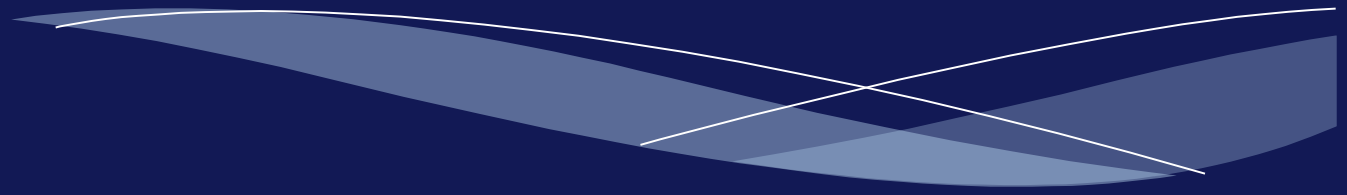
ASIC	Pins	BSC (Pins)
Switcher	96	10
DCD	431	80
DHPT	255	97

- 132.800 bump bonded ASIC pins
- 30.720 accessible through BS

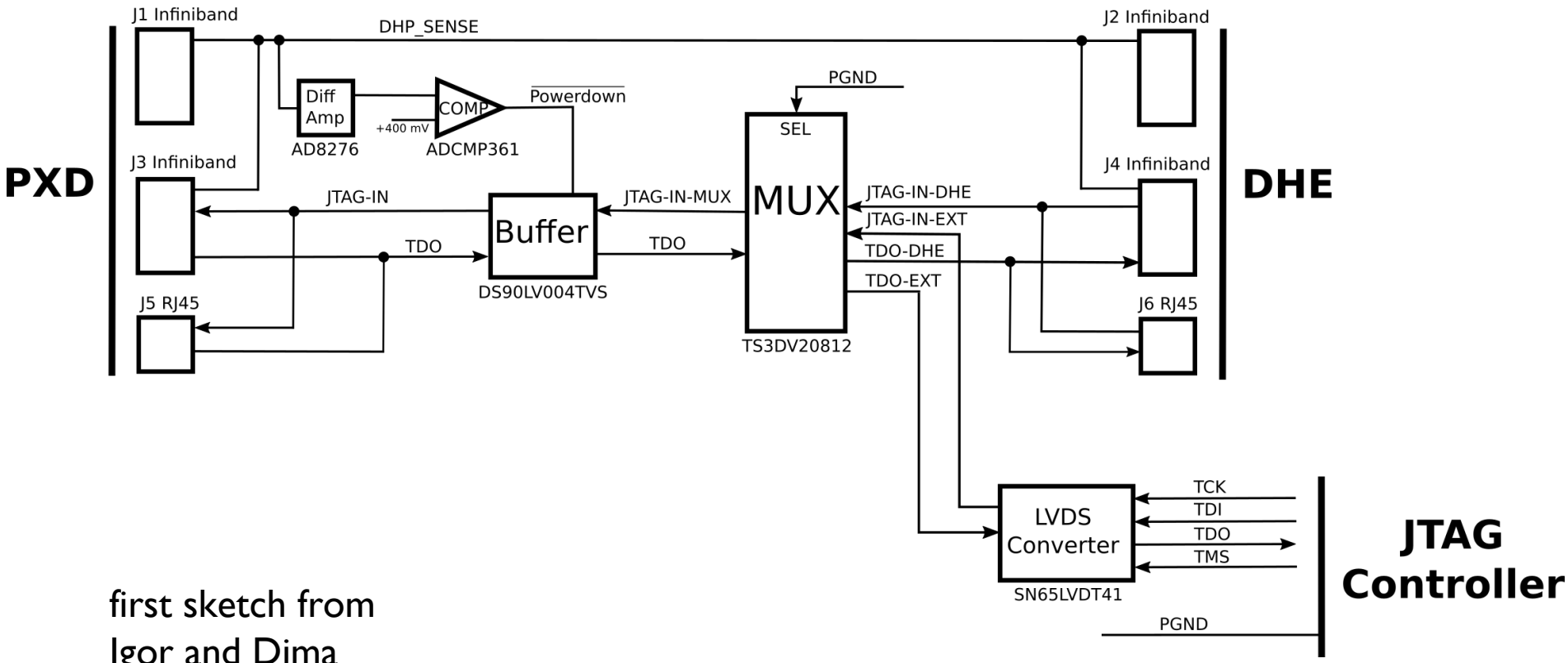
→ ~ 23% direct test coverage
(additional functional tests:
power pins, JTAG pins, CLK, ...)

HARDWARE

http://twiki.hll.mpg.de/bin/view/DepfetInternal/JTAG20Breakout20Board20(JBB)

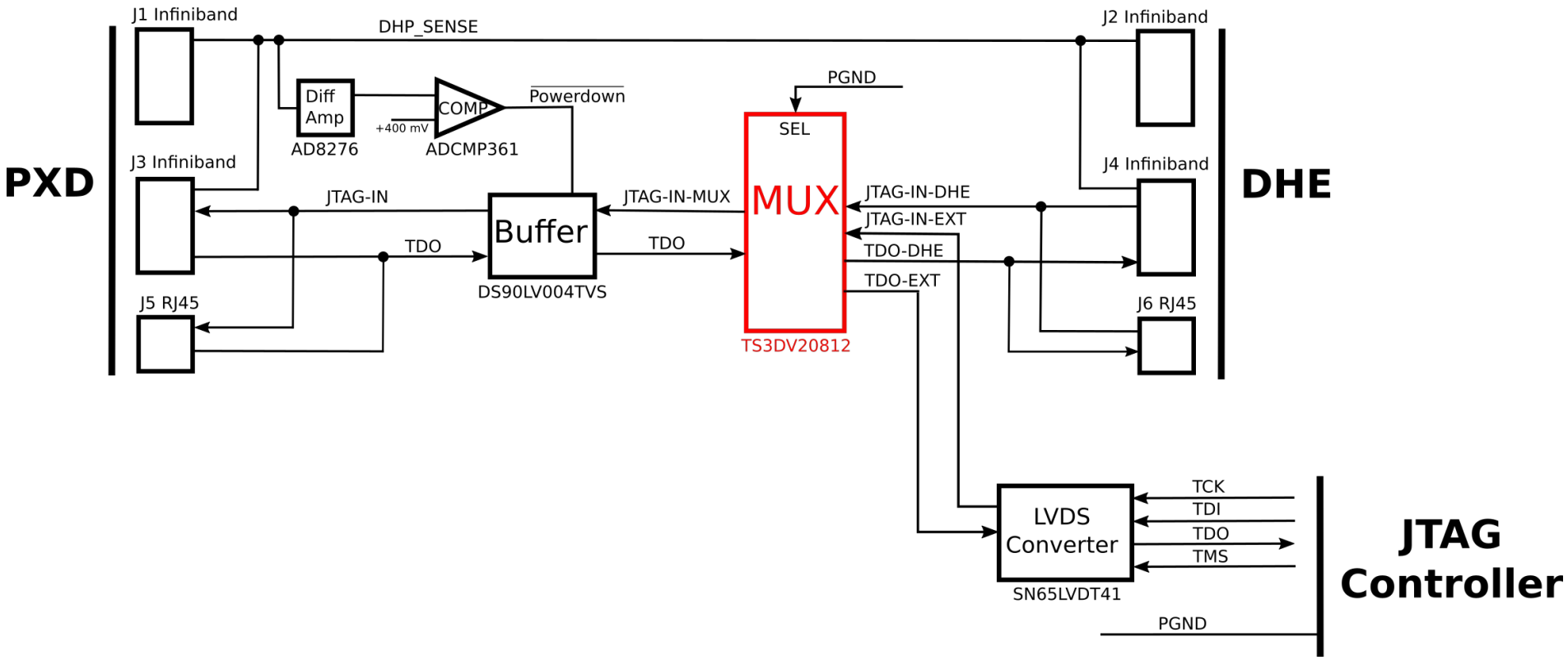


JTAG Breakout Board

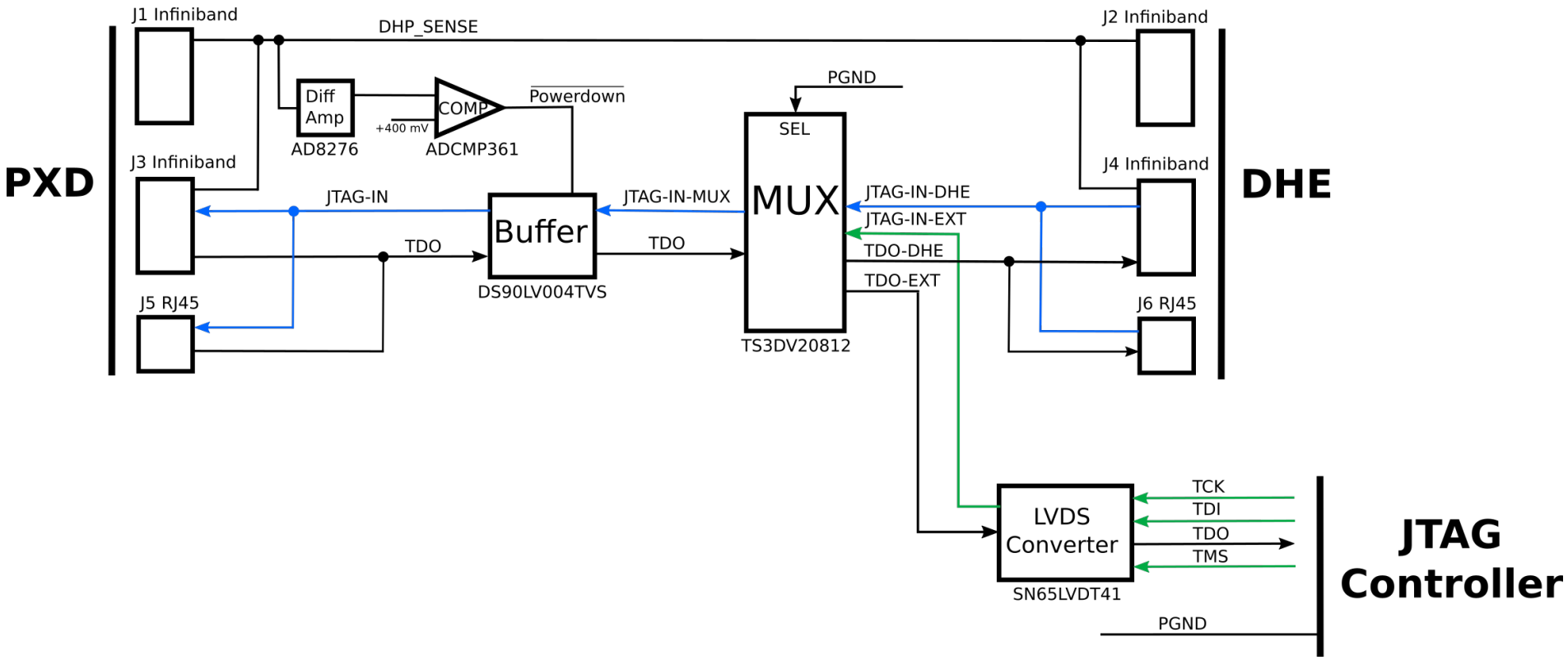


first sketch from
Igor and Dima

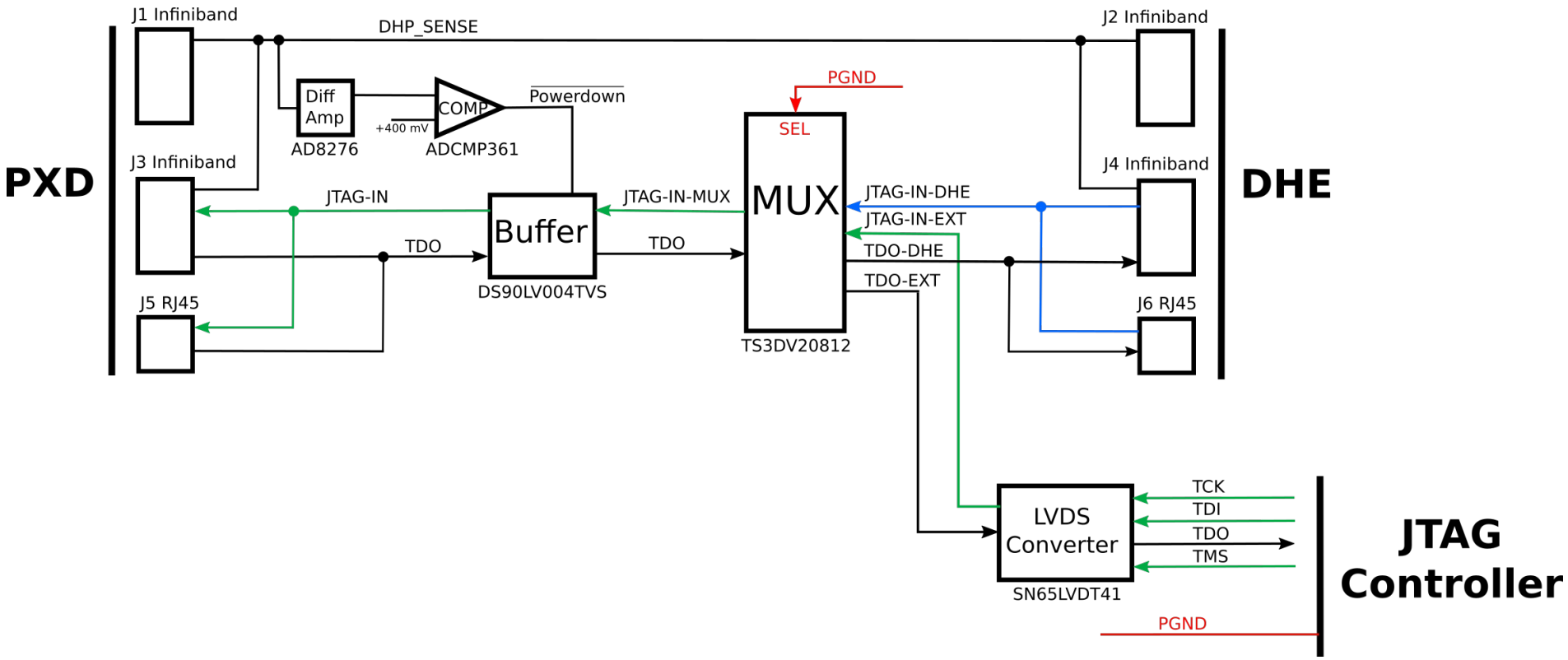
JTAG Breakout Board



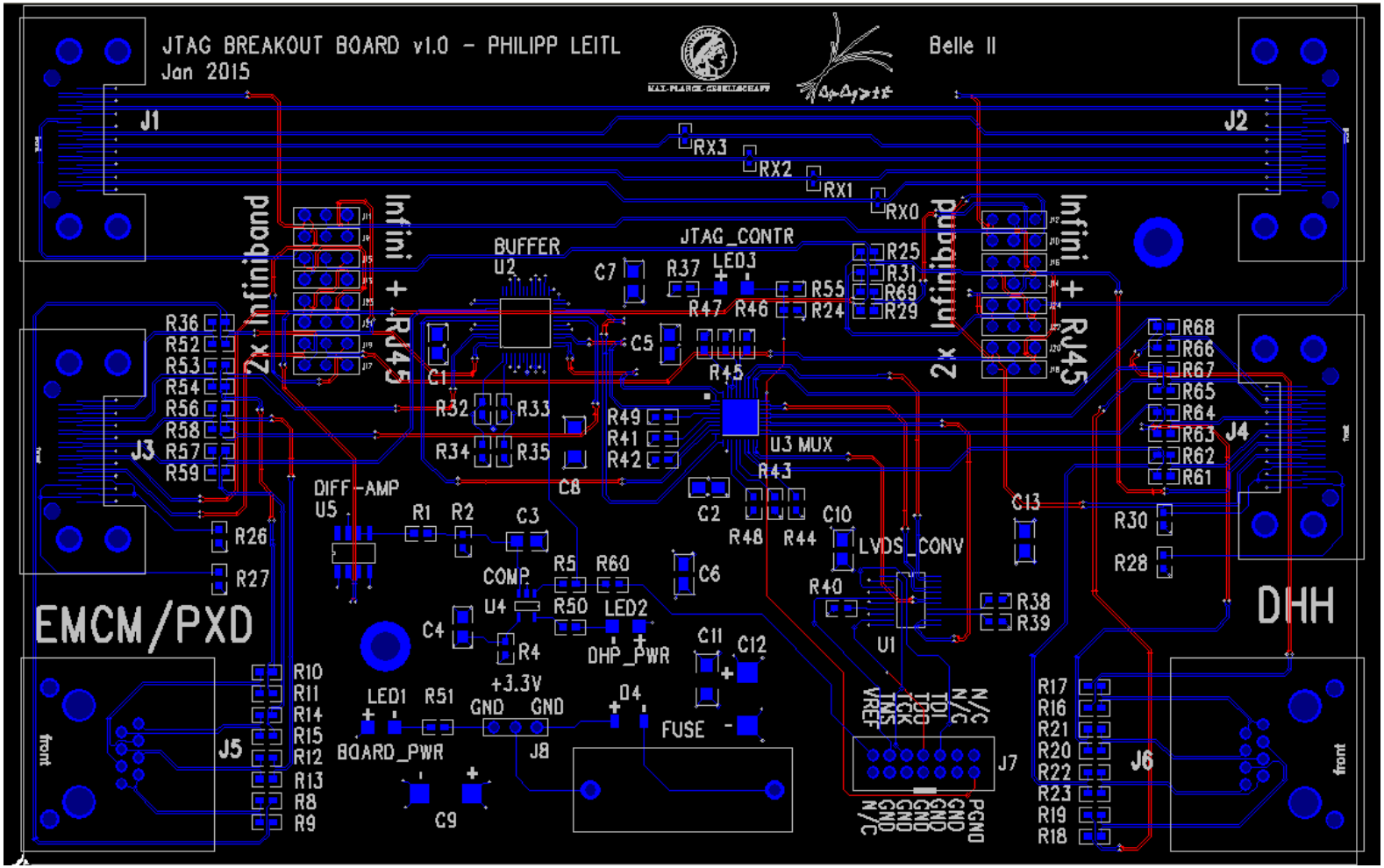
JTAG Breakout Board



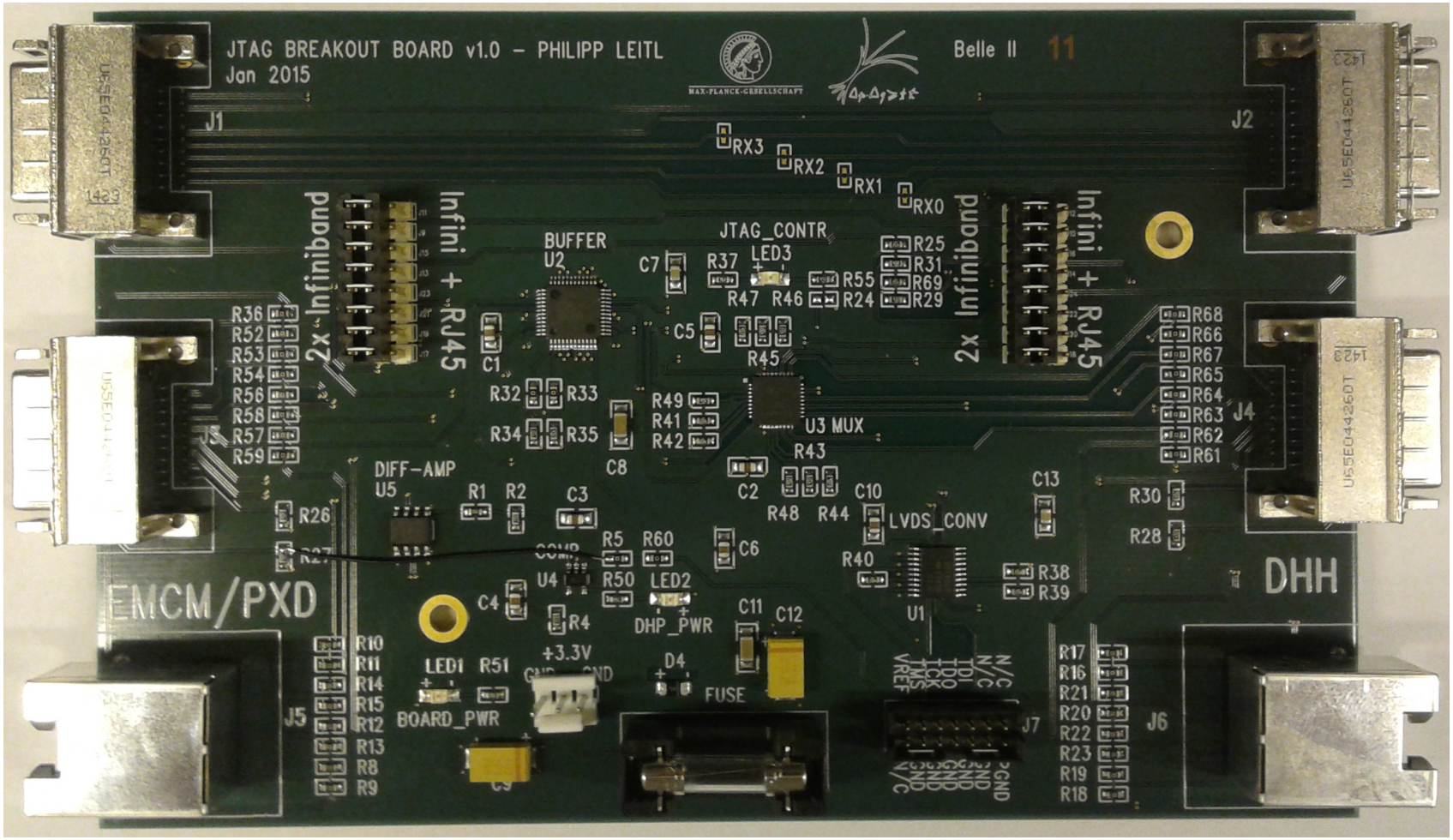
JTAG Breakout Board



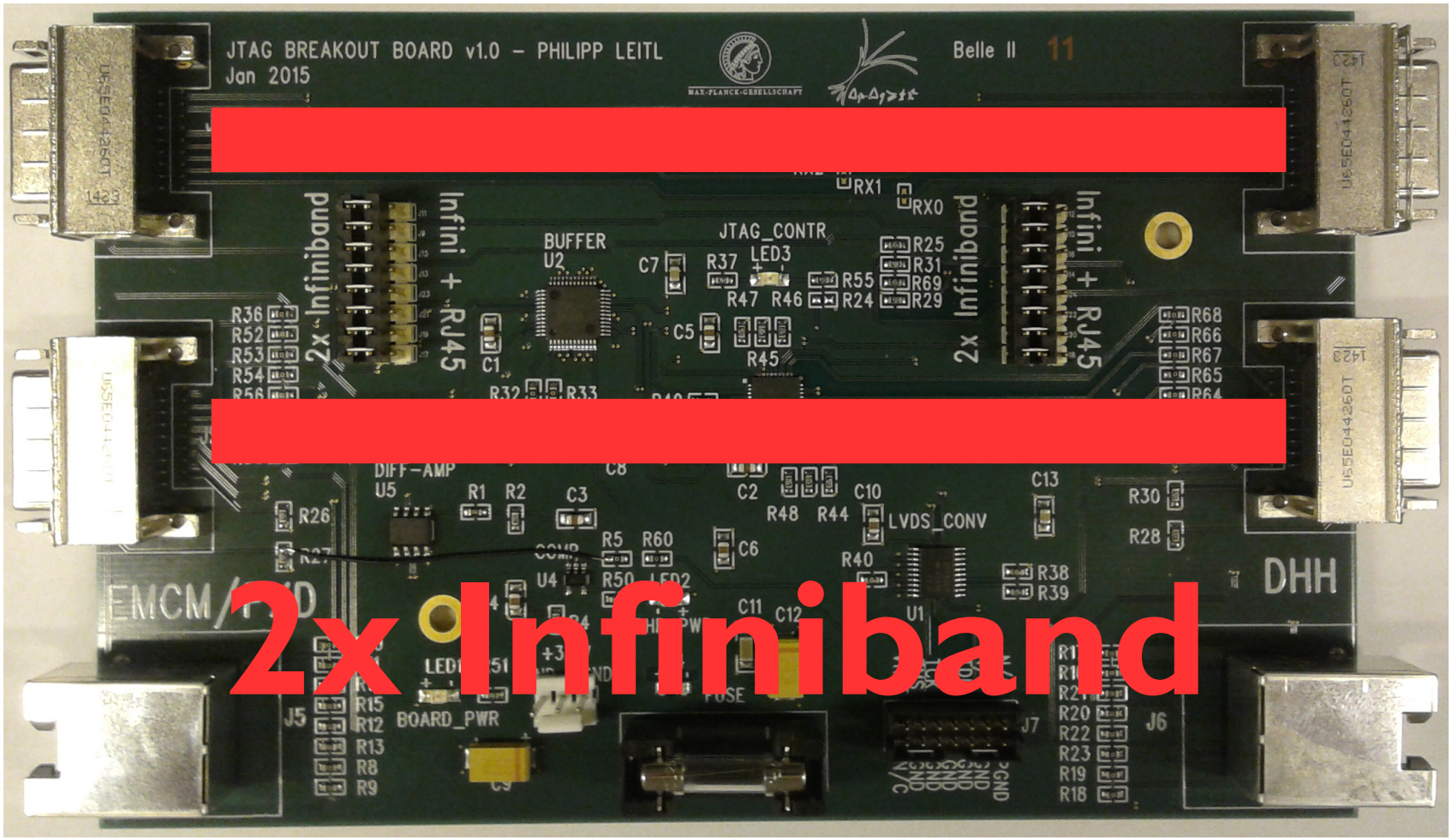
JTAG Breakout Board



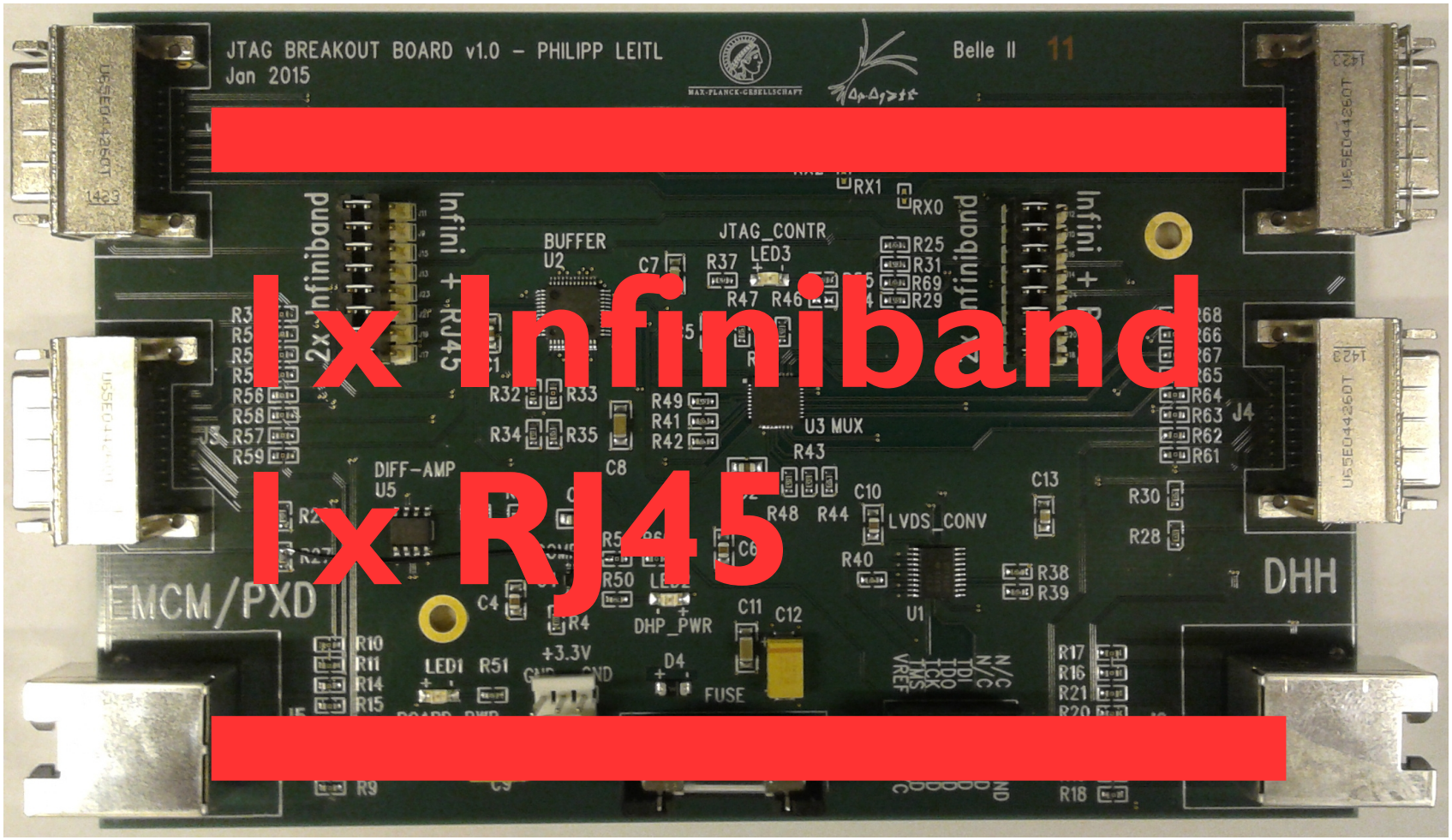
JTAG Breakout Board



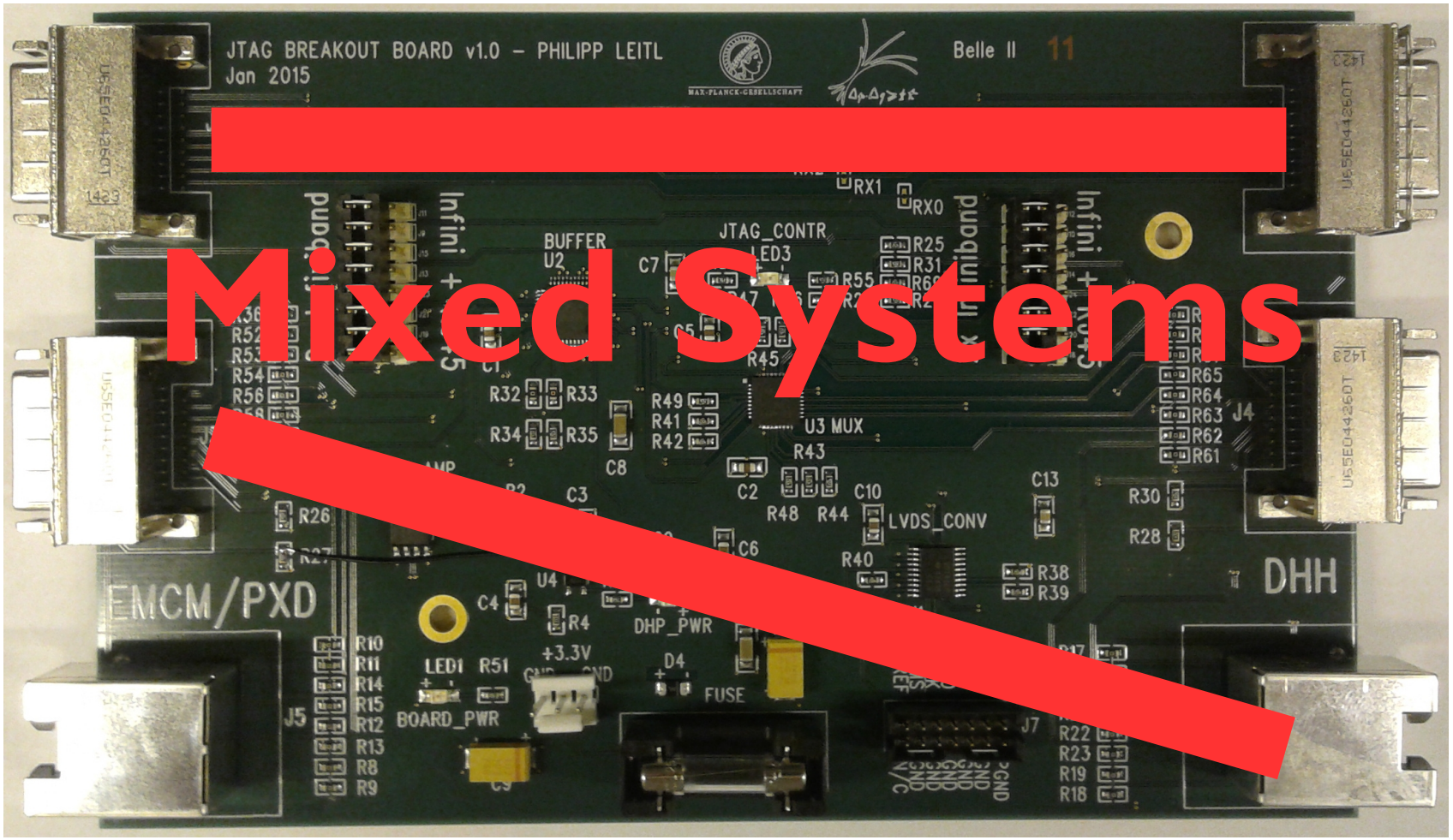
JTAG Breakout Board



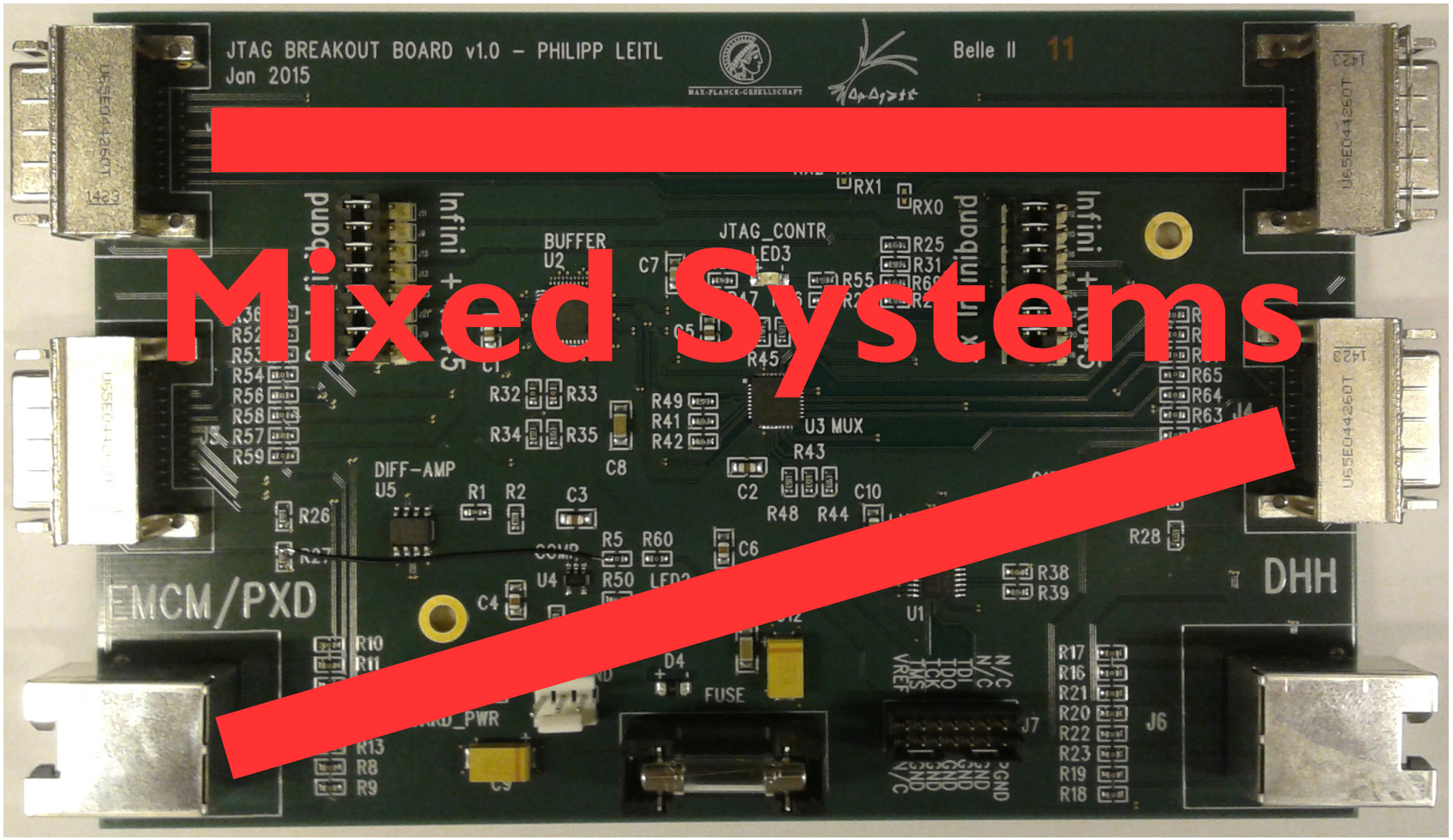
JTAG Breakout Board



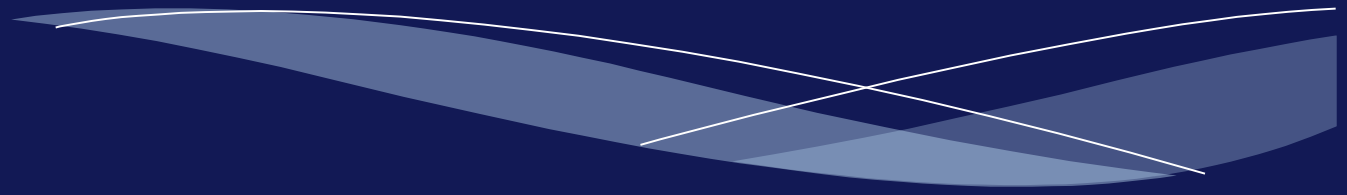
JTAG Breakout Board



JTAG Breakout Board



SOFTWARE



Boundary Scan Software

- New commercial system needed → offers from different vendors
  - demo-version in the meantime
  - different JTAG controller → adapter needed
  - decision for XJTAG

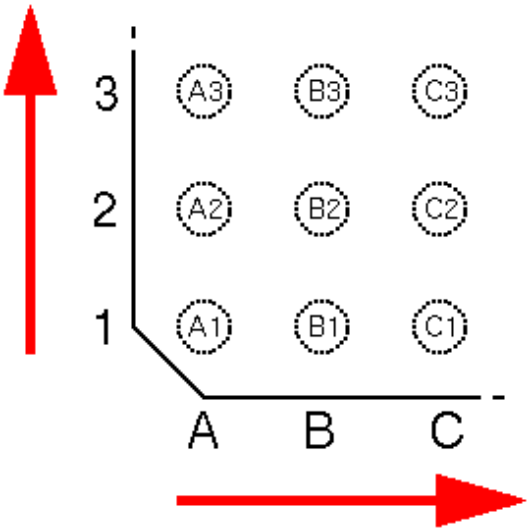
- Boundary Scan Description Language (BSDL) files
  - DHP02 and DHPT10: software generated
  - SwitcherB18 v1 and v2: manually written by Christian Kreidl
  - DCD-Bv2 and Bv4-pipeline: manually written by me

} several versions

- Netlist
  - problematic EDIF format ("flavours")
  - import settings for EDIF (XJTAG support)
  - manually edited

Boundary Scan Software

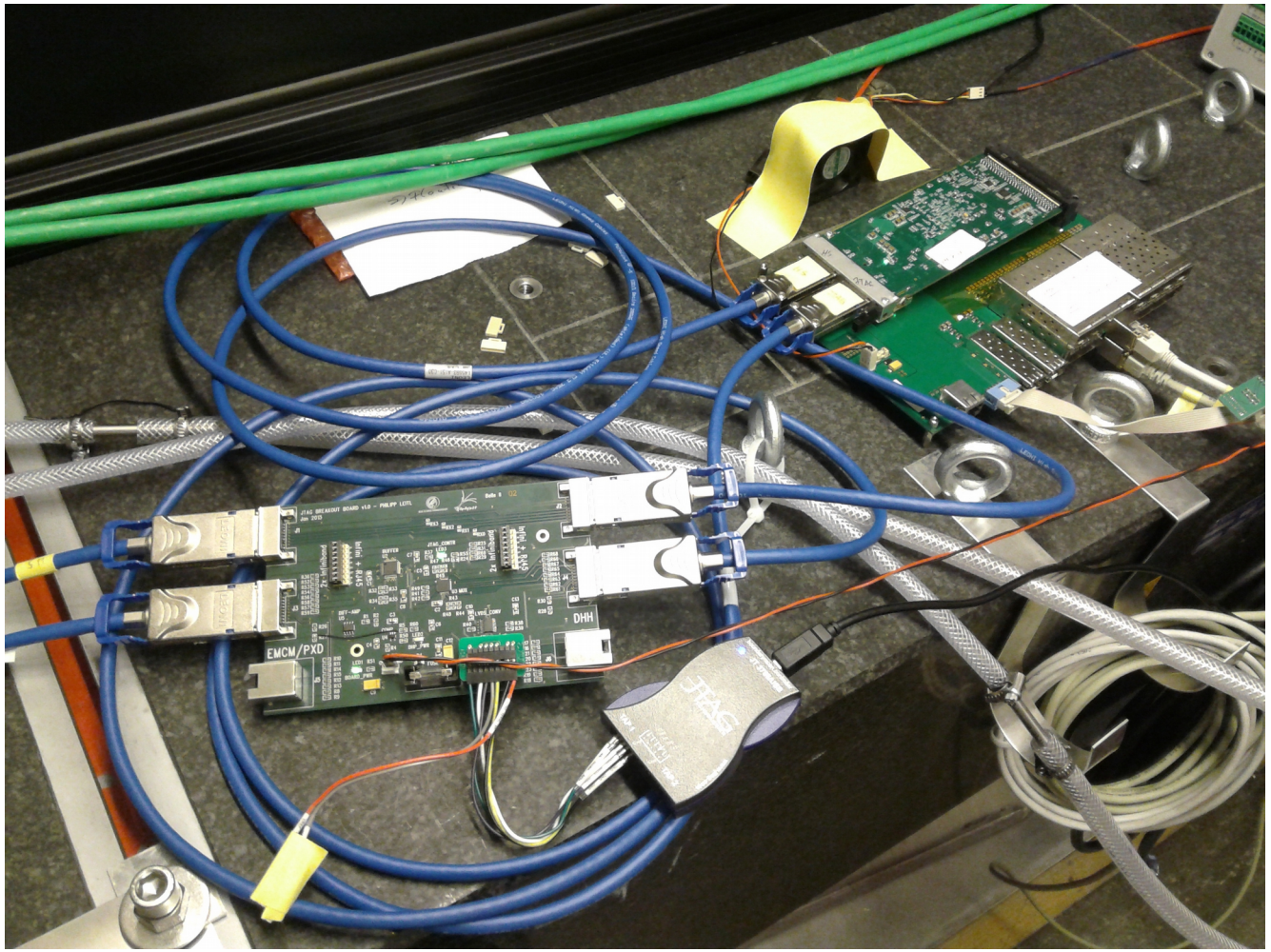
- Boundary Scan Description Language (BSDL) files
  - redefinition of pin arrays: bit_vectors → bit
  - correctly defining voltage differential pins
  - introducing alphanumeric numbering scheme



now using the same names and numbers

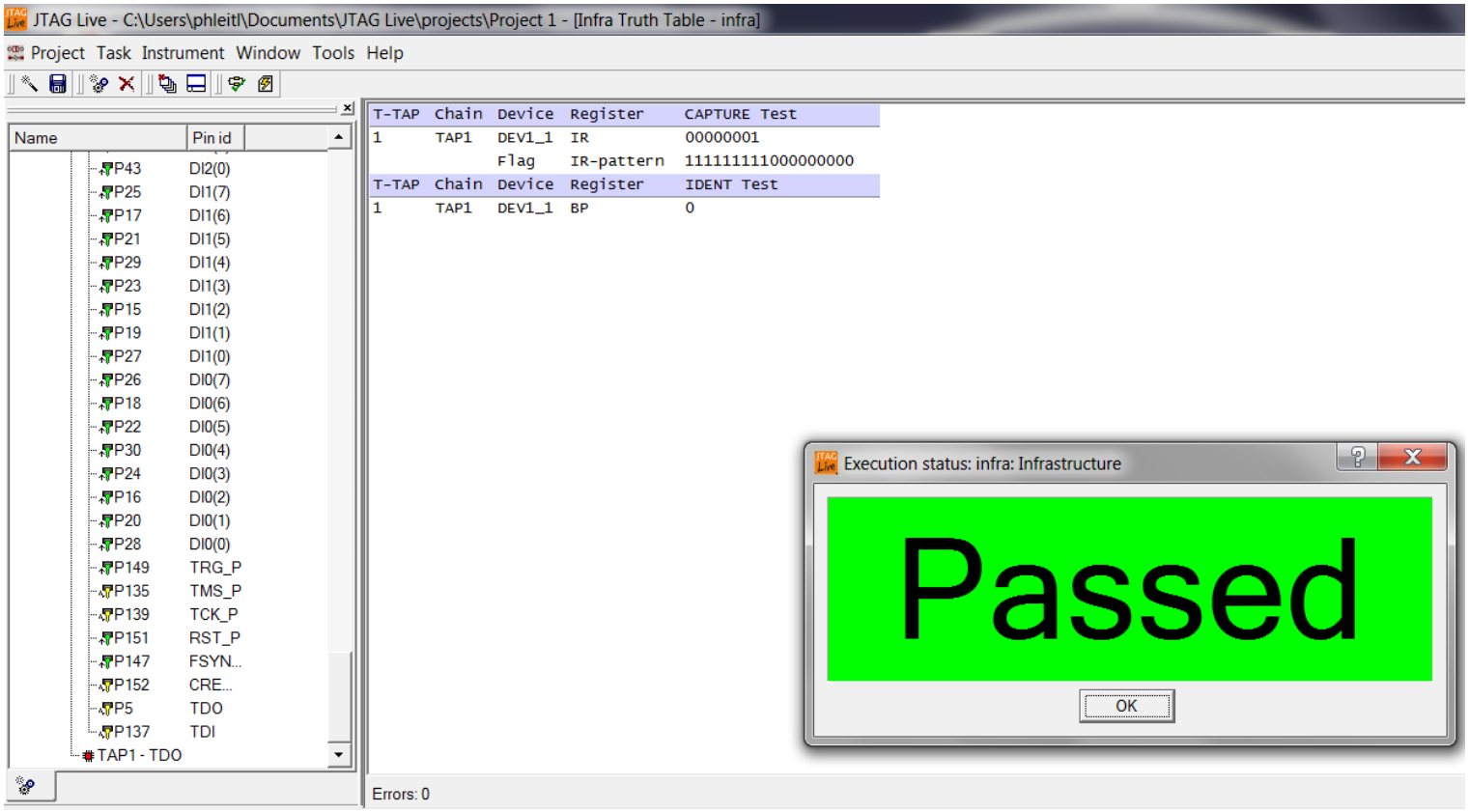
- Netlist
  - different versions for fully / not fully populated EMCMs
  - missing pin numbers → python script reads BSDL files and inserts pin numbers into the netlist
  - different versions for old / new ASICs

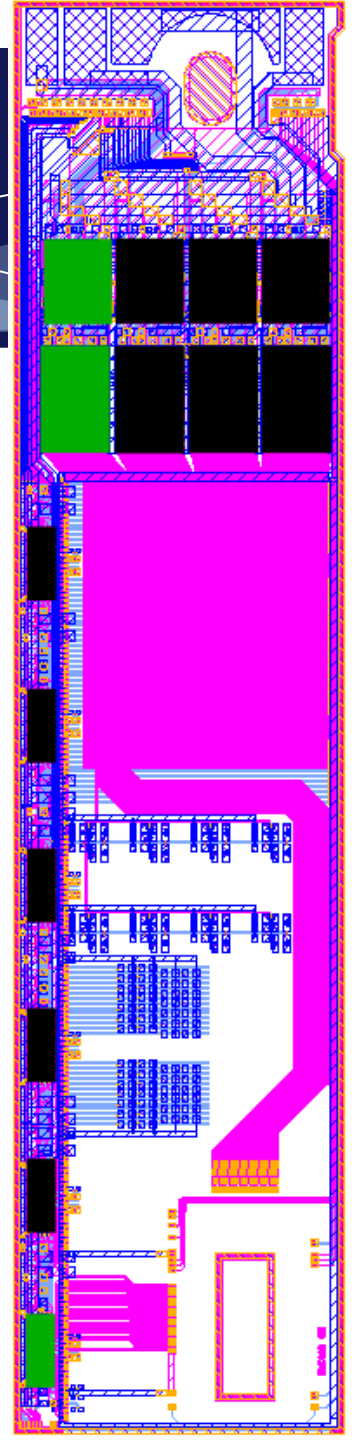
Boundary Scan Tests



EMCM P6-1

old ASICs: 1x DHP0.2, 1x DCD and 1x SwitcherB18v1





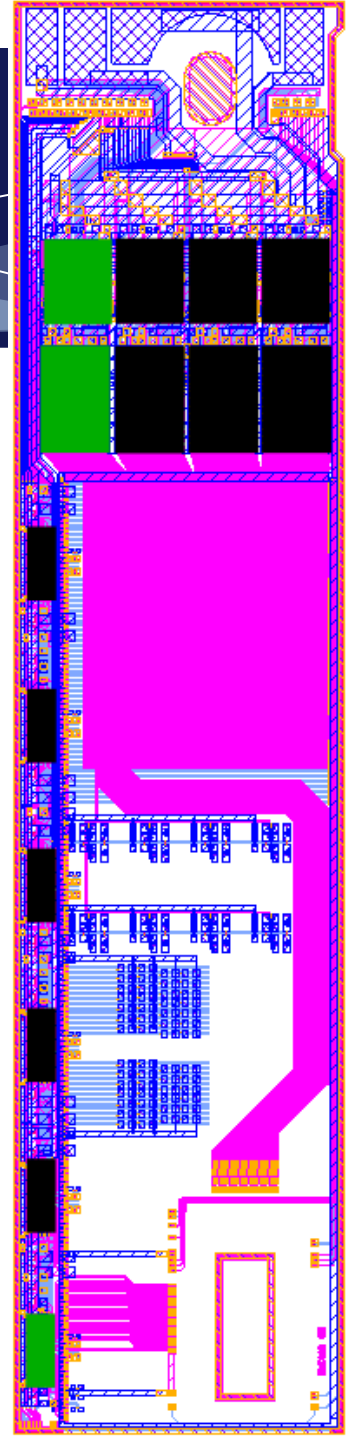
EMCM P6-1

#3670

Checking the integrity of the JTAG chain.
CheckChain passed

>>>> PASSED <<<<

NAME	RESULT		TIME
⊞ JTAG-Test	Passed		1,277
TOTAL TIME			1,277



EMCM P6-1

#3670

Error on net SW_Clk_P: Stuck at 1.
- Net Detail
- Error Detail

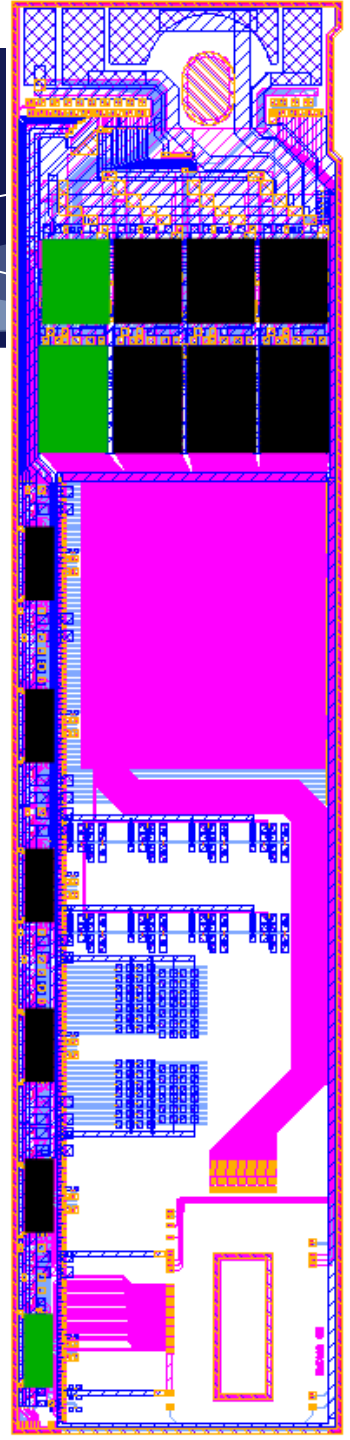
Error on net SW_StrG_P: Stuck at 1.
- Net Detail
- Error Detail

Error on net SW_StrC_P: Stuck at 0.
- Net Detail
- Error Detail

Test Summary: 3 errors
CONNTEST failed

>>>> FAILED <<<<

NAME	RESULT	SUMMARY	TIME
JTAG-Test	Failed		1,225
TOTAL TIME			1,225



EMCM P6-1

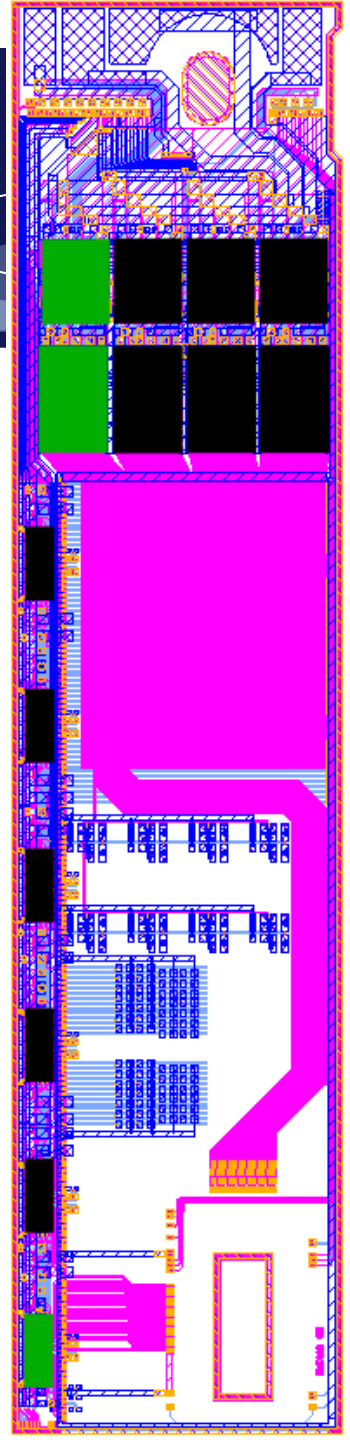
global register: enable sw_enout (and driver strength)

#3670

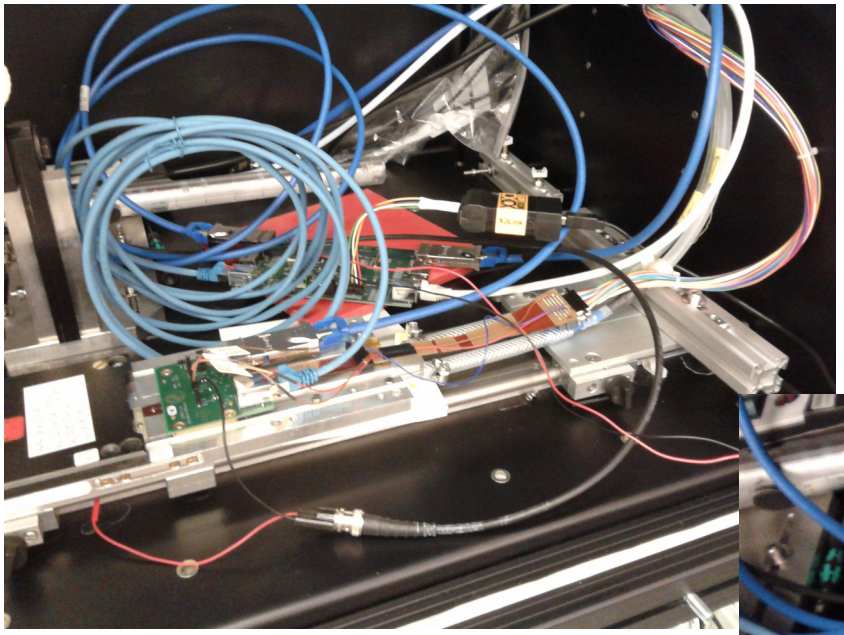
CONNTEST passed

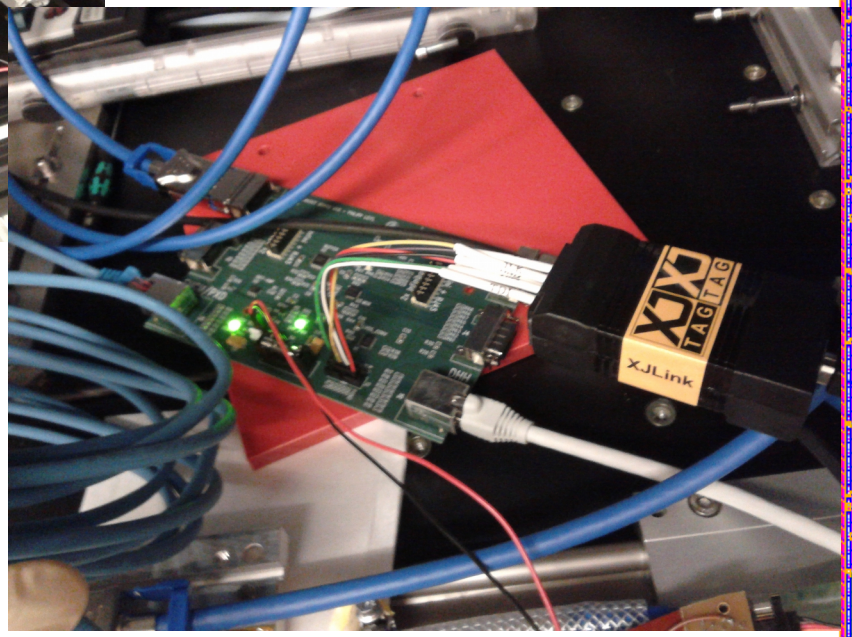
>>>> PASSED <<<<

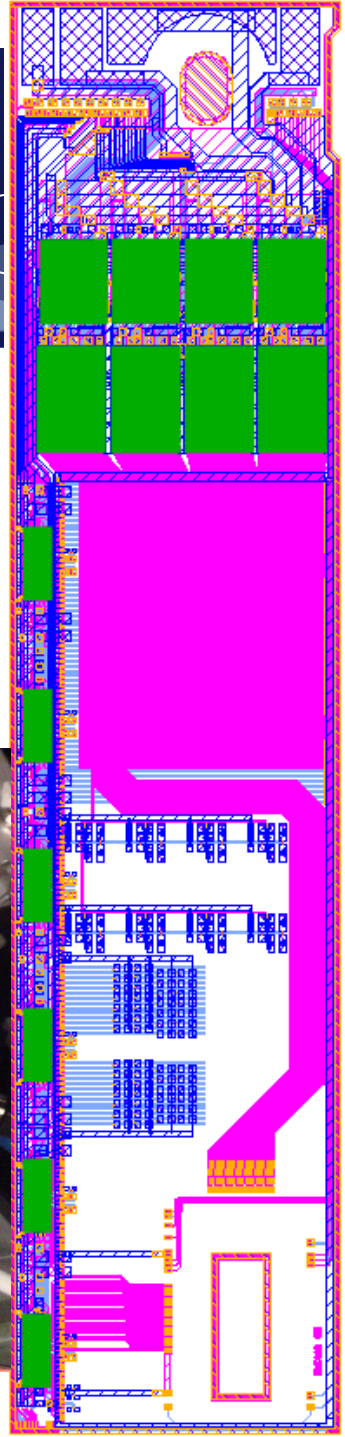
NAME	RESULT		TIME
⊞ JTAG-Test	Passed		1,235
TOTAL TIME			1,235



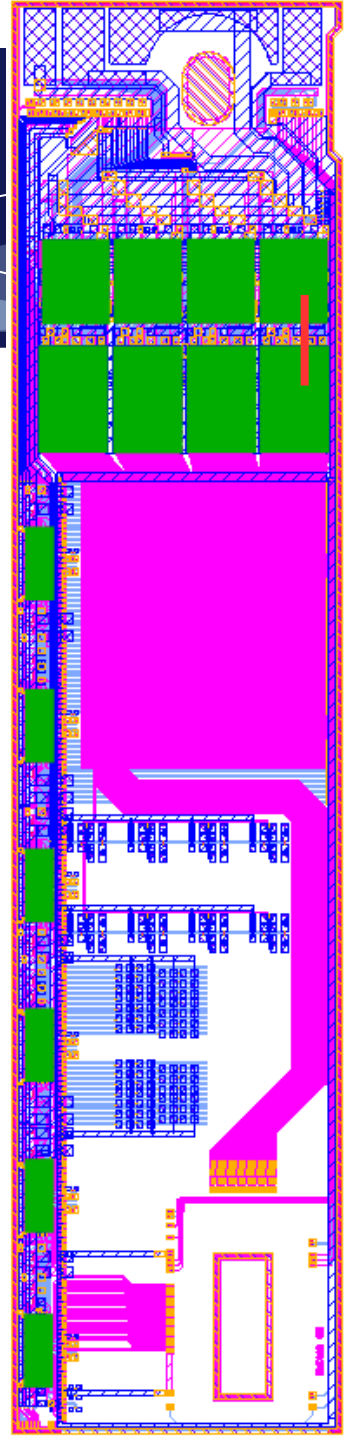
EMCM W18-3







EMCM W18-3



Infrastructure Test (goepel) – CheckChain (XJTAG): **OK**

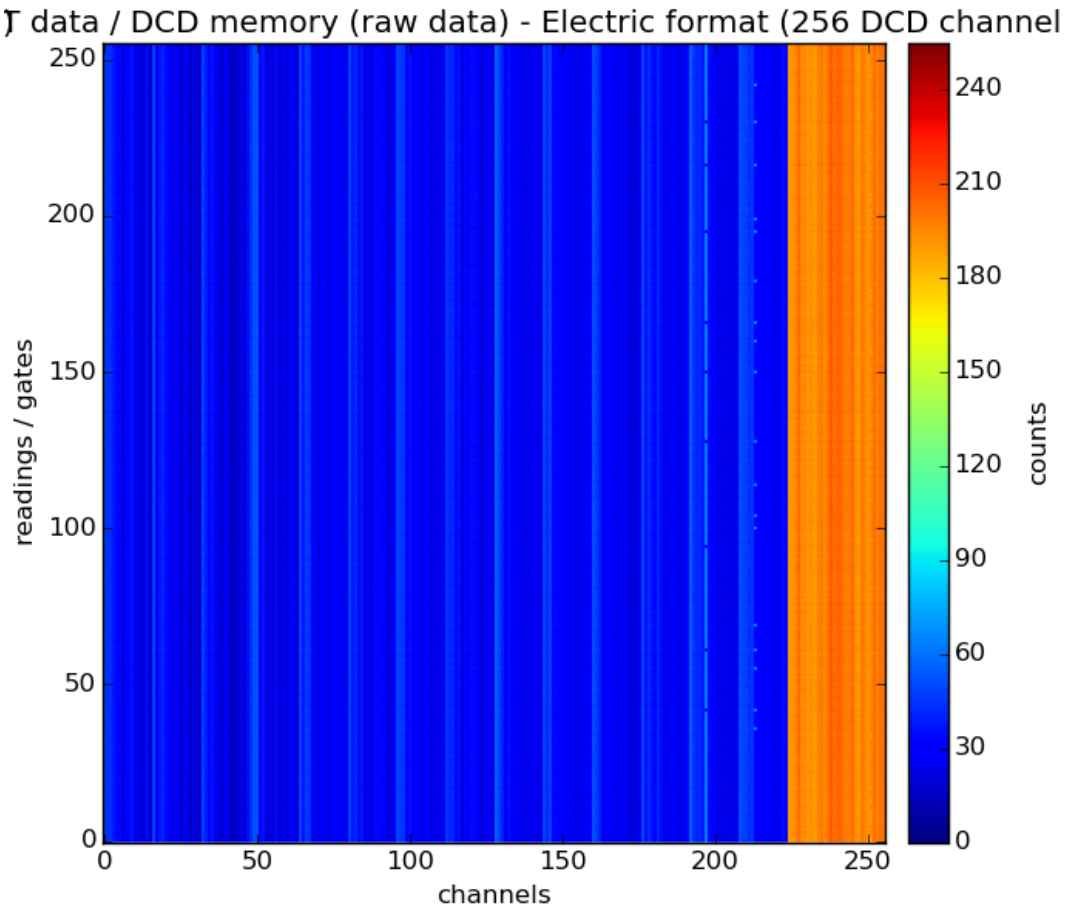
Interconnection Test - goepel:

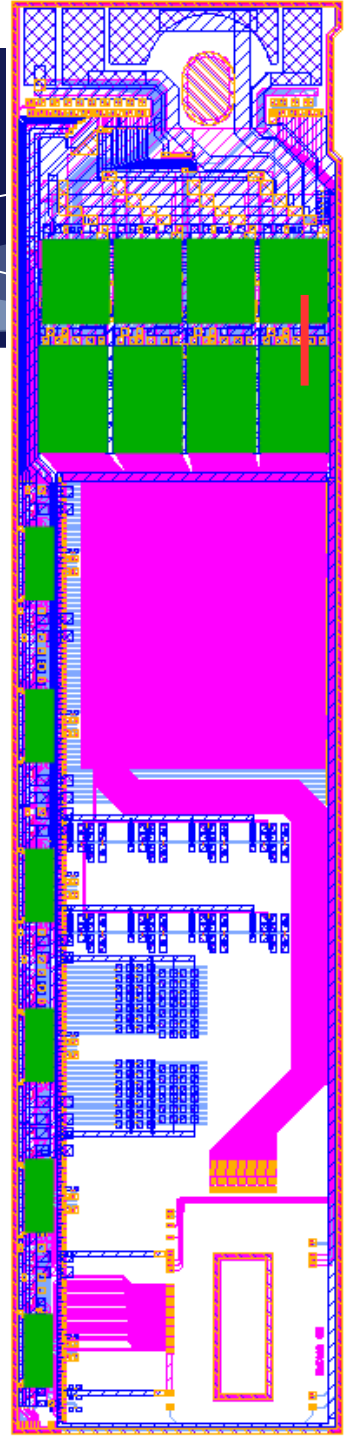
6/15/2015 2:19:33 PM UUT: EMCM-P6-1 Start Test: Interconnection
==========
DCD0:DI7_0(#P14)EL MH

- 1- Line NET0191_1 defective:
-73- 1. pin <: Out DHP0:DO7_0(#93) {BScan} DHP10_FOOTPRINT NET0191_1
-73- 2. pin >: In DCD0:DI7_0(#P14) {BScan} DCD_FOOTPRINT NET0191_1
- 9- Stuck at High of the line

-24- Test step table of the line NET0191_1:
-25- Expected H L H L H H H H H H L L H L L L L L L H
-29- Measured <Stuck at high>
-30- Output pin DHP0:DO7_0(#93) H L H L H H H H H H L L H L L L L L L H
-31- Input pin DCD0:DI7_0(#P14) H>H H>H H H H H H H H>H>H H>H>H>H>H>H>H>H H
==========
2:19:33 PM F A I L Elapsed Time 00:00:00.232
==========

EMCM W18-3


T data / DCD memory (raw data) - Electric format (256 DCD channel
readings / gates
channels
counts
0
50
100
150
200
250
30
60
90
120
210
240



EMCM W18-3

Interconnection Test - XJTAG:

#3670

Error on net net0191<1>: Stuck at 1.

- Net Detail

  Net net0191<1> contains:

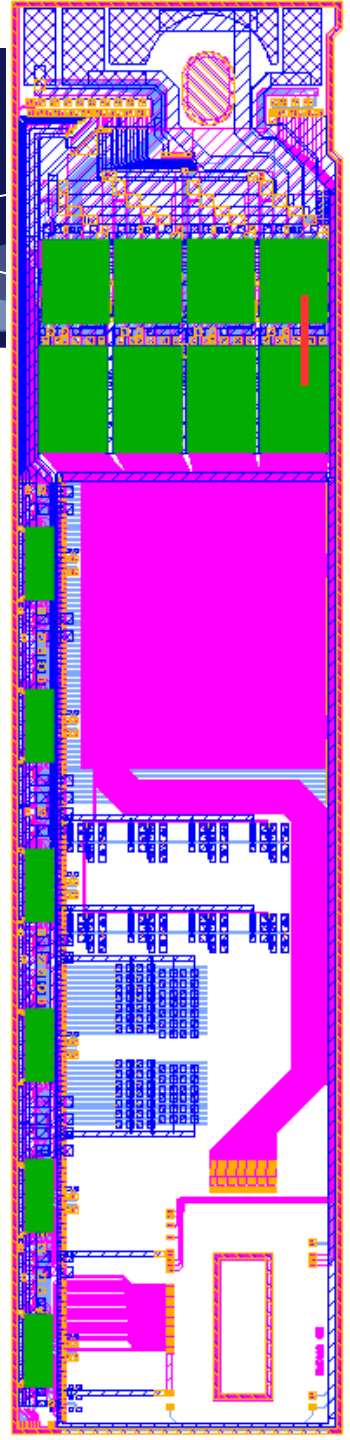
  - dcd0.B2(DI7_0)
  - dhp0.H30(DO7_0)

- Error Detail

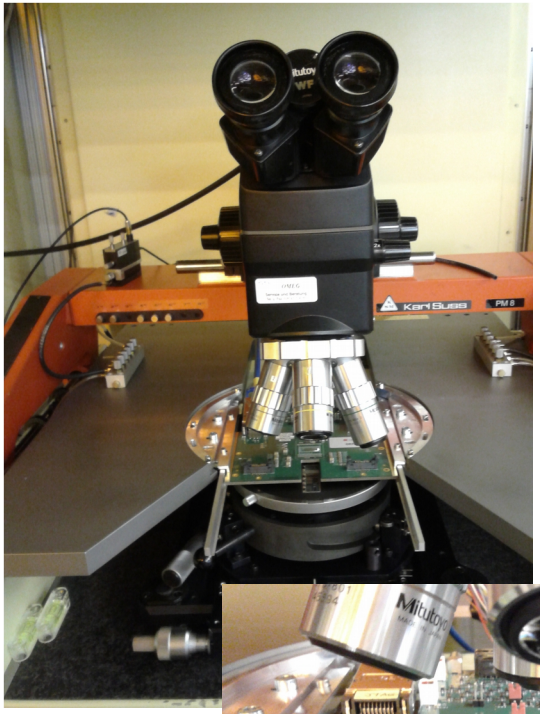
Test Summary: 1 error
CONNTEST failed

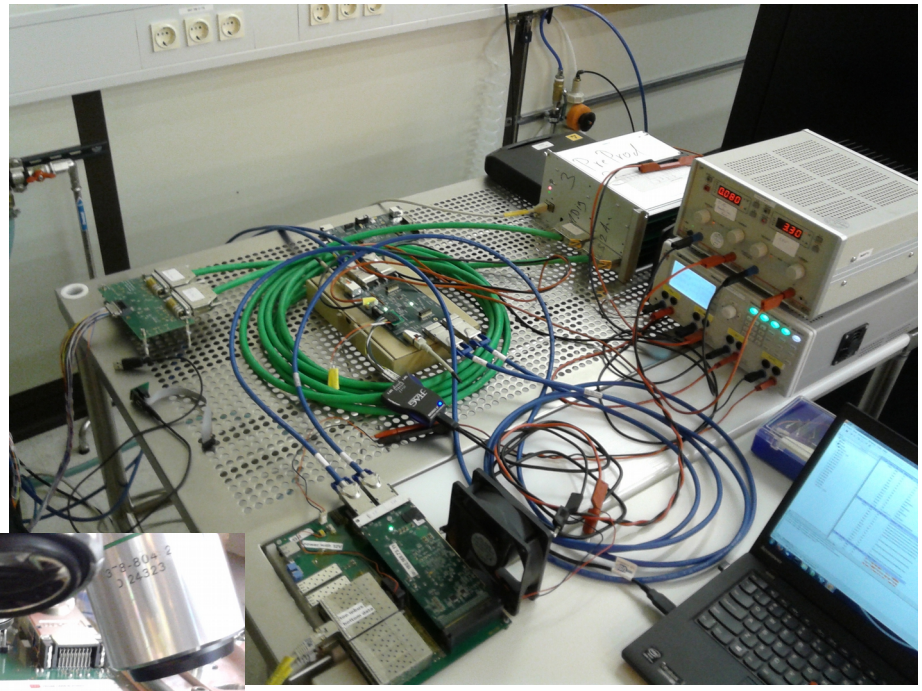
>>>> FAILED <<<<

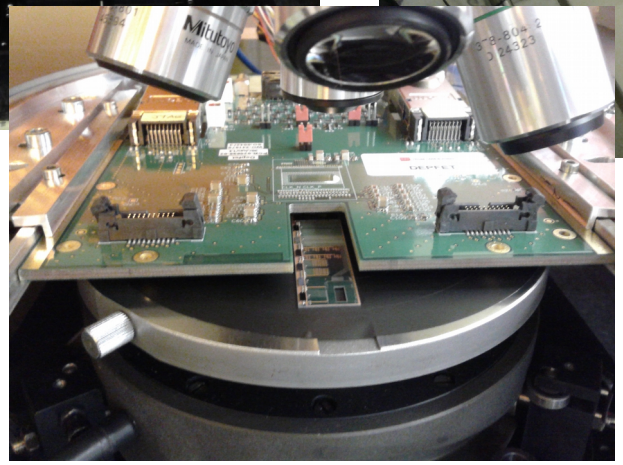
NAME	RESULT	SUMMARY	TIME
JTAG CON	Failed		1,544
TOTAL TIME			1,544

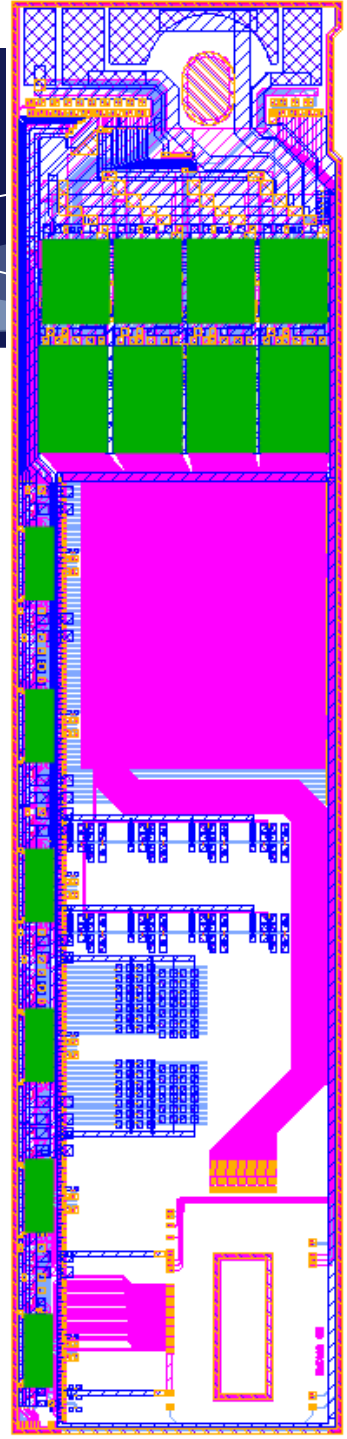


EMCM ProbeCard

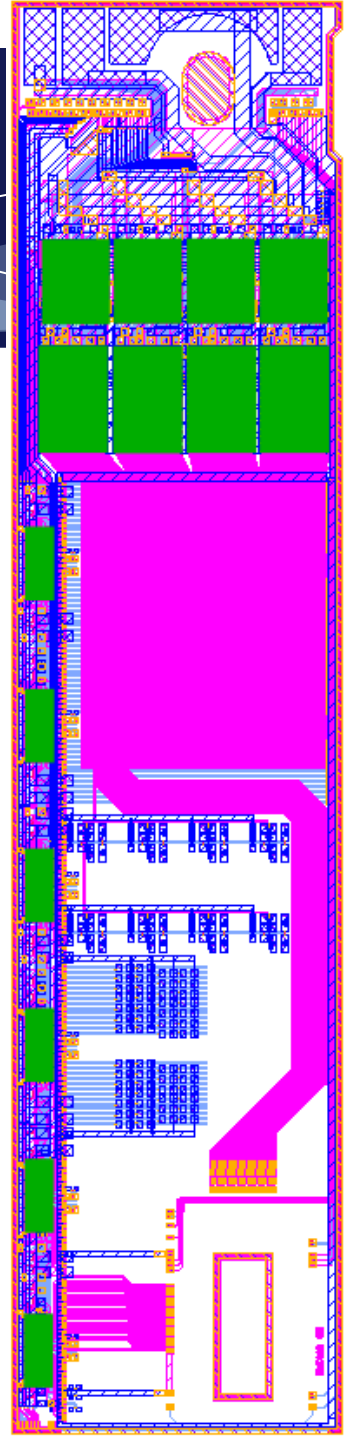








EMCM W17-4



Infrastructure Test: **PASS**

6/15/2015 3:53:14 PM UUT: EMCM-P6-1 Start Test: Infrastructure

==========

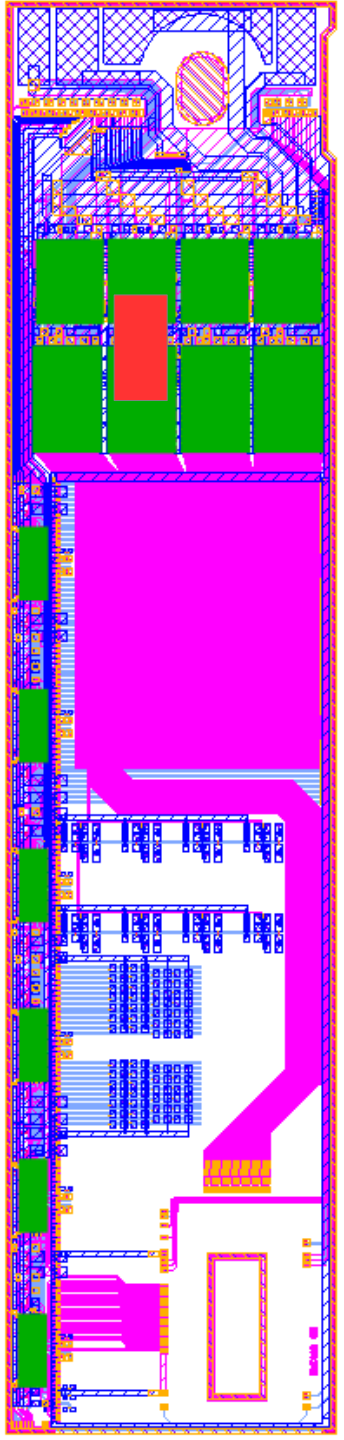
Testing boundary register SWITCHER_5 ...Ok
Testing boundary register SWITCHER_4 ...Ok
Testing boundary register SWITCHER_3 ...Ok
Testing boundary register SWITCHER_2 ...Ok
Testing boundary register SWITCHER_1 ...Ok
Testing boundary register SWITCHER_0 ...Ok
Testing boundary register DCD3 ...Ok
Testing boundary register DHP3 ...Ok
Testing boundary register DCD2 ...Ok
Testing boundary register DHP2 ...Ok
Testing boundary register DCD1 ...Ok
Testing boundary register DHP1 ...Ok
Testing boundary register DCD0 ...Ok
Testing boundary register DHP0 ...Ok

==========

3:53:14 PM P A S S Elapsed Time 00:00:00.111

==========

EMCM W17-4



Interconnection Test:

...

- 1- Line NET0141_0 defective:
-73- 1. pin <: OUT DCD2:DO7_7(#P79) {BScan} DCD_FOOTPRINT NET0141_0
-73- 2. pin >: In DHP2:DI7_7(#99) {BScan} DHP10_FOOTPRINT NET0141_0
- 8- Stuck at Low of the line

-24- Test step table of the line NET0141_0:
-25- Expected H L L L H L H L H L L H H L H L H L H H
-28- Measured <Stuck at low>
-30- Output pin DCD2:DO7_7(#P79) H L L L H L H L H L L H H L H L H L H H
-31- Input pin DHP2:DI7_7(#99) >L L L L>L L>L L>L L L>L>L L>L L>L L>L>L

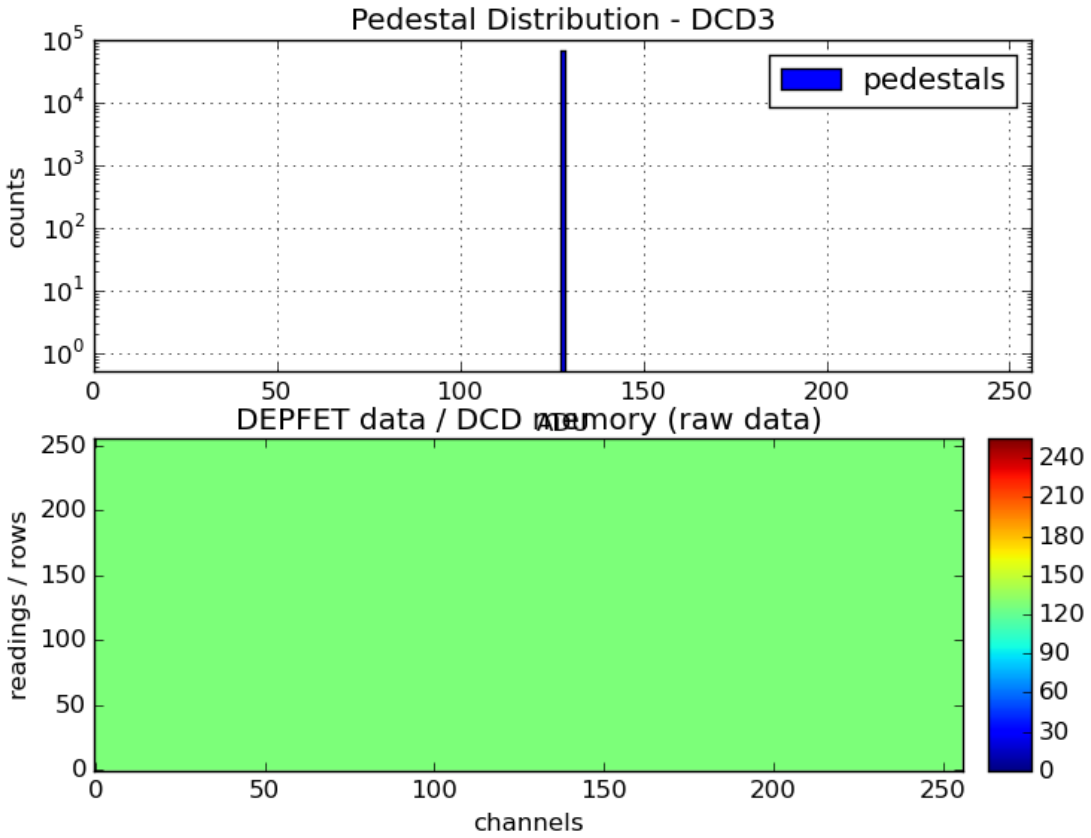
...

→ stuck at low for all DCD:DO → DHP:DI lines of the third pair
(DHP:DO → DCD:DI lines are working)

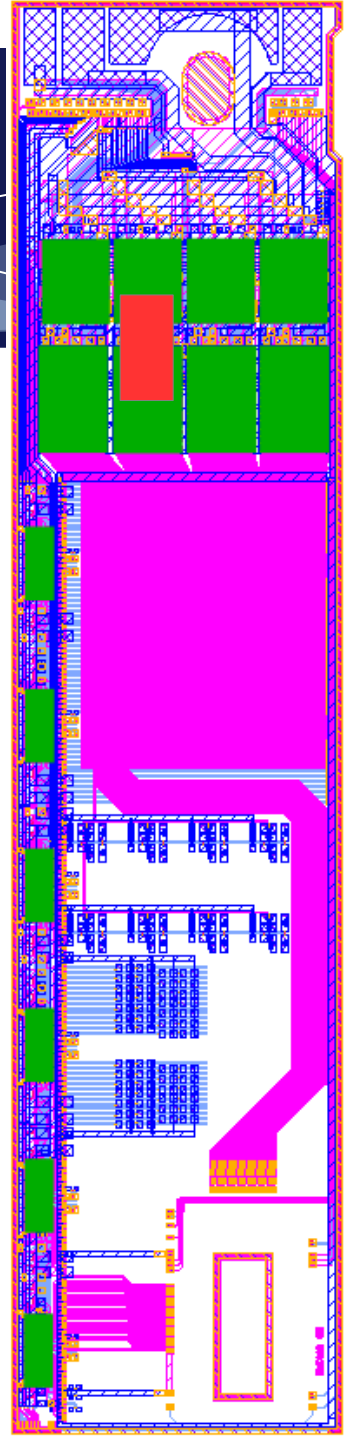
→ maybe a problem with the reference voltage between DHP and DCD

EMCM W17-4

Pedestals:



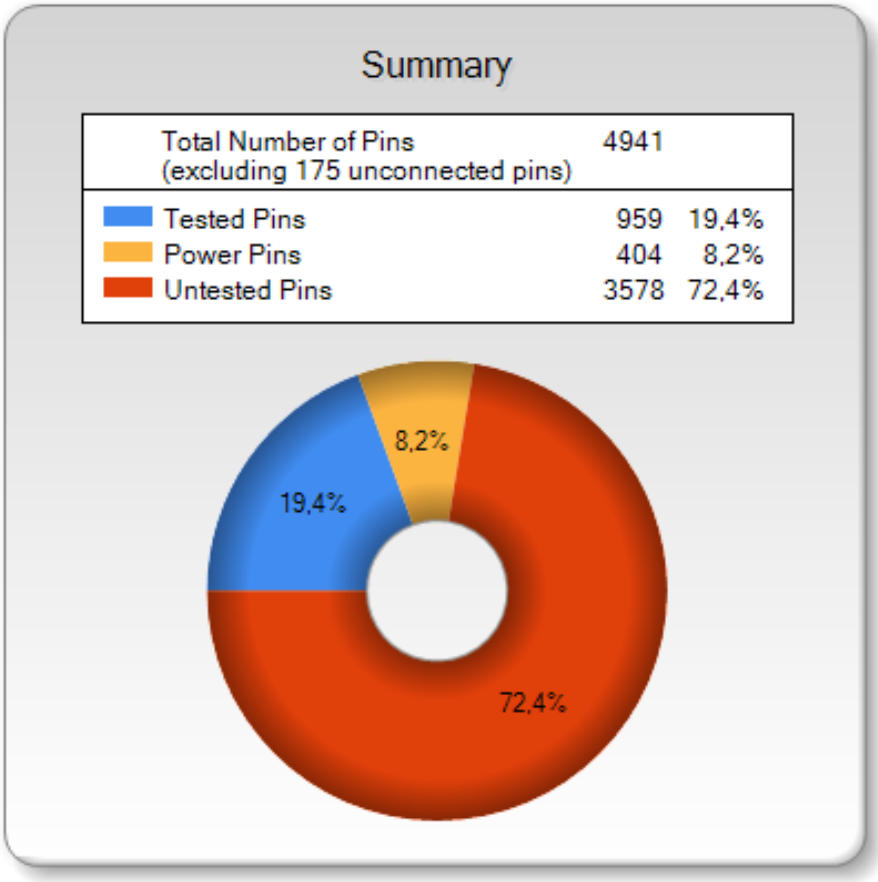
value of 128 corresponds to the logical low of the lines



Boundary Scan Tests

Board EMCM

EMCM P6-1	✓
EMCM P6-2	✓
EMCM W17-4	✗
EMCM W18-3	✗
EMCM W18-4	✓
EMCM W31-3	✓
EMCM W31-4	✓



~ 23% test coverage of ASIC pins

~ 19.4% of total number of EMCM pins (including e.g. passives and kapton pins)

Summary and Outlook

- Overview of Boundary Scan method
- Introduction of JTAG Breakout Board (JBB)
  11 boards assembled and successfully tested
- System of hardware (incl. probe station) and software (incl. BSDL files and netlist) working
- Development of a standardized procedure for testing the new PXD9 modules (XJTAG project)

- Documentation of Boundary Scan system and testing procedure
- Installation of Boundary Scan Test setup for PXD9 modules