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DEPFET

Active Pixel Detector

PXD Electronics

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DEPFET Collaboration

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Useful Links

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- **Belle II PXD ASICs review II**

https://indico.mpp.mpg.de/conferenceDisplay.py?confId=3736

- **PXD ASICs Planner 2015**

https://docs.google.com/spreadsheets/d/1OVASA4uVWEmoNZSZnSXNDR2uCe2bCWhkqrnfIKvhg_g/edit#gid=2101922850

- **DCD and Switchers Report**

https://indico.mpp.mpg.de/getFile.py/access?resId=0&materialId=2&confId=3736

Structure of the Review

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Wednesday, 15 July 2015

10:00 - 10:20	Introduction, Schedule, Overview *20'* Sprecher: Laci Andricek (MPG Halbleiterlabor) Material: **Sildes from Oct. 2014 review**	
10:20 - 10:40	DEPFET Drain Current Dispersion - What to expect *20'* Sprecher: Rainer Richter (MPG HLL)	Interface to the DEPFET
10:40 - 11:00	DEPFET Drain Current Dispersion - impact on Dynamic Range *20'* Sprecher: Florian Luetticke (Uni Bonn)	
11:00 - 11:20	Coffee Break	
11:20 - 11:40	Summary of the recent X-Ray irradiation campaign *20'* Sprecher: Benjamin Schwenker (University of Göttingen) Material: **Slides**	System tests before and after irradiation
11:40 - 12:00	Gated Mode seen from the DCD/DHP and SWB perspective *20'* Sprecher: Christian Koffmane (MPI Halbleiterlabor) Material: **Slides**	Gated mode status
12:00 - 13:00	Lunch	
13:00 - 14:00	DCD-DHPT Interface & DHPT Re-design Status *1h0'* Sprecher: Hans Krueger (Uni Bonn) Material: **Slides**	DHPT-DCD interface
14:00 - 14:20	Coffee Break	
14:20 - 15:05	DCD - Status and Plans *45'* Sprecher: Ivan Peric (KIT) Material: **DCD/SWB related answers to last review (Ivan)**	Detailed talks by the designers - Status - Response to the prev. review - Submissions plans
15:05 - 15:50	SwitcherB - Status and Plans *45'* Sprecher: Ivan Peric (KIT)	
15:50 - 16:35	Closed Session *45'*	

Thursday, 16 July 2015

09:00 - 12:00	Q/A, Discussions

Plans with Pilot Run Modules

Yield (%)			
	W30	W35	W36
IF	75.0	100.0	100.0
OF1	100.0	100.0	100.0
OF2	100.0	100.0	100.0
OB1	99.8	99.4	0
OB2	99.6	0	99.8
IB	100.0	0	100.0

- Wafer level testing
  - I_D/V_{th} Dispersion
  - Metal system integrity
- Module level testing
  - Assembly with prototype ASICs
    - ↘ Electrical verification of periphery
  - Assembly with new (final) ASICs
    - ↘ Test of final ASICs/system in the beam

- W30-OB1, W30-OB1, W36-OB2 → Assembly with prototype ASICs, kapton interconnection
- W30-OF1, W30-OF2 → Assembly with prototype ASICs, H7

- W30-IB and W35-IF → L1 ladder for test beam and BEAST
- W35-OF1 and W35-OB1 → L2 ladder for test beam and BEAST

Schedule (as by July 2015)

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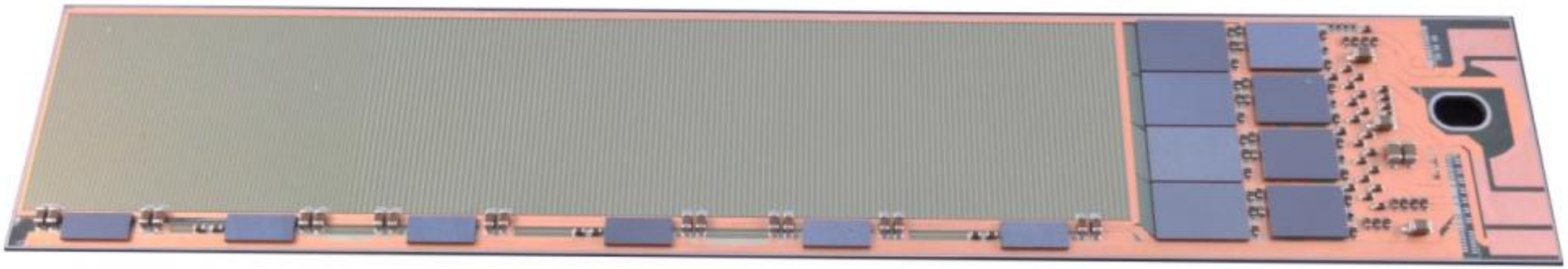
- PXD9 pilot run and beyond

Sensors by	July 2015
All ASICs (prototypes) are pre-tested and available	
Assembly (FC+SMD)	August 2015
Tests to understand periphery performance:	Sept - Nov.
Start phase II and III of sensor production (metal sys.)	Dec. 2015



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- ASIC submissions (including bumping)

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After test and verification of specs re-order new wafers (within 6 months)

- ASIC testing	Jan/Feb 2016
- Assembly of test beam/Beast modules	March 2016
- VXD combined test beam at DESY	April 2016
- Start PXD module production	Summer 2016

DHP Changes

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- Serializer: timing bug
  - Mistake during extraction and simulation with all process corners (slow NMOS)
  - Workaround for DHPT1.0: VDD = 1.6V for GCK=80 MHz
  - Fixed for the DHPT1.1, with all corners simulated

- CML driver enhancement: reduce parasitic resistance
  - Works fine but still output amplitude doubled by increasing pre-emphasis
  - Signal integrity OK (kapton+ 20 m cable)
  - No TID induced degradation up to 100 Mrad

- Delay elements issue: duty cycle distortion
  - Overlooked during DHPT1.0 sign off
  - Fixed by custom delay elements made by identical inverters in the chain

- Data receiver robustness: duty cycle distortion with non-symmetric input edges
  - Corrected. See next slides.

DHP Changes

- Radiation damage
  SEU: Proton irradiation done. Calculations cross checked.
  TID: Data, offset and JTAG working

- Memory dump issue
  Only affects few per mil pedestal data frames
  Well localized fixed pattern

- Data processing

So far, no issues seen (high occupancy tests, …)

→ Further tests needed (esp. Gated Mode)

All the bugs understood, identified, reproducible. Re-design on schematic and layout levels done. Simulations of extracted layout (with corners) performed.

Executive Summary (as by July 2015)

- DHP: Ready for submission with minor changes
  - The documentation of the problems and corrective actions was thorough and sufficient to assess readiness for submission. Further verification to be completed prior to tape-out

- DCD: Submission on hold until further tests

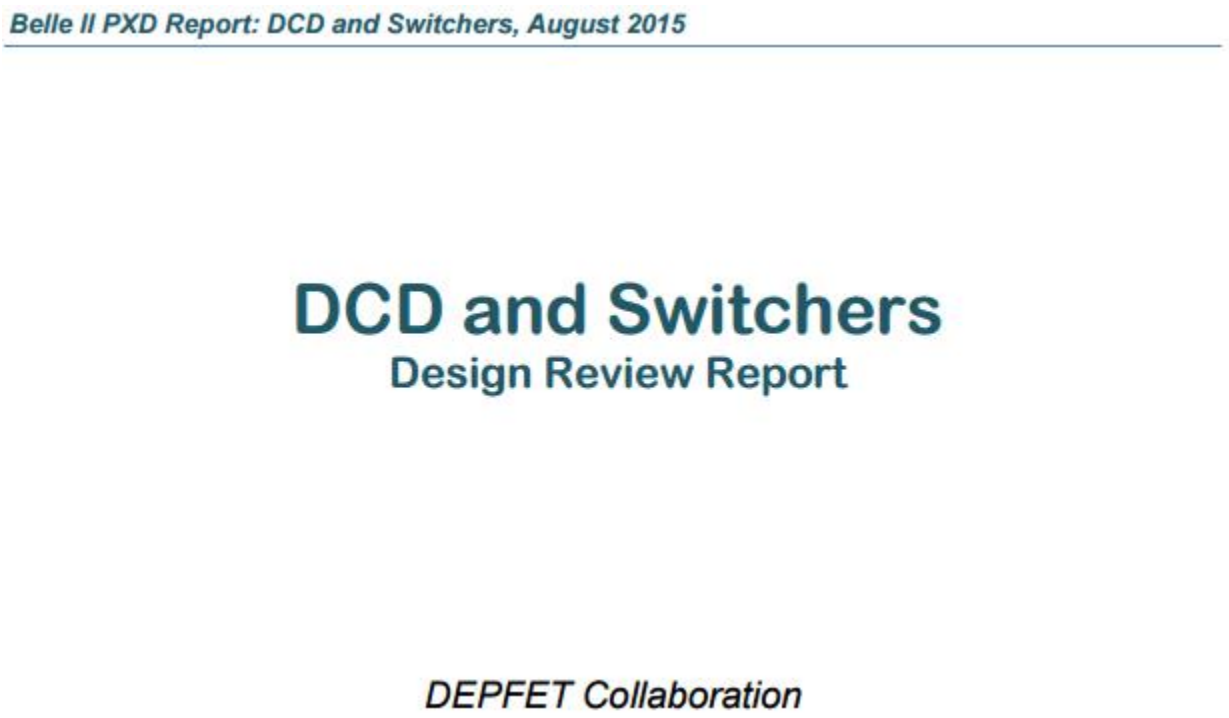
- Switcher: Submission on hold until further tests

Executive Summary: Recommendations

General recommendations:

1. DHPT should be ready for late August submission
2. For the DCD, comparison with simulation of the test results and risk assessment
3. A deadline of 2-3 weeks to complete and distribute this DCD test summary was set
4. Submission of the Switcher possible after small layout changes

Actions Taken



- Top level specifications
- Chip history
- Summary of latest results
- Next version: DCDB4.1 and SwitcherB1.8-v2.1
- Submission plans

Test Systems

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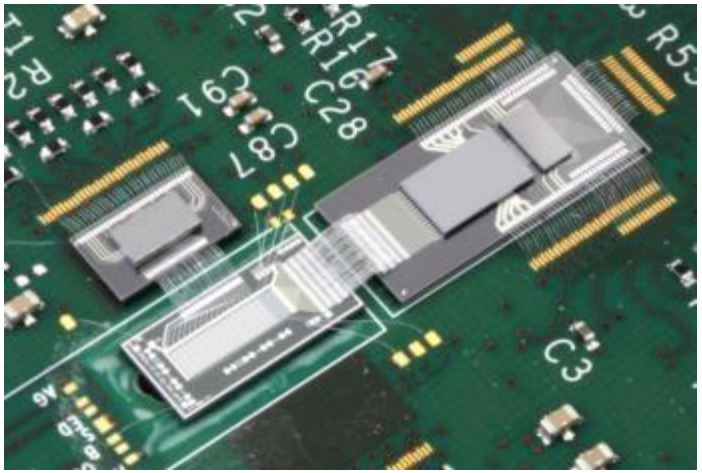
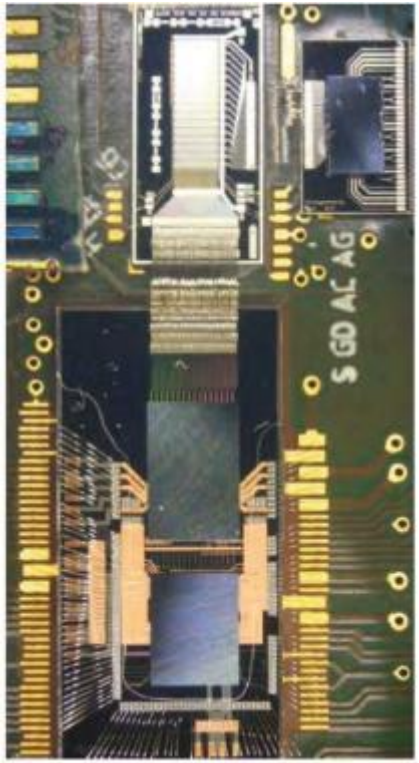
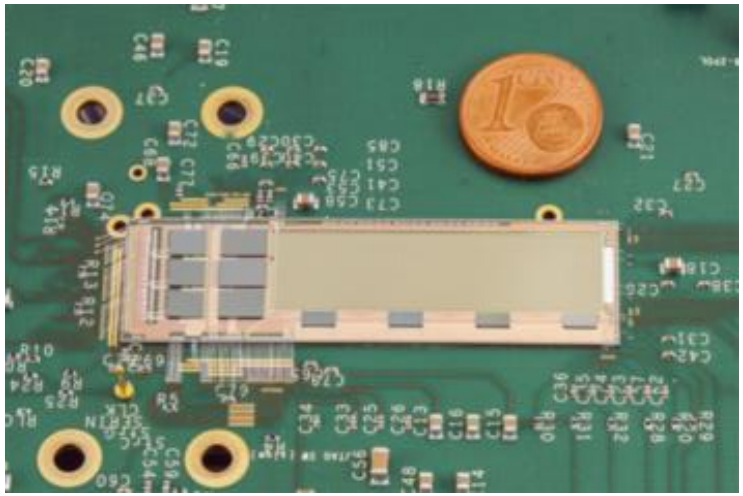
Hybrid4



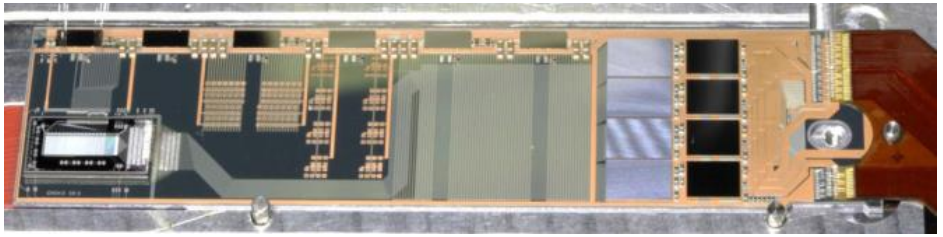
Hybrid5



Hybrid6

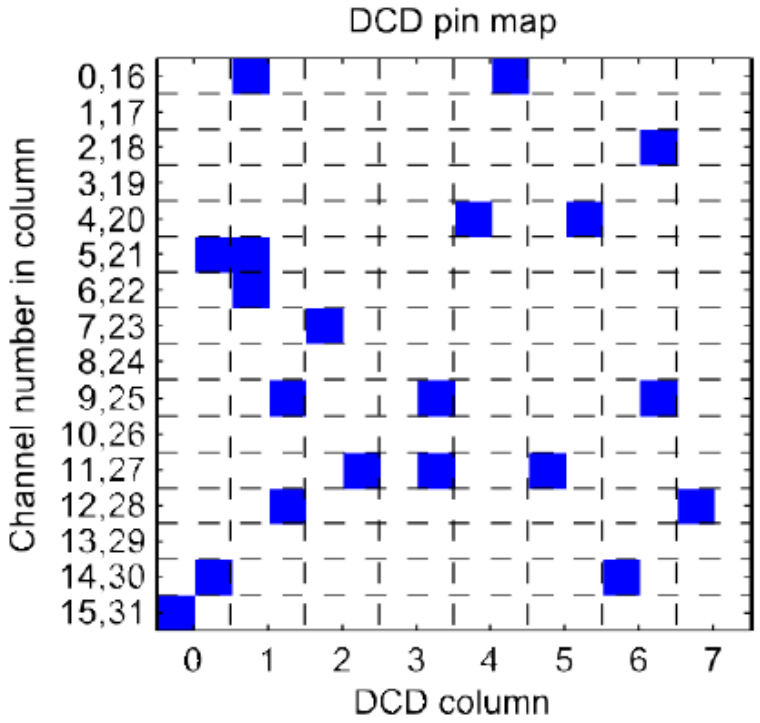


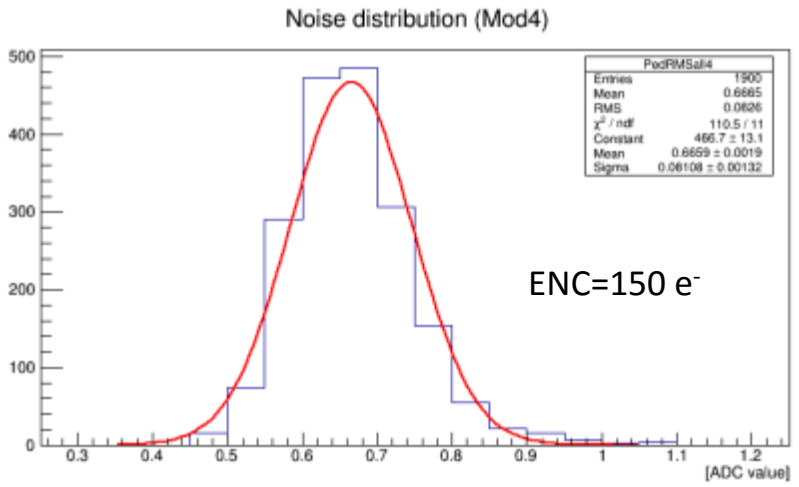
EMCM



Hybrid 4.1

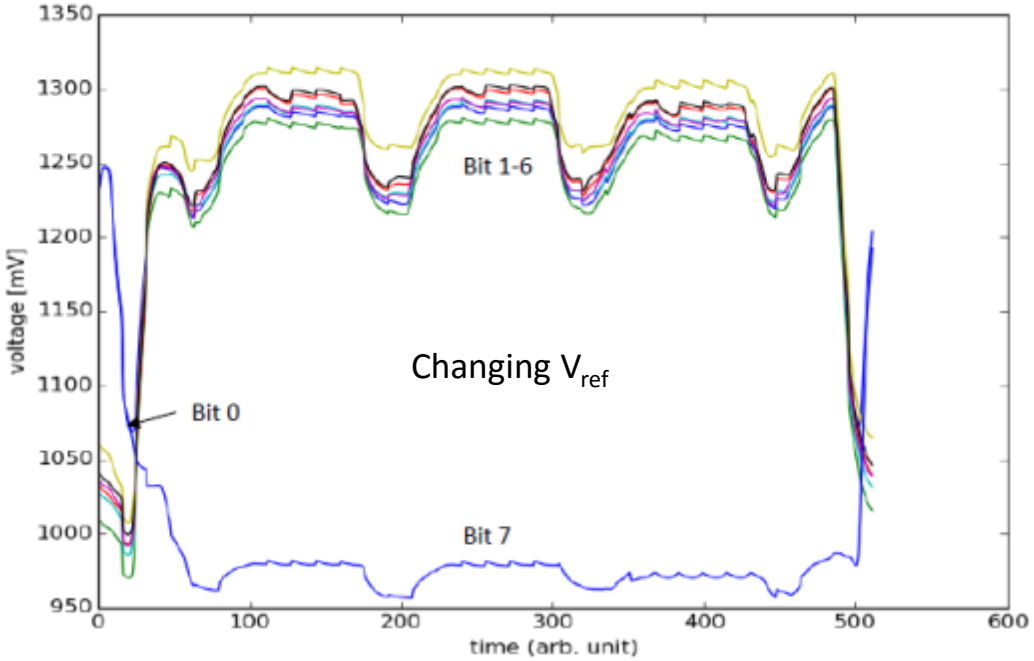
- 3 boards with DCDBPipeline assembled
- 1 board with PXD6 matrix
- VDDD=1.9 V to avoid bit errors
- The 256 channels were scanned at nominal speed 305 MHz
- Missing codes popping up depending on bias and DACs conditions but not position dependent

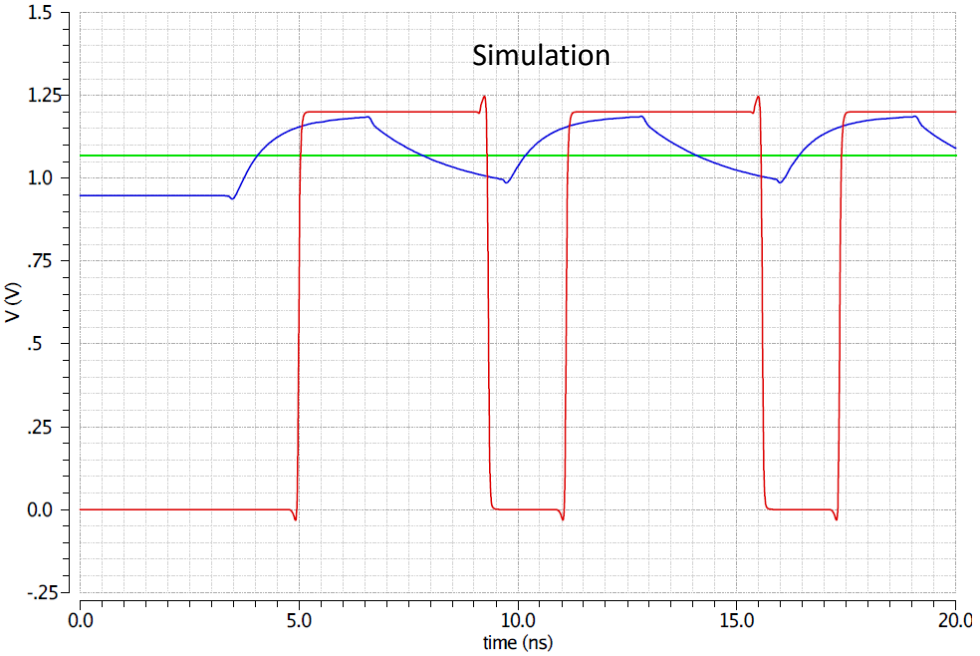




Hybrid 5.0

- 5 boards with DCDBPipeline assembled
- Main investigations on DCD-DHP data transmission
- 64 data links tested using DCD test pattern
- Main issue revealed: Critically small sampling window!



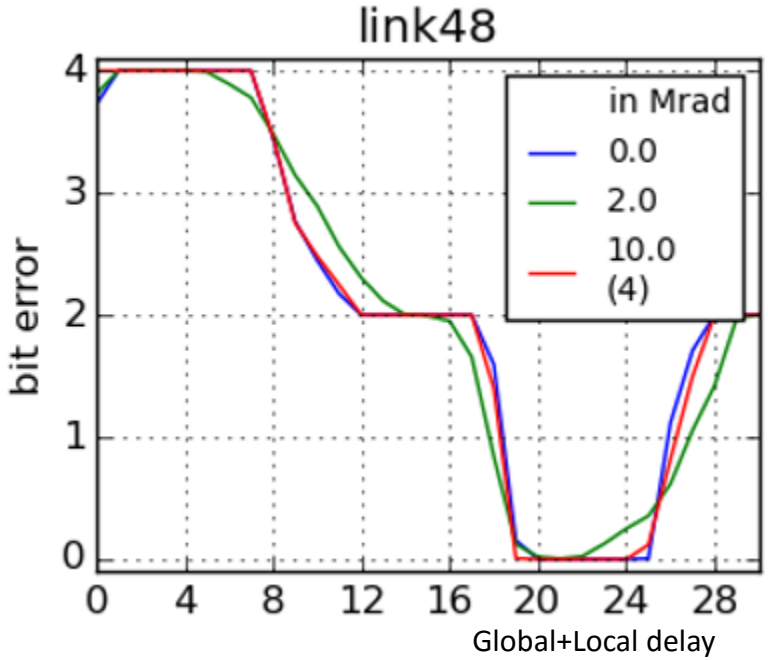


Ideal logic zero sampling window : **3.125 ns**

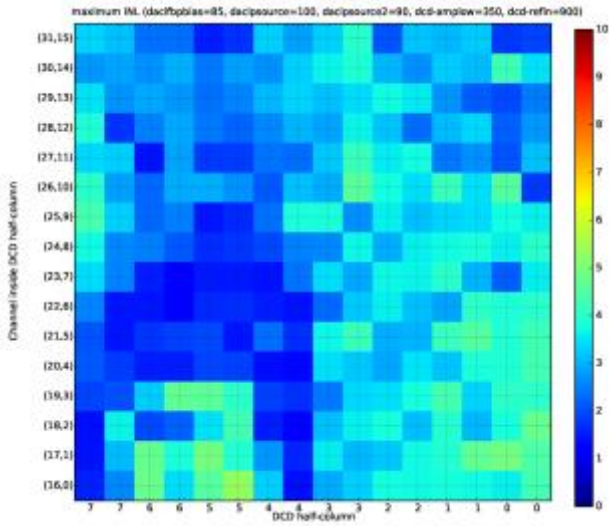
Measured logic zero sampling window = **1 ns**

EMCM

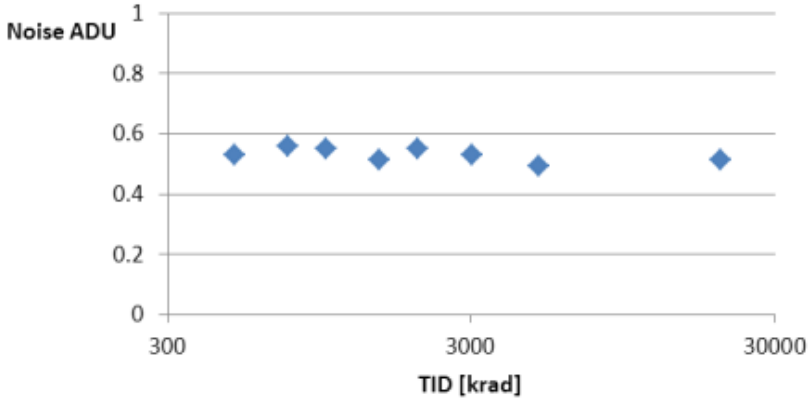
- 6 EMCMs with DCDBPipeline and DHPT assembled
- Investigation on DCD ADC performance
- DCD-DHP data transmission
- X-ray irradiation



At 2 Mrad the delay tolerance shrinks, although we always found a region with no transmission errors

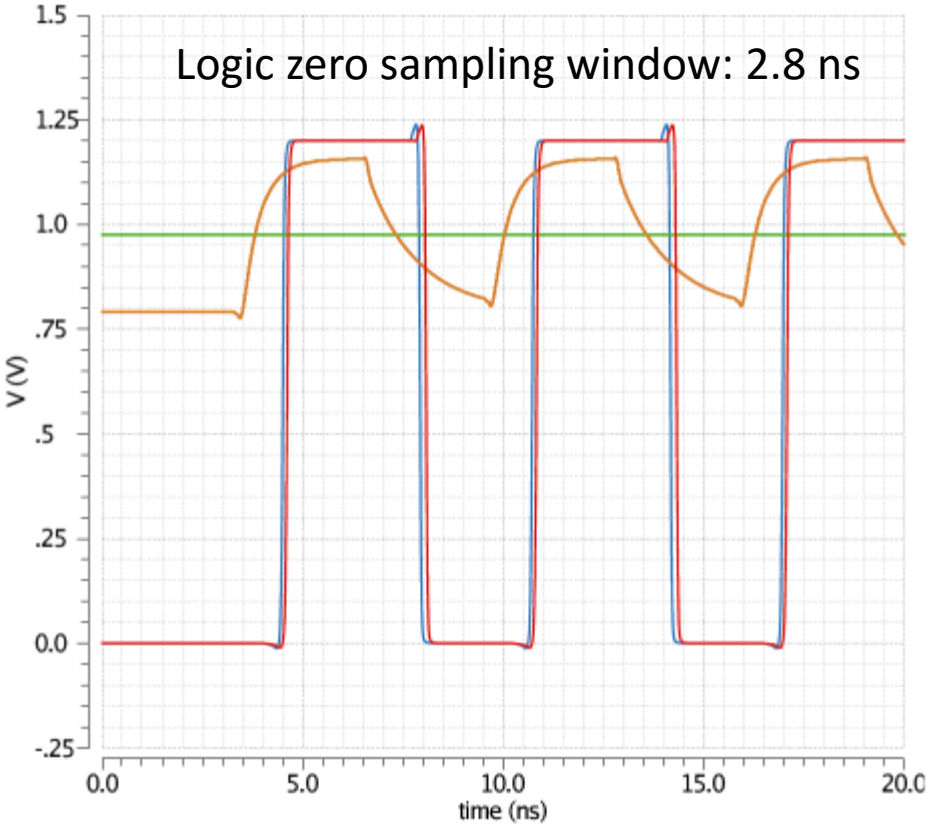


INL vs DCD position



Main DCD Changes

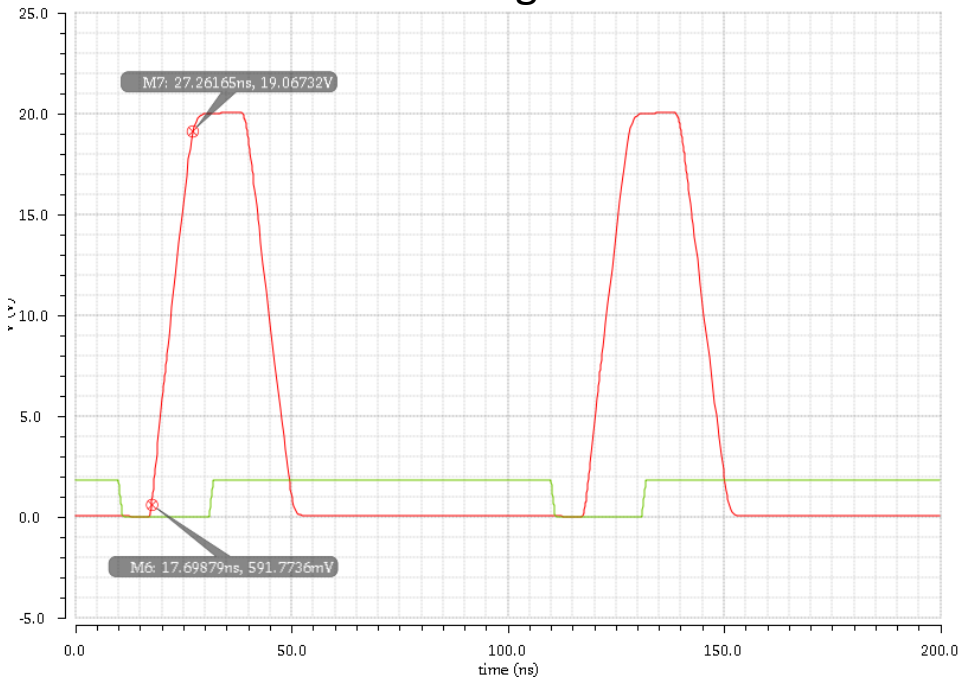
- Digital transmission DCD-DHP:
  - Reduce parasitic capacitance of DHP input pads
  - Remove hysteresis on the receiver side
  - Increase the DCD output strength
- Missing codes:
  - Minimized by optimized DAC and bias settings
  - Not relevant for the experiment
- Internal gain and pedestal correction:
  - Adapt based on recent PXD9 static measurements
- Change sampling polarity according to standards:
  - Sampling data at JTAG TCK raising edge
  - Release data at falling edge



Main Switcher Changes

- Faster rise time:
  - Larger switching transistors
  - Increase decoupling capacitors
- Termination resistors always on
- Bump pads:
  - Resize of pads on last metal layer

Rise time: 10 ns
Capacitor = 150 pF
ClearHigh = 20 V



Submissions

Based on the previous tests and simulations, the deficiencies are understood and minimal risk changes are proposed

↘ **Green light for submissions**

- **DHP**: Submitted cw35. MPW. Turnaround time 56 days
- **Switcher**: Submitted cw35. MPW.
- **DCD**: To be submitted cw39. Engineering run with bumping. Cost shared KIT+DESY+HEI

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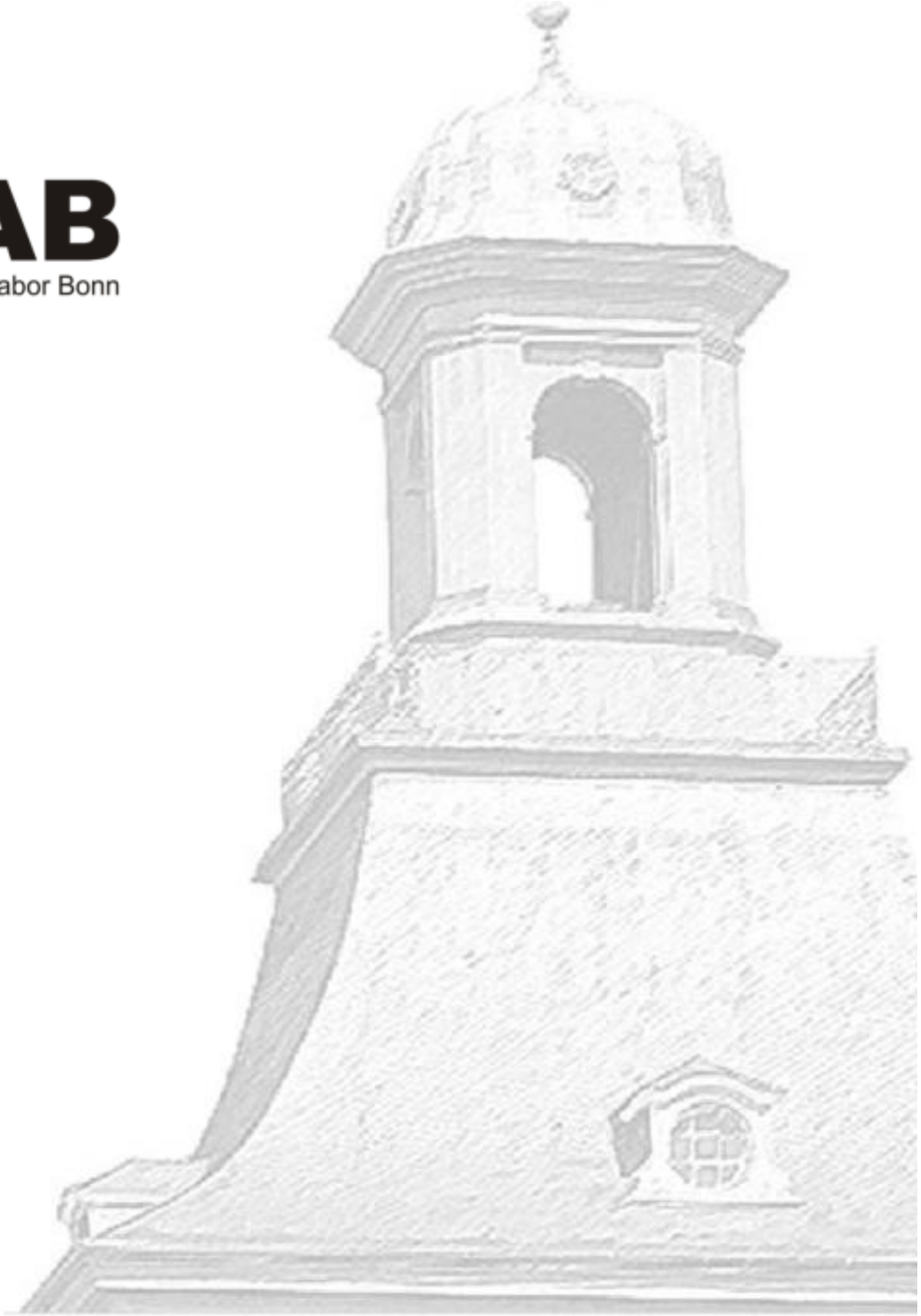

Thank you

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