DCD and Switchers
Design Review Report

DEPFET Collaboration

Contents

1. Introduction

This document summarizes the status of the Switchers and DCDs for the Belle II PXD. The goal is to have final chips available on a time scale compatible with the Belle II installation and commissioning schedule. We will present a plan and schedule to achieve this goal, based on the data in this document.

Many details are skipped to keep this document short. The complete documentation of both chips is found in the Reference Manuals attached at the end of this document.

1.1. Top level Specifications

These top level specifications were defined at the start of the development. Some specifications are not fixed yet (gain ranges, noise, INL) and will change after the first tests of large DEPFET matrices. They will partly be discussed later in this document.

1.1.1. DCDB

- ADC resolution 8 Bit
- ADC calibration DAC – resolution 9 Bit
- Pre ADC offset correction 2 Bit
- Conversion rate 10Mhz
- ADC LSB (fine mode) ~ 200 e (~80 nA)
- ADC LSB (coarse mode) ~ 400 e (~160 nA)
- ADC nonlinearity (peak to peak) in the range -/+ 100 ADC counts: < 6σ noise (tbc)
    - that corresponds to 480 nA in the fine mode or 960 nA in the coarse mode
- Number of localized code jumps < 6σ noise (LSB)
- DCD noise < 300 e (SNR 20)
- Analog common mode correction
- Power consumption < 2 W
- Current consumption < 800 mA
- PSRR DC < 50 mV Vpp
- PSRR AC ~ 2.5 µV
    - (in the frequency range 1 MHz to 250 MHz, else ~10 mV)
- Radiation tolerance 20 Mrad

1.1.2. Switcher-B

- Number of channels 32
- Speed 10 ns rise time to 20 V with 150 pF capacitive load
- Voltage range 27 V
- DC current consumption < 50 mA
- Radiation tolerance 20 Mrad

2. Chip History of DCDs and Switchers

2.1. DCD – Drain Current Digitizer

DCD ASICs are based on current mode ADCs. The development of the current mode read-out chips is inspired by the architecture of the CURO readout chip. These chips utilized current memory cells to store and manipulate the DEPFET signal currents. In this way the whole signal processing was done in the current domain. The CURO had analogue readout with a regulated cascode as the first stage. After correlated double sampling of the DEPFET currents and zero suppression the analogue signal was transmitted off-chip for digitization.

The following ASICs TCUM1 to TCUM3 were test chips with on-chip current-mode ADCs based on improved CURO current memory cells. The analogue to digital conversion was tested in both architectures, the cyclic and pipeline ADC configuration.

DCD1 and DCD2 were 72-channel ASICs with regulated cascodes as first stages and different realizations of the cyclic ADC, mainly improvements and variations of the comparator and transconductor of the ADC current memory cell.

2.1.1. The DCDB chip family

2.1.1.1. DCDB1

DCDB1 was the first Belle II PXD chip designed for flip-chip interconnects to the all-silicon module of the PXD. A transimpedence amplifier (TIA) was implemented instead of the DEPFET current receiver, which used regulated cascodes.

The use of TIA has several advantages over the regulated cascode. The time constant of the amplifier is signal independent and it is possible to implement gain in the first stage by varying the resistor values. The output of the amplifier is converted to current using a resistor.

The analog part of the ADC was the same as in DCD2. Apart from the already mentioned change in the front-end, the main new features introduced in DCDB1 were:

- 2-bit DAC for each channel for pedestal correction before the TIA
- Designed to work in single sampling mode
- Cyclic ADC
- Separated digital block on-chip for calculation of the digital output
- Low-voltage single ended IOs as interface to the DHP

Most of the functionalities and features of the final chip were already implemented in this first full-size prototype version. DCDB1 was extensively tested within a PhD Thesis, to be found here:

http://archiv.ub.uni-heidelberg.de/volltextserver/12706/1/Thesis_Jochen_Knopf.pdf

Issues seen with this prototype:

- Noise at nominal read-out speed of 100 ns somewhat higher than expected (70 nA – 120 nA, with the mean value at ~95 nA)
- A small fraction of the ADCs show reduced linearity and missing codes
- Bias voltage as delay control for current memory cells was at the lower margin
- Broken interconnect lines (antenna problem or broken vias) between ADCs and digital block caused a few (typically 3%) non-functional channels/chip
- Small operation margin for the voltage RefIn

2.1.1.2. DCDB2 and DCDB3

These issues have been successfully addressed in the following version DCDB2:

- Changes in the comparator (coupling caps and negative input clamping to VNMOS potential)
- Additional antenna diodes were placed to avoid broken interconnects to digital block
- The NSubIn current sources for static pedestal current subtraction are doubled to allow for higher pedestal currents.
- Analogue common mode correction before the TIA was introduced in the chip.

Noise measured without attached DEPFET is now typically 65 nA at 100 ns sampling (average value) the majority of ADCs have the noise between (60 and 80 nA) with e.g. 2 ADCs noise >80 nA. A mean INL of 2.8 LSB was achieved (max value 4.1 LSB).

No completely “broken” ADCs were found in these chips.

DCDB3 was a smaller test chip with the same architecture as DCDB2 but with 16 instead of 256 channels. The functionality of the TIA and the common mode correction was successfully tested on this smaller test chip.

DCDB2 was extensively characterized and was the main “work horse” for many beam tests with various test hybrids and DEPFET matrices. The following table shows the systems under test, the hybrid version, and the digital I/O ASIC. Results of the beam test go beyond of the scope of this document and are reported elsewhere (e.g. PhD Thesis Benjamin Schwenker http://hdl.handle.net/11858/00-1735-0000-0023-992D-9).

test system	Hybrid 4.1.04	Hybrid 4.1.11	Hybrid 4.1.15	Hybrid 4.1.16	Hybrid 5.0.03	Hybrid 6.0	Hybrid 6.0
#DCDB2	1	1	1	1	1	1	3
I/O ASIC	DCDr/o	DCDr/o	DCDr/o	DCDr/o	DHP0.2	DHP0.2	3xDHP0.2

Table 2-1 List of test beam systems, DCDr/o is the driver chip as interface to the FPGA system, if no DHP is used

A detailed characterization of the chip was done at Uni Heidelberg and Uni Bonn. The report of the Bonn group is attached at the end of this document as Addendum A3.

The main issues with these chips were the so called “missing” or “long codes” in a fraction of the ADCs operated at full speed. The number of channels showing these long codes was smaller at lower clock rates and it was found that changing the control voltage RefIn helps to reduce this number. At that time it was understood that the main cause of this feature is in the dynamic part of the comparator which transmits fast signals (missing contacts, damage by the antenna effect during processing). The timing effects are much more pronounced in a cyclic ADC, because it operates at a clock speed twice as high as the pipelined ADC.

2.1.1.3. DCDB4_cyclic and DCDB4_pipeline

The latest version DCDB4 was designed to mitigate the problems of the missing codes. The main changes are:

- Added antenna diodes and doubled contacts in the comparator
- Positive clamp diode of comparator connected to VPMOS instead of RefIn
- Improved test current source with on-chip DAC
- Temperature stable band gap current reference
- Analogue common mode correction switchable individually per channel
- Two versions of the DCDB4 were designed, one with cyclic ADC as used in the DCDB2 and another one with a completely different digital block and a pipeline ADC (DCDB4_cyclic and DCDB4_pipeline, resp.)

The main emphasis of the testing was on the DCDB4_pipline, which will be described in detail in the subsequent sections. The advantage of the pipeline ADC over the cyclic one is that for the same conversion time only half of the clock speed is needed. It was assumed that in addition to the layout changes in the comparator, the slower ADC rate would also reduce the number of channels with missing codes.

2.2. Switcher-B

Switcher-B is an analogue multiplexer chip to control the gate and clear voltages of 32 DEPFET matrix rows. The first prototypes were designed 2008.

It uses the AMS HV technology in a MPW run. The chip relies on bump bonding. The bump pads are arranged in a 4x24 grid with a pitch of 150 µm.

Switcher-B uses an improved output stage design, which is adapted from previous versions to the needs of Belle II. The chip addresses channels sequentially using a shift register. Neighboring chips can be daisy-chained by connecting the shift register output of one chip to the input of the next chip. The timing of gate and clear outputs is controlled with strobe signals.

The few remaining control registers are configured via JTAG interface. It also allows a boundary scan to check the input pads.

Since no commercial bumping is available for AMS chips in a MPW run, the bumping of the chips is done on die level by an Electro-less Nickel Immersion Gold (ENIG) process for the UBM and subsequent balling with SAC305 balls utilizing the so-called SB2 process at PacTech, Nauen, Germany.

Short chip history:

- **Switcher-B33 v1.0**:
  - Initial submission of adopted Switcher4 design. 3.3 V supply and max. 50 V output voltages. 0.35 µm HV technology
- **Switcher-B18 v1.0**:
  - Redesign 0.18 µm HV technology. 1.8 V supply and max. 20 V output voltages, referenced to GND
- **Switcher-B18 v2.0**:
  - Added Gated Mode operation and improved voltage range. 1.8 V supply and max. 50 V output voltages with max. 25 V swing.

3. Summary of latest test results

3.1. DCDB4_pipeline

The following section gives an overview of the different assemblies. We will focus on the main properties of the chip: read-out of a prototype matrix, tests of the digital data transmission between DCD and DHP, missing codes, noise, and INL/DNL. Noise and digital data transmission have been tested also as a function of the total ionizing dose TID.

3.1.1. Hybrid 4 - sensor read-out at full speed

Nineteen Hybrid 4 boards have been assembled with the different versions of the DCD. Three have been assembled with the DCDB4_pipeline and were tested at the University of Heidelberg and the MPG HLL. The single-ended digital outputs of the DCDB4_pipeline are connected to the DCDr/o which does a conversion to differential signals and amplifies the signal amplitude to be transmitted to an FPGA.

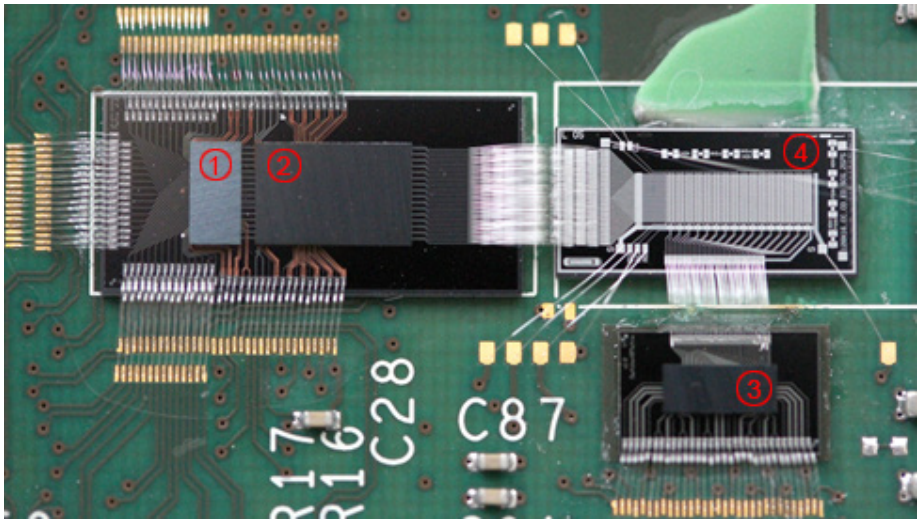

Fig. 3-1 Hybrid board H4.1.07 with 1) DCDr/o, 2) DCDB4_pipeline, 3) Switcher-B18 v2.0 and 4) DEPFET matrix

Table 3-1 lists the three boards with DCDB4_pipeline and their configuration.

Board Label	DCD Version	SWB Version	DEPFET Matrix
H4.1.07	DCDB4_pipeline	Switcher-B18 v2.0	PXD6, W22, L05, 50 µm x 75 µm, L_{Gate}=6 µm
H4.1.17	DCDB4_pipeline	Switcher-B18 v2.0	
H4.1.18	DCDB4_pipeline	n/a	

Table 3-1 List of Hybrid 4 boards with the DCDB4_pipeline, Full list of all hybrid boards: http://twiki.hll.mpg.de/bin/view/DepfetInternal/ShoppingMall#Hybrid_4_1_DCDB_DCDPipeline_DCDR

In addition to the results presented below there are also stand-alone tests of two DCDB4-pipeline chips in a setup at Uni Heidelberg. In each chip half of the ADCs (128 per chip) have been tested. The most relevant results are:

Chip#1:

INL: 127 channels between 1 and 2.7 LSB, 1 channel ~5 LSB due to missing code

Noise: 0.6 LSB (~46 nA)

Chip#2:

INL:	128 channels between 1 and 2.5 LSB
Noise:	0.6 LSB (~46 nA), a channel had stuck LSB and therefore noise 0.8 LSB

Both chips were operated at a digital supply voltage of VDDD = 1.864 V. With the exception of the stuck bit, no digital communication problem was observed.

Hybrid 4.1.07 is equipped with a 50 µm thin DEPFET matrix. It has 2048 pixels which are arranged in a 32 x 64 pixel array and is connected to 16 channel-pairs (*Clear* and *Gate*) of the Switcher-B18 v2.0 and 128 DCDB4_pipeline inputs.

On this hybrid we characterized all 256 ADCs of the DCDB4_pipeline with the internal current source. An overlay of all 256 transfer curves is shown in Fig. 3-2. Twenty out of 256 channels showed missing codes larger than 5 ADUs. The number of the channels showing missing codes depends on the RefIn voltage and settings for IPSource and IPSource2. It is not completely clear whether the used settings were optimal.

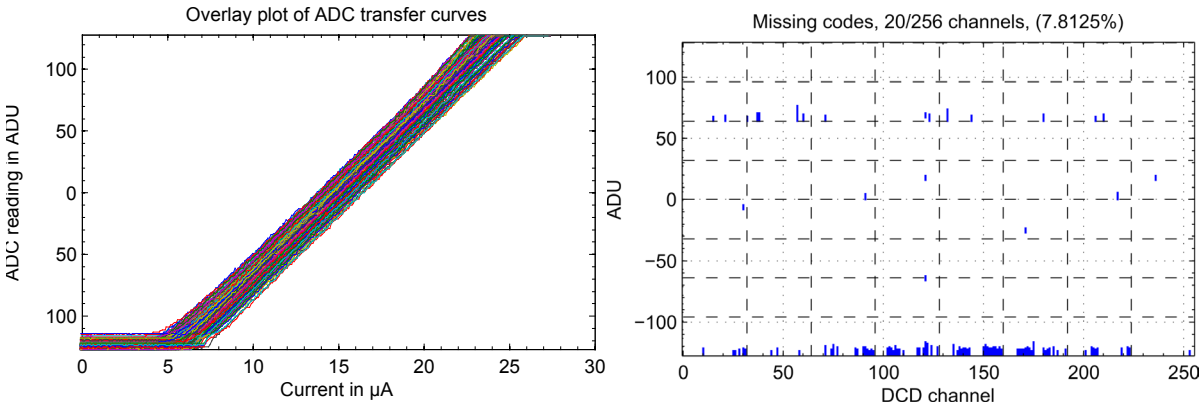

Fig. 3-2 Overlay of the 256 transfer curves, 8% showed missing codes > 5 LSB

A dependence on the position of the ADC channel within the DCDB4_pipeline die could not be found. Fig. 3-3 shows the channels with missing codes larger than 5 ADUs in blue.

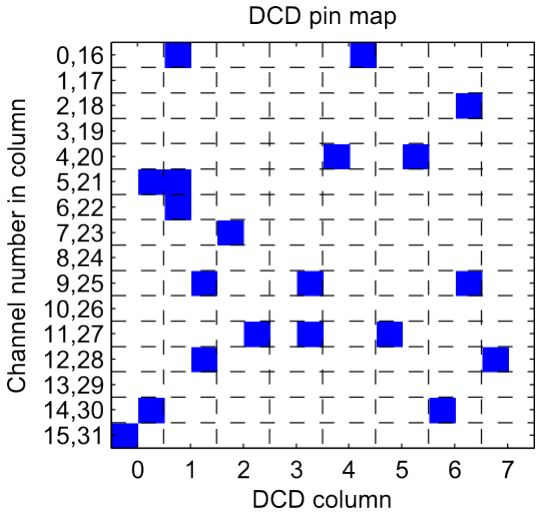

Fig. 3-3 Position of the channels with missing codes > 5 ADU within the DCDB4_pipeline on Hybrid 4.1.07

The measured mean of the INL values of all channels is at 2.3 ADU. There are several curves which show larger INL values. They coincide with the channels showing missing codes.

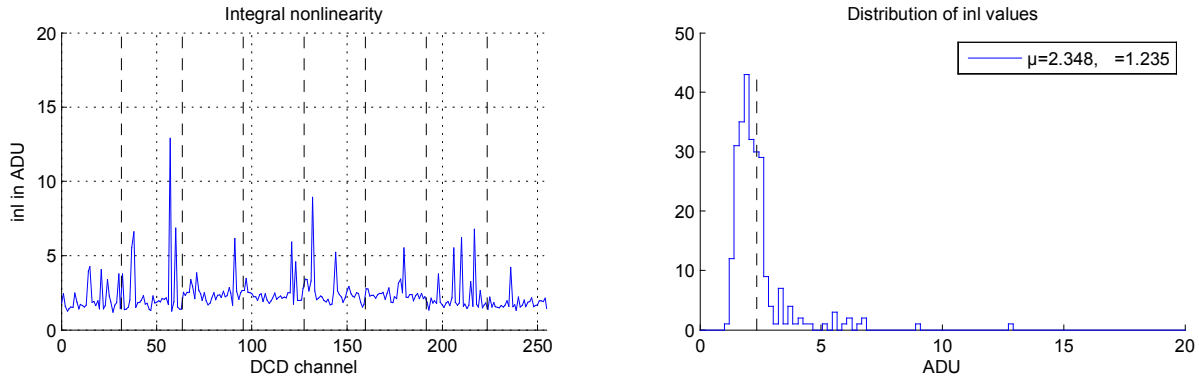

Fig. 3-4 INL of DCDB4_pipeline on Hybrid 4.1.07

The matrix was optimized with respect to its operational voltages (*Clear*, *ClearGate*, *Gate*) and tested with a laser source and a Cd109 radioactive source. The DCDB4_pipeline was operated with the nominal clock frequency of 320 MHz which translates to a read-out time of 100 ns for one DEPFET row (128 pixels are read-out in parallel). Within this time the DEPFET drain current is digitized by the DCDB4_pipeline. The noise (defined as the standard deviation of the pixel pedestal currents) is shown in Fig. 3-5 (right). Its mean value is at 0.7 ADU. The left plot of Fig. 3-5 shows the cluster charge of the Cd109 source. The 22 keV x-rays generate 6100 e- signal charge, similar to the most probable value for a mip in 75 μm silicon. The signal-to-noise ratio (SNR) has the very comfortable value of the 47.

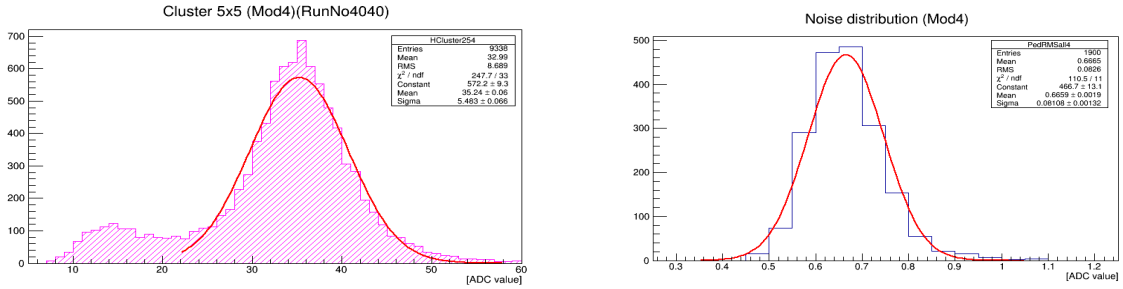

Fig. 3-5 Cd109 signal (6100 e-, similar to a mip in 75 μm Silicon) @33 ADU, noise @0.7 ADU, SNR of 47.

During pedestal measurements a random appearance of negative codes was observed. Codes of -32 ADU or -64 ADU appeared for random pixels. This phenomenon seems to be associated with bit errors in the communication between the DCDB4_pipeline and DCDr/o plus FPGA. On the Hybrid 4.1.07 board an increase of the digital supply voltage of the DCDB4_pipeline by 100 mV (to 1.9 V) eliminated these bits.

3.1.2. Hybrid 5 – direct test of the digital communication

Six Hybrid 5 boards are assembled; three being used for DHPT stand-alone tests and three equipped with both DHPT and DCDB4_pipeline ASICs. The chips are bump-bonded to a silicon interposer and from there on wire bonded to the hybrid. The DHPT is read out by the DHE back-end electronics system with the same software as used for the EMCM setup.

The Hybrid 5 setup allows direct access to VRef, the reference voltage for the LVSS data transmission between DCD and DHP (for the block diagram see Fig. 3-8). Applying an external voltage to the VRef input of DHP and scanning this voltage allows the direct measurement (in a sampling oscilloscope manner) of the digital output signals of the DCDB4_pipeline. Hence, any issues in the data transmission are directly visible.

Code	Tags	State	Item Quality	Components	Location
Hybrid_5.0.03	digital OK analog OK analog @ 160 MHz NEEDS CONFIRMATION	unset	not classified	0/6 attached	SiLAB Bonn
Hybrid_5.0.07	DHPT1.0 DCD pipeline no matrix attached Passives equipped	untested	Class A	3/6 attached	SiLAB Bonn
Hybrid_5.0.06	DHPT1.0 DCD pipeline no matrix attached	untested	Class B	3/6 attached	SiLAB Bonn
Hybrid_5.0.01	DHPT1.0 DCD pipeline no matrix attached digital OK digital @ 160 MHz	unset	not classified	3/6 attached	SiLAB Bonn
Hybrid_5.0.05	SWB gated mode DHPT1.0 DCD pipeline no matrix attached	unset	Class A	1/6 attached	SiLAB Bonn
Hybrid_5.0.04	SWB gated mode DHPT1.0 DCD pipeline matrix attached	unset	Class A	2/6 attached	SiLAB Bonn

Table 3-2 List of assembled Hybrid5 systems

The output of 32 DCDB4_pipeline channels is multiplexed into an 8-bit data bus. Consequently, we have 8 of these data buses, with a total of 64 data links.

A hard-coded test pattern is implemented in the DCDB4_pipeline in order to test these data links. This test pattern has three different bit sequences: one for the MSB links, one for the LSB links, and one for all other links.

ADC Index	29	30	31	0	1	2	3	…	29	30	31	0
MSB	0	0	0	1	0	0	0	…	0	0	0	1
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
	1	1	0	0	0	1	1	…	1	1	0	0
LSB	1	1	0	1	0	1	1	…	1	1	0	1
Value	**127**	**127**	**0**	**-127**	**0**	**127**	**127**	…	**127**	**127**	**0**	**-127**

Table 3-3 Digital test pattern of the DCDB4_pipeline

Fig. 3-6 shows a direct measurement of one data bus, i.e. eight data links. Note that bit 0 does not reach the nominal zero level.

This measurement confirms the simulations in section 4.1. Please note that his behavior will be improved by increasing the DCD's output driver strength and by reducing the capacitance of the DHPT input pads.

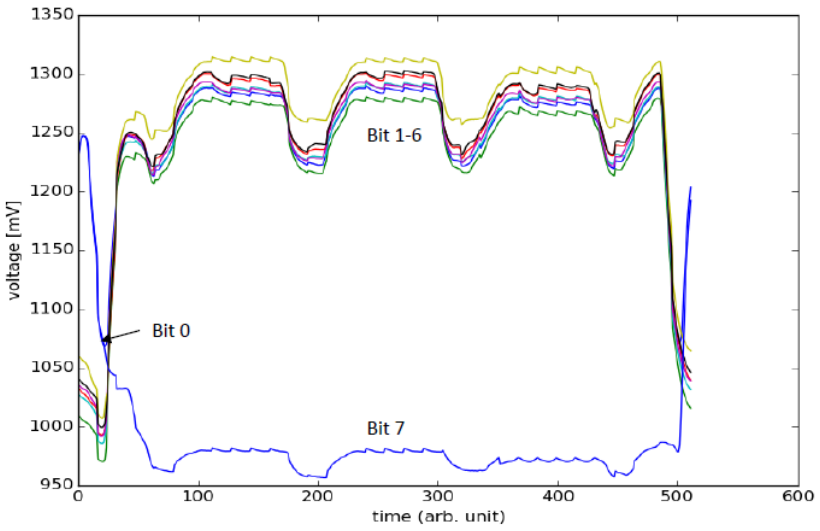

Fig. 3-6 Changing VREF - the DHPT can measure the DCDB4_pipeline output like a sampling oscilloscope

3.1.3. Measurements on the Electrical Multi-Chip Module (EMCM)

Six EMCMs are equipped with the set of latest ASICs 4xDHPT1.0, 6xSwitcher-B18 v2.0, and 4xDCDB4_pipeline. Table 3-4 lists the EMCMs.

ID	EMCM version	Status
W17-3	EMCM3	Crack in Si-substrate, jig for cooling broken, module has to be checked after leak of cooling tubes
W17-4	EMCM3	No kapton – used for probe card testing
W18-3	EMCM3	Small PXD6 matrix attached
W31-3	EMCM3	Used for DHPT/ DCDB4_pipeline irradiations
W31-4	EMCM3	Assembled, to be tested, crack in Si-substrate
W18-4	EMCM3	Assembled, to be tested

Table 3-4 List of EMCMs with DCDB4_pipeline and DHPT1.0

3.1.3.1. Digital data transmission DCD-DHP

One can change the sampling point of the DHPT receivers with respect to the DCDB4_pipeline clock by two delay settings: a “global” delay g and a “local” delay l. In the block diagram in Fig. 3-8 the global delay acts on DCD_CLK, and the local delay acts on the 64 data receivers. The digital test pattern is used to detect bit errors as function of these two delays g and l. The number of found bit errors is shown in Fig. 3-7. The optimal setting is the one without any bit errors

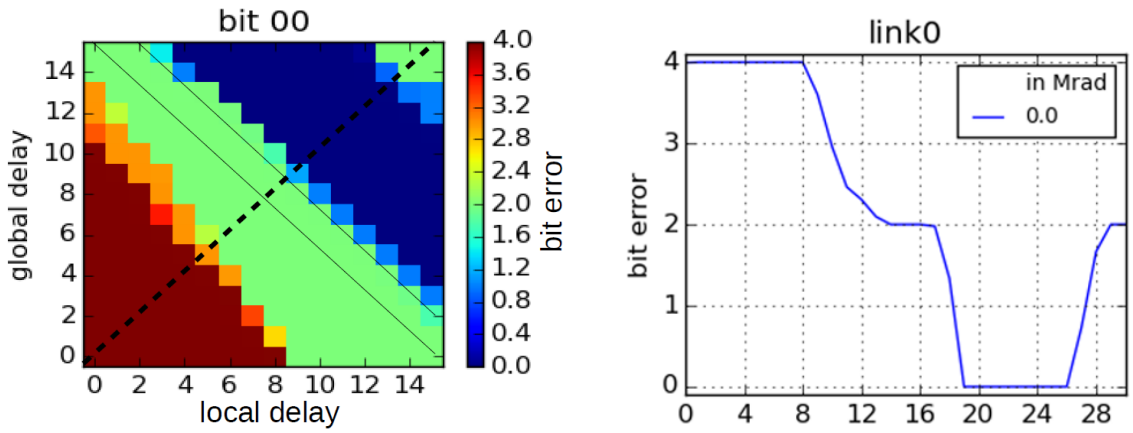

Fig. 3-7 Example of the optimization of data transmission. Left: Global and local delays are scanned. The points in the “valley” with zero bit errors are possible operating points. Right: cut along the dashed diagonal line. We call the width of the valley “delay tolerance” and use it as a figure of merit.

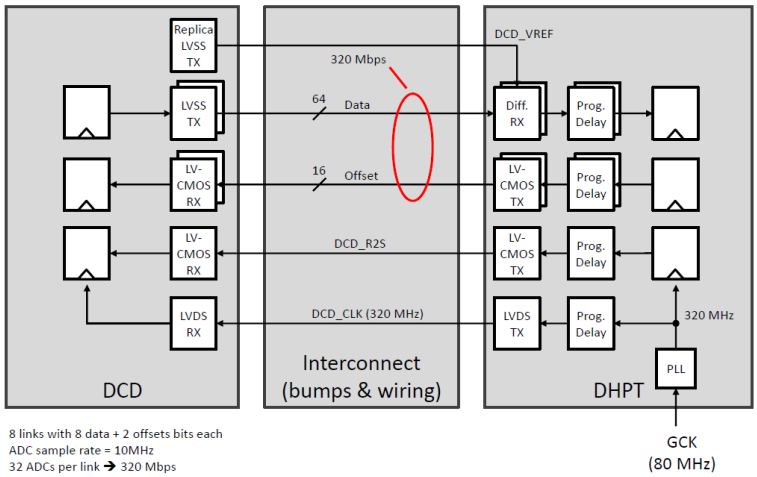

Fig. 3-8 Block level schematic of the DCDB4_pipeline -DHPT interface

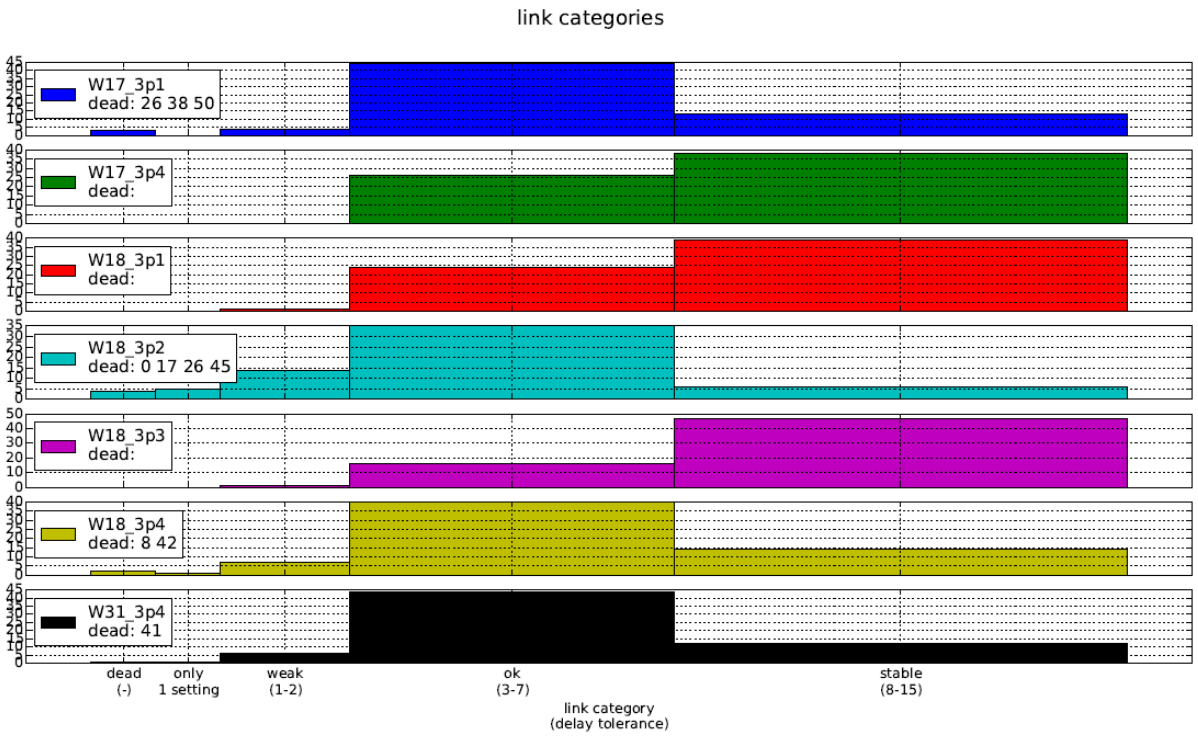

Fig. 3-9 Summary of the optimization procedure on seven DHP/DCD pairs on three different EMCMs

The summary of the delay measurements in Fig. 3-9 shows that there are data links which fail in this test. All links passed the low-speed boundary scan before, but there are ten inks where no stable data transmission can be found, and an even higher number of links with a very small delay tolerance of one to two possible settings for g+l.

There are links which pass this test, but fail when real data are transmitted. One example of such a link is the MSB (link23) of EMCM W31_3_p4. It fails during the measurement of ADC transfer curves as shown in Fig. 3-10, but has no bit error in the test with the digital test pattern.

In Addendum A4 a detailed analysis of the delay scans of in total seven ASIC pairs on the EMCMs W17-3, W18-3 and W31-3 is given.

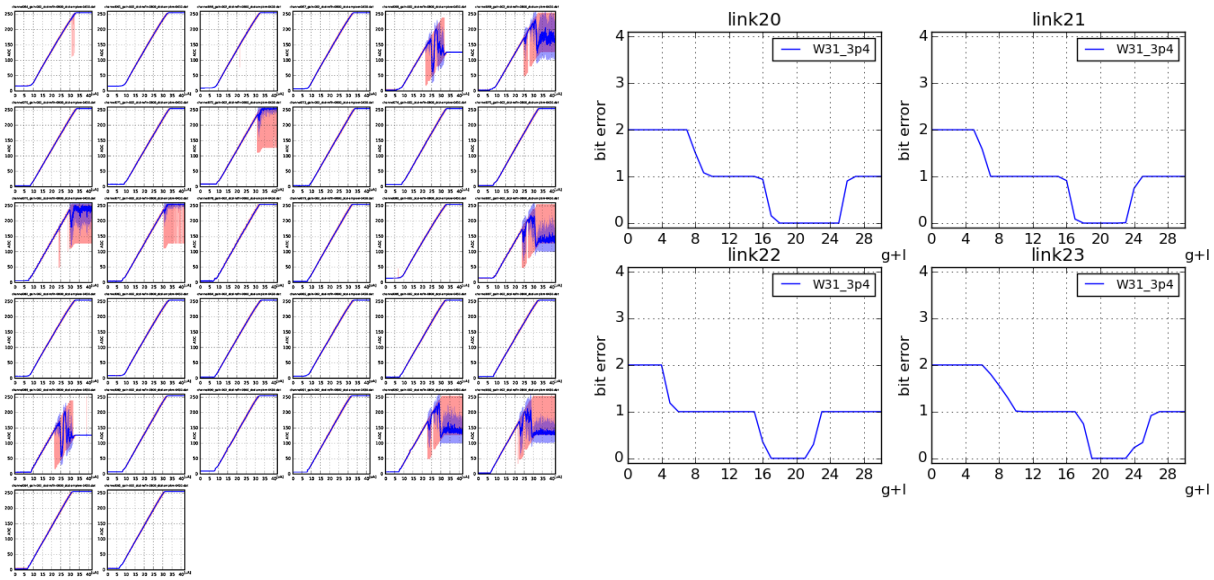

Fig. 3-10 EMCM W31-3_p4 all ADC channels of data bus 2; links optimized with digital test pattern and acceptable quality (right plot) are still showing problems when transmitting real data. The left plot shows transfer curves of all channels which transmit their MSB via link 23. For many of them the MSB toggles.

3.1.3.2. Missing Codes

The number of channels showing missing codes strongly depends on the RefIn voltage and the settings of IPSource and IPSource2. The results reported so far were not obtained with the optimal settings. Careful and time consuming optimization of IPSource and IPSource2 reduces the number of missing codes larger than 5 ADU to zero. Just for internal use and for completeness, Table 3-5 lists the values for the other parameters.

The result of such an optimization scan IPSource vs. IPSource2 on EMCM W31_3p1 (ASIC pair 1) is shown in Fig. 3-11. There are several regions without missing codes. This is being repeated on other chip pairs on EMCMs and confirms the findings done on single chip setups. The number of channels with missing codes is highly setting dependent.

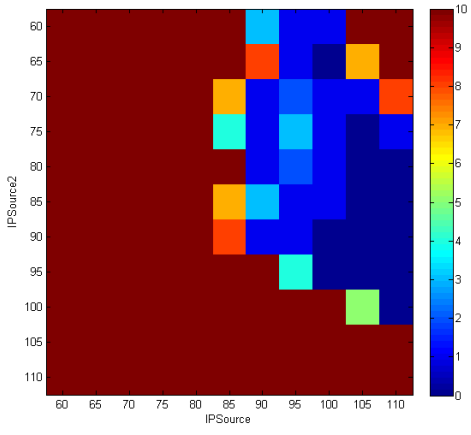

Fig. 3-11 IPSource vs. IPSource2 scan, color code is the number of channels with missing codes larger than 5 ADUs

ipsource	ipsource2	ifbpbias	vnsubin	channels	gain	refin	amplow	Current Source
[60,110]∩k*5, k∈ℕ	[60,110]∩k*5, k∈ℕ	85	7	[0,255]∩k*1, k∈ℕ	1	900	350	[500-11000]∩k*10, k∈ℕ

Table 3-5 Parameter of the IPSource vs. IPSource2 scan

3.1.3.3. Noise

While the ADC transfer curves are important to determine INL, DNL and check for missing codes, they are not suitable to measure the noise of the ADC channels, because in that case the noise is dominated by the noise of the current source. Therefore, we extract the noise using raw frames without any external current.

We shift the pedestals into the dynamic range by adding and/or subtracting currents from two global current sources (IPAddIn and IPSubIn). Then we record a raw frame, which consists of 256 readings of each channel. The noise is calculated as the average of those 256 readings.

This procedure results in reasonable noise figures – as can be seen in Fig. 3-12 to Fig. 3-15. These plots show the histogram of the pedestals, the histogram of the noise and the noise as function of the channel number, for four different mean positions of the pedestals. In Fig. 3-12, the peak on the right side of the pedestal distribution is due to an additional current which is flowing into channel 2 (provided by the internal current source). Several peaks in the noise distribution show up at random channel positions. They may still be an artefact of the DCDB4_pipeline -DHPT communication issue.

For completeness and also for internal use: the settings for all following noise measurements, including the ones during irradiation are:

Parameter	Setting
IPSource	90
IPSource2	70
IFBPBias	90
RefIn	1.2V
Amplow	0.4V

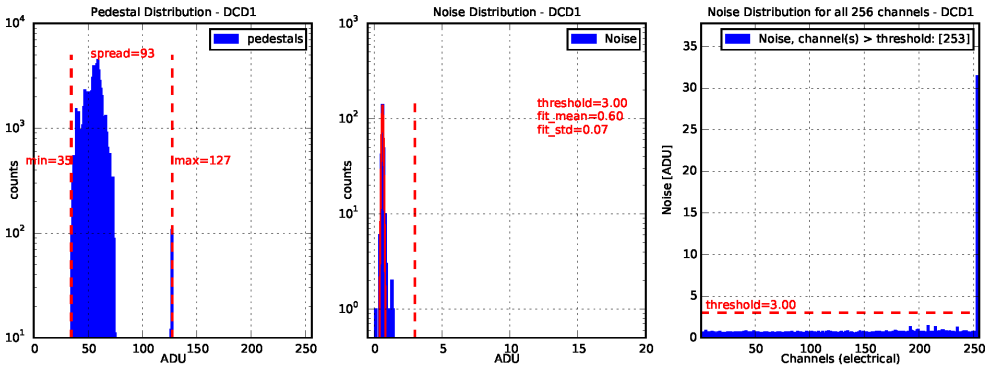

Fig. 3-12 EMCM W31-3 P1, pedestals around 50 ADU: Noise 0.6 ADU - one channel with high noise due to communication issue

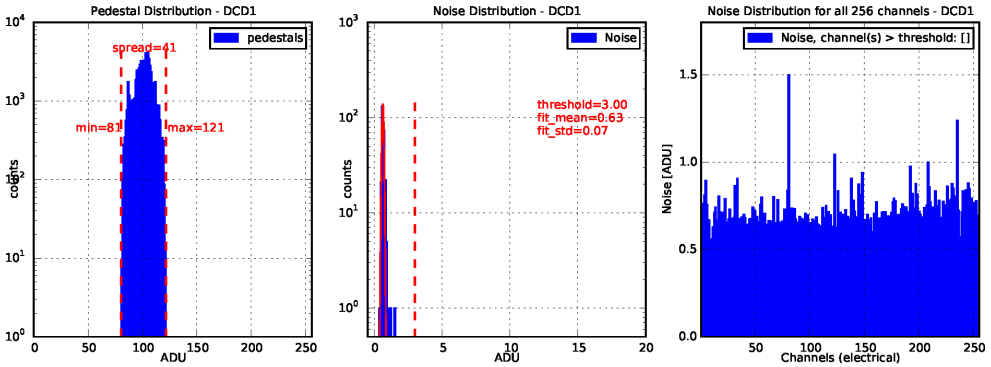

Fig. 3-13 EMCM W31-3 P1, pedestals around 100 ADU: Noise 0.63 ADU

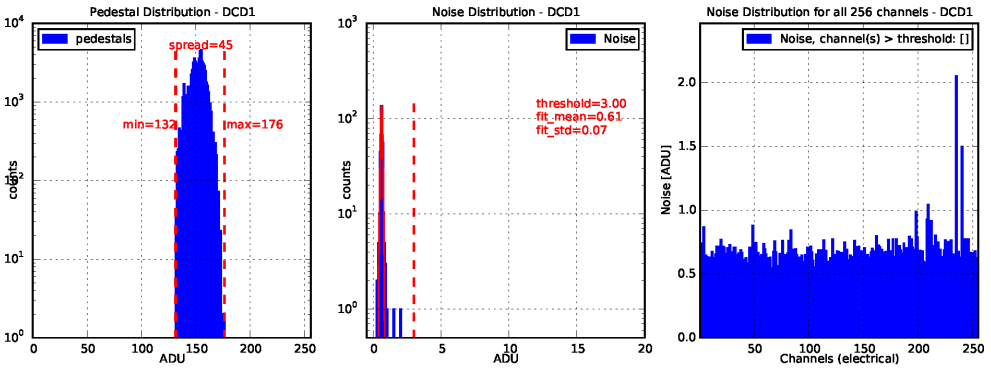

Fig. 3-14 EMCM W31-3 P1, pedestals around 150 ADU: Noise 0.63 ADU

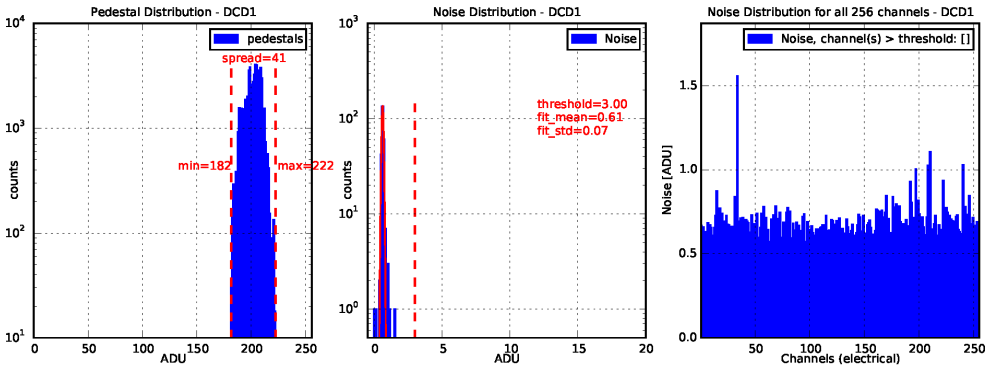

Fig. 3-15 EMCM W31-3 P1, pedestals around 200 ADU: Noise 0.63 ADU

3.1.3.4. Integral and differential non-linearity

The integral nonlinearity (INL) is defined as the maximum deviation of the ADC transfer characteristic from the best straight line fit, in the range between -100 and 100. 256 ADC are characterized on EMCM W31-3 P1 yielding 256 curves and fits. The INL of the ADCs (channels) is then plotted against the channel number in Fig. 3-16. The INL of the 256 ADCs is well below 5ADU and with that within the specification.

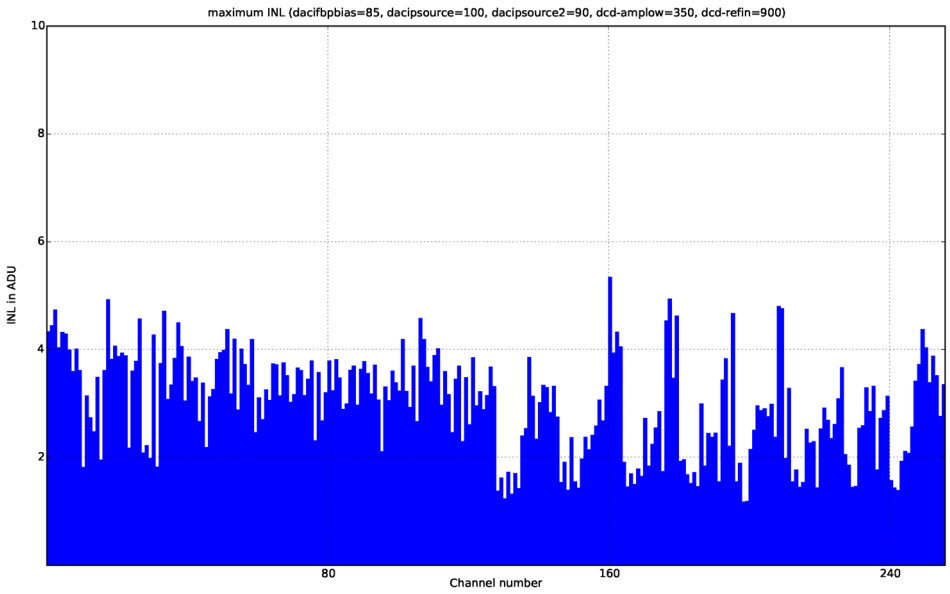

Fig. 3-16 EMCM W31-3 P1: INL vs. DCD channel

One can observe a distinct pattern, and Fig. 3-17 suggests that this is linked to the organization and physical location of the ADC channel on the DCD. This is work in progress and has to be confirmed by characterization of other chips to be understood.

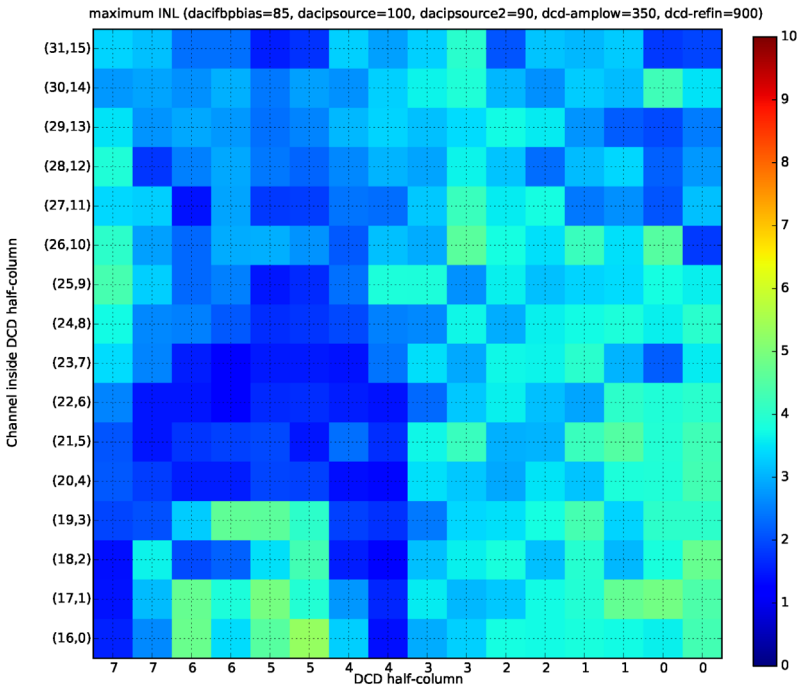

Fig. 3-17 EMCM W31-3 P1: INL vs. ADC position on the DCD

Fig. 3-18 shows the differential nonlinearity (DNL) as function of the ADU value, for an arbitrary set of channels. A few channels show DNL values of -1, which corresponds to a small missing code.

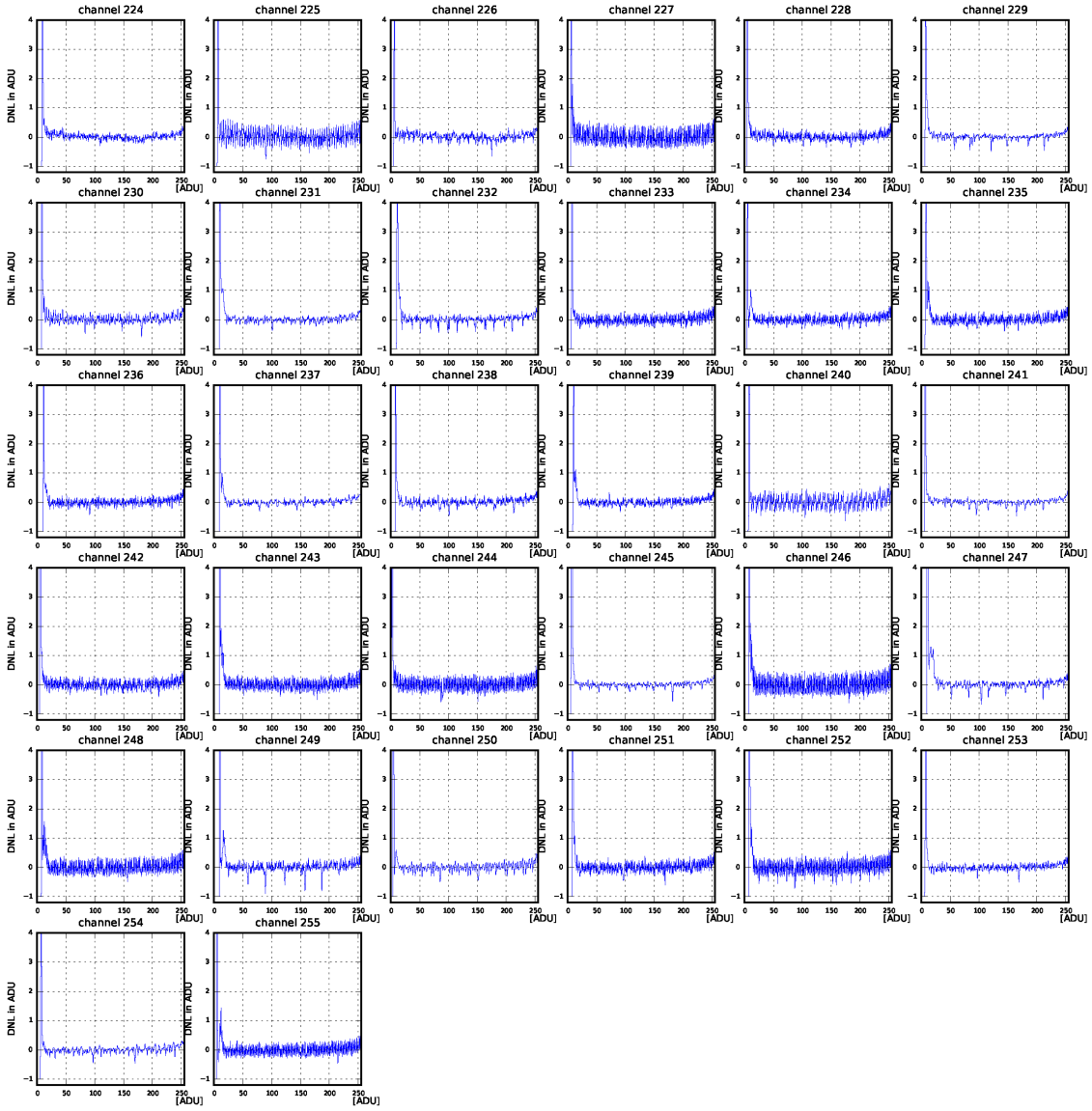

Fig. 3-18 Example of DNL measurements for 32 ADC channels. According to the definition of DNL, one missing code can be seen by a DNL of -1 for this ADC value (see channel 249).

In order to characterize the whole chip with a small set of numbers, we judge the DNL of one channel by using the median of the absolute deviation from the median (mad), again in the range between -100 and 100 ADU. We then plot the mad(DNL) of each ADC. The result is seen in Fig. 3-19: the mad(DNL) is mostly below 0.1, with a few channels going to around 0.4.

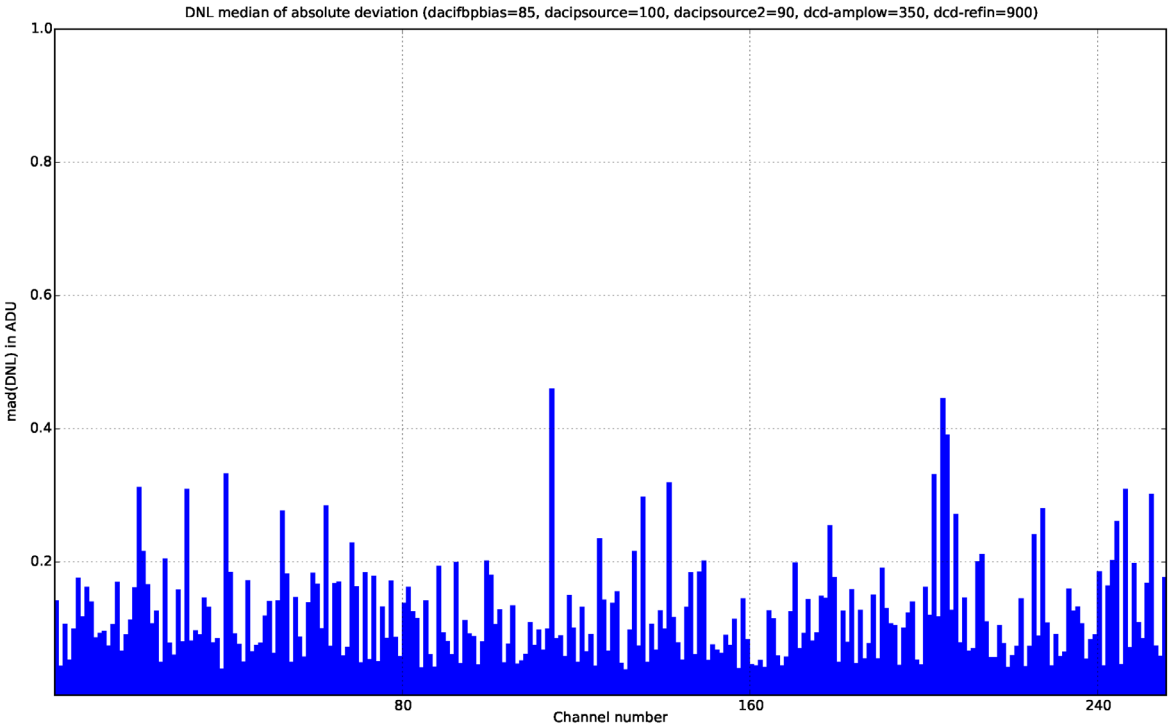

Fig. 3-19 mad(DNL) versus ADC channel

3.1.4. X-ray irradiation results – EMCM W31-3-p4

As presented in the July review the EMCM W31-3 ASIC pair p4 was irradiated with 60 keV photons up to 20 Mrad. The setup was described in detail in the presentation.

3.1.4.1. Noise versus TID

At the review preliminary data was presented. In particular the noise figure during and after irradiation was not fully understood. Additional measurements revealed that the main contribution to the claimed noise values came from the external current source. New measurements, just looking at the standard deviation of 256 readings without external current at a reasonable offset value for the ADC, show much lower noise figures. Before irradiation this was shown already in section 3.1.3.3. Fig. 3-20 shows now the noise at various TIDs. The noise is comparable with the un-irradiated ASIC pair p1 on the same EMCM and does not depend on TID.

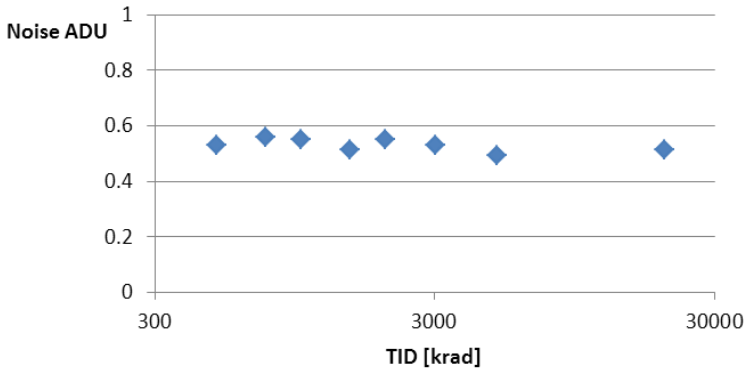

Fig. 3-20 Evolution of noise with higher TID

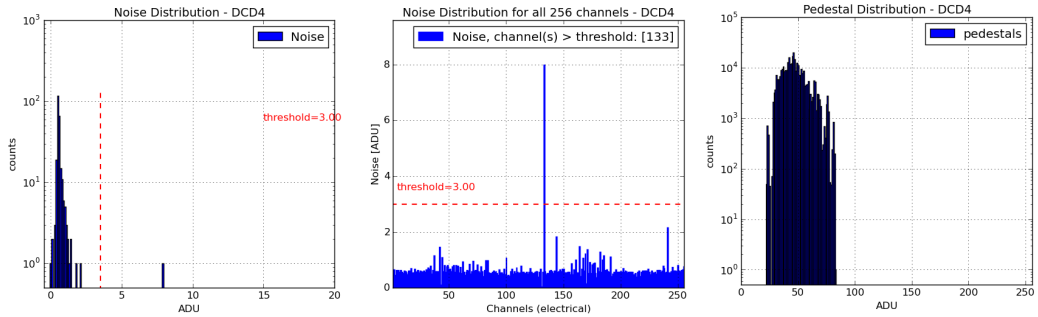

Fig. 3-21 As an example for the raw data: Noise measurement at 3 Mrad

3.1.4.2. Digital Data transmission versus TID

Already in section 3.1.3.1 we showed the issue of the digital data transmission from the DCD to the DHP. The delay tolerance was defined as a figure of merit. After each irradiation step this delay tolerance was measured to investigate whether the quality of the links degrade with irradiation. The findings are plotted in Fig. 3-22. At 2 Mrad there are more links that fail but were good before irradiation. Link 41 has zero tolerance already before irradiation and stays bad. After 10 Mrad, all links are as “good” as before.

As a conclusion, it can be said that the links are getting weaker at the critical dose around 2 Mrad but recover again at higher doses. This has to be repeated with the new DHP/DCD pairs with improved link stability (see section 4.1), to see if this is still an issue.

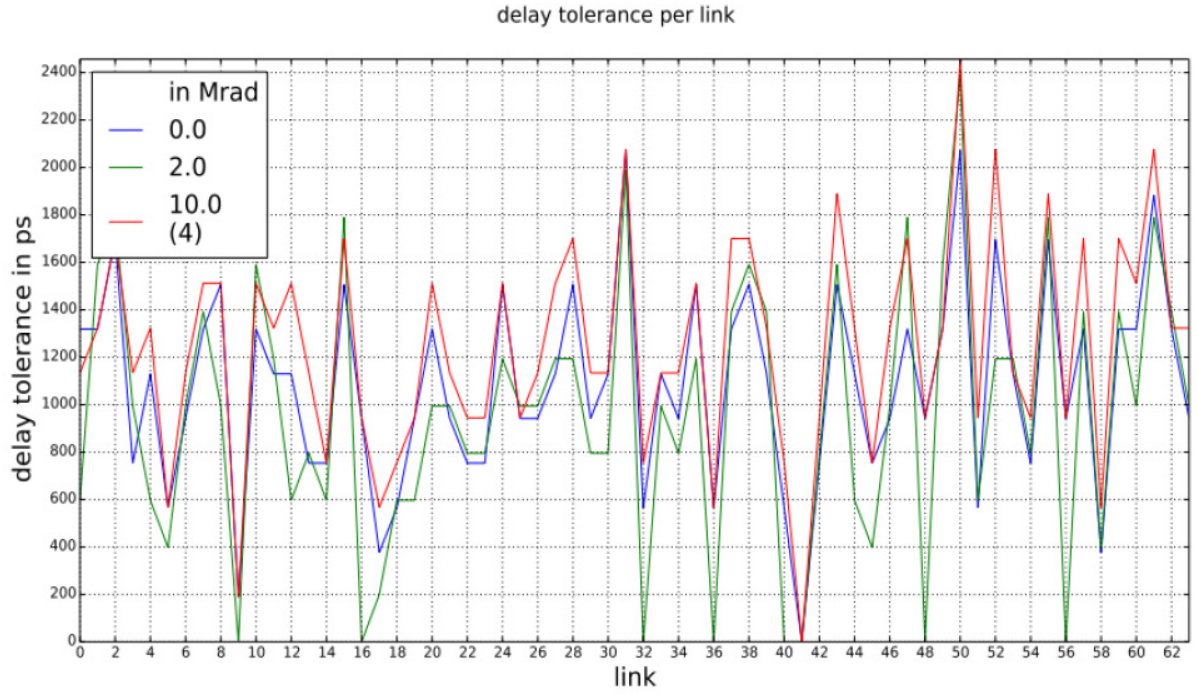

Fig. 3-22 EMCM W31-3-p1: Delay tolerance per link before irradiation, after 2 Mrad, and after 10 Mrad

3.2. Switcher-B18 v2.0

The Switcher-B18 v2.0 was extensively discussed already at the 1st review in October 2014. Since then, there are no new results worth mentioning here. In addition to the presentations last October, the Reference Manual is attached as Addendum 2 to this document. There you will find the detailed description of the functionality and test results of stand-alone tests. The chip is used in all test setups including a DEPFET matrix and works reliably.

As a summary of the main findings described in Addendum 2:

- It delivers the specified voltage range for DEPFET *Gate* and *Clear*
- It supports the operation of the DEPFET Matrix in “gated mode”
- It was irradiated up to a TID of 21 Mrad without significant performance loss

Unfortunately the data taken at lower TIDs are lost (hardware problem) and cannot be recovered anymore. Data are available only for 500 krad and 21 Mrad. We will repeat the irradiation with chips from the next submission to verify the results presented in Addendum 2. We don’t expect significant issues since the chip is done in AMS 180nm technology with all transistors having thin gate oxides. The radiation tolerance is expected to be comparable to other deep submicron technologies.

The dynamic performance after irradiation is shown in Fig. 3-23. The rise time to 20 V is about 15 ns and confirms the simulation in section 4.5; please see this section for detailed discussion of the planned changes for the next submission.

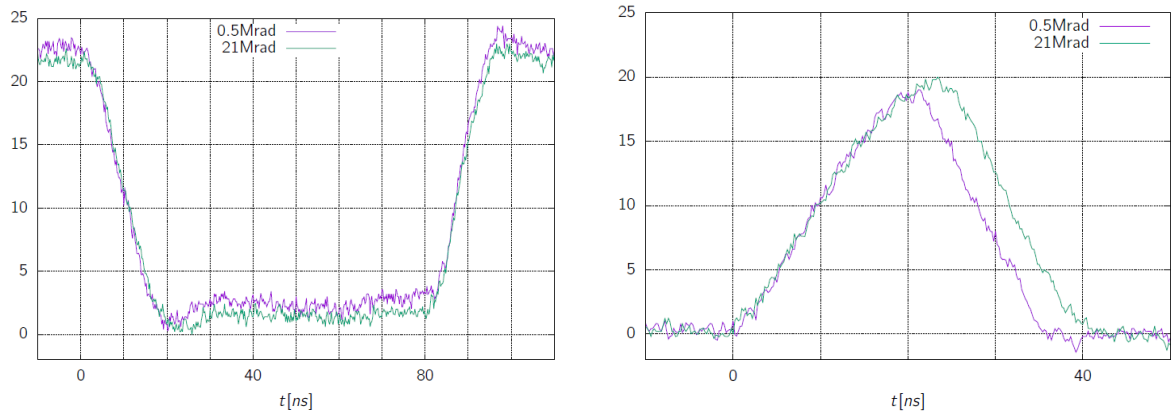

Fig. 3-23 Switcher-B18 v2.0 rise and fall times of the Gate (left) and Clear (right) outputs with 150 pF load after 500 krad and 21 Mrad

4. Next version of the ASICs: DCDB4.1 and Switcher-B18 v2.1

Following the results presented in the previous sections we conclude that the current DCDs and Switchers fulfill the specifications to a large extent. The performance of front-end and ADC of the DCDBv4_pipeline in terms of noise and linearity is good enough for the final application in the experiment. However, there are still a few issues worthwhile clarification and optimization, which warrant a new submission.

For the DCDBv4_pipline:

- It was clearly shown that the digital data transmission between DCD and DHP has to be improved. This has been discussed at the review; changes to the DHP receiver side are already proposed and will be implemented. The required changes in the DCD will be discussed below.
- The few “missing codes” in the ADC transfer curve (their frequency being below the specified level) are not critical for the operation in the experiment. This will be shown below. Nevertheless, we would like to understand their origin and remove them with as little risk as possible.
- In the light of recent static measurements on the pedestal spread coming from the DEPFET we have to slightly re-adjust the gain ranges of the front-end and the range of the DAC for pedestal correction (IPDAC)
- The DCDB4_pipeline samples the global control- and pixel-data at falling TCK edge; this will be changed to rising edge to be conformal with the industry standard.

The basic functionality of the Switcher-B18 v2.0 including the operation in “gated mode” of the DEPFETs was shown. The improvements for the new submission are:

- The rise time of the clear signal for the high capacitive load of the *Clear* net will be decreased
- The on-chip termination of the serial input SerIn should be, in contrast to the other LVDS pads, always enabled.
- The bump pad geometry and size was done for the initially planned Au-stud/SAC305 balls bumping. The bumping technology has changed to ENIG/SAC305 balls and with this the LM pads for the bump have to be changed

4.1. Digital Data transmission DCD to DHP

From the data presented in the previous section and as discussed in the July review it is obvious that the digital communication between DCD and DHP needs improvement. Already in July it became clear that the main changes to improve the digital data transmission are to be done on the DHP side. The agreed changes to the DHP design according to the July review are:

- Reduce the parasitic capacitance of the DHPT input pads
    - C_{PAD} ~3 pF is dominated by ESD protection; to be minimized to ~1 pF
- Remove the hysteresis on the DHP receiver side
- Fix the delay line asymmetry

4.1.1. Required changes at the DCD side

A new set of simulations was done on the DCD side to understand the origin of the observed problems and to find the appropriate countermeasures.

Fig. 4-1 shows the simulation of the data line waveform with the present DCDB4_pipeline output buffer for the line capacitance 1, 2, and 3 pF (typical capacitances) and for the present DHP input capacitance of 3 pF. The reference voltage V_{RefOut}, generated by DCD, is also shown.

There is a duty cycle asymmetry with the width of the logic zero being 2.28 ns (ideally, it would be 3.125 ns). 2.28 ns is expected to be long enough for a safe sampling of logic zero. However, the measurements show a much smaller sampling window.

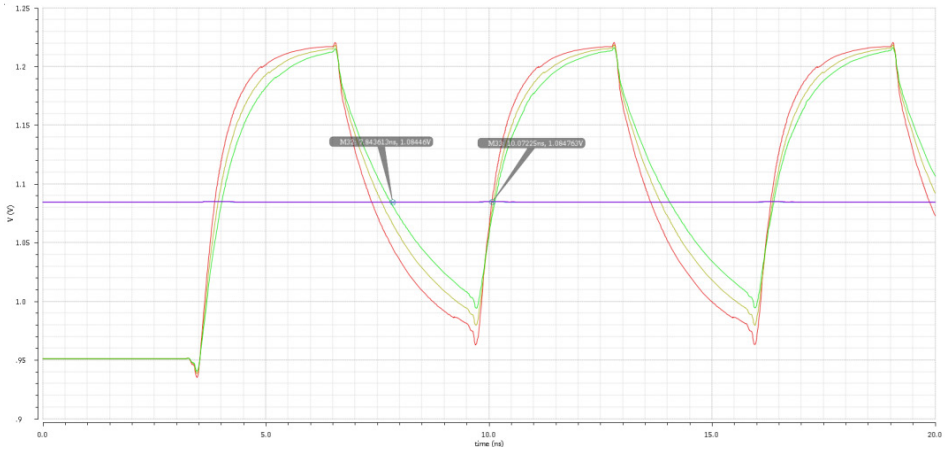

Fig. 4-1 Data line output of the current DCDB4_pipeline; capacitive load 3 pF from DHP and 1 to 3 pF for the line capacitance as parameter

Fig. 4-2 shows the input and output waveform in the case of current DHP receiver. The width of the logic zero after the receiver is ~1.75 ns. Here the duty cycle reduction of the delay elements (~700 ps)

should be also taken into account. The logic zero window after the delay elements is estimated to be ~1 ns. This corresponds to a duty cycle of 16%.

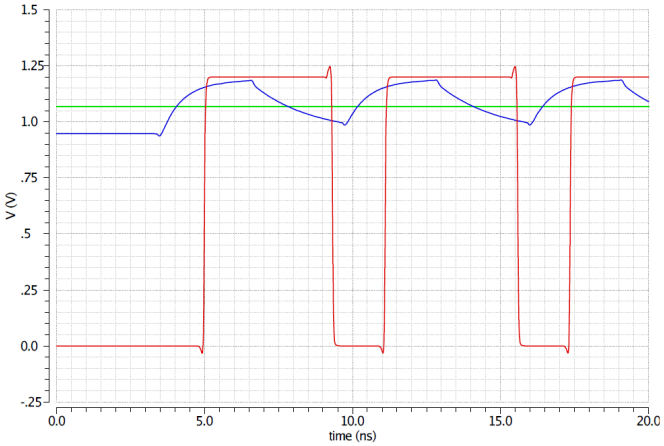

Fig. 4-2 Simulation of the present data communication with 3pF line capacitance and 3pF at the DHP receiver

Removing the hysteresis completely as discussed during the July review but keeping the line and DHP input capacitance unchanged shows already an improvement. Adding the planned reduction of the DHP input capacitance to 1 pF, but keeping the DCD output stage unchanged results in a safer data transmission as shown in Fig. 4-3.

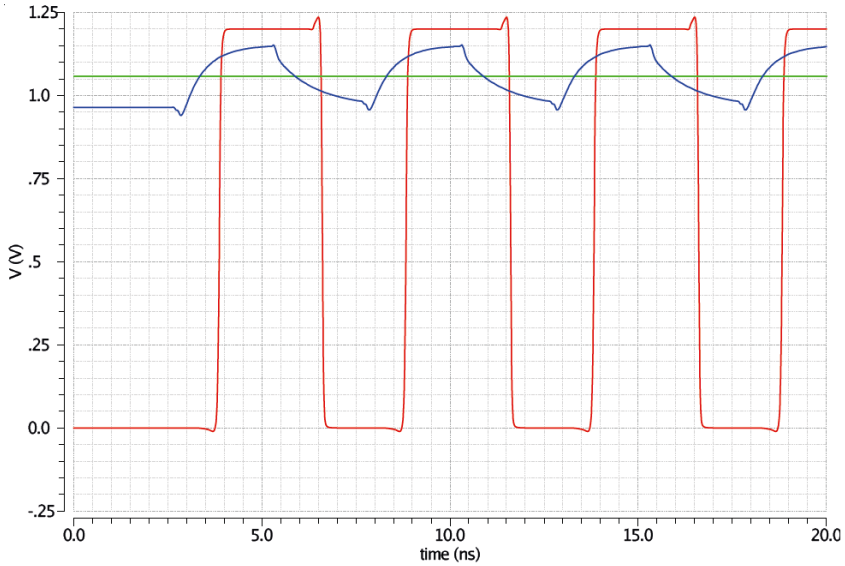

Fig. 4-3 In- and output of the DHP receiver without hysteresis with the reduced DHP capacitance of 1pF

According to these simulations the changes at the DHP side are almost sufficient to ensure a safe data transmission and a change to the DCD driver is not mandatory. The proposed DHP changes will increase the sampling window from estimated 1 ns to ~2.3 ns.

However, for safety reasons and to improve the operation window on the module, it would be advantageous to have in addition the possibility to increase the DCD output strength by adding an additional switch and a resistor for the bias boost at the DCD output (from 1.3 mA to 1.8 mA). This would add, if enabled, about 12% to the digital power consumption of the chip, which is well within the specs of the system. The change in the DCD is uncritical and would add operation safety. Fig. 4-4 shows the simulation of the proposed scheme with bias boost at the DCD output.

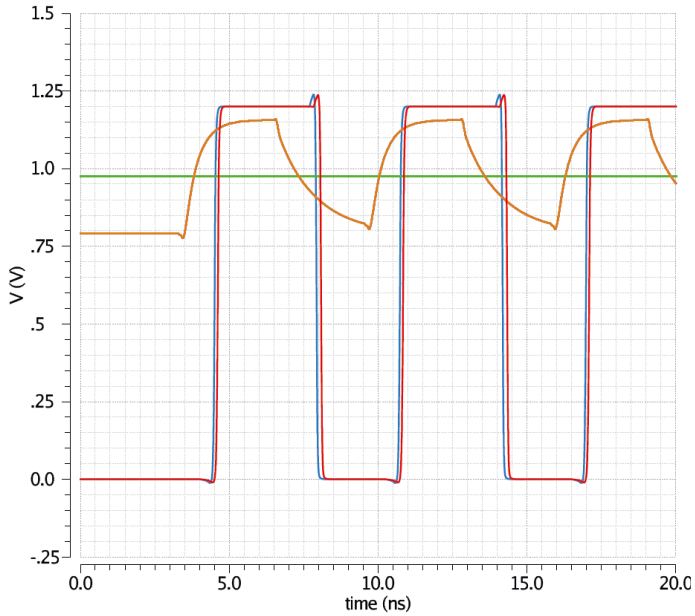

Fig. 4-4 Simulation of the proposed scheme, DHP load 1 pF, no hysteresis, bias boost at DCD output.

Changes in DHP and DCD	Logic zero sampling window (ns)
Current configuration	1
Current receiver with ideal delay element (DHP)	1.7
No hysteresis, 1pF DHP cap, ideal delay, current DCD	2.3
No hysteresis, 1pF DHP cap, ideal delay, boosted DCD	2.8

Table 4-1 Summary of the simulation results in various configurations.

In addition to simulations presented here, there are more detailed analyses on the influence of VDDD jitter and voltage drops on the data transmission are attached at the end of this document (Addendum A6). Moreover, corner simulations and the simulations from the extracted layout are added there as well.

The conclusion concerning the digital communication issue is that the agreed changes at the DHP side are almost sufficient to ensure a safe data transmission. As additional safety measure, to widen the operation window, the possibility to increase the DCD output driver current will be implemented.

4.2. ADC issues – “missing codes”

In this section we will discuss the “missing” or “long codes” issue. This feature of the ADC was present already in the first DCDB submission and was discussed in detail at both reviews. Actually, the relevance of these “missing codes” for the experiment is rather small. This will be shown in section 4.2.1. In addition, recent measurements on EMCM test devices show that the frequency of these faulty conversions is indeed very small, if the chip is configured correctly. In section 4.2.2 we will discuss the origin of these “missing codes” and possible measures to eliminate them completely.

In addition to the missing code study, the following simulations have been done and are described in detail in Addendum A6:

- ADC corner simulation
- Simulation of the sensitivity to global voltage drops (which were estimated from the layout)
- Simulations from the RC extracted layout.

The ADC works well in all simulations. Only in the case of Monte Carlo simulation, missing codes of length 1 are observed – typically in one out of 16 ADC characteristics. Monte Carlo simulations with increased transistor size show no missing codes.

4.2.1. Relevance for the experiment

"Missing code" means that for a certain analog input range the ADC does not digitize properly but delivers the digital value at the beginning of this range. The code values within the range are therefore 'missing'. Above the range the ADC works normally, meaning it 'jumps' to the correct value. If, e.g., from 120 on 8 codes are missing (assuming a strictly linear ADC with 150 nA/ADU and no noise) a current of 18.00 µA will be digitized as 120. The next current step of 18.15 µA should yield 121, but will also result in 120. This continues up to 19.20 µA, always delivering a code of 120. At a current of 19.35 µA the ADC will then correctly digitize 129 and continue normally. Practically this means that the ADC resolution will deteriorate in this current range from about σ = 0.8 ADU (120 nA) to $\sigma = 8/\sqrt{(12)}$ (=350 nA). This has two effects:

1. For inclined tracks (and due to diffusion) the charge generated in the depleted region is spread over two or more pixels. This effect is used to improve the spatial resolution by calculating a weighted mean of the pixel positions. For single pixels with 50 µm pitch (as in r-ϕ) the binary resolution is 50 µm/$\sqrt{(12)}$ = 14.4 µm. Applying charge sharing this can be improved to 7.6 µm. Clearly, this improvement depends on the ADC resolution and becomes worse if the resolution deteriorates. A missing code can only influence the position measurement if the affected channel is part of a cluster of two pixels, and the signal of one of the pixels is changed by the missing code. Both are unlikely events. In addition, a missing code can change the signal measurement only by a fraction (enter the percentage here, using the typical signal of a MIP and the corresponding signal error caused by the missing code). Keep in mind that this is the maximal signal change, which again happens rarely. If both conditions are fulfilled, a signal change would shift the position measurement only by one micrometer on average, which is well below the typical spatial resolution.
2. It could happen in principle that a cluster is ignored because the seed pixel charge falls below threshold due to the missing code error. However, this should be extremely rare since 8 missing codes correspond to only 1200e. Such a low charge for the seed pixel can only happen for the very rare cases of cluster sizes larger than 5. (the total charge of a MIP is around 6000e).

The small effect of the missing codes on the space point resolution (less than 1 µm) is confirmed by MC simulations. In several MC experiments 8 missing codes were assumed at ADC values of 7, 12, 24 and 35 (covering most of the Landau distribution in a single pixel, see Fig. 4-5). The other pixels in the cluster were digitized correctly. The result on the resolution is given in Table 4-2.

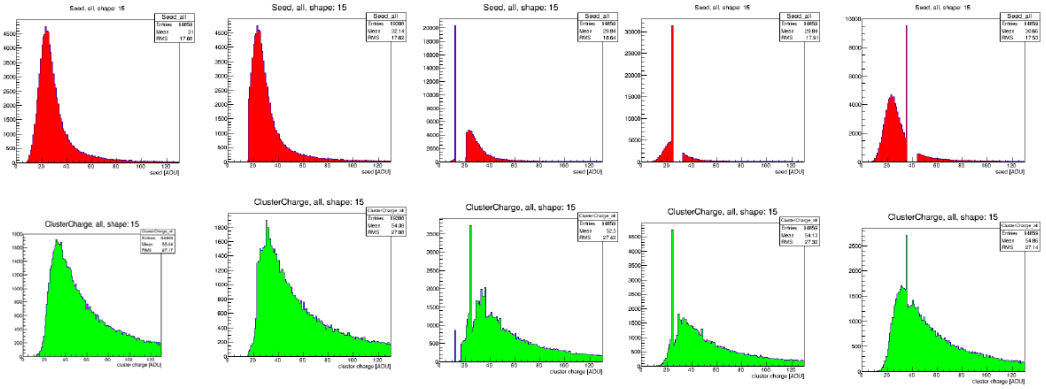

Fig. 4-5 Upper row: pixel charge distributions (in ADU) for a normal ADC and with 8 missing codes starting at ADU = 7, 12, 24, and 35 (from left to right). Lower row: corresponding cluster charge distribution.

ADC performance	Resolution in z	Resolution in r-ϕ
Perfect ADC	8.6 µm	7.6 µm
8 missing codes starting at 7	9.4 µm	8.5 µm
8 missing codes starting at 12	9.0 µm	8.0 µm
8 missing codes starting at 24	8.7 µm	7.6 µm
8 missing codes starting at 35	8.6 µm	7.6 µm

Table 4-2 Spatial resolution for a perfect ADC compared to ADCs with missing codes.

As a conclusion, the effect of missing codes is indeed very small. For smaller numbers of missing codes («5) the effect will be even less important. In practice this is further diluted if the missing code range is outside the signal range of a MIP (pedestal or above). Of course, the effect on the space point resolution will become important when the missing code range increases. However, with the present statistics we do not observe any larger ranges.

4.2.2. Cause of "missing codes" and plans for the next submission

Concerning the patterns for the "missing codes", the observations are the following:

- Optimizing RefIn, IPSource, and IPSource2 (i.e. the LSB width) results in almost complete elimination of the "missing codes"
- If there are still missing codes, they appear mostly at ADC values of -64, 0, and 64

With the transition from cyclic to pipeline ADC and the resulting 2-fold reduction of the clock speed for the comparators, there is most likely only one reason left for the remaining very small number of "missing codes": This is the effective mismatch within the transconductors, either caused by random mismatch of the transistors or by systematic effects like different transistor orientations, different transistor environment, and possibly local voltage drops within one ADC channel.

It has been shown by an analytic approach that transistor mismatch leads to missing codes. The conclusion was that one gets missing codes, if the error in the copy of the input current (I_{copy}) is exceeding 2 µA (e.g. 10 µA instead of 12 µA), which is 12.5% of the signal range. This means, due to the complex design of the transconductor, a mismatch of only 2/24 = 8.3% in one device can cause a dangerous change of the threshold voltage. When the ADC is simulated under such conditions, we obtain the result as shown in Fig. 4-6.

4.2.2.1. Random mismatch

In addition of the analytical approach, Monte Carlo simulations have been performed to investigate the effect of random mismatch of the transistors. At time of the July review, it could not be quantitatively confirmed that the mismatch alone leads to the effect.

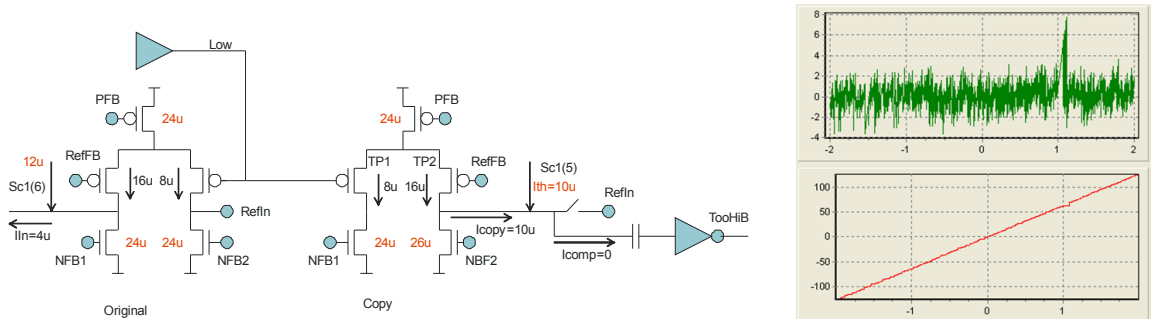

Fig. 4-6 Schematic and analytical simulation result showing a missing code

More recent MC Simulations now confirm that missing codes with length 1 can indeed be expected. The difference to the simulations at the July review is that the LV-PMOS transistors were not varied in the old MC simulation. Hence the effect of the random mismatch was underestimated. This is now corrected.

Notice, however, that even the present simulation model is not perfect: On four of the transistors in the transconductors antenna diodes are lacking in the design. According to the UMC documentation missing antenna diodes lead to a larger mismatch. As an example, a 10 µm/1.5 µm NMOS transistor has a 1 σ spread in V_{th} of 1.02 mV with and 2.79 mV without the diode. This larger mismatch of transistors without antenna diodes is not taken into account in the current simulations since the antenna effect can vary. Also, it was assumed in the simulations that LV-PMOS and TW-NMOS transistors have the same mismatch parameters as the normal PMOS and NMOS transistors.

The result is shown in Fig. 4-7: σ = 575 nA, or 6σ = 3.45 µA, for the simulated offset distribution; a value that would explain a small number of short missing codes. Results of the Monte Carlo (transient) simulation of the full DCD channel are also shown in the figure. These results confirm the analytic model mentioned above.

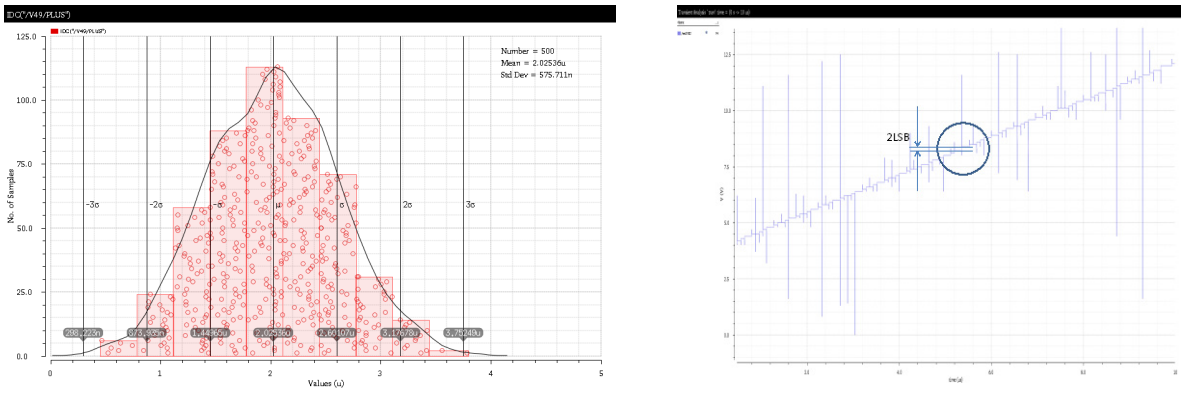

Fig. 4-7 Offset of the comparator – ADC simulation (left) and transient Monte Carlo simulation of the ADC (right). One of the characteristics within 16 iterations shows missing codes.

4.2.2.2. Systematic effects

The facts that missing codes appear mostly at -64, 0, 64, and that very rarely longer missing codes are observed point to additional systematic problems affecting only the comparator in the first stage of the conversion. Candidates for systematic effects are:

- Local voltage drop e.g. the RefIn or VDDA lines can cause an offset adding to the mismatch
- Different transistor orientations in the first stage.
- Missing dummy structures:
    - one of the two transconductors that should match is placed at the edge of the layout. The environment for the edge transistors is different (no dummy structures) which can produce a systematic offset that adds to the mismatch.

Concerning the first point, i.e. the influence of the local RefIn or VDDA voltage drop, a Monte Carlo transient simulation of the DCD channel has been done. The simulated netlist contains the parasitic capacitances and resistances – the extraction of these elements has been done with Quantius QRC tool. No missing codes have been observed (the simulation of limited set of codes and only 6 iterations takes about 50 hours). This is in agreement with the simulation shown in the July review (DCD presentation slide 27) which confirms that only a large RefIn voltage drop of about 600 mV can significantly influence the ADC. The estimated actual local voltage drops (0.3 mV for RefIn and 0.4 mV for VDDA) are much smaller.

The second point would require a redesign of the cell and is considered not to be worthwhile considering the potential risk.

To address the third point is straightforward and will be done by introduction of appropriate dummy structures.

In summary, the comparator offset caused by a combination of random and systematic mismatch can produce missing codes. To minimize these we will

- Add antenna diodes to the critical transistor gates to reduce the random mismatch
- Add dummy structures to transistors at the edge of the comparators of the first stage

Further reduction of the random mismatch by increasing the transistor size would require a substantial change of the layout. For instance, insertion of the large NFB (see Fig. 4-6) current source (the largest source of random mismatch) would blow up the ADC layout, strongly reducing the space for the decoupling capacitors in the channel. This in turn could cause other kinds of problems (e.g. increased noise). The risk for this change therefore is high and the benefit would only be marginal.

4.3. Gain and dynamic range

The gain of the DCD has to be chosen such that pedestal spread can be accommodated and suffcient resolution and noise margin remains for an adequate setting of the threshold.

Using:

Dynamic range of DCD: ΔI_{DCD}

Signal Range: I_{sig} (should cover 3 MIPs)

Corrected pedestal spread: $I_P = \Delta I_{DCD} - I_{sig}$

Raw Pedestal spread before 2-Bit DAC correction: $I_{Praw} = 4\ I_P = 4\ (\Delta I_{DCD} - I_{sig})$

(assuming that the 2-bit DAC is working fine without non-linearity etc)

The expected signal with 6000 e (most probable) charge for one MIP and g_q = 0.5 nA/e a MIP is 3 µA, so

$$I_{sig} = 9\ \mu A$$

The expected initial raw pedestal spread is 35 µA. This is from the measured maximum drain current spread of 28 µA from DC measurements on large final DEPFET matrices and 7 µA due to assumed imperfections of the pedestal subtraction procedure. The required minimal dynamic range of the DCD is

$$\Delta I_{DCD} = 35\ \mu A/4 + 9\ \mu A = 18\ \mu A.$$

Trivially, the lower the gain the higher the dynamic range. However, at some point it will be difficult to set the threshold: as a rule of thumb, the threshold should exceed 5σ of the noise (including some safety for the case of non-Gaussian noise contributions). With an expected noise of 0.8 ADU the threshold is then be above 4 ADU.

The upper limit of the threshold is for efficiency reasons 2000 e (confirmed in simulations and test beam analyses).

A 2nd criterion can be obtained demanding that the spatial resolution obtained using charge sharing does not suffer too much by losing pixels of a cluster. A detailed analysis is shown in the addendum. In summary, also this 2nd criterion leads to the same requirement that the threshold should be below 2000e-.

Setting 4 ADU threshold to 2000 e one gets a LSB of 500 e, or with a g_q of 0.5 nA/e of 0.25 µA. The dynamic range of the ADC is then

$$\Delta I_{DCD\_max} = 64\ \mu A$$

with a maximal raw pedestal spread as large as 220 µA.

So far nominal values of all parameters were used; in practice more conservative values should be chosen: Noise: 1 ADU, Minimal Threshold: 1500 e (at least 5 ADU), Pedestal compression of 2 bit DAC: 3.5 .

Taking this into account, the pedestal spread and S/N for various gain settings are shown in Fig. 4-8, the ADU settings for various thresholds in Fig. 4-9.

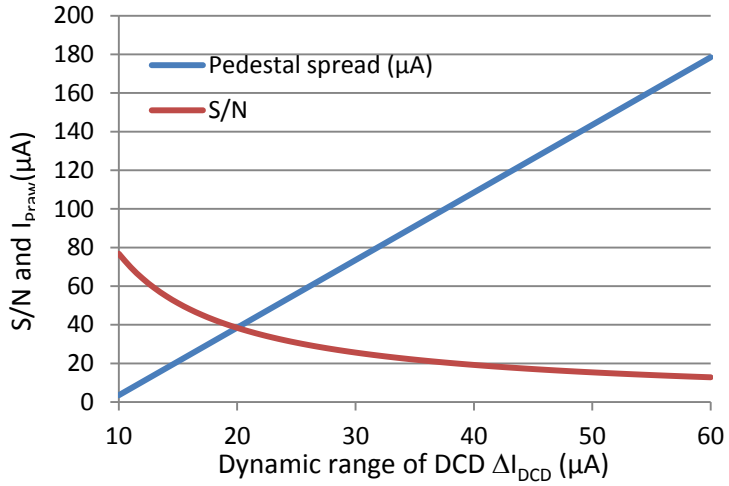

Fig. 4-8 Maximal raw pedestal spread versus dynamic range of the DCD (blue line). The red line indicates the S/N for a MIP.

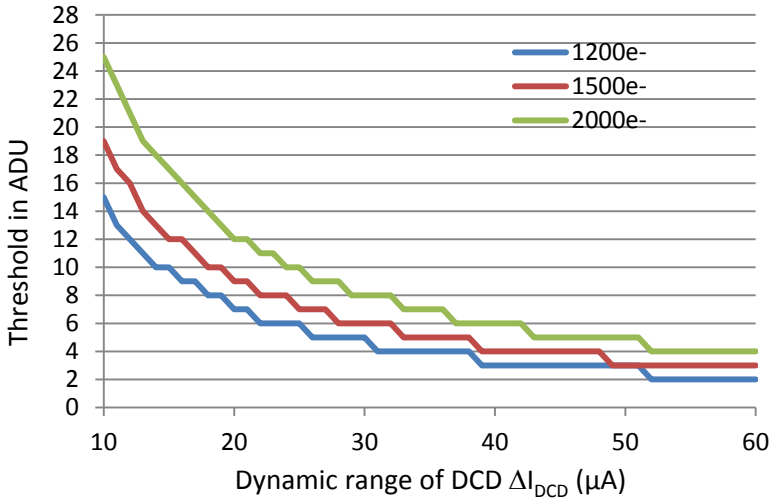

Fig. 4-9 Threshold in ADU versus DCD dynamic range (in µA).

ΔI_{DCD}(µA)	I_{Praw} (µA)	LSB (nA)	S/N	Threshold in ADU for 1200e-	Threshold in ADU for 1500e-	Threshold in ADU for 2000e-
15	21	58	51	10	12	17
22	46	85	35	6	8	11
35	91	137	22	4	5	7

Table 4-3 Proposed gain/dynamic range settings, possible range for the max pedestal spread, resulting value per LSB, expected S/N values, and threshold values in ADU for given signal threshold.

Table 3-1 lists the proposed gain ranges for the new DCD. Three gain ranges are chosen:

- High gain: 58nA/LSB, for calibration purposes and tests with small matrices
- Default gain: 85nA/LSB, for standard operation in the experiment
- Low gain: 137nA/LSB, as safety option; after irradiation or unexpectedly large spread

The proposed changes in the design of the DCD are quite simple and straightforward.

Together with the change of the gain settings, the additional change of the full range for IPDAC (the pedestal current subtraction DAC) is planned. Currently it is 120µA; to make finer adjustments possible, a change to 60µA full range is planned. Also here, the changes in the design are simple and with minimal risk.

4.4. JTAG TCK

The present DCDB4 “samples” the data for the global and “pixel-” (channel-) registers at the falling TCK edge and releases the data at rising edge. This was done deliberately in the first DCD to avoid setup and hold problems between the synthesized JTAG block and the full custom global- and pixel resistors. The scheme has been kept until DCDB4_pipeline for compatibility reasons. The DHP can cope with the sampling at falling edge since it has added the possibility to invert TCK when writing into these registers. The scheme is working well on the test systems (EMCM).

We will change the sampling polarity for the pixel and global register to rising edge and the data output to falling edge to be on line with the industry standard. There is no need for a new synthesis of the digital block - the digital block has been already prepared for the last submission.

4.5. Switcher-B improvements

4.5.1. Rise time of the *Clear* signal

Safe operation of the DEPFET matrix requires almost complete clearing of the internal gate after read-out. A typical voltage for this is expected to be close to 20V including about 20% safety margin. The time for this step of the read-out cycle should be as short as possible to allow a settling of the DEPFET drain current before it is read out by the DCD. With the current DCD scheme, a read-out time of 100ns is planned including a period of about 20ns for the clear pulse after read-out. The *Clear* voltage has to be applied to a distributed RC network with a series resistor of R≈30Ω in and a capacitor of C≈150pF.

The simulation of the current driver scheme in Fig. 4-10 show a rise time of about 15ns at a 150pF load.

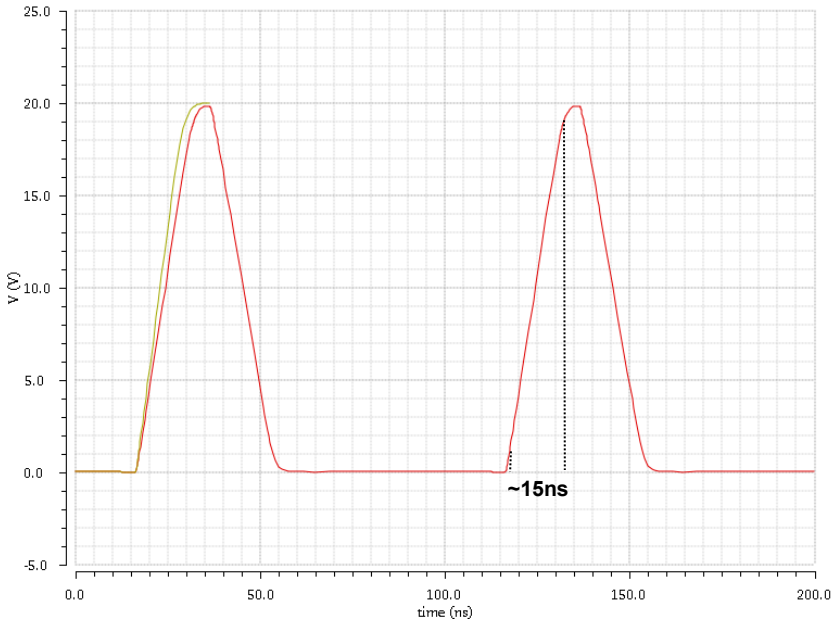

Fig. 4-10 Simulated 20V clear pulse with 150pF load and the present scheme, the rise time is about 15ns.

It is likely that such a pulse width would also be fine for the operation of the PXD. However, to increase the sampling time window and to add some safety for the operation, a faster rise time is desirable.

This can be done by

a. An increase of the on-chip decoupling capacitor by a factor of 2 to provide the current for the large switching transistors
b. An Increase the size of the switch transistor by a factor of 2.

There is space for a second on-chip decoupling and, if the width of the chips is increased by 220µm (14%), also larger transistors can be accommodated. Fig. 4-11 shows the current layout and the space needed for these improvements.

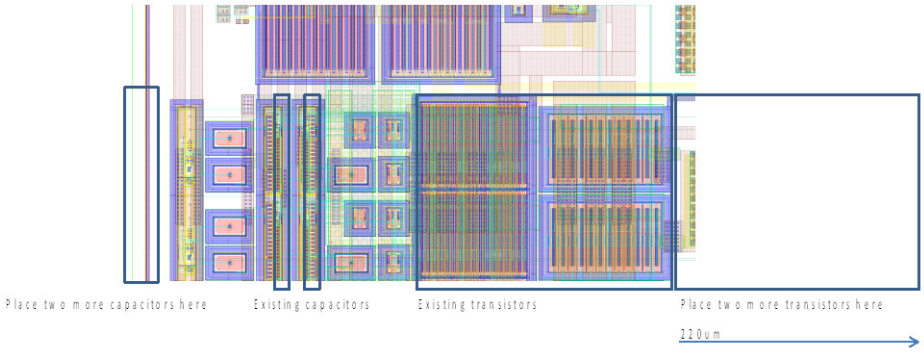

Fig. 4-11 Current layout of the Switcher-B18 V2.0 and the space allocated for rise time improvement.

A simulation of the proposed improvement is shown in Fig. 4-12; the rise time is now about 10ns.

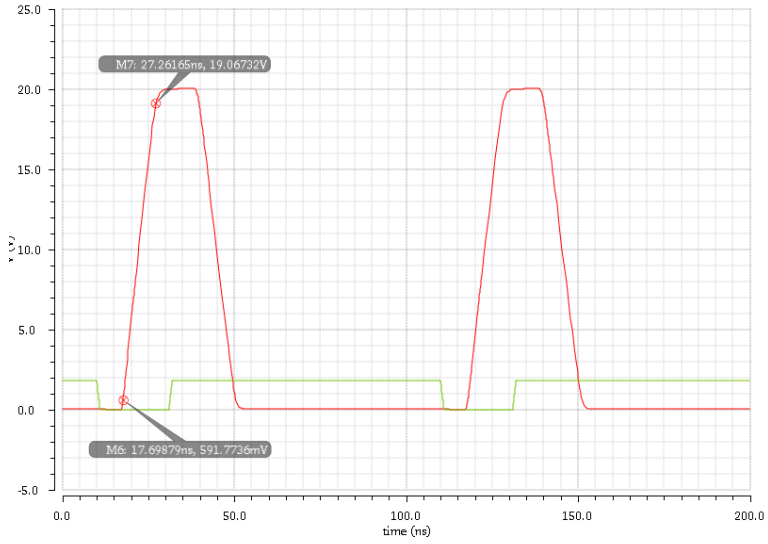

Fig. 4-12 Simulation with the new design.

4.5.1.1. Electro-migration considerations

Neglecting the 30 Ω line resistance on the matrix, a simple calculation yields for C=150 pF, t_{rise}=10 ns, and V_{peak} = 20 V a peak current of I_{peak}=300 mA (bi-directional).

The duty factor is 10 ns/20 µs=5e-4, therefore the mean current is estimated to be 150 µA only.

The calculations for electro-migration effects for arbitrary waveforms are rather complex (see e. g. "*Projecting interconnect electro-migration lifetime for arbitrary current waveforms*", Nathan W. Cheung et al., Dept. of Electr. Eng., California Univ., Berkeley, CA, IEEE Transactions on Electron Devices,

06/1990; 37(5):1343 - 1351. DOI: 10.1109/16.108197). In summary it can be said that for pulsed DC currents the mean time to failure (MTF) scales like

$$MTF_{pulsedDC} = MTF_{DC} / (\text{duty factor})^2$$

For pure AC without DC offset and symmetric wave forms (considering the AC peak currents):

$$MTF_{AC} \approx 1000 \cdot MTF_{DC}$$

The present design of the Switcher-B uses stacks with 32x V5 vias and 800x V4–V2 vias for the connections of the bump bond pads with the large HV-transistors. The large 32xV5 vias can stand a DC current of 67 mA without electro-migration related degradation. The 800x V4-V2 vias can stand a DC current of 224 mA. The weakest point in the series is the 9 µm wide and relatively short M2 line, which can sustain an RMS current of 65 mA.

Together with the fact that electro-migration exponentially depends on the temperature and that the maximum temperature of both the Switchers and the DEPFET matrix is close to room temperature, we conclude that the electro-migration has a minor significance for the safe long-term operation in PXD.

4.5.2. Termination resistor

The present Switcher-B18 V2.0 has the possibility to disconnect or to connect on-chip termination resistors to the LVDS input pads. This feature is controlled for all inputs in parallel with one single configuration bit. In the new switcher version, the serial input should be excluded from the switching scheme; its termination resistor should always be on to allow a safe operation in the chain of six Switchers on the module.

This is an uncritical change that will be implemented.

4.5.3. Bump pads

Due the change of the bumping technology the size of the current LM pad for the bumps has to be changed to allow a low-stress connection between ASIC and substrate.

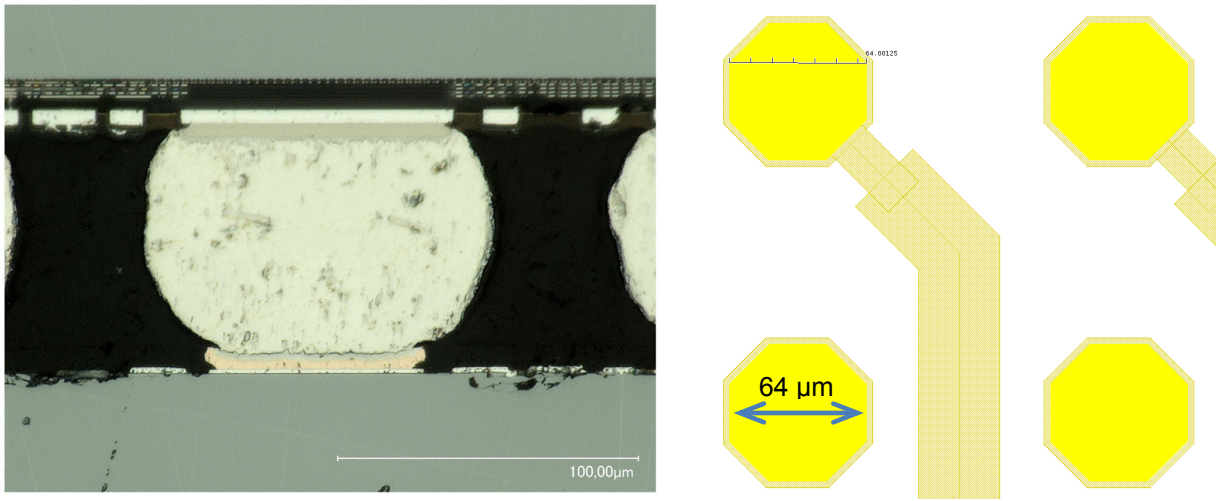

Fig. 4-13 Cross section of the bump bond between Switcher (top) and substrate (bottom) in the left picture. The different UBM diameter on ASIC and substrate generates stress in the interconnection. Ideally both sides have the same diameter of the UBM. The size and shape of the landing pad is depicted on the right.

The diameter of the LM pad for the UBM on the Switcher needs to be re-sized to 64 µm, circular or octagonal.

This is a minor change affecting only the last metal layer and passivation.

5. Summary and submission plans

In the preceding chapter we have presented a detailed discussion of the intended design changes for both the Switcher-B and the DCDB4_pipeline, with the aim to produce their final versions. Both ASICs

need to be submitted in August/September so that they are back for detailed tests by the end of this year (2015). The need for prompt submission is driven by the overall schedule of Belle II, requiring a final beam test at DESY by April of 2016, with these ASICs (and the new DHPT1.1) mounted on the sensors from the pilot run now becoming available. In the DESY test, two full ladders (layer 1 and layer 2, with two modules each) will be installed, together with samples of the four final ladder types of the SVD and arranged in a close-to-experiment geometry. The next step is then the installation of this final sensor arrangement in the commissioning detector for Phase 2 and its installation into Belle II, where first collisions are expected in early summer of 2017. The installation of the complete VXD (PXD + SVD) for physics data taking is planned for the spring 2018.

Intensive tests with the present generation of ASICs (DCDB4_pipeline, Switcher-B18 V2.0, DHPT1.0) mounted on the pilot run sensors will start in September 2015 and will be completed by the end of November 2015. These tests are mainly conducted to verify the metallization scheme of the sensor and to give “green light” for the start of the last metallization steps (and thinning) for the main sensor production. While at the moment we do not see any problems for the operation of the large matrix with the new ASIC generation, issues may come up during the final beam (laboratory) tests. In that case (mid 2016) there is still time, although getting very tight, for yet another submission before the actual assembly of the VXD.

Still, it is definitely much too risky to wait with the submission and hope to see the “new” problems using the present generation of ASICs with their known issues, mounted on the precious sensors, rendering them unusable for the commissioning detector. A submission now for the ASICs is therefore mandatory.

Based on the tests conducted (Chapter 3) and the simulations and analyses presented (Chapter 4) we conclude that the deficiencies of the present generation of ASICs are understood and the proposed changes (“Switcher-B18 V2.1”, “DCDB4.1”) are well motivated (the changes for the DHPT were already agreed upon during the last ASIC review in July 2015). The changes we propose are in all cases of minimal risk, no new syntheses of the digital blocks are required beyond those already prepared for the last submission.

Specifically, for the Switcher-B we will

- decrease the rise time of the CLEAR pulse from 20 ns to 10 ns in order to widen the sampling time window for safer operation,
- exclude the serial input from the switching scheme for safer operation (the scheme disconnects or connects the termination resistors to the LVDS input pads),
- and change the size of the current LM pads for the bumps to allow a low-stress connection between ASIC and substrate (this is required by a change in the bumping technology to ENIG/SAC305).

For the DCDB we will

- support the safe communication between DCD and DHPT by an increase of the DCD output strength, making the increase switchable by adding a switch and a resistor for the bias boost at the DCD output,
- mitigate the “missing code” feature by adding antenna diodes to the critical transistors in the transconductor,
- adding dummy structures to the transistors at the edge of the comparators of the first stage, which is also suited to reduce the mismatch between the transistors, causing “missing codes”,
- optimize the gain and the dynamic range of the DCD by changing the various resistances concerned, taking into account conservative estimates of the required physical performance,
- and change the sampling polarity for the pixel and global JTAG registers to rising edge and the data output to falling edge to be in line with the industry standard.

For the Switcher-B we will submit to a conventional Multi Project Wafer (MPW) run, for which the date is already fixed and must be kept: Aug 24, 2015. It is guaranteed to have the changes proposed above ready by this time.

For the DCDB we have two possibilities in principle: an MPW run and an Engineering Run (ER). According to our inquiries, the ER, contrary to the MPW, can be submitted until the end of September, with the ASICs still delivered before the end of the year. Although the changes proposed for the DCDB4.1 are of limited complexity, the gain in time (one more month) for the ER seems advantageous for a thorough cross-check of the implementations. In addition, the ER wafers will be delivered fully bumped so that the individual ASICs can be tested much more conveniently on the wafer (no need for proper alignment of the individual ASICs as in the case of the MPW run). Since the cost is about the same for the MPW and the ER (sharing of cost with two other projects of similar nature), it was decided to go for an ER and submit by the end of September 2015, in time with the required schedule for delivery.

6. Addendum

The supporting documents are available at the indico page of the July review:

https://indico.mpp.mpg.de/conferenceDisplay.py?confId=3736

A1: DCDB4_pipeline Reference Manual
A2: Switcher-B18 v2.0 Reference Manual
A3: Summary of the DCDB2 characterization at Bonn
A4: Summary of delay scans on EMCMs
A5: On pedestal spread and gain ranges
A6: Latest DCDB simulations (Ivan's original document)