Characterization DCDBv2

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Introduction: In this document the main results of the characterization of the DCDBv2 will be reported. These results were already reported in the DEPFET Collaboration meetings in Wetzlar (Feb 2013), DESY (Nov 2013) and Kloster Seeon (June 2014 and May 2015). Please, refer to those slides for more details.

The first important thing to notice is that the former version of the DCDB chip (DCDBv2) described here was tested in platforms that allowed access to the inner half of the DCD channels only. As a reminder, the DCDBv2 used a cyclic ADC architecture instead of the current pipelined option. The operation of the chip was done at nominal speed 320 MHz, and small noise increase was observed with respect to its operation at 100 MHz. Some channels showed DNL issues (missing codes) which origin, at that point in time, was not identified although several options were discussed: biasing problems, comparator threshold issues, voltage drops… As an example of a 'bad' channel having all the features we also see in the DCDBPipeline, see figure 1:

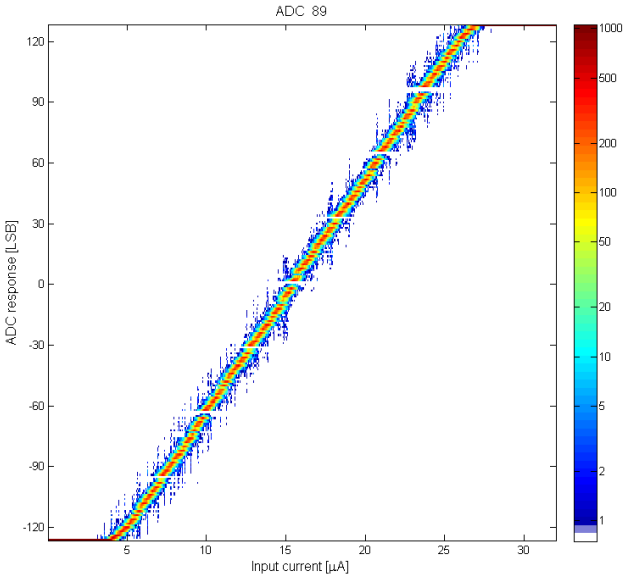

Figure 1: Example of a problematic ADC curve in one bad example

It should be noticed that this is a particularly very bad example and most of the issues seen in this plot can be cured by using proper settings.

Analog Power: For the optimization on analog power, RefIn was scanned between 0.9 V and 1.3 V, while for AmpLow the range was between 0.15 V and 0.55 V. For optimization, one bad and two good channels were investigated in detail. The quality indicator we used for optimization was the linearity of the linear fit of the ADC transfer curve between ±115 LSB (usable part of the dynamic range). The χ^2 of the linear fit of each ADC transfer curve was plotted versus the different investigated voltages (see figure 2), and the region where a common χ^2 minimum was identified for the three channels was taken as *optimal*. Finding optimal values for all the accessible channels was not always possible since different ADCs showed different results.

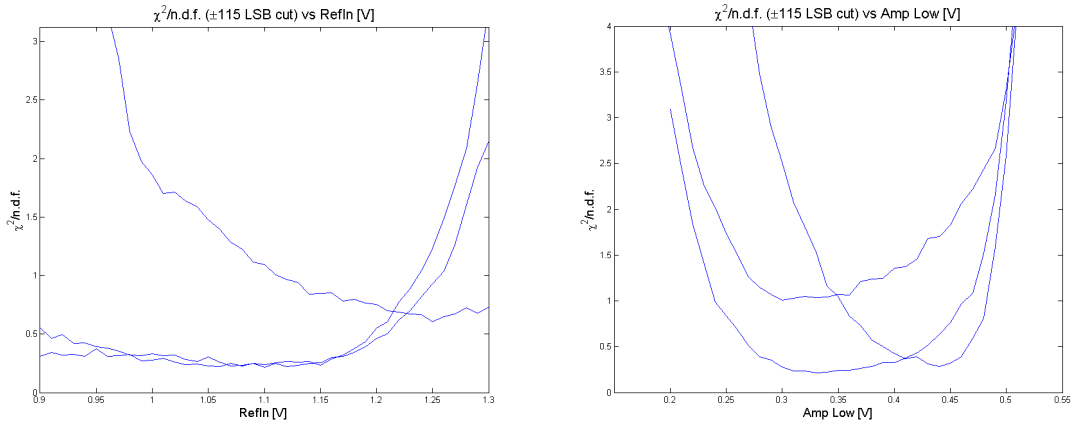

Figure 2: RefIn and AmpLow scans on three representative channels

Additionally a voltage sweep around central values for RefIn (RefIn at 1.05 V, 1.1 V and 1.15 V) versus AmpLow (AmpLow at 0.4 V, 0.35 V and 0.3 V) for all the channels was performed (see figure 3). The mapping corresponds to the physical position on the DCDB and especially for certain voltage configurations, a trend suggesting some voltage gradient is somehow observed:

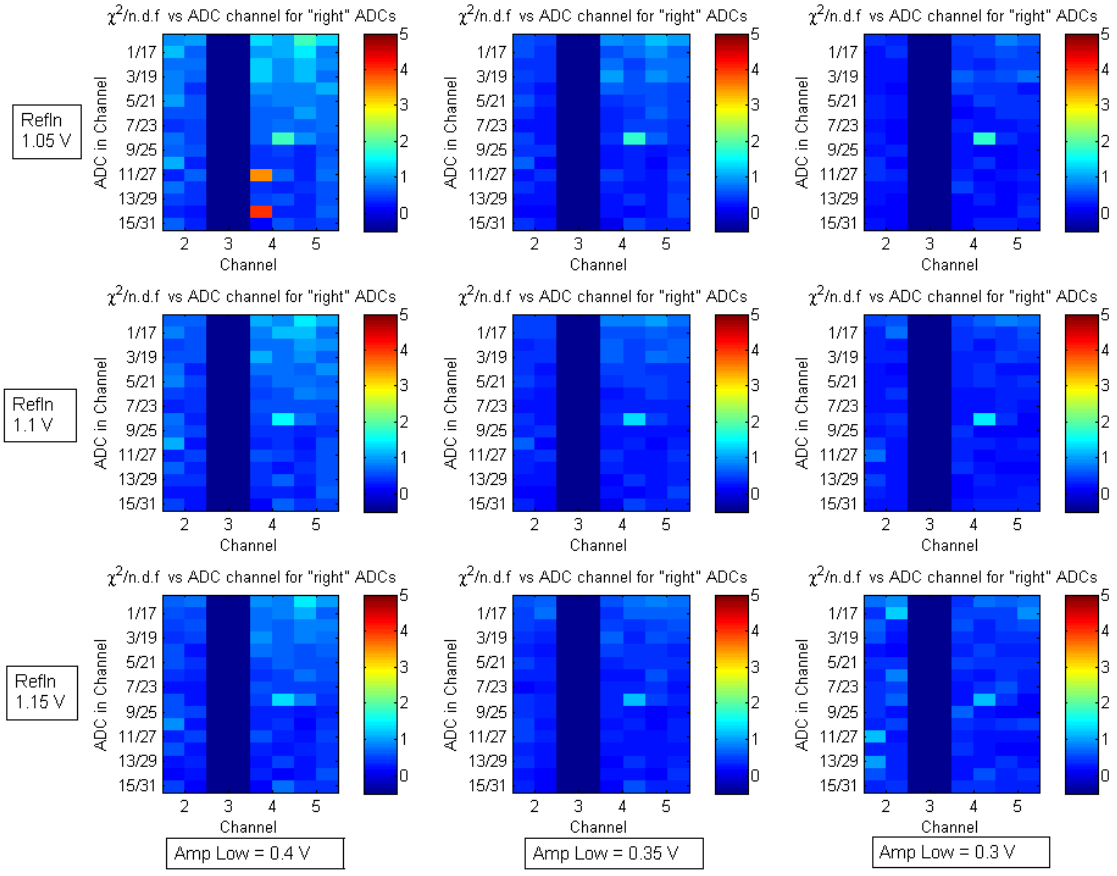

Figure 3: RefIn and AmpLow sweep for all the DCD channels

DACs: Out of the total DACs available inside the DCD, the ones expected to have a more pronounced impact in the DCD performance were investigated: IPSource, IPSource2, IFBRef, IFBNCasc, IFBPBias.

IFBRef vs IFBNCasc: IFBRef was scanned between 54 and 74, while IFBNCasc was scanned between 0 and 20. Although these parameters are involved in the comparator bias, no big influence in the performance is observed and default values were chosen (IFBNCasc=0, IFBRef=64).

IFBPBias: This DAC was scanned between 90 and 110. IFBPBias is the bias voltage for the comparator in the ADC and also no noticeable variation was observed. Therefore, also the default value of 100 was chosen in this case.

IPSource vs IPSource2: These two DACs are important for setting the LSB width. IPSource was scanned between 95 and 115 while IPSouce2 was varied between 90 and 110. The results of the scan for three different channels are shown in figure 4:

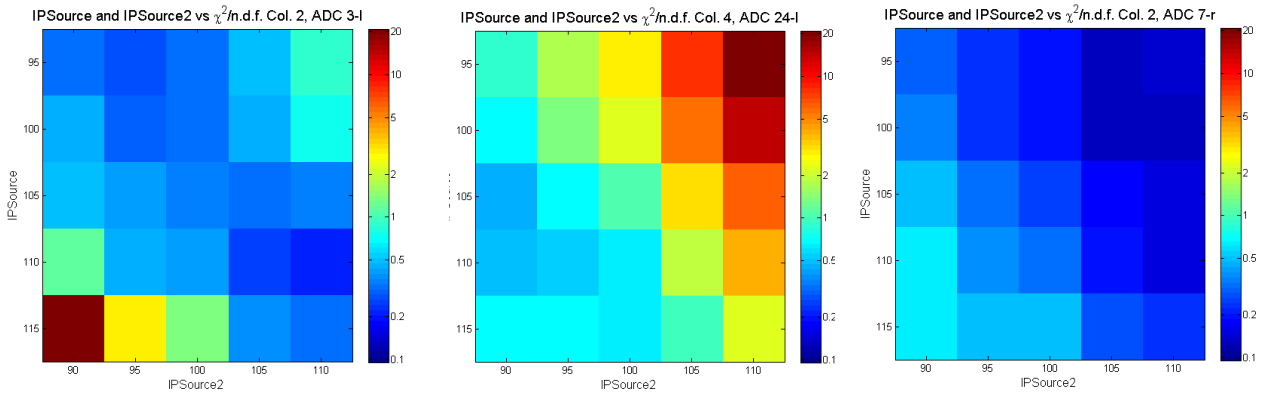

Figure 4: IPSource and IPSource2 scan for three representative channels

It is clear that the right combination of these two values is crucial to get good performance. From the previous plots is visible that both parameters should be very similar and therefore IPSource was set to 110 and IPSource 2 to 95.

Sampling Point: In the following, the result of the DCD dynamic measurements (at 100 MHz) is shown (figure 5), demonstrating that on short matrices the settling time seemed to be long enough. It was observed that better performance was achieved (reduced overshoots) with enabling capacitances in the TIA feedback loop (EnCap). On top, a dip was observed right before the clear (precisely at the sampling point) and the plateau (indicating drain current settlement) was never flat. Overlapping gates and sampling point at full speed were never done.

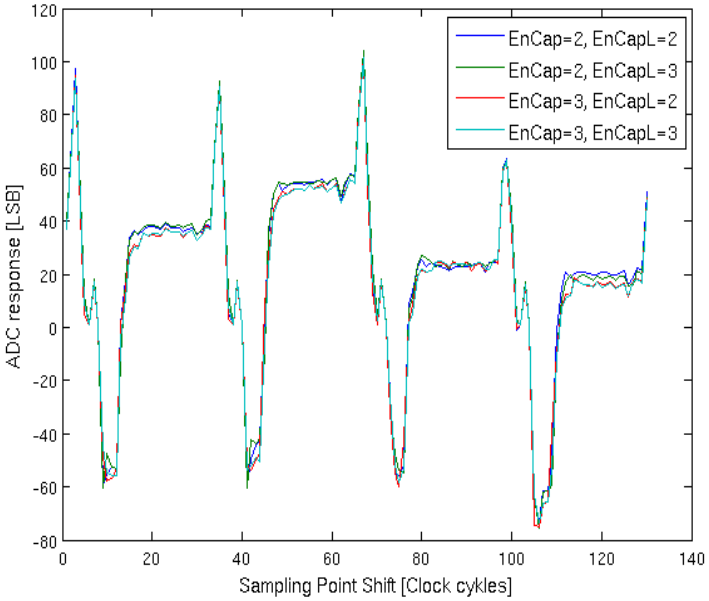

Figure 5: Sampling point investigations

Irradiations: Irradiations of the DCDBv2 assembled on a Hybrid 4.1 (no matrix attached) were done with 60 keV X-rays. After each irradiation step (0.5 Mrad, 1.0 Mrad, 2.0 Mrad, 3.5 Mrad, 6.0 Mrad, 10 Mrad, 20 Mrad), the chip was characterized before and after annealing (100 minutes at 80 °C). The object of investigation were 4 ADCs and, for them, the transfer curves were extracted for different bias voltages and DAC settings. Figures investigated (see figure 6 for the pre-irradiation): INL, gain, offset, χ^2, maximum noise and dynamic range.

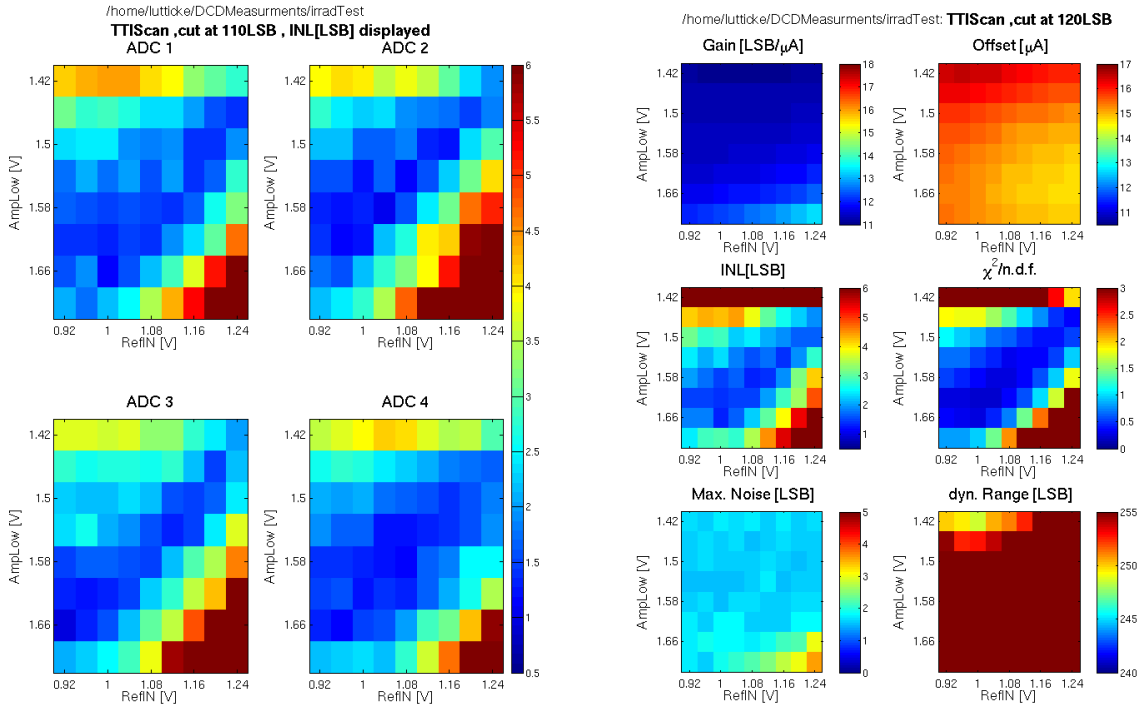

Figure 6: Pre-irradiation characterization

The most critical region was found between 2 Mrad and 3.5 Mrad TID, where it was even impossible to switch off the analog part of the chip (as an example, see the figure 7) and the power consumption on VDDD was very high. After 10 Mrad, the chip was again fully operational and at the end of the irradiation period no degradation was observed compared with the initial performance. The temperature of the chip was not known (only air cooling) and the power consumption decreased over time (additional self-annealing?).

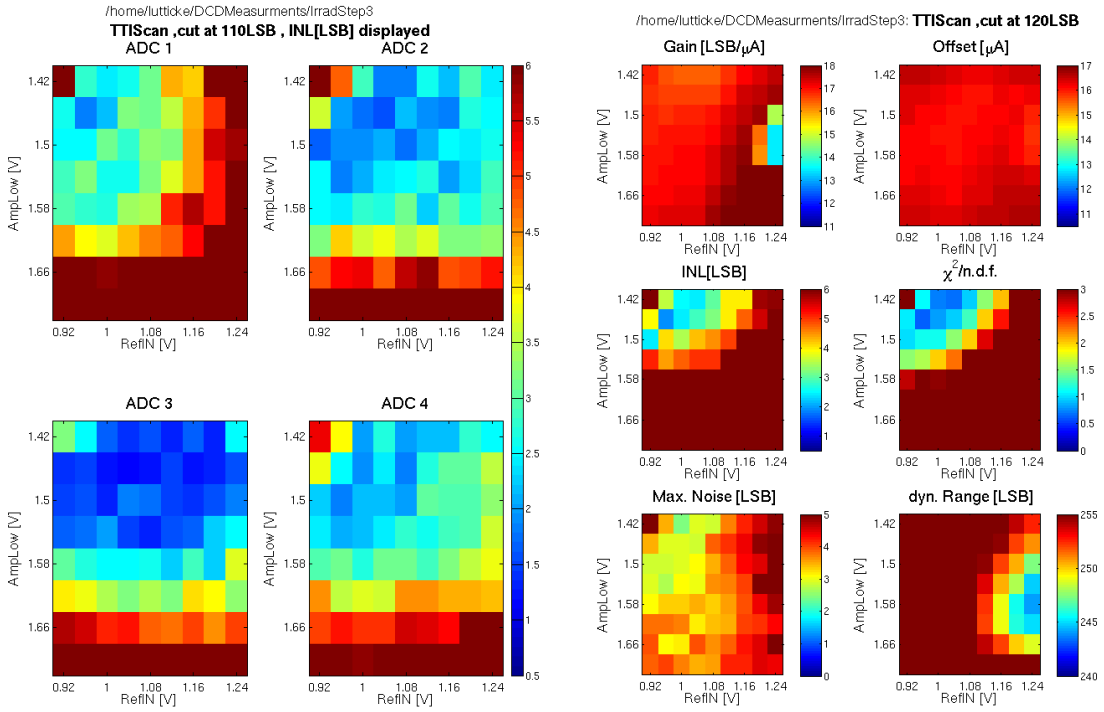

Figure 7: Characterization after 2 Mrad TID

Temperature dependence: After irradiation, the DCDB was also characterized inside the climate chamber between -30 °C and + 30 °C, in steps of 10 °C. In all these temperatures scanned it was possible to find a wide operational window where the chip performed well. It has been also observed that the current consumption changes with temperature 5% decrease every 5 °C (250 mA in VDDA at -30 °C).

Offset DAC Operation:

The DCDB features an offset current compensation, which shall reduce the spread of the incoming current. This compensation consists of one dynamically switchable 2-bit DAC in each drain line. The data for this is streamed from the outside into the DCDB over 8 2-bit links, operating at 320 MHz. The amount of

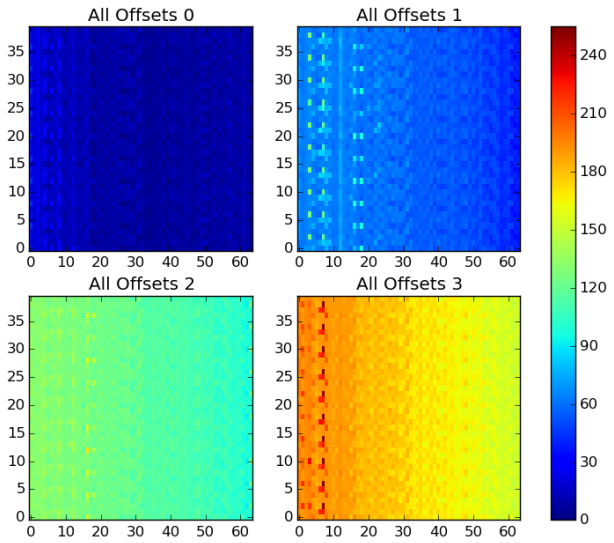

Figure 8: Offset current sources switched to constant values. The 2-bit Offset DACs show a different strength, depending on the drain line.

current one LSB of the 2-bit DAC corresponds to, can be set via the 7-bit IPDAC . The strength of the 2-bit DACs is very high, the IPDAC value of 28 of 127 is strong enough to move the input current from below the dynamic range, to above the dynamic range, even if the 2-bit current cell is set to the value one. In addition to that, the 7-bit DACs used in the DCDB2 have a nonmatching LSB, so that the DAC effectively loses one bit accuracy.

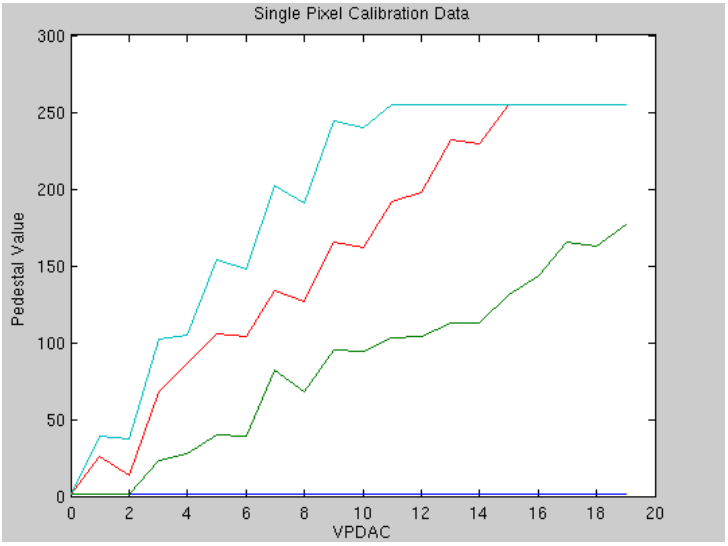

Figure 9: Offset 2-bit DAC strength of a single ADC for different IPDAC values. DAC Value 1 in green, DAC Value 2 in red, DAV value 3 in

Care needs to be taken for the TIA settings. If the settings are not correct, the setting of the 2 bit DAC influences both the current and the next digitization cycle.

With the system as is, one can compress pedestals to around a third of their value (if the spread is big enough to begin with), with a better chosen strength for the Offset DACs, compression factor around 3.5 seem feasible

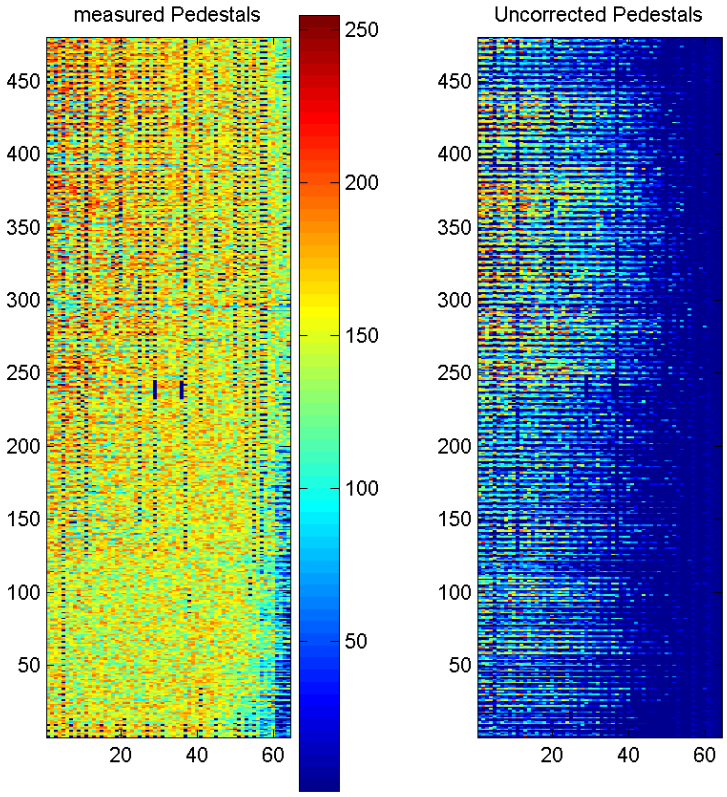

Figure 10: Pedestal compression on a large PXD6 matrix with DCDBv2 and DHPT0.2 Uncompressed, part of the pixel is out of the dynamic range.