Schaltungstechnik
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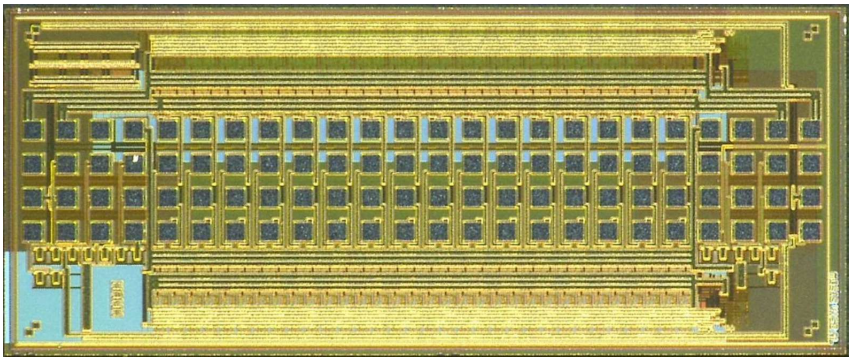

SwitcherB18 (Gated Mode)
Reference Manual

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for chip version 2.0
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Revision History

version	date	author	change
1.0	08.10.2010	C. Kreidl	initial version
1.1	05.11.2010	C. Kreidl	fixed column mismatch in location of clear and gate outputs in table 1.5.
2.0	23.11.2011	L. Raffelt	added information for new SwitcherB18
3.0	26.10.2012	C. Kreidl	new document: SwitcherB18 v2.0 (Gated Mode)
3.1	29.10.2012	C. Kreidl	fixed typo, updated table 4.3
3.2	17.02.2014	C. Kreidl	fix: only 100Ω term. resistors available
3.3	10.10.2014	C. Kreidl	- replaced remaining `VDDJT` occurances with `VDDD` for JTAG i/o voltage - updated chip dimensions in figure 1.1 and table 1.2. Added top metal string.
3.4	15.10.2014	C. Kreidl	- added inverter to mux input '1' in figure 3.1 - replaced inverter by buffer in figure 3.2 - added irradiation results

Contents

1 Overview

The Switcher-B18 chip is used in the Belle-II Pixel Vertex Detector to control the rows of a DEPFET sensor matrix. Every row requires a negative going `Gate` signal to activate a row for readout and a positive going `Clear` signal to remove charges from the internal gate of the DEPFET devices. The Switcher-B18 chips are located on the narrow 'balcony' at the side of the module.

Each chip has 32 channels. Each channel contains two high voltage switches used for the `Clear` and `Gate` outputs. The outputs switch between upper (`CHi`, `GHi`) and lower voltages (`CLo`, `GLo`), respectively. The digital part is supplied by an additional 'floating' 1.8 V supply (`GNDD`, `VDDD`) which must be within the 'high voltage' supplies (see 1.3).
Channels are activated one after each other by means of a shift register which is running along the channels. It is fed with a single '1' externally through its serial input. This '1' is clocked through the channels. The HV switches are activated for the selected channel by fast `Strobe` signals (see 3.1). Using different `Strobe` timings, the `Gate` outputs can be operated in non-overlapping, overlapping, skip or gated mode. In gated mode are all clear outputs enabled to dump noise in the detector while shielding the internal gate. The clear outputs are switched on in four groups to limit inrush currents.
Several chips can be daisy chained by connecting the serial output to the serial input of the next chip. The chip is bump bonded to the sensor. Slow control is via JTAG, fast timing is provided by a few differential control signals. It features a power saving circuit which switches the power consuming levelshifters of an output row from sleep mode into boost mode prior the row is selected and switches them back after selecting the next row.

The chip is the successor of Switcher-B18v1 and contains additional logic for gated mode operation. The changes are summarised in chapter 6.

1.1 Physical Dimensions

The physical dimensions of the chip as designed and as measured on a cut die are listed in table 1.2.

The bumpbond pads are rectangular shape, their parameter are shown in table 1.4.

	designed	measured
x	1470μm	1530μm
y	3627μm	3660μm

Table 1.2: Chip Size

Size	80x80μm^2
Pitch x	150μm
Pitch y	150μm

Table 1.4: Bumppad Parameter

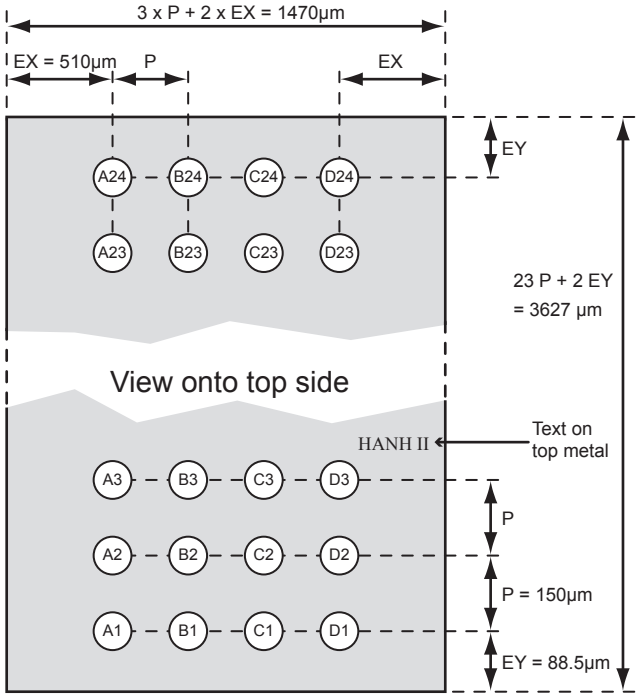

Figure 1.1: Geometry of the Switcher-B18 chip, seen from the top (circuit) side.

Figure 1.1 shows the geometry of the chip. The bump pads are arranged on a regular 4×24 grid with a pitch of $P = 150\mu m$. The figure also shows the numbering of the pads as seen from the circuit side. When flipping the chip upside down onto a substrate, the image must be mirrored! The text '`HANH II`' written on the top metal layer is visible with an microscope.

The lower 4×4 pads and the upper 4×4 pads are used for IO, the central 4×16 pads are the outputs. The location of the various signals is given in table 1.5. The pins are assigned such that every second pad on the outer rim must be contacted during probe station testing.

1.2 Pad Description

Table 1.5 lists all chip pins, their location and function. The exact geometric location of the pads is shown in Fig. 1.1, the arrangement of the upper and lower IO blocks is shown in Fig. 1.2.

A monitor pad is foreseen, but not connected in this chip revision. This signal will not be used during normal operation and is for debugging and probe station testing only.

Name	Location	i/o-family	description
`VDDD`	B1,B24	Supply	1.8 V Digital Supply (2 pads)
`GNDD`	C1,C24	Supply	Digital Ground (2 pads)
`CHi`	A1,A24	Supply	`Clear` high supply (2 pads)
`CLo`	A2,A23	Supply	`Clear` low supply (2 pads)

Name	Location	i/o-family	description
GHi	A3,A22	Supply	Gate high supply (2 pads)
GLo	A4,A21	Supply	Gate low supply (2 pads)
TRSTB	D23	CMOS In	JTAG reset (activ low), $50k\Omega$ pull-up
TCK	D4	CMOS In	JTAG clock
TMS	D3	CMOS In	JTAG mode select
TDI	D1	CMOS In	JTAG data input
TDO	D24	CMOS Out	JTAG data output
no connect	D2		not used any more. was VDDJT. Pad is unconnected.
CLK P/N	B22,C22	LVDS In	Shift register clock
SERIN P/N	B2,C2	LVDS In	Shift register serial input
SEROUT P/N	B23,C23	LVDS Out	Shift register serial output
StrG P/N	B3,C3	LVDS In	Strobe for Gate channels
StrC P/N	B4,C4	LVDS In	Strobe for Clear channels
Vsource	C21	Supply	Reserved for onchip decoupling capacitors of Clear and Gate voltages to Vsource. Not implemented! Pad is unconnected.
sub	D21	Supply	Chip substrate, connect to lowest supply voltage.
Monitor	D22		Not implemented! Pad is unconnected.
Vref	B21	Supply	Reference voltage (1.8 V) input for level shifters.
Clear⟨0⟩	A5	Analog Out	Clear switch output, 1^{st} channel
Gate⟨0⟩	B5	Analog Out	Gate switch output, 1^{st} channel
Clear⟨1⟩	D5	Analog Out	Clear switch output, 2^{nd} channel
Gate⟨1⟩	C5	Analog Out	Gate switch output, 2^{nd} channel
Clear⟨31⟩	D20	Analog Out	Clear switch output, last channel
Gate⟨31⟩	C20	Analog Out	Gate switch output, last channel

Table 1.5: I/O-Description and Pad Names

1.3 Power Supply

The Switcher-B18 needs a 1.8 V supply for the digital part and 4 voltages for Gate and Clear referred to as 'analog' supply voltages. Connect sub to the lowest of all supply voltages. The highest analog voltage must not exeed 50 V relative to sub. The voltage difference between analog high and low must not exceed 20 V! The pad i/o voltage is VDDD. A reference voltage is needed for the build-in regulators which needs to be 1.8 V above sub potential. The GHi and CHi voltages need to be at least $5V$ higher then GLo and CLo respectively. See also figure 1.3 showing the floating voltages.

NOTE: Apply a current limit on the power supplies, to protect against damages due to high currents.

The given current limits in table 1.6 are suggested values. For Gate and Clear you should apply a limit

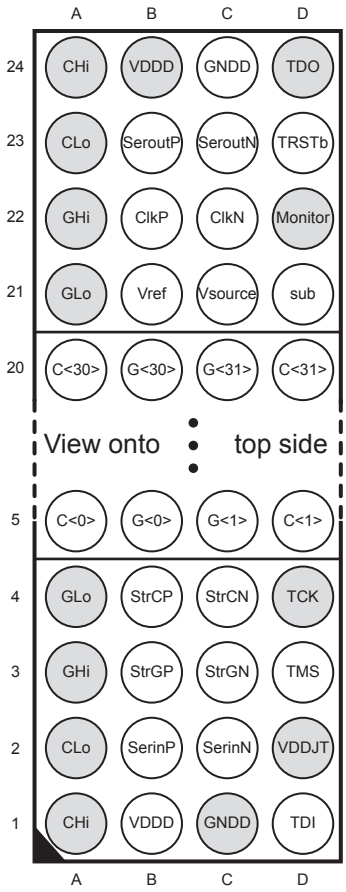

Figure 1.2: Location of the signals in the upper and lower part of the chip. The pads required for probing are marked darker.

slightly higher than the expected current consumption for the load capacitance and clock frequency of your application. The expected values are shown in chapter 4 on page 19.

net	voltage	current limit
VDDD	$1.8V$	$10mA$
sub	$0V$	$1mA$
Vref	sub $+ 1.8V$	$1mA$
Clear	$\leq 50V$	$\approx 30mA$
Gate	$\leq 50V$	$\approx 30mA$

Table 1.6: Power Supply Voltages and Current Limits

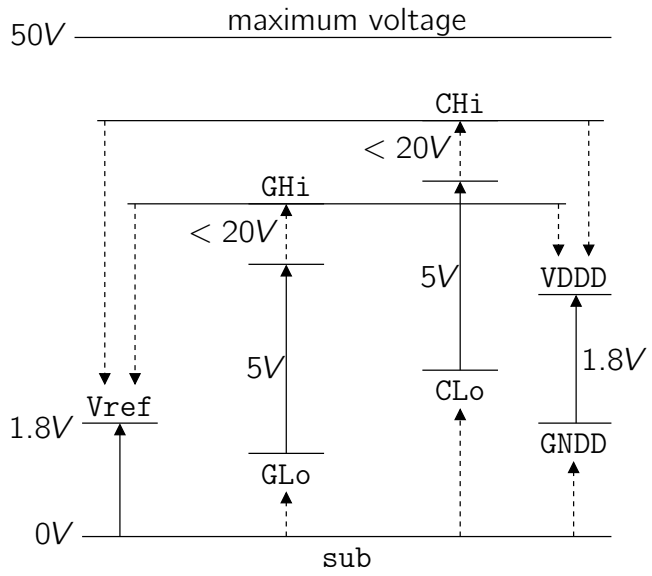

Figure 1.3: Floating Supplies Voltage Ranges

1.3.1 Power Up Sequence

When powering up, it is essential to follow the power-up sequence given here. Otherwise the chip may be damaged because of high currents, if no current limit is applied!
The shift register, which enables the output rows, may contain multiple 1's. These 1's wake up the channels, including it's predecessor and successor, from their sleep mode and cause high static current consumption in the level shifters.

NOTE: Always apply a current limit on the power supplies!

1. switch on the digital supply voltage
2. clear the shift register (fill with 0's)
3. switch on the analog supply voltages
4. start operation

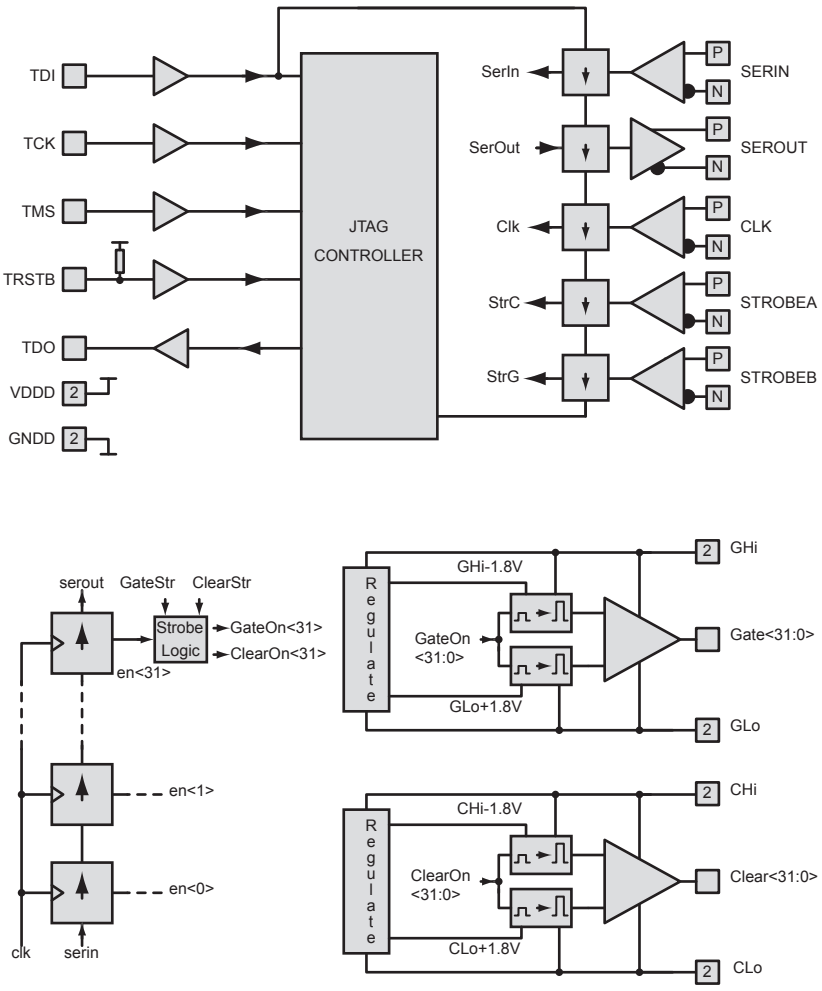

Figure 1.4: Blockdiagram Toplevel

1.4 Block Diagram

Figure 1.4 shows the toplevel blockdiagram of the Switcher and the major connectivity between the blocks.

1.5 Digital Input / Output Pins

The *CMOS input pads* used for JTAG are operated from the VDDD supply. The input threshold is designed to be at half the supply voltage. The pad has protection diodes to VDDD and GNDD. The *CMOS output pad* for JTAG generates levels of GNDD and VDDD. Protection Diodes are to VDDD and GNDD.

The *LVDS input pads* is supplied by GNDD and VDDD and has protections to these voltages. Internal termination resistors of $\approx 100\Omega$ are available in this chip revision. They have to be enabled by JTAG configuration. The *LVDS output pad* is supplied from GNDD, VDDD and has protections to GNDD and VDDD.

2 JTAG Interface

The JTAG interface is designed to be compatible to the IEEE 1149 standard. The JTAG CMOS input pads TRSTB, TCK, TMS, TMS, TDI and the CMOS output pad TDO are operated from the supply VDDD. The reset signal TRSTB keeps the JTAG state machine asynchronously in an inactive state an can be used to prevent any SEU during operation. Contrarily to the JTAG standard the TDI and TMS input pins have no pullup resistors and the TDO has no high impedance state!

TRSTB asynchronously reset

TCK clock

TMS mode select

TDI data input, LSB first

TDO data output

The JTAG controller implements the following registers:

1. The required instruction register (IR) with a length of 3 bit. In the CAPTURE-IR state, it is loaded with the constant test value 3'b101.
2. The 1 bit long *Bypass Register* required by the standard. It is selected by IR = 3'b111.
3. A 32 bit long *ID Register* selected by IR = 3'b010. The hard coded ID must still be fixed, keeping in mind that the LSB must be set to 1. A chip pin could be introduced into the ID word for debugging.
4. A $8 \times 3 = 24$ bit long *User Register*, accessed by IR = 3'b011. Every stored bit is triplicated for SEU tolerance and the majority vote is used internally. The User Register can be read back to check for the occurrence of SEU.
5. The 5 bit long *Boundary Scan Chain* accessible via IR = 3'000 (EXTTEST mode) or IR = 3'001 (SAMPLE/PRELOAD mode)

2.1 Instruction Register

The commands in the instruction register IR are summarized in table 2.1.

IR Value	Function	Comment
000	EXTEST	IO pins controlled by Boundary Scan Chain
001	SAMPLE/PRELOAD	sample pin state, R/W Boundary Scan Chain
010	IDREG	read 32 bit ID
011	USERREG	R/W user register
111	BYPASS	TDI passed to TDO with one clock delay

Table 2.1: Codes of instruction register (IR)

2.2 User Register

The short *User Register* contains some control bits to set some bias DACs. Every bit must be written three times in a sequence, so that a majority voter can produce a SEU tolerant information. SEUs can be detected by reading back the register. The usage of the bits is summarized in table 2.2. The LSB, bit 0, is the first bit clocked in and the first to come out.

Bits	Name	Function
2:0	Termination	activate the termination resistors on the LVDS inputs
5:3	IBias ⟨1⟩	Bias current for level shifter in sleep state, high bit
8:6	IBias ⟨0⟩	Bias current for level shifter in sleep state, low bit
11:9	IBiasBoost ⟨1⟩	Bias current for level shifter in boost state, high bit
14:12	IBiasBoost ⟨0⟩	Bias current for level shifter in boost state, low bit
47:15	Reserved	Reserved for future use

Table 2.2: User Register contents.

The bias currents can be set using a 2bit DAC which uses PMOS transistors with 11 for the slowest and 00 for the fastest setting.

2.3 Boundary Scan Chain

The Boundary Scan Chain (BSC) is used to access all non-JTAG digital pads, i.e. SERIN, SEROUT, CLK and the strobes StrC and StrG. Each pad has one scan flipflop which can be used to sample the pin state (in modes EXTTEST or SAMPLE/PRELOAD) or to drive a signal onto the pin (in mode EXTTEST), as specified by the JTAG standard. The order of the bits is listed in table 2.3. Bit 0 is the bit which comes out first / which is written first.

Bit	Pad
0	StrG
1	StrC
2	CLK
3	SEROUT
4	SERIN

Table 2.3: Bit order in Boundary Scan Chain.

2.4 ID Register

The 32 bit long *ID Register* contains a constant value. It is not a serial number! The LSB, bit 0, is the first bit to be shifted out.

IDREG[31:0]=0x23456789 (hex)

3 Operation

3.1 Strobe Operation

Depending on the relative position of StrG to CLK three different strobe modes can be used:

overlapping the gate signal of the next row is enabled before the current row is switched off

non-overlapping the gate signals of neighbor rows don't overlap

skip rows can be skipped. Their output state doesn't change

gated mode All clear outputs are switched on (high voltage level) and all gate outputs are switched off (high voltage level).

gated mode read-out The channels are cycled through for read-out without clearing. All other channels are in the gated mode.

Figure 3.1 shows the channel logic controlling the internal Gate enable signal and the boost signal, which switches the levelshifter from low power sleep mode to the fast boost mode. The logic to enable the gated mode operation is shown in figure 3.2. It enables the gated mode sequencially in groups of 8 channels to limit the current on the CHi supply lines and avoid damages to the chip.

The figures 3.3, 3.4 and 3.5 show the strobe operation modes. The signals $\texttt{En}\langle 0\rangle$ and $\texttt{En}\langle 1\rangle$ show the internal enable signal which switches a row to boost mode and makes it sensitive to the StrG signal.

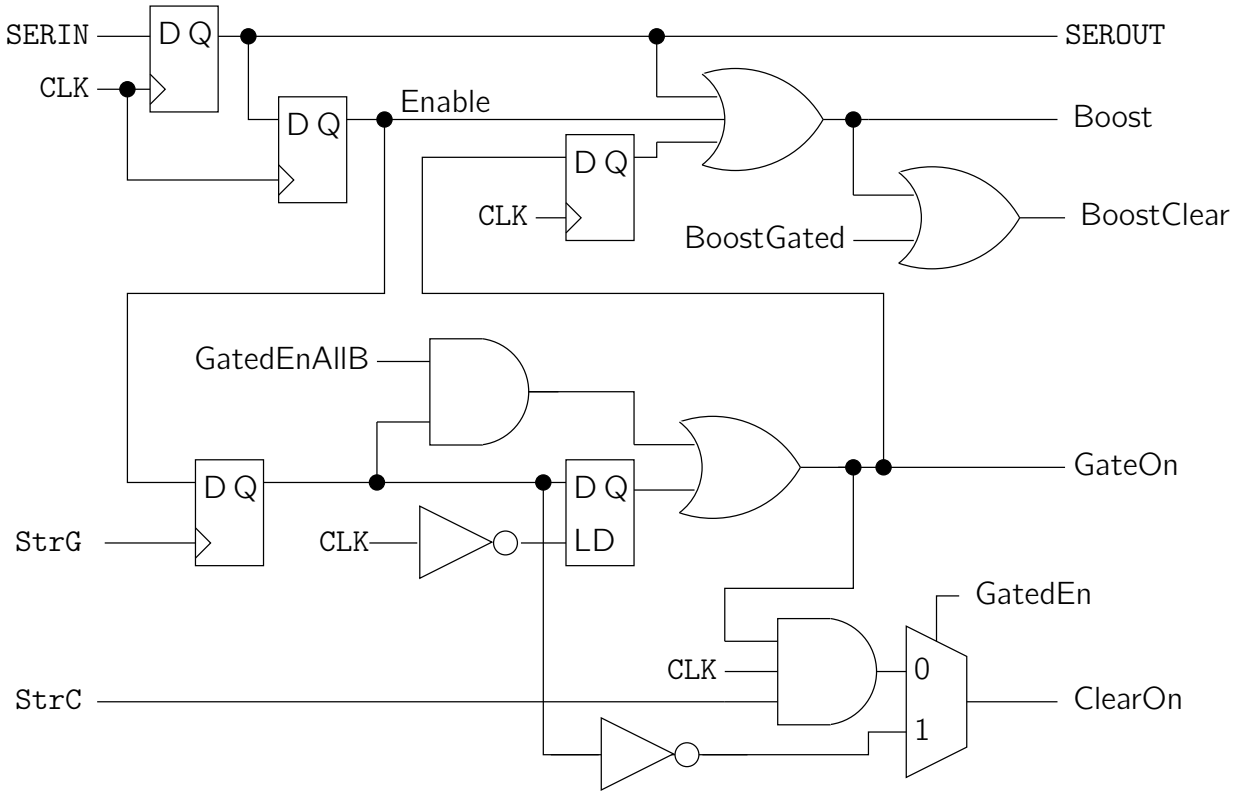

Figure 3.1: Schematic of the strobe logic of one channel.

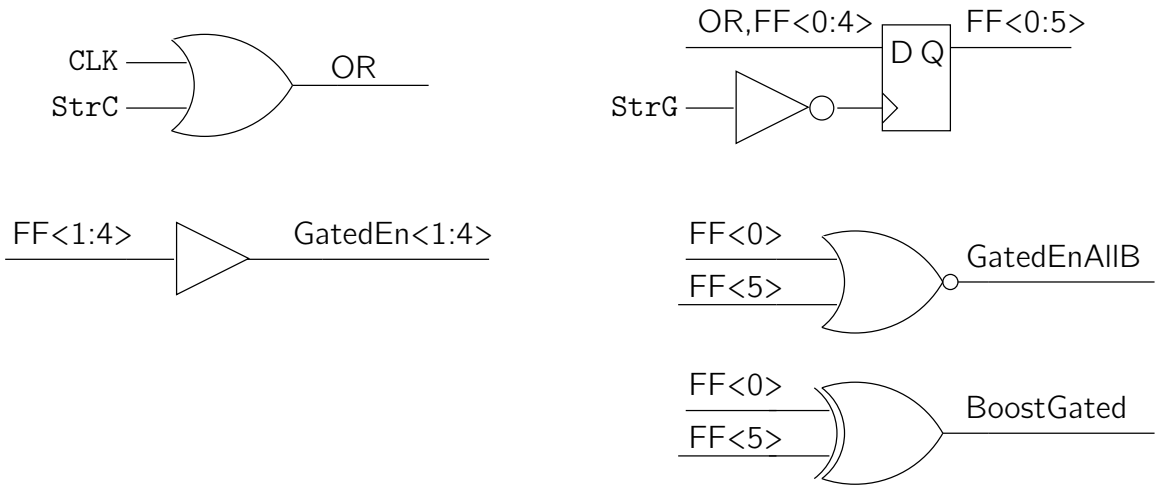

Figure 3.2: Schematic of the gated mode logic controlling all channels.

3.1.1 Non-overlapping Gates

For non-overlapping gate signals it is essential that the *rising* edge of `StrG` has to be *after* the falling edge of `CLK`. The `Gate` output is switched off as soon as the next `Gate` is switched on. See figure 3.3.

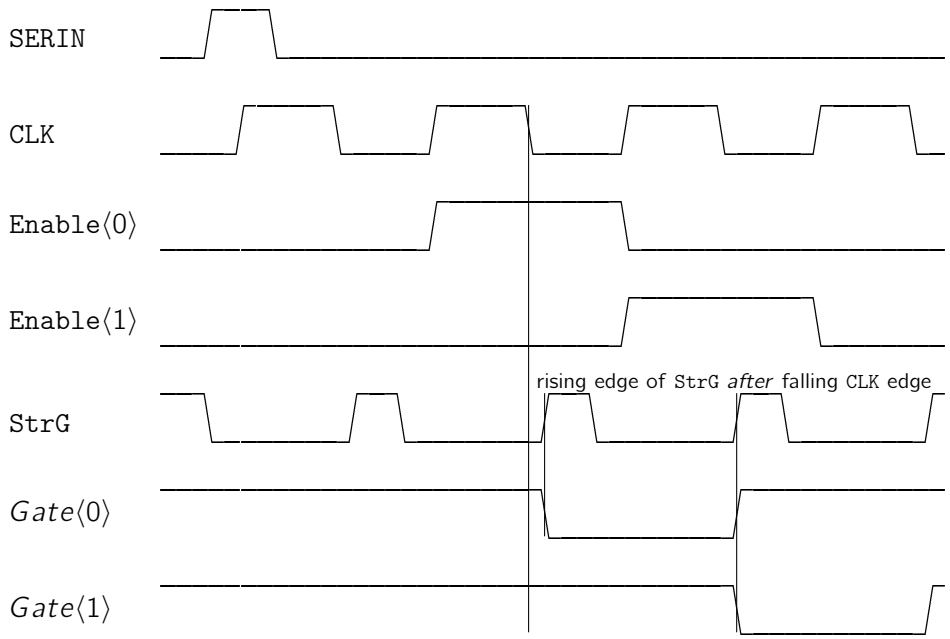

Figure 3.3: Non-overlapping gate strobe timing.

3.1.2 Overlapping Gates

To use overlapping gate signals the *rising* edge of `StrG` has to be *before* the falling edge of `CLK`. The amount of overlap is equal to the time between the rising edge of `StrG` and the falling edge of `CLK`. The `Gate` output is switched off with the falling edge of `CLK`. See figure 3.4.

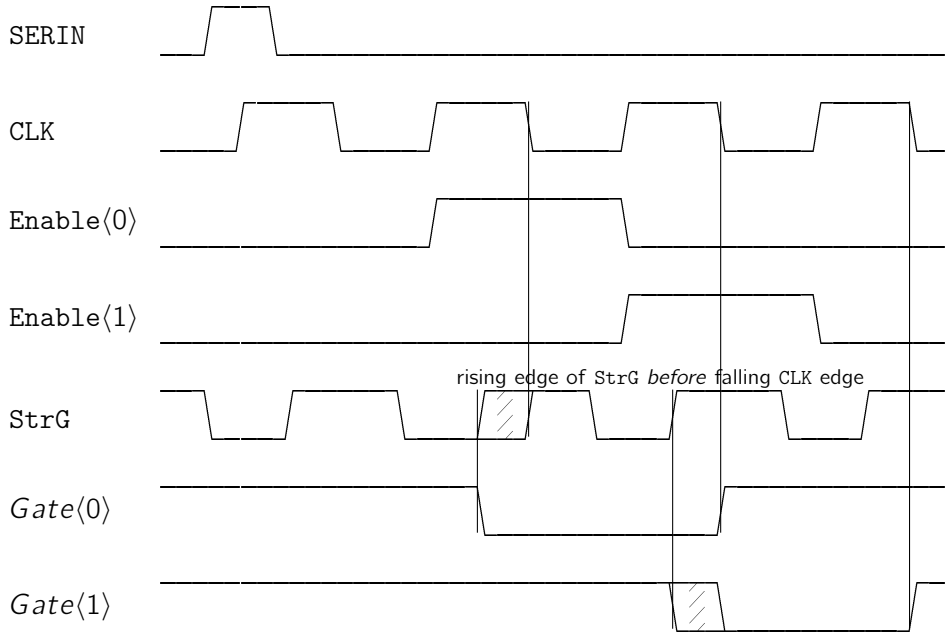

Figure 3.4: Overlapping gate strobe timing.

3.1.3 Row Skip Mode

For skipping rows the StrG signal has to be omitted. See figure 3.5 for an example for skipping the 2nd row.

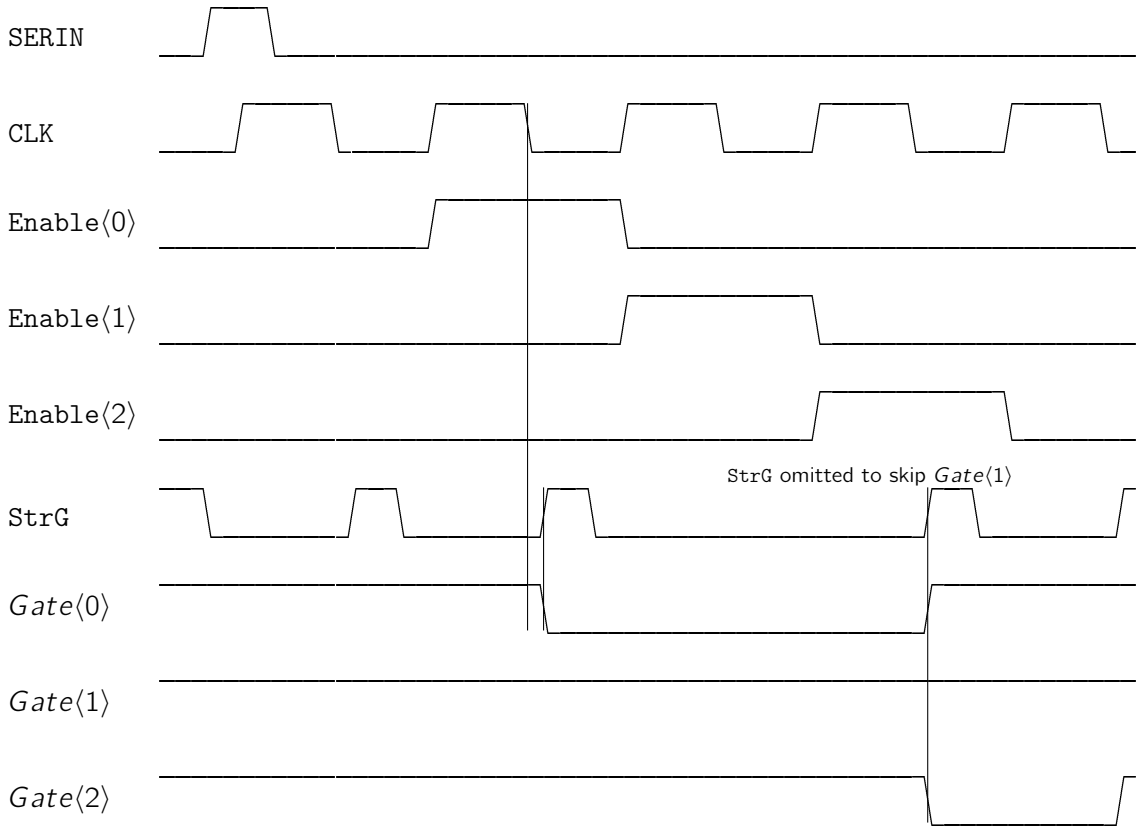

Figure 3.5: Gate strobe timing for skipping the 2nd row.

3.1.4 Clear

The `Clear` pulse is only working when the gate is switched on (internal GateOn signal is high; see fig. 3.1) and the `CLK` is high, too.

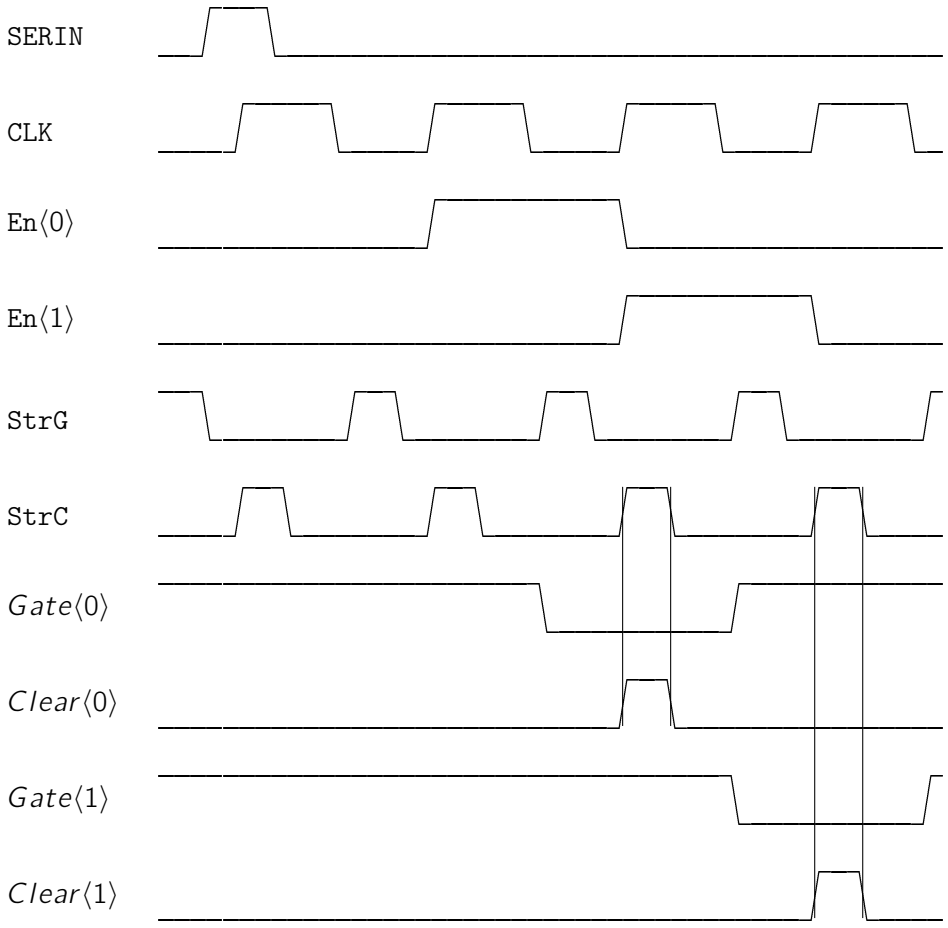

Figure 3.6: Clear timing

Clear during overlapping of gates

When using overlapping gates it A clear pulse occurs at the beginning and at the end of a gate-on interval if it is located within the overlapping phase. It thus clears the signal before and after sampling! See figure 3.7 for an example.

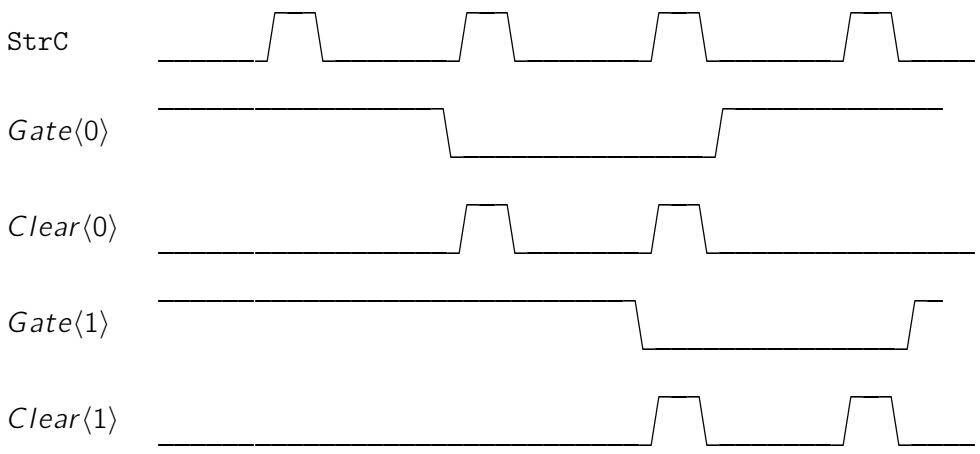

Figure 3.7: Clear timing during overlapping gates example

3.1.5 Gated Mode

The gated mode without read-out is enabled by stopping `CLK` while `StrC` is high and `StrG` is running. It is disabled by switching `StrC` to low and sampled by the falling edge of `StrG`. A minimum length of 8 falling `StrG` is required for a gated mode cycle.

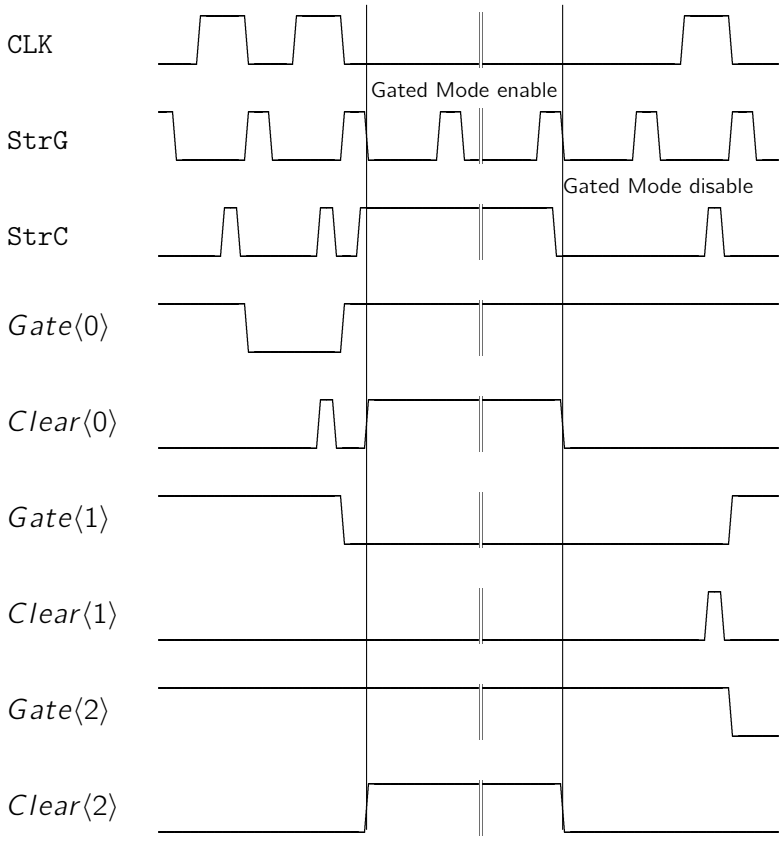

Figure 3.8: Gated mode timing without read-out

3.1.6 Gated Mode with read-out without clear

Gated mode with read-out is trigger by a high level on `CLK` or `StrC` at the falling edge of `StrG`. The clock continues to run.

The clear changes to high level immediately on non-active channels (see Clear<0>). Channels currently enabled (low gate voltage) will be switched to gated mode when they are disabled (see Clear<1>). No clear pulse is applied!

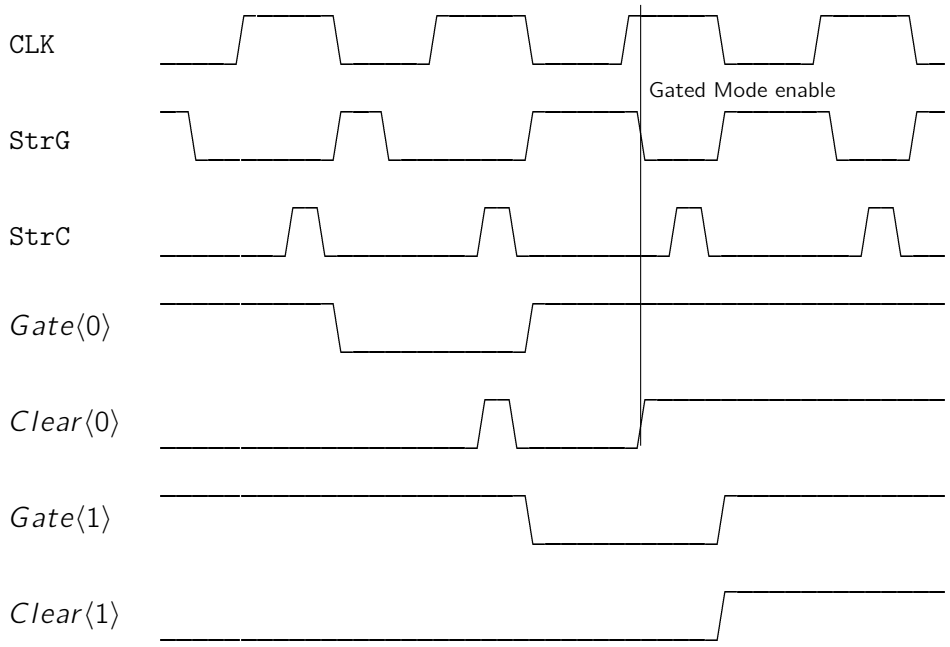

Figure 3.9: Gated mode timing with read-out

4 Typical Operation Characteristics

4.1 Power Consumption

Table 4.1 show the measured current on `Vref`. The current on `sub` depends on switching frequency of the HV output drivers and is shown in table 4.2. Figure 4.1 shows the power consumption of `GNDD` and `VDDD` as a function of the `CLK` frequency.

net	voltage	current
`Vref`	$1.8V$	$90\mu A$

Table 4.1: Current on `Vref`

net	voltage	0MHz	6.25MHz	12.5MHz	25MHz
`sub`	$0V$	$88\mu A$	$98\mu A$	$106\mu A$	$122\mu A$

Table 4.2: Static and dynamic current on `sub`

4.2 DAC Settings

The influence of the DAC setting in the power consumption on the V_{hi} supply is shown in figures 4.2 and 4.3. The chip is operated without a `CLK` signal at a supply voltage of $V_{hi} = 9V$.

Figure 4.4 shows the speed of the levelshifter for different `IBiasBoost` settings, resulting in shorter delays between the strobe edge and output signal for higher currents.

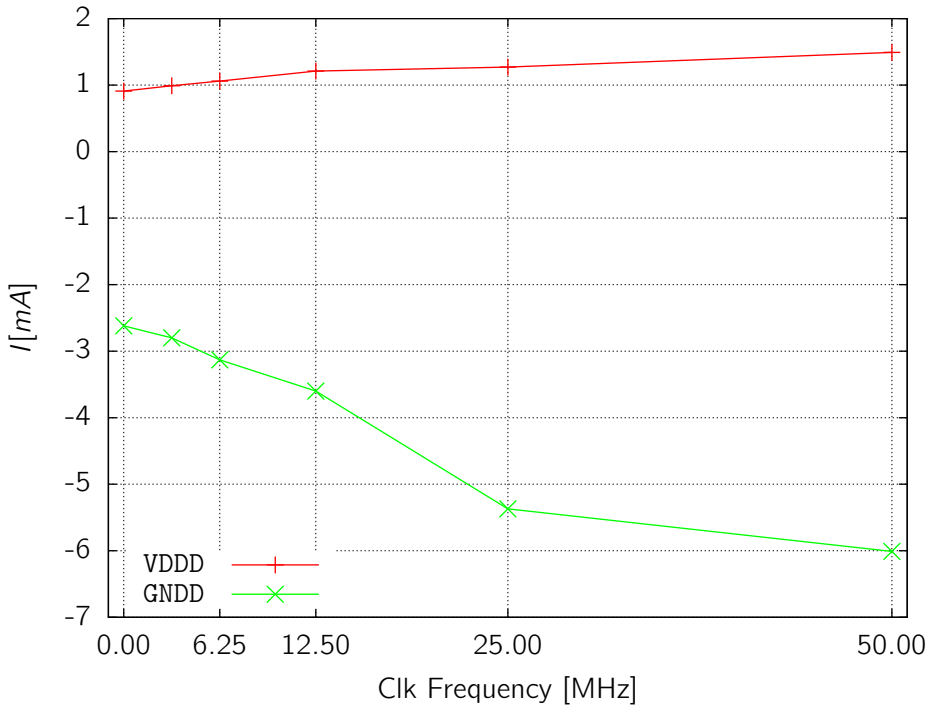

Figure 4.1: Measured current on VDDD and GNDD as a function of CLK frequency. VDDD $= 1.8V$, GNDD $= 0V$, IBias $= 1\mu A$, IBiasBoost $= 30\mu A$

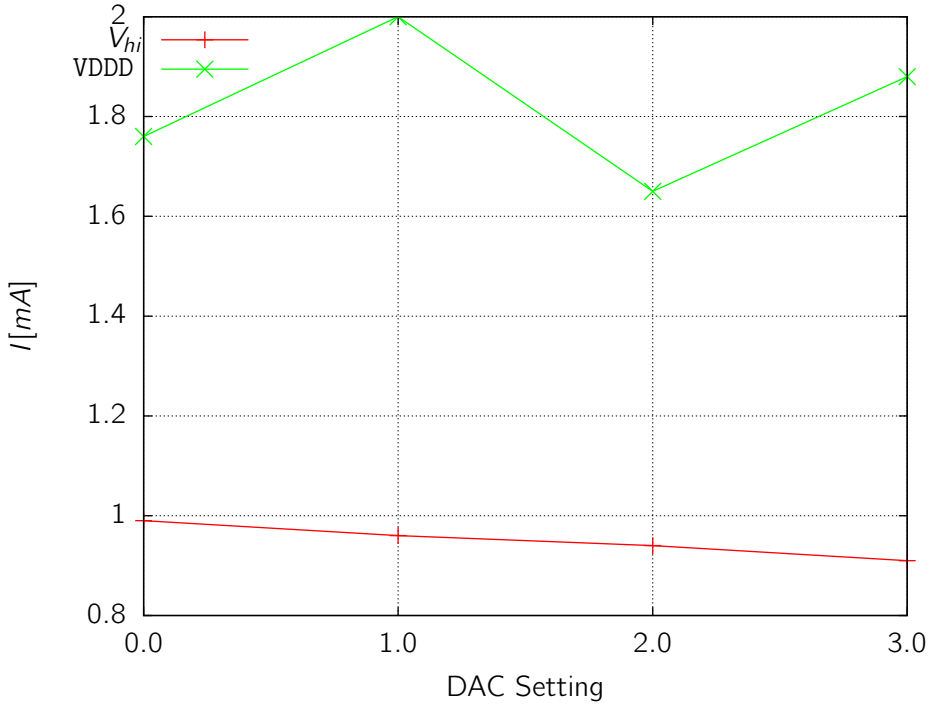

Figure 4.2: Measured static current on V_{hi} and VDDD as a function of IBias DAC setting. $V_{hi} = 9V$, VDDD $= 1.8V$

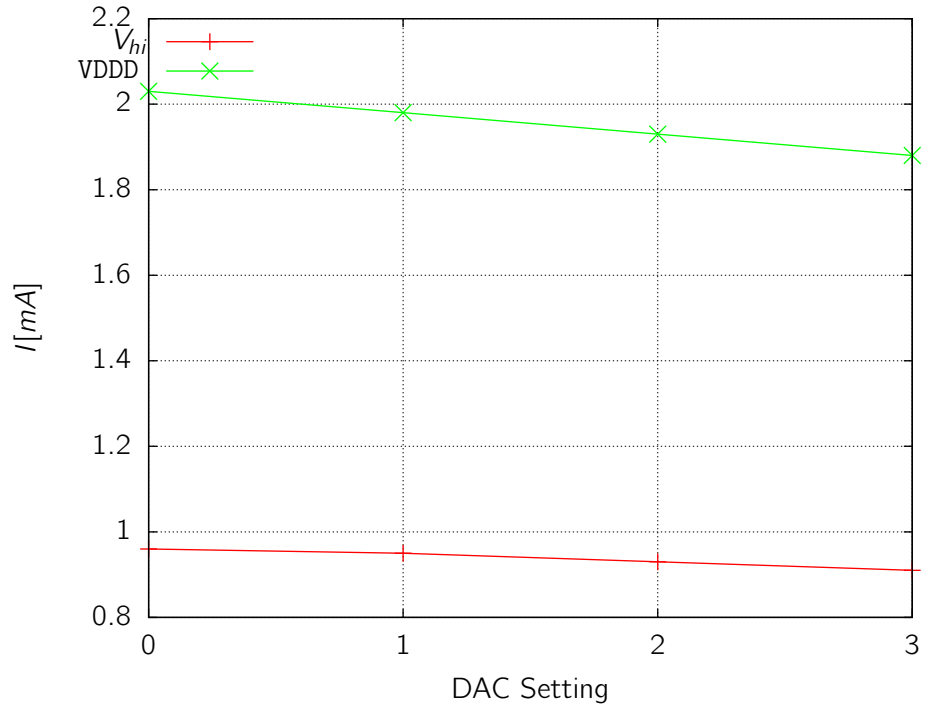

Figure 4.3: Measured static current on V_{hi} and `VDDD` as a function of `IBiasBoost` DAC setting. $V_{hi} = 9V$, `VDDD` $= 1.8V$

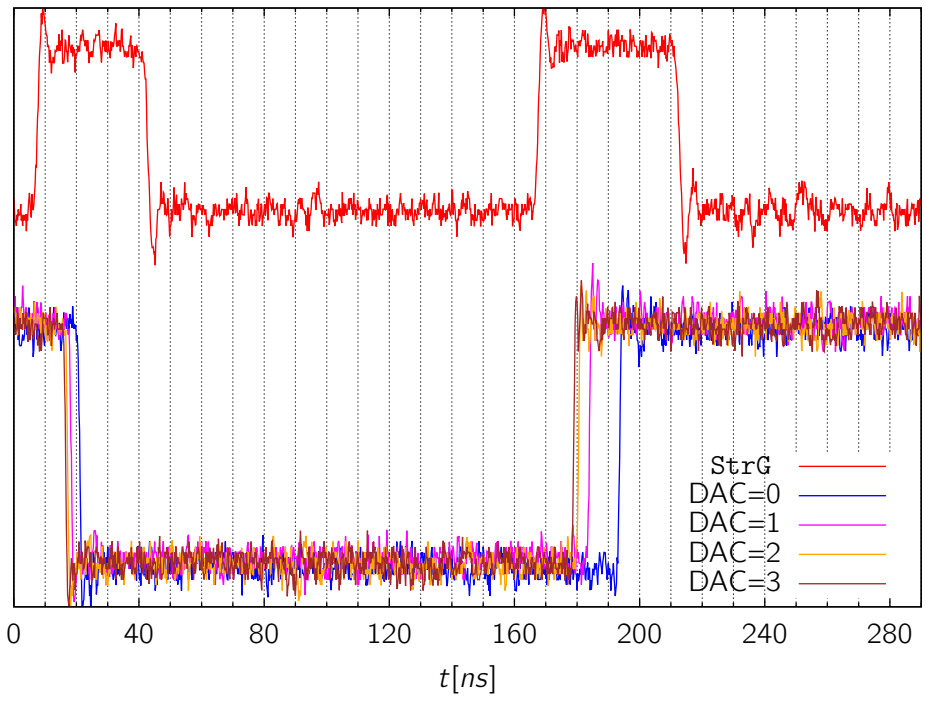

Figure 4.4: `StrG` to `Gate` delay at different `IBiasBoost` settings

4.3 Output Timing

This section shows measurements of the HV output drivers. They are operated at $V_{hi} = 9V$ and `IBiasBoost` $= 0$. Different load capacitors were connected to the outputs. The PCB capacitance is $\approx 8pF$ and has been added to the given nominal capacitor value.

Table 4.3 lists the rise- and falltimes calculated from 10% to 90% signal level. The output measurements are shown in figures 4.5 for the falling and in 4.6 for the rising edge.

capacitance	**rising**	**falling**
$\approx 8pF$	$0.8ns$	$0.9ns$
$\approx 30pF$	$1.8ns$	$2.0ns$
$\approx 55pF$	$2.8ns$	$3.3ns$
$\approx 76pF$	$3.6ns$	$4.0ns$
$\approx 98pF$	$4.2ns$	$4.8ns$

Table 4.3: Rising and falling edge timing for 10% to 90% signal levels.

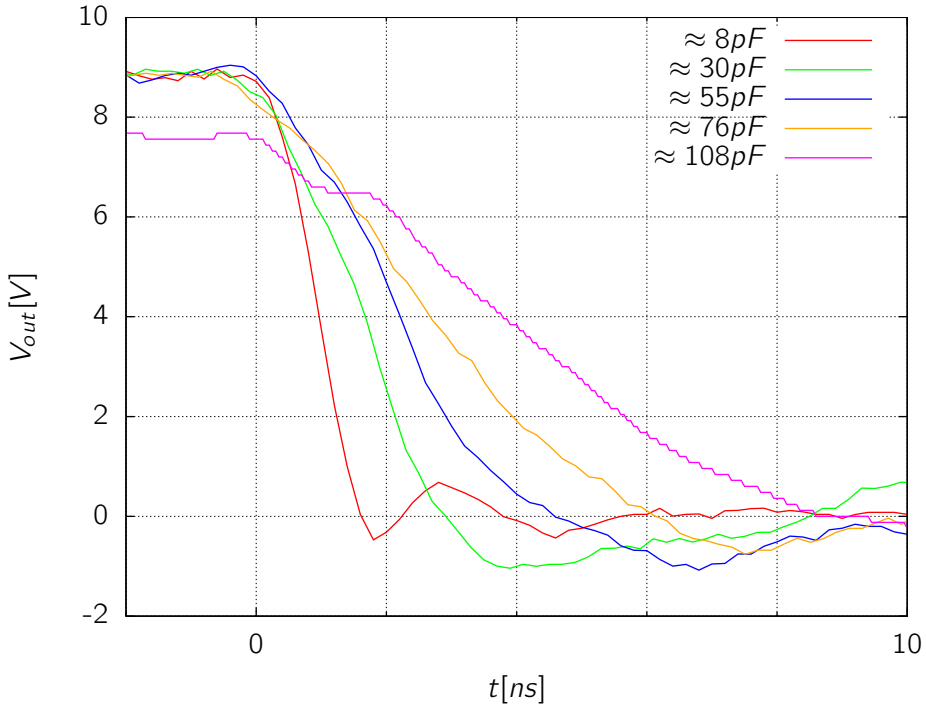

Figure 4.5: Falling edge for different load capacitors, $V_{hi} = 9V$

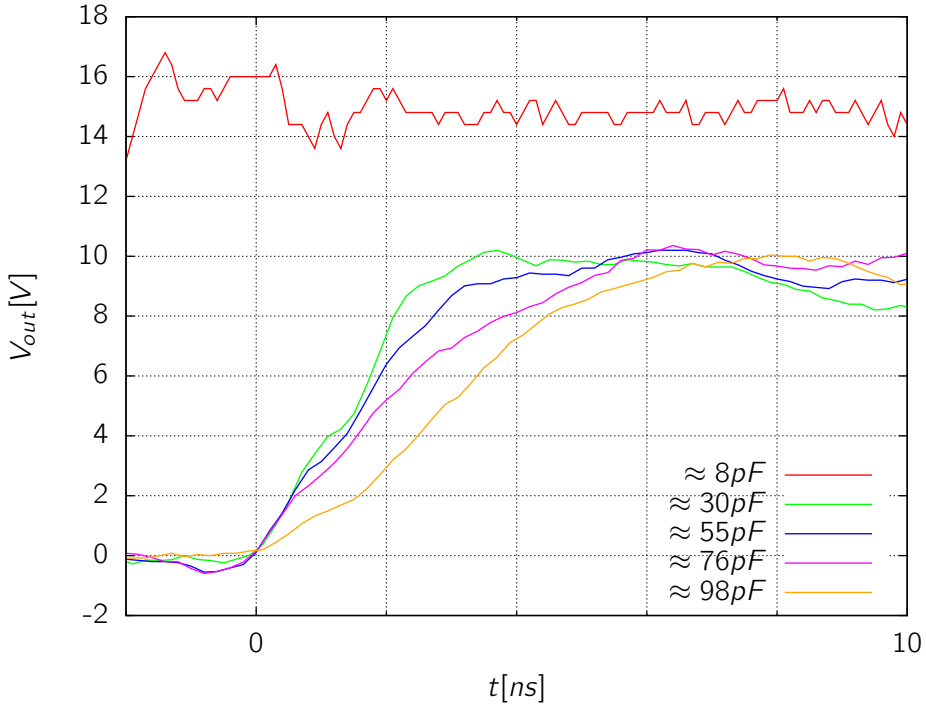

Figure 4.6: Rising edge for different load capacitors, $V_{hi} = 9V$

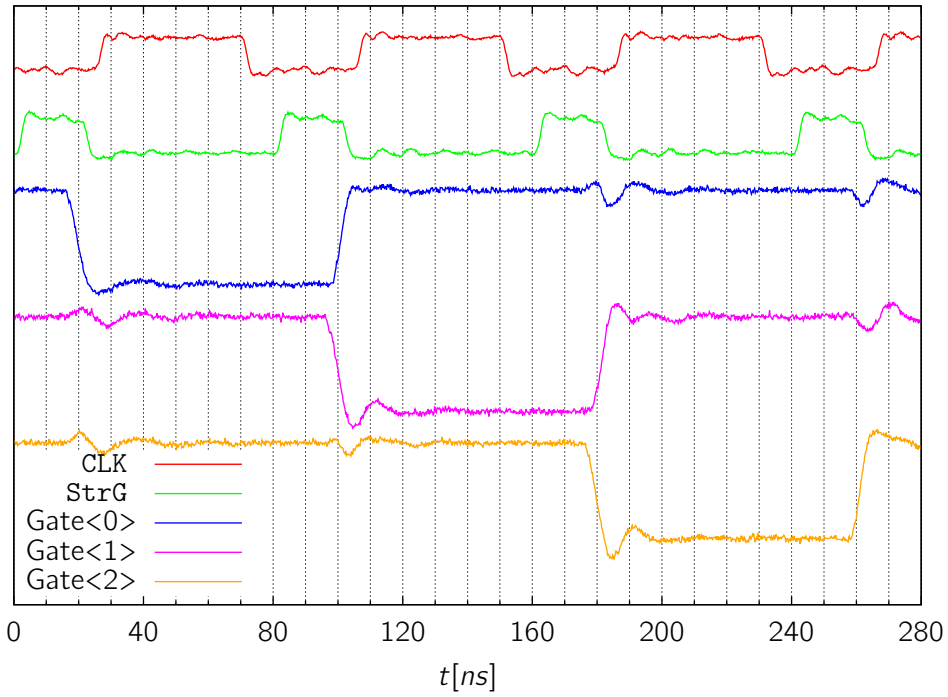

Figure 4.7: `CLK`, `StrG` and three `Gate` signals with $90pF$ load capacitor and $80ns$ `Gate` timing, $V_{hi} = 9V$

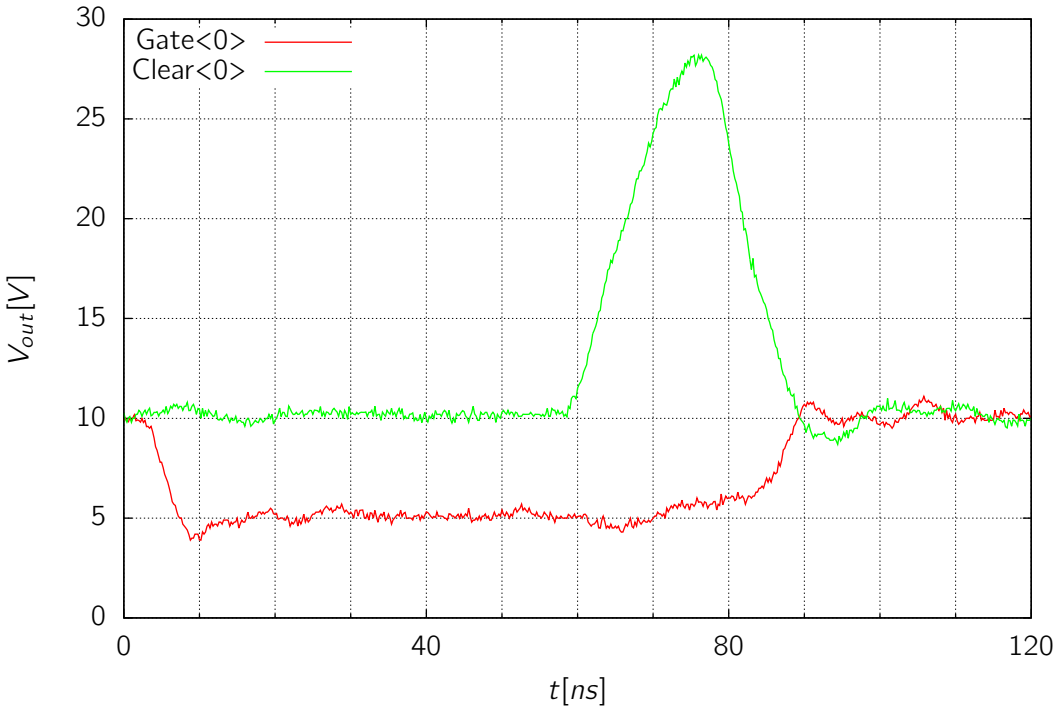

Figure 4.8: Single sampling scheme with $80ns$ timing $90pF$ load, $V_{GateHi} = 10V$, $V_{GateLo} = 5V$, $V_{ClearHi} = 27V$ and $V_{ClearLo} = 10V$.

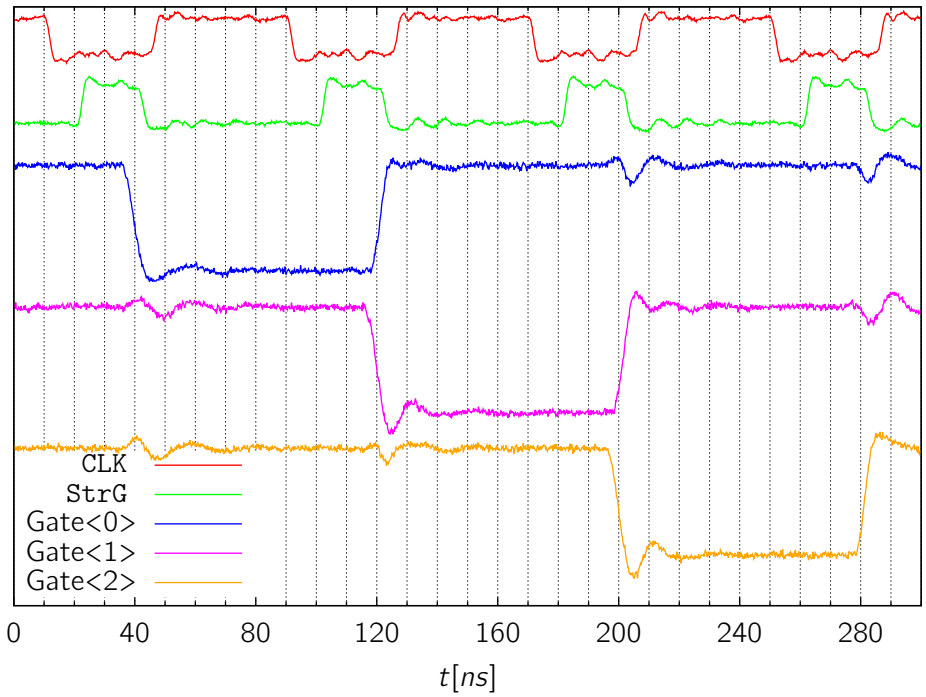

Figure 4.9: Non-overlapping `Gate` outputs.

4.4 Strobe Timing

This section shows example plots of the different strobe modes described in section 3.1. and the `Clear` timings for single-sampling and the gated mode operation.

In figures **??** and 4.12 is the row skipping technique shown, which omits the `StrG` signal for the skipped row.

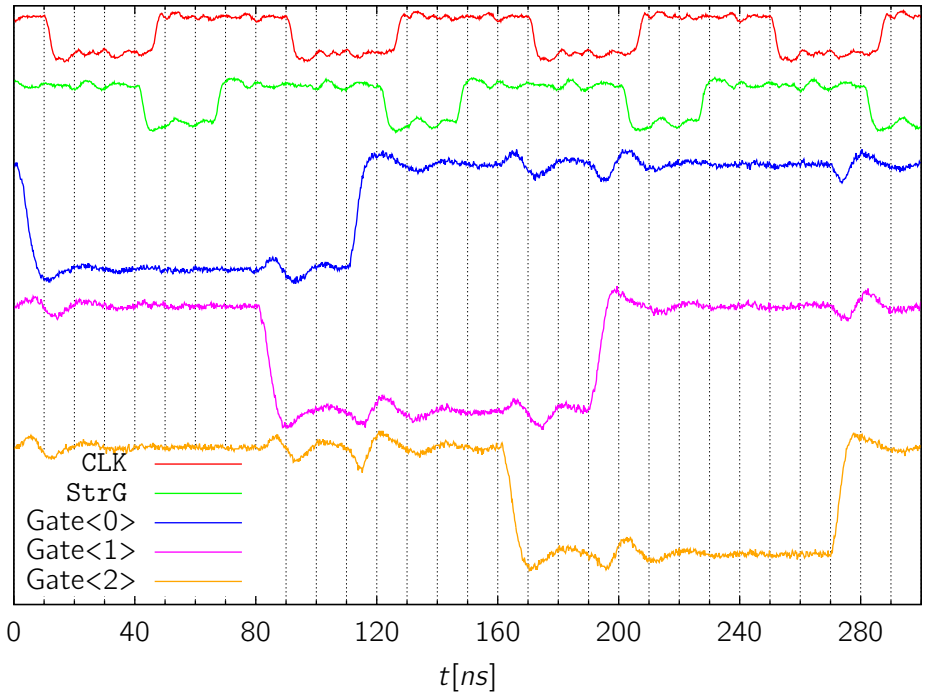

Figure 4.10: Overlapping `Gate` outputs.

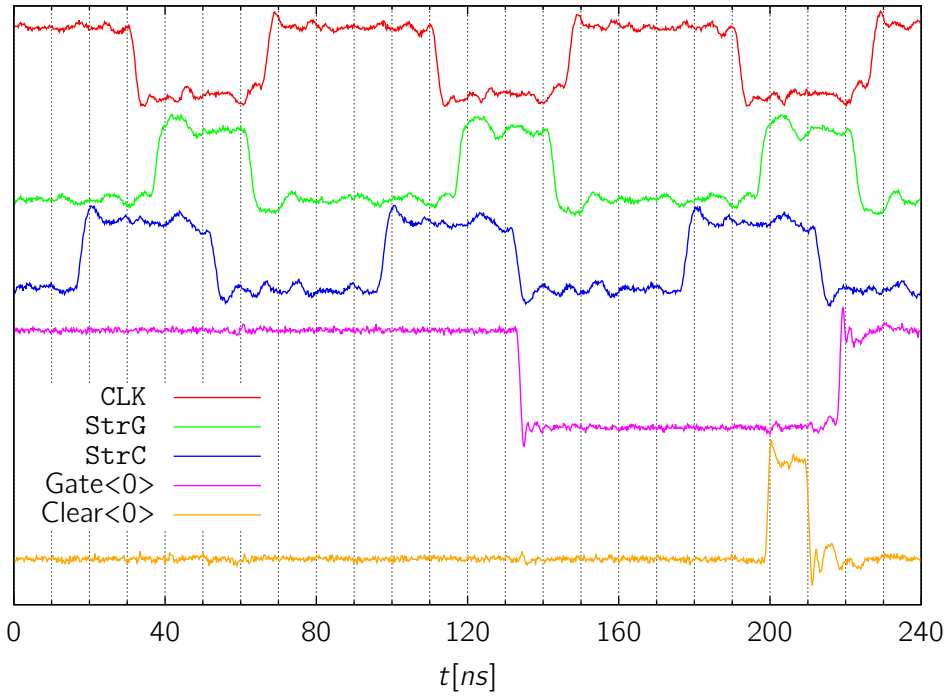

Figure 4.11: `Clear` at the end of `Gate` suitable for single sampling.

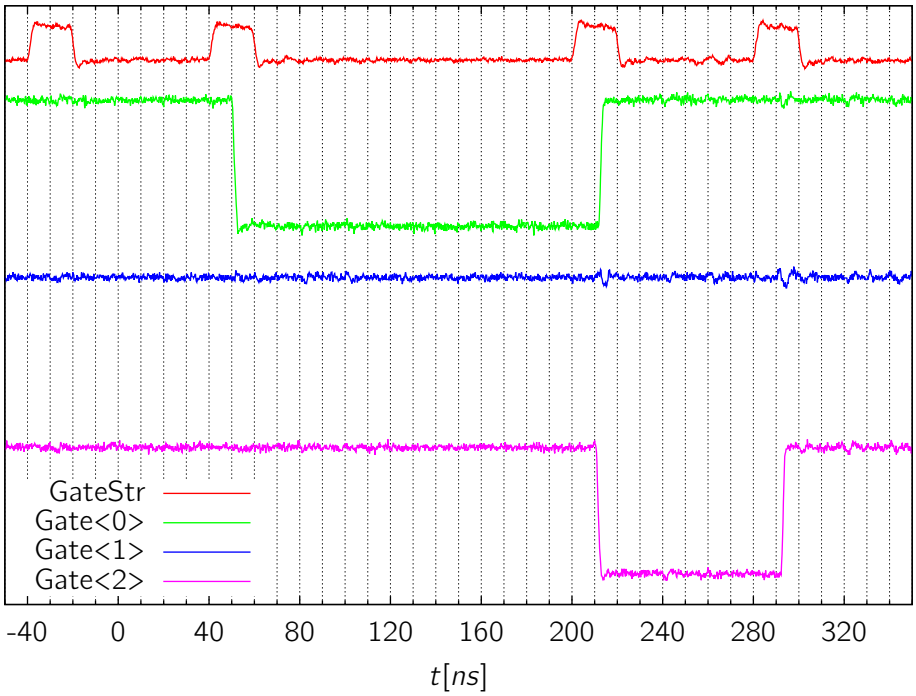

Figure 4.12: StrG and three Gate signals with skipping of Gate <1>.

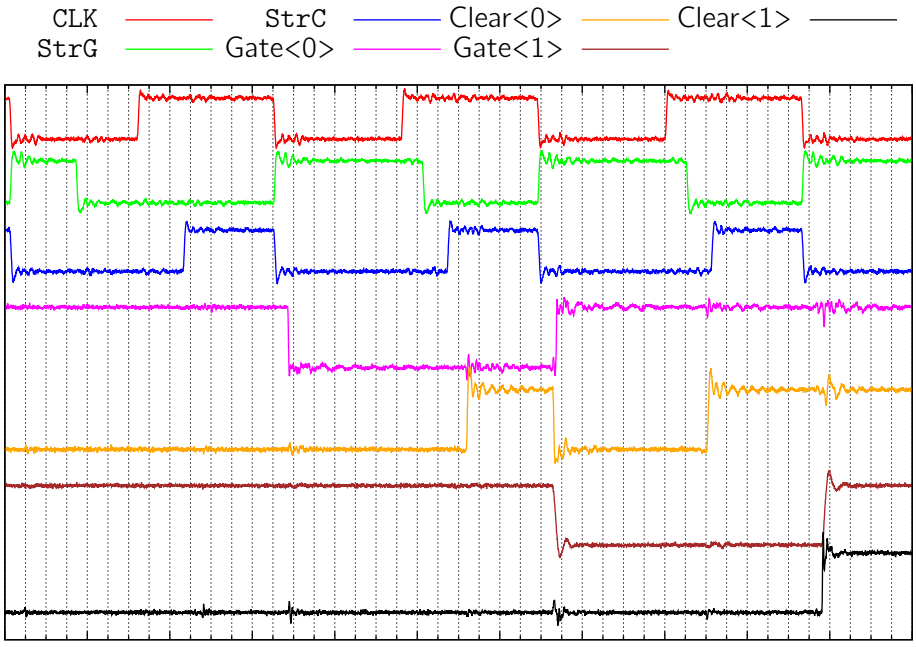

Figure 4.13: Gated mode with read-out without clear.

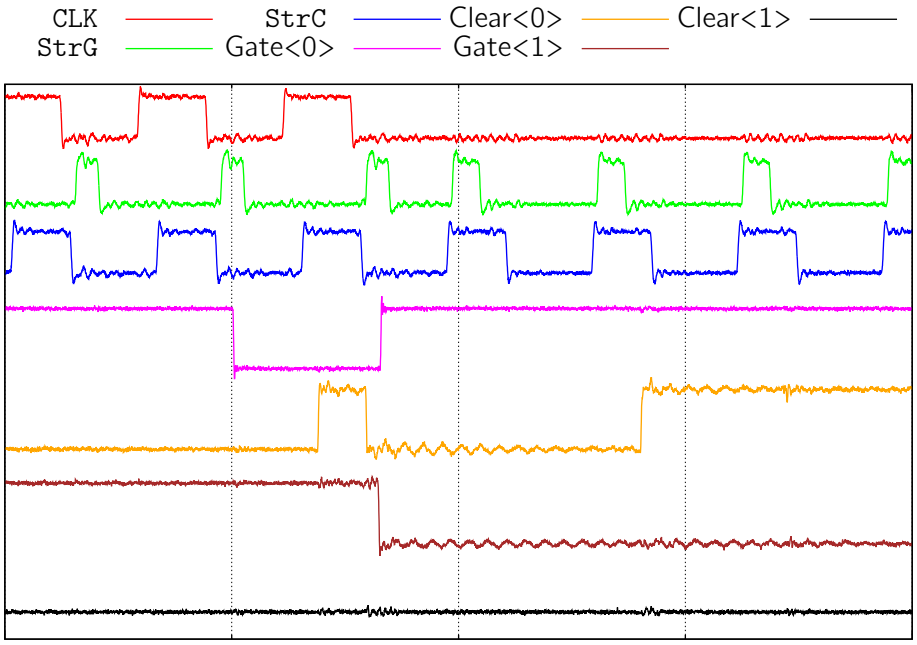

Figure 4.14: Gated mode without read-out without clear.

5 Irradiation

5.1 Setup

Irradiation has been done using the X-ray facility at Karlsruhe Institute of Technology (KIT). The parameters used are:

- 60kV, 33mA, Vanadium-filter
- 100mm distance $\Rightarrow$ 1117krad/h
- 21Mrad (200kGy)

The chip has been biased and was running at 12.5MHz (100ns timing) during irradiation. One `Gate` and one `Clear` output have been monitored. A load capacitance of 150pF was connected to both outputs. The chips setting were:

- `VDDD` = 1.8V
- `IBias` = 6.6μA
- `IBiasBoost` = 210μA
- `GHi` = `CHi` = 20V
- `sub` = `GNDD` = `GLo` = `CLo` = 0V
- on-chip termination enabled

5.2 Results

Due to software crashes it was only possible to get measurements at 0.5Mrad and 21Mrad.
After a dose of 0.5Mrad the supply current rises on `VDDD` from 1mA to 3mA and stays constant. On `GHi` and `CHi` together it rises from 18mA at a dose of 0.5Mrad to 25mA at 21Mrad.
No malfunction has been observed.

dose	Gate rising	Gate falling	Clear rising	Clear falling
0.5Mrad	14ns	14ns	15ns	12ns
21Mrad	14ns	14ns	17ns	15ns

Table 5.1: Rising and falling edge timing for 10% to 90% signal levels with 150pF load.

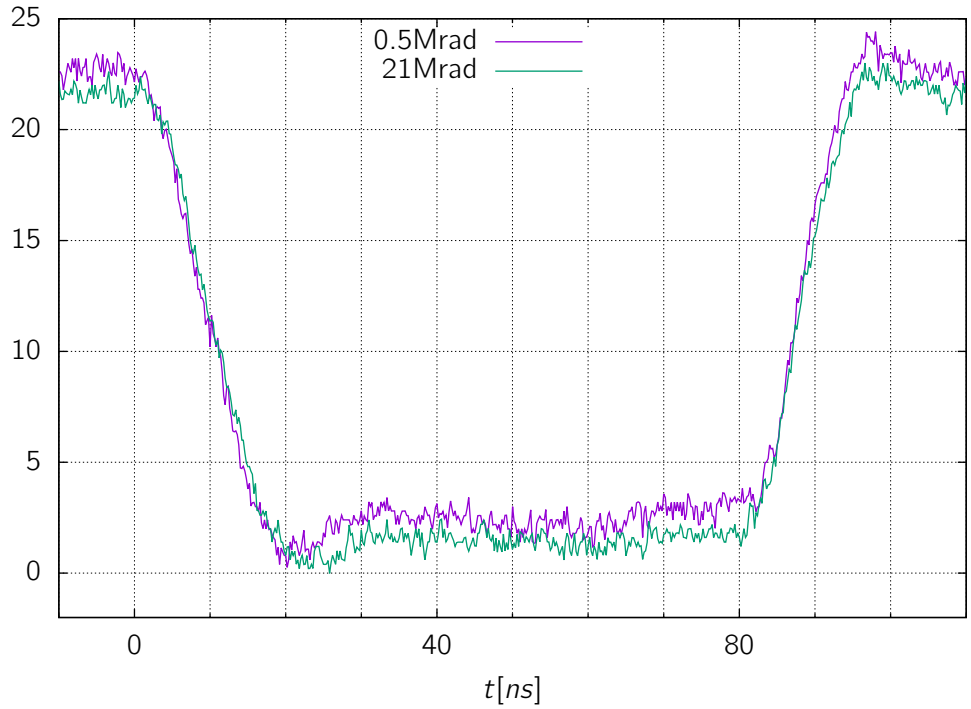

Figure 5.1: `Gate` output at 0.5Mrad and 21Mrad dose.

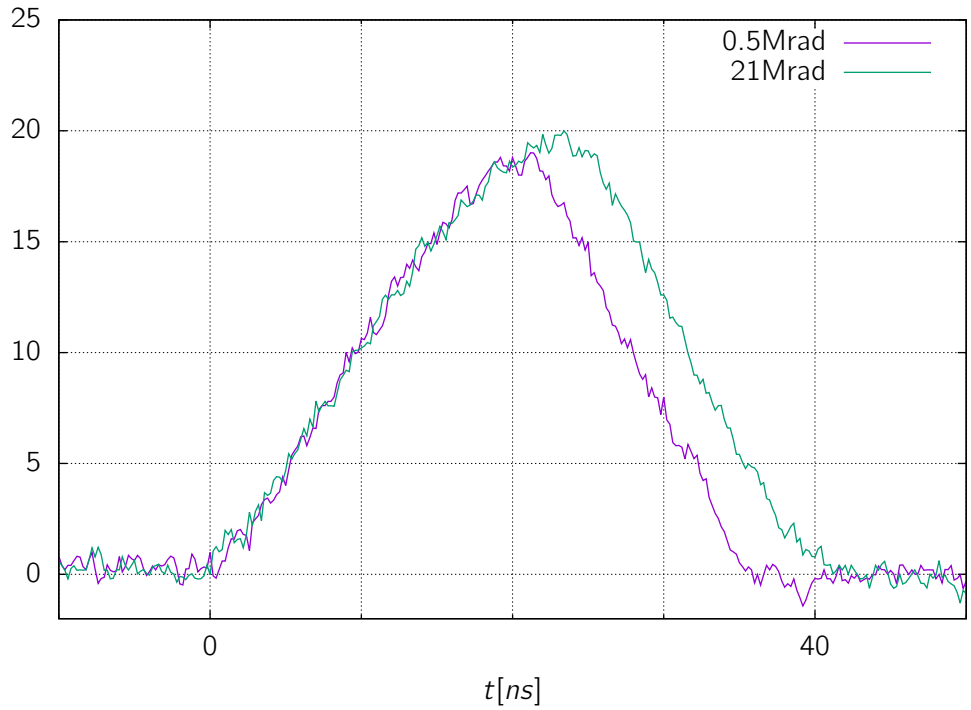

Figure 5.2: `Clear` output at 0.5Mrad and 21Mrad dose.

6 Chip History and Changes

6.1 SwitcherB33 -> SwitcherB18 v1.0

- Technology: AMS 180nm HV
- Chip size: same length, but smaller width
- Supply Voltages: VDD=1.8V, VDDJTAG not used anymore, Vref=1.8V
- Output Voltages: max 20V, faster output transistors
- LVDS: configurable internal termination resistors
- JTAG: user register bits changed

6.2 SwitcherB18 v1.0 -> SwitcherB18 v2.0 (Gated Mode)

- Gated mode operation added
- Output: absolute max. 50V with max. 20V swing!

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