DHPT↔DCD Data Link Delay Analysis
EMCM ASIC Pairs Summary

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1. Introduction

From the delay measurements done during the irradiation campaign at Karlsruhe in June 2015 on EMCM W31-3p4 (ASIC pair 4) the following observations were made:

- Irradiation has almost no effect on mean inverter pair delay times, which are also homogeneous among all links (around 190 ps).
- Most links delay tolerance and asymmetry are hardly affected by irradiation.
- 6 links fail (no optimal delay) at 2 Mrad, recover until 10 Mrad.
- Delay tolerance shows large variation among links (200 ps to 2.4 ns).
- Consequently also asymmetry shows large variation among links (400 ps to 2.8 ns).

It is now important to understand, whether this behavior is representative for other ASIC pairs and if new effects occur in other ASIC pairs. To investigate this we modified the delay analysis script to produce standardized output plots on any data delay scan measurement. The HLL provided delay scan datasets from two other EMCMs ('pX' indicates ASIC pair X on this module)

- W17-3p1 and W17-3p4
- W18-3p1, W18-3p2, W18-3p3 and W18-3p4

W31-3p4 was the EMCM ASIC pair measured during the irradiation campaign.

2. Analysis Script 'delay_analysis.py'

Here we give a brief description of the analysis script and how to use it. The script is named 'delay_analysis.py' and is available in the svn directory /cs-studio/analysis/delays. It needs the 'delay_analysis.ini' file for setting parameters and uses 'plot.py' in the above directory.

2.1 Prerequisites

Modify the 'delay_analysis.ini' file:

- Set paths to datafiles in [datapaths]. Keys will show up in legends, choose proper labels.
- Set global [parameters]: GCK (global clock) and number of ASIC pair.
- Each dataset can have different GCK and ASIC value (keys must match).
- Set path to folder for plots.

Datapaths must contain the 'overview_asicpairX.npy' file.
Important: For the algorithm to work the overview file, and thus the delay matrix, must be given with the full good band (zero bit error region) visible and well defined. If this is not the case initially, a shifted testpattern check is necessary. Use the 'analyze_delays.py' script (producing the overview file) with parameters '–shiftpatternup' or '–shiftpatterndown' and a global delay range given by '–gmin' and '–gmax' for this purpose.

2.2 Analysis and Output

The script produces the 1D delay matrix diagonal projections or "g+l plots" per link. The algorithm tries to determine a good region (bit error == 0) and its delay tolerance. Also the asymmetry plateau width will be measured. Delay tolerance + asymmetry plateau width corresponds to a full clock period, thus yielding a mean delay time per inverter pair. With this delay tolerance and asymmetry are translated into units of time.
The output plots that are produced:

- g+l plots per link
- mean delay element per link and as histogram
- delay tolerance and plateau width top view per link
- delay tolerance per link and histogram
- asymmetry per link and histogram
- a link categories histogram (categorizes links according to their delay tolerance)

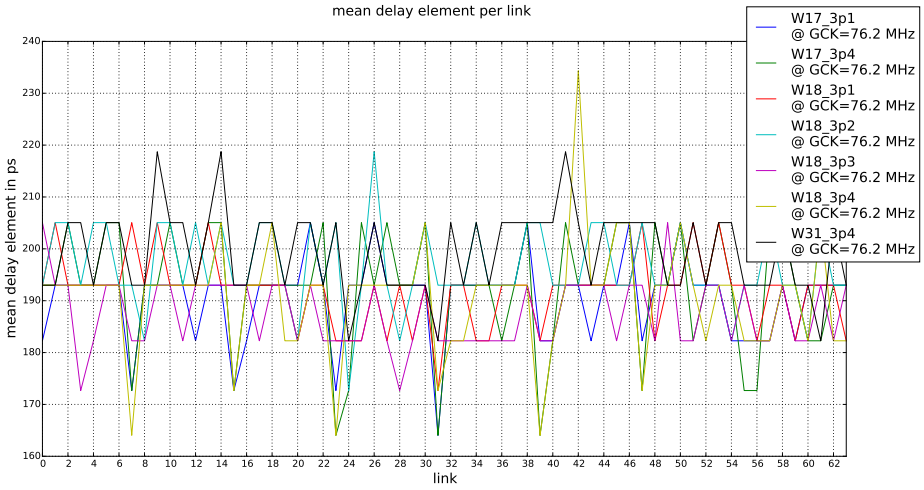
If multiple datapaths are given, e.g. multiple EMCM ASIC pairs, all will be plotted for comparison. If only one datapath is given the script will also produce the corresponding 2D delay matrix plots with continuous bit errors.

3. Results of ASIC Pairs Comparison

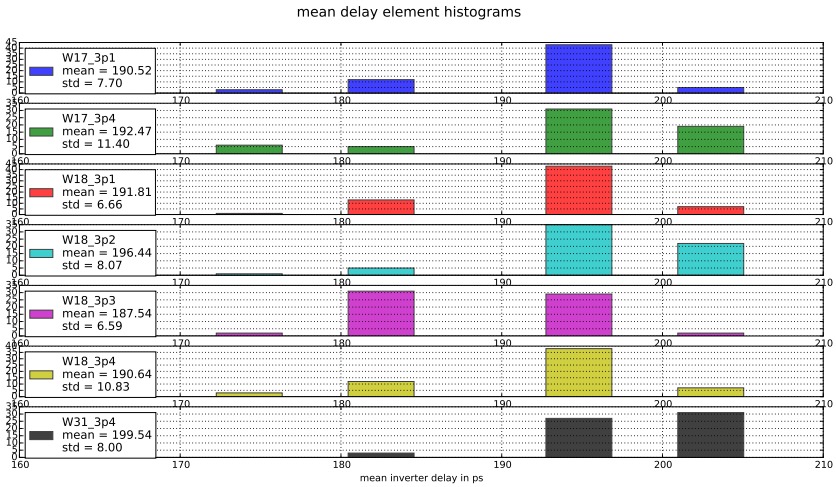
The script was run on the provided EMCM ASIC pairs datasets. For all datasets the testpattern needed to be shifted up (= delayed by one clock period) in the full global delay range to have a well defined and fully visible good region band. It was assumed that the GCK used in all measurements was GCK = 76.2 MHz (as DHP_Core voltage was at 1.62 V).

3.1 Mean Delay per Inverter Pair

Figure 1 shows the results of the mean delay element analysis for all ASIC pairs. Figure 1a shows the mean delay element per link. It is apparent that all 64 links of every ASIC pair of every EMCM agree very much with each other in this mean delay element time with only a small spread (around 190 ps±10 %). Figure 1b showing the histograms of the mean delay element for each ASIC pair separately also confirms this: the means are all around 190 ps with rms values in the order of 10 ps.



(a) Mean delay element per link for all EMCM ASIC pairs.



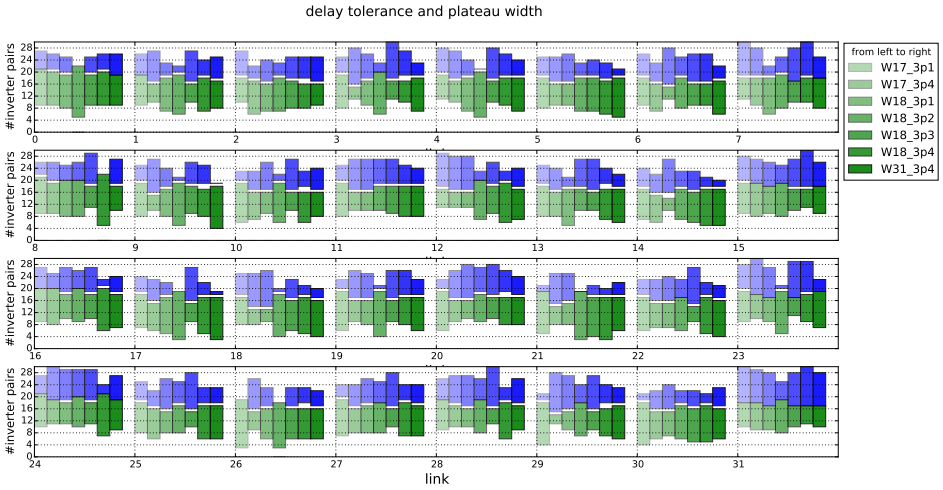
(b) Mean delay element histograms for all EMCM ASIC pairs.

Figure 1: Mean delay element comparison. All ASIC pairs links are homogeneous and consistent with 190 ps with small spreads.

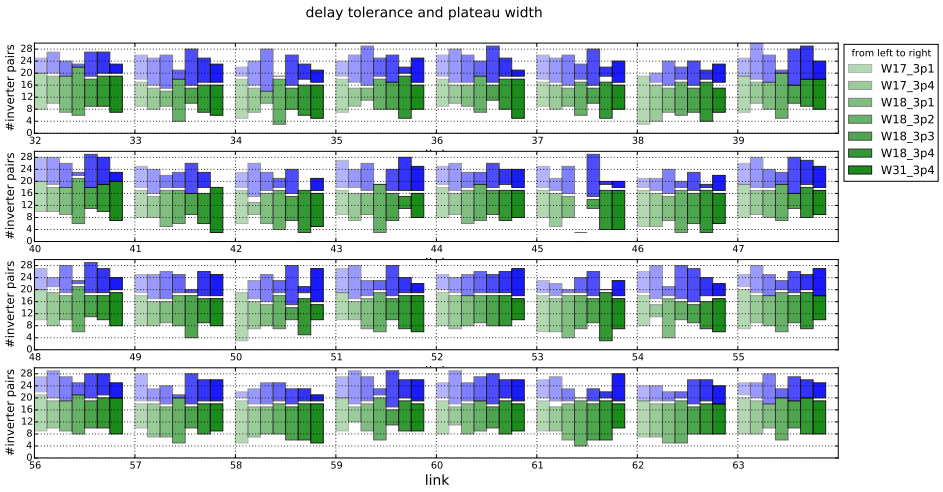
3.2 Delay Tolerance and Asymmetry Overview

In figure 2 the measured delay tolerances and asymmetries per link per ASIC pair are shown as a top view on the g+l plots. Green bars indicate the asymmetry plateau, blue bars indicate the good region/delay tolerance. All links show similar behavior in the sense that the asymmetry plateau is always on the same side of the good region and the total width of tolerance+asymmetry is a constant. Although in the irradiation data 3 LSB links and 2 AOB links where found to fail at 2 Mrad, which might have indicated some LSB

specialty, it can not be confirmed that LSB links are more prone to fail as AOB or MSB links.



(a) Delay tolerance and plateau width top view, link00 to link31.



(b) Delay tolerance and plateau width top view, link32 to link63.

Figure 2: Delay tolerance and asymmetry for all links and all ASIC pairs as a top view on g+l plots. Blue: good region. Green: asymmetry plateau. All links show overall similar behavior with the asymmetry plateau always on the same side of the good region and a constant tolerance+asymmetry width. LSB links are not more prone to failing than AOB or MSB links.

3.3 Delay Tolerance in Detail

The delay tolerance in units of #inverter pairs for all 64 links is histogrammed for each ASIC pair in figure 3 with the ASIC pair measured during the irradiation campaign (W31-3p4) at the bottom. Comparing the histograms and categorizing the ASICs by their mean delay tolerance, three types can be recognized:

- high mean tolerance of ≈ 8 #inverter pairs for W17-3p4, W18-3p1 and W18-3p3
- medium mean tolerance of ≈ 5.50 #inverter pairs for W17-3p1, W18-3p4 and W31-3p4
- low mean tolerance of < 4 #inverter pairs and many 0-tolerance links for W18-3p2.

Note that 0-tolerance links are either dead links or links with just one possible good setting, see figure 6 for more details. From this comparison the irradiation ASIC pair (W31-3p4) is recognized as showing a typical and representative delay space distribution. Also high and medium category ASIC pairs are likewise found between ASIC pair number 1,3 and 4. A low category ASIC pair is only found for an ASIC pair number 2. However, there are no other ASIC pair #2 data to compare to, thus it cannot be concluded whether ASIC pair #2 is in general of low category (e.g. due to routing on EMCM module), or just this pair happens to be problematic.

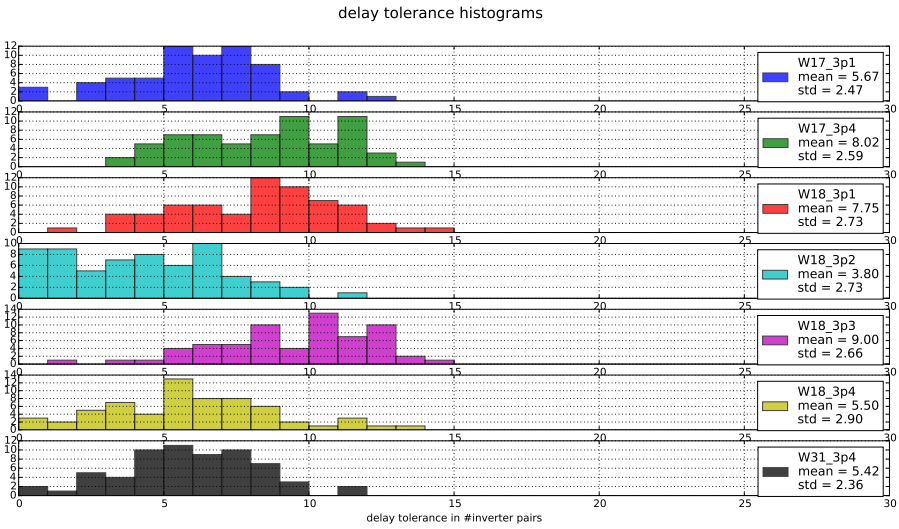


Figure 3: Histograms of the delay tolerance in #inverter pairs per ASIC pair. The histogram at the bottom is from the irradiation ASIC pair. Note: A delay tolerance of 0 can indicate a dead link or a link with just one possible good region setting.

3.4 Asymmetry in Detail

Looking at the asymmetry histograms 4 confirms the above interpretation, which is expected since:

$$\text{delay tolerance} + \text{asymmetry width} \approx \text{const.} = \text{clock period}.$$

High asymmetries correspond to low category ASIC pairs (e.g. W18-3p2). Again the irradiated ASIC pair W31-3p4 shows a very typical asymmetry distribution and is thus a representative ASIC pair.
Regarding new types of link defects one may investigate the 0-asymmetry link found in ASIC pair W18-3p2 (in the 0 bin), which is link45. Figure 5a shows this link for ASIC pair W18-3p2. The link does not show a distinct good region. On the contrary, there is a small peak towards higher bit errors around the total delay region, where the good region would be expected according to most other links. This could correspond to an extremely large asymmetry. Considering the actual delay matrix for this link (figure 5b) confirms a largely extended asymmetry region. The excess of bit errors in the expected good region might be an overlap effect.

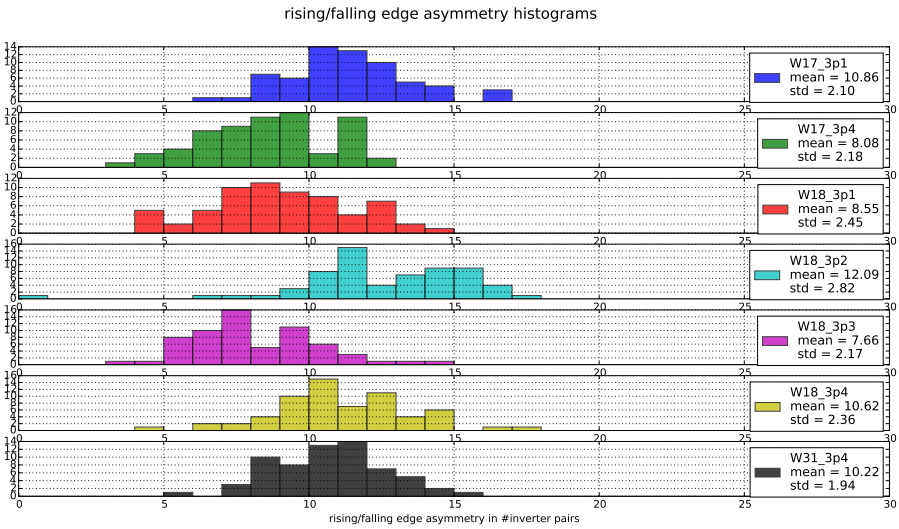
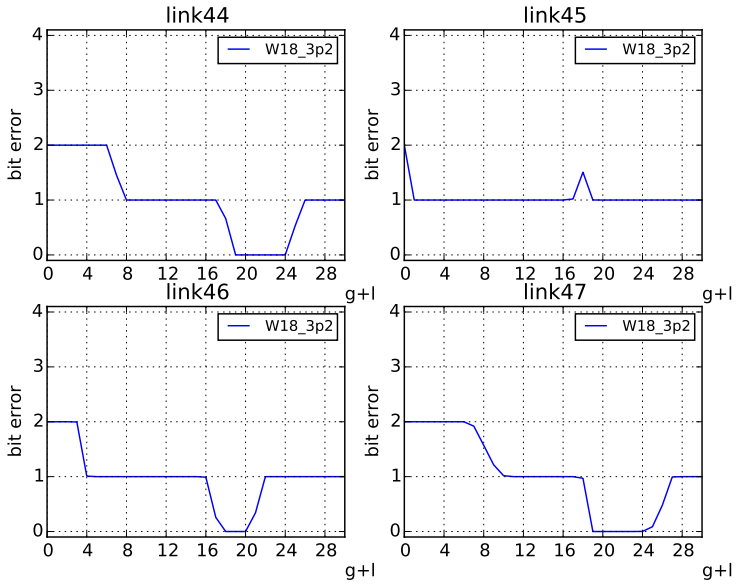
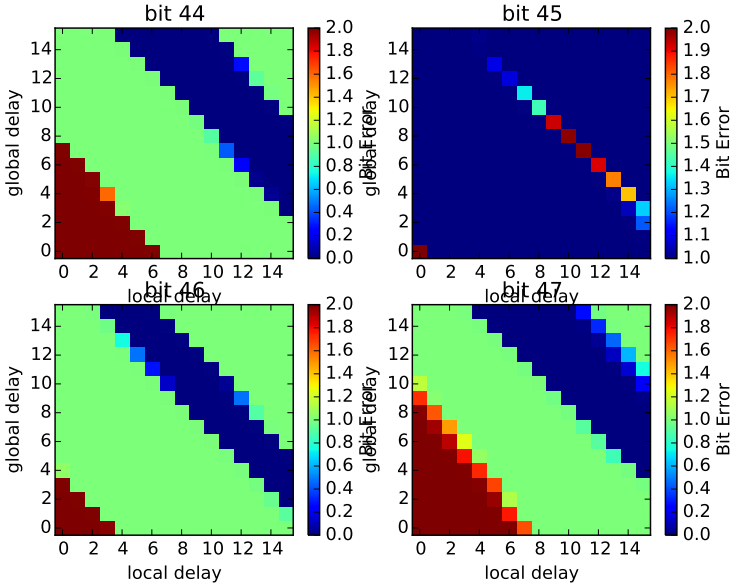


Figure 4: Asymmetry width in #inverter pairs for all 64 links histogrammed per ASIC pair. Bottom histogram is from the irradiated ASIC pair.



(a) 1D bit error diagonal projection of delay matrix (or g+l plot) for link45 on ASIC pair W18-3p2. No distinct good region in this link, widths finding algorithm does not yield usable result.



(b) 2D bit error delay matrix for link45 on ASIC pair W18-3p2.

Figure 5: Details for link45 on ASIC pair W18-3p2.

3.5 Link Categories Overview

For a quick overview one may also consider the link category histograms 6. According to their delay tolerance links are categorized into:

- stable: delay tolerance of 8 – 15 #inverter pairs
- ok: delay tolerance of 3 – 7 #inverter pairs
- weak: delay tolerance of 1 – 2 #inverter pairs
- only one good delay setting
- dead links, no working delay setting with 0 bit errors.

We recognize the same ASIC pair qualities:

- W17-3p4, W18-3p1 and W18-3p3 have a lot of very stable links and no dead or only-1-setting links as these ASIC pairs showed larger delay tolerances and smaller asymmetries.
- W17-3p1, W18-3p4 and W31-3p4 have mainly links with medium delay tolerance of 3 – 8, but also some weak and even dead links. Again the irradiated ASIC pair W31-3p4 shows very representative behavior.
- W18-3p2 is a rather bad ASIC pair with many dead and weak links, which was expected from the previous results.

Remark: The definition of a dead link used here is, that a link does not have any g+l (total delay) value for which the bit error is exactly 0. However, it might still be, that there exists a specific global delay, local delay setting for which the bit error is 0. Due to the diagonal projection in the delay matrix this is not visible in the g+l plots. Thus, the applied dead link definition is a little more conservative.

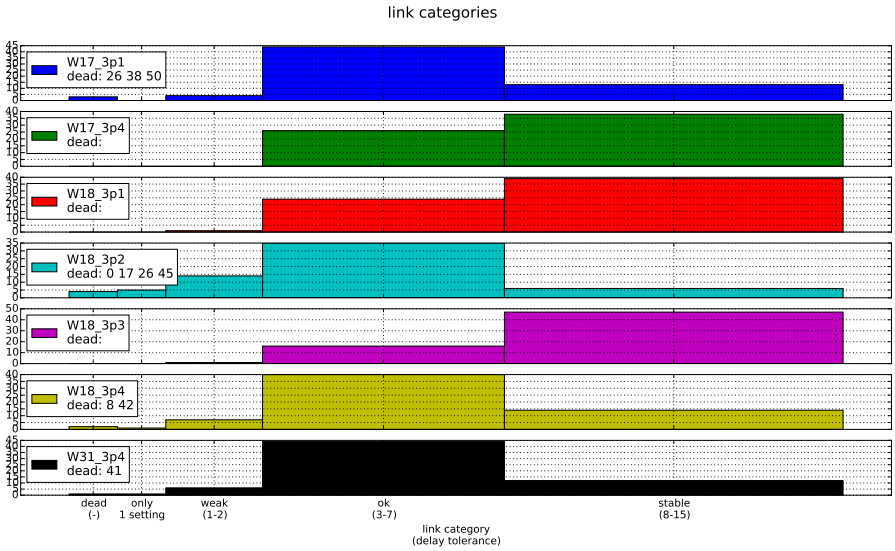


Figure 6: Categorization of links per ASIC pair according to their delay width.

4. Conclusion

Considering the initial question of how the irradiated ASIC pair compares to other EMCM ASIC pairs we conclude:

- The irradiated ASIC pair shows very typical and representative behavior regarding mean delay element time, delay tolerance and asymmetry distributions.
- One new link problem was seen in link45 in ASIC pair W18-3p2. It is not completely clear what the interpretation of this problematic behavior is.

We also confirmed that large spreads in delay tolerance or asymmetry, respectively, cause largely varying link qualities in a single ASIC pair and are present in all ASIC pairs. This causes some links to fail initially, before any irradiation, for some ASIC pairs. The bad overall quality of W18-3p2, an ASIC pair #2, might be connected to the routing on the EMCM modules, or could be an individual case.