Karlsruhe Irradiation Campaign June 2015

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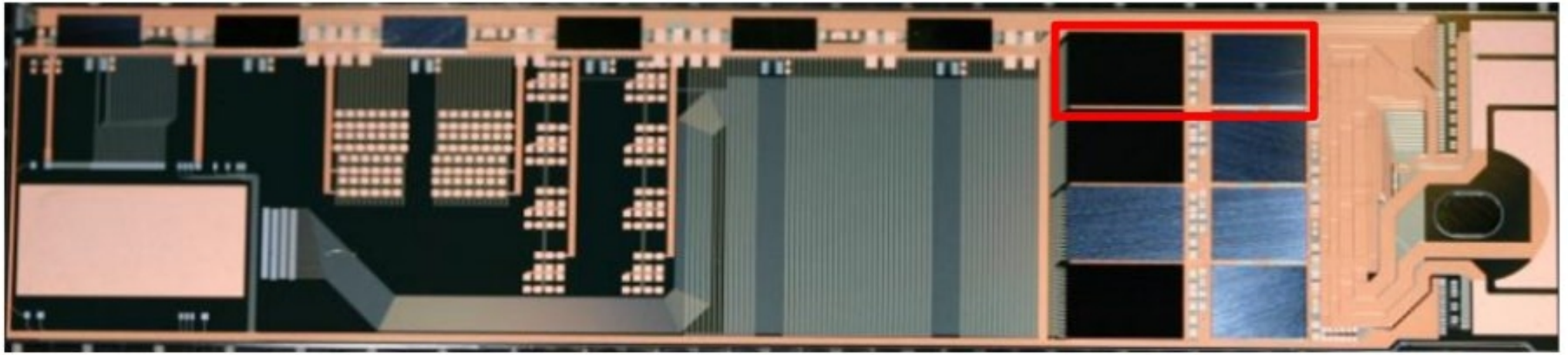
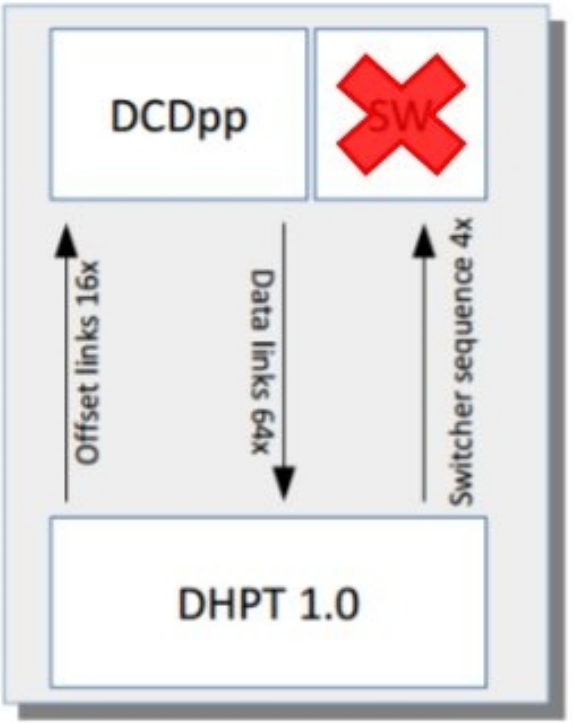
Setup - DUT



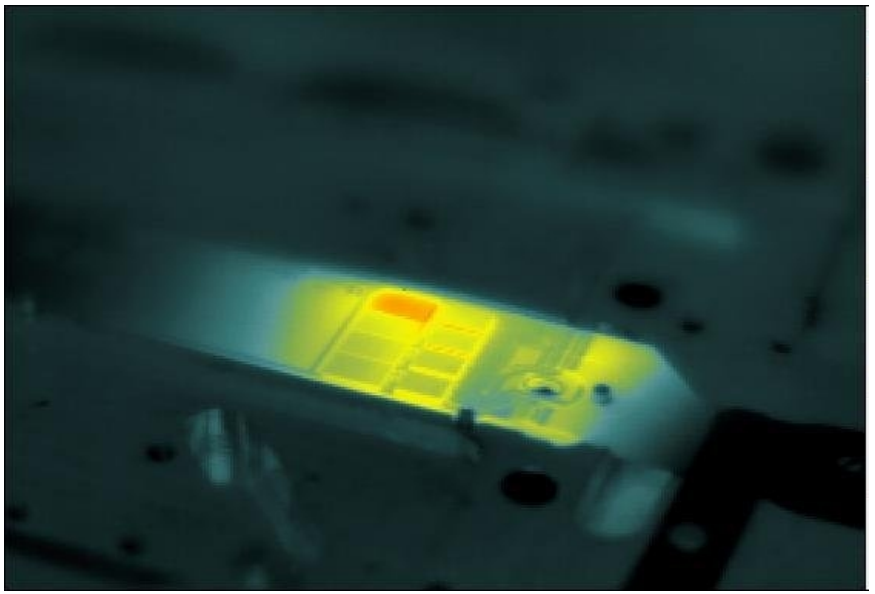
- EMCM fully populated (W31-3)
  - 4 DCDBPipeline
  - 4 DHPT1.0
  - 6 SwitcherB1.8G
- Kapton, Infiniband, CAT6
- DHE
- Belle II Power Supply
- Cooling plate



Setup – X ray chamber

Operation

irradiation steps:
0.5, 0.75, 1.0, 1.5, 2.0, 3.0, 5.0, 10.0, 20.0 Mrad



- DHPT core voltage @ 1.62V during measurements to have full 76.2 MHz GCK clock
  - thus delay inverter pairs operate faster

    -> smaller delay times per delay element
- during irradiation DHPT powered @ 1.2V
- after each irradiation step, before measurements:

  complete power cycle (EMCM, DHE, PS, PC)

Part 1:

Data Delay Measurements

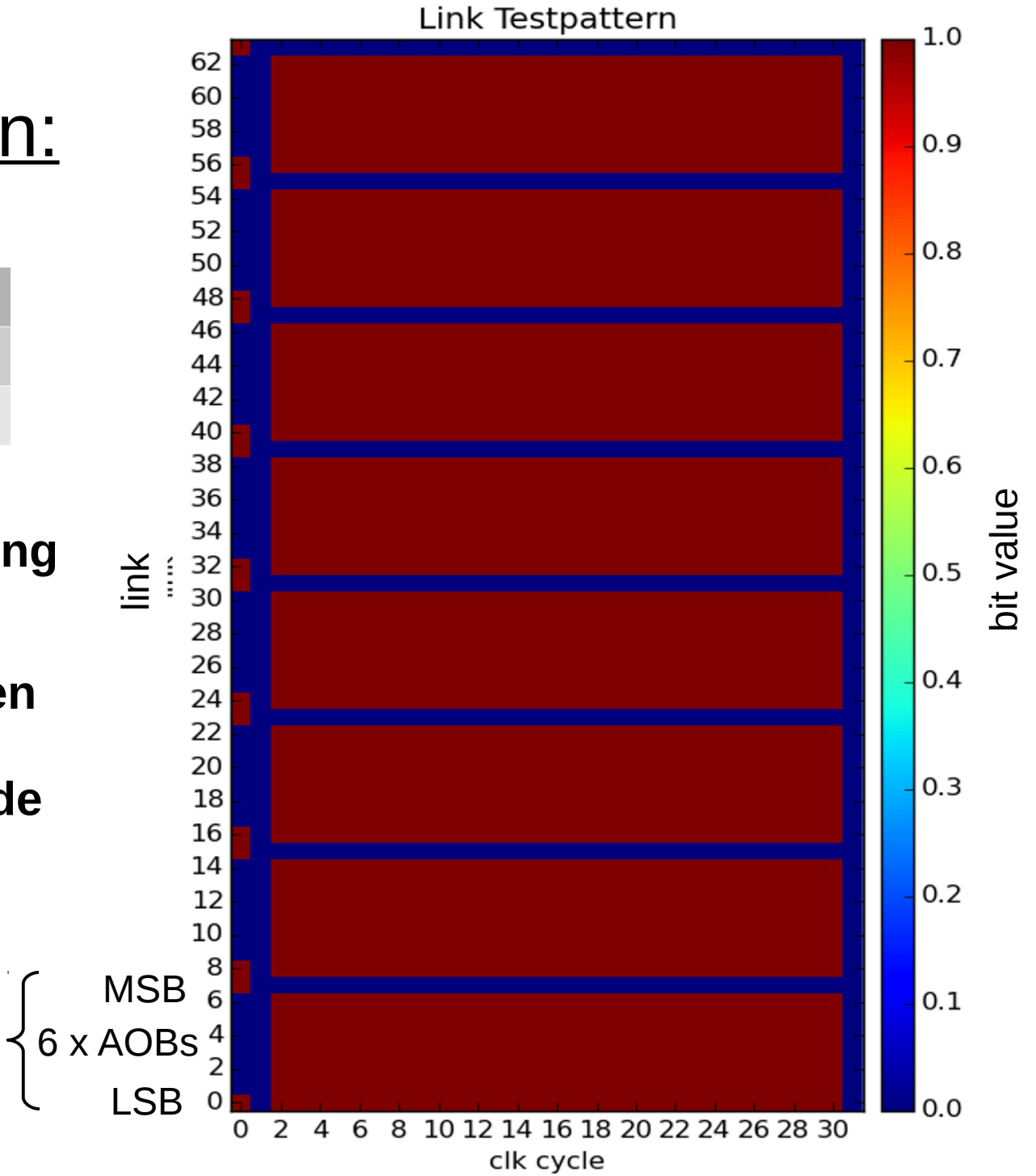
DCD testpattern:

LSB	1 0 1 1 1 ... 1 1 1 0
AOBs	0 0 1 1 1 ... 1 1 1 0
MSB	1 0 0 0 0 ... 0 0 0 0

32 clock cycles long

:-64 digital links between DCD-DHP
:-8 links sent a ADC code per clock period.

DCD column pair



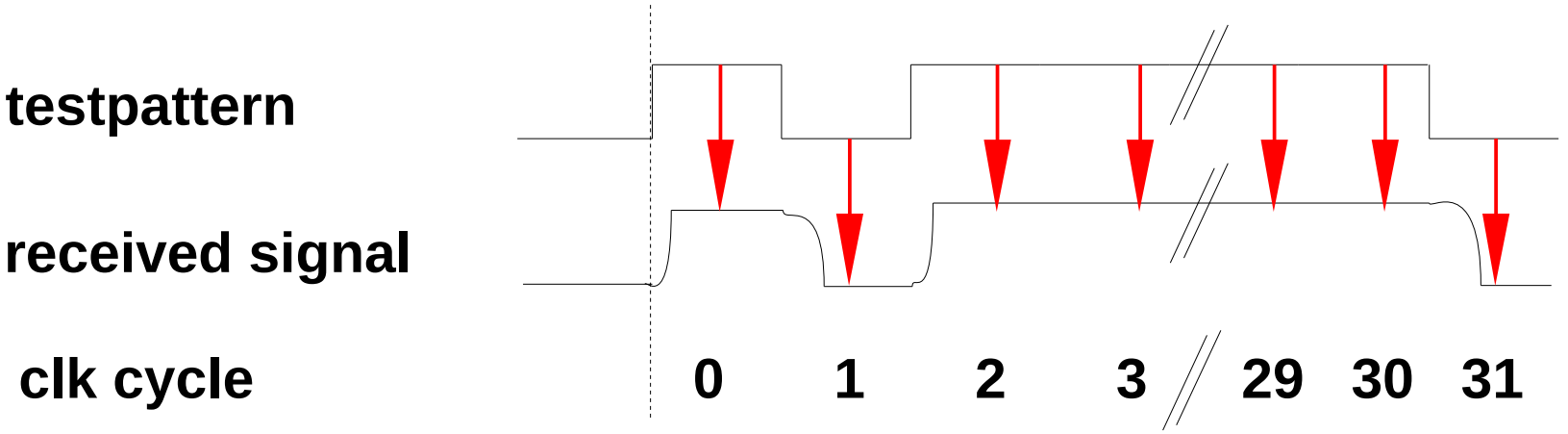
testpattern repeats after 32 clock cycles

Bit error measurements

consider one LSB link

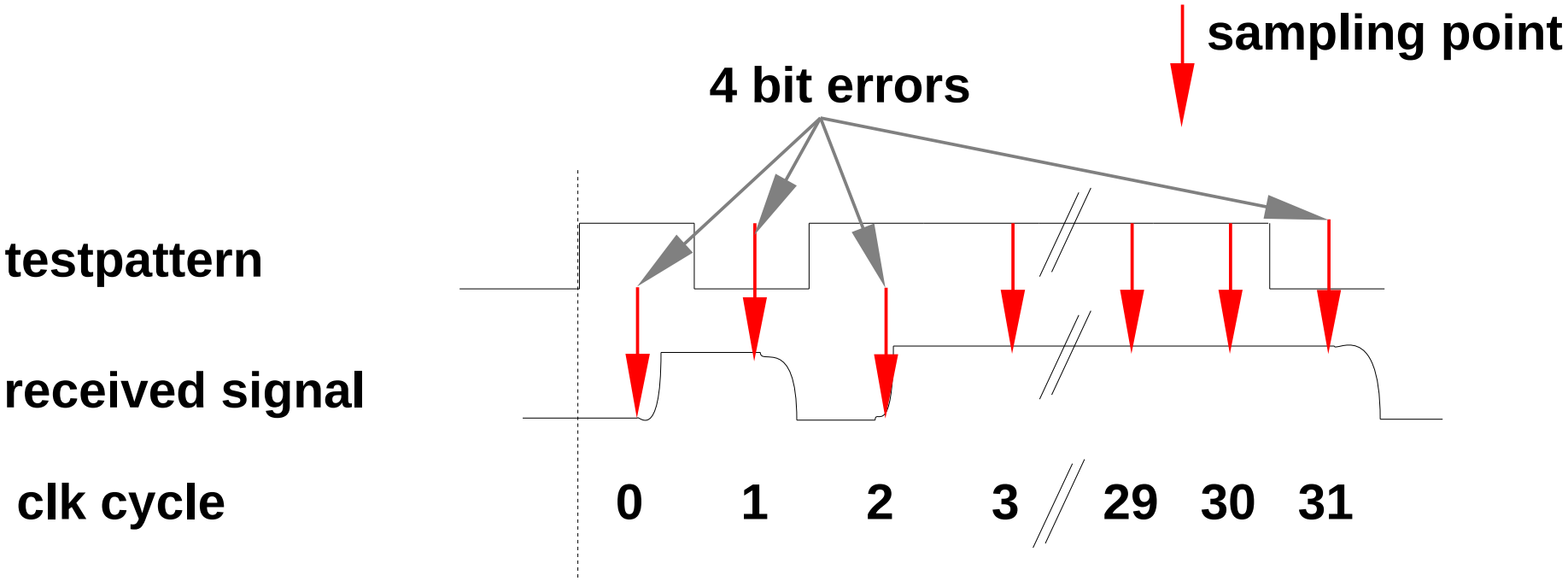
0 bit errors

sampling point



-> all bits received correctly at DHPT

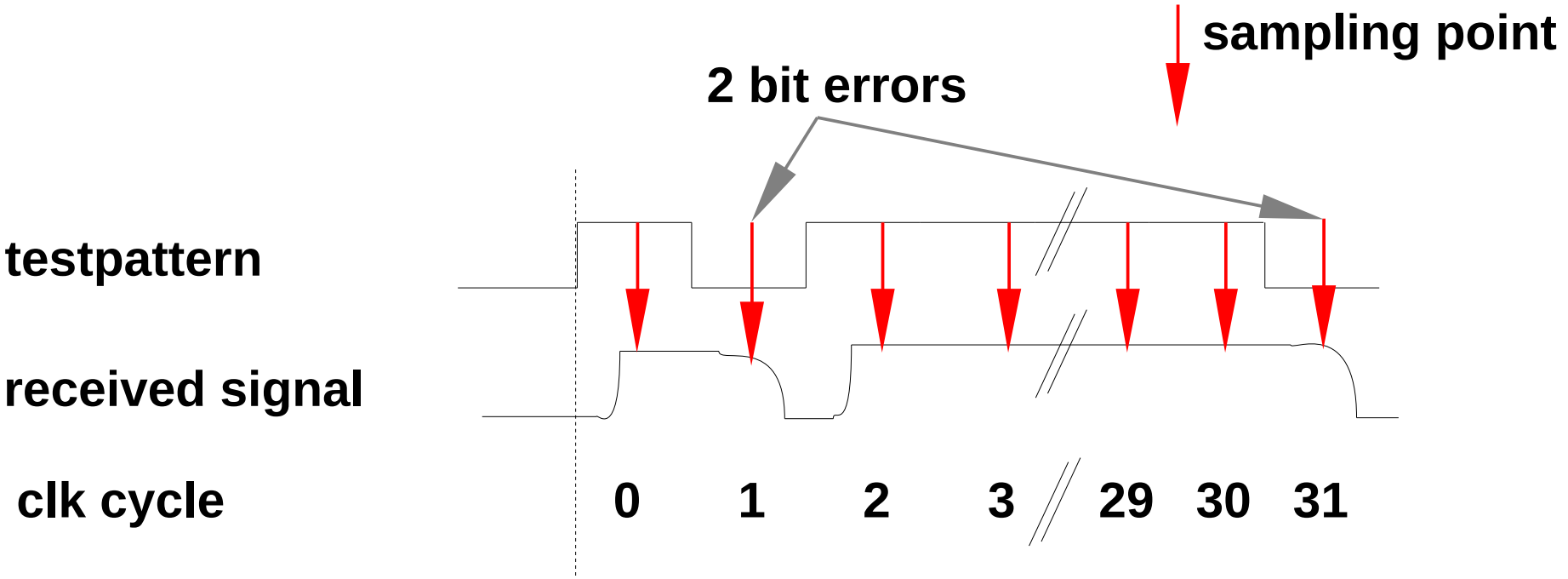
Bit error measurements



→ **received signal phase shifted with delay elements**

→ **too large delay, four bits are wrong (maximal 4 bit error, all edges wrong)**

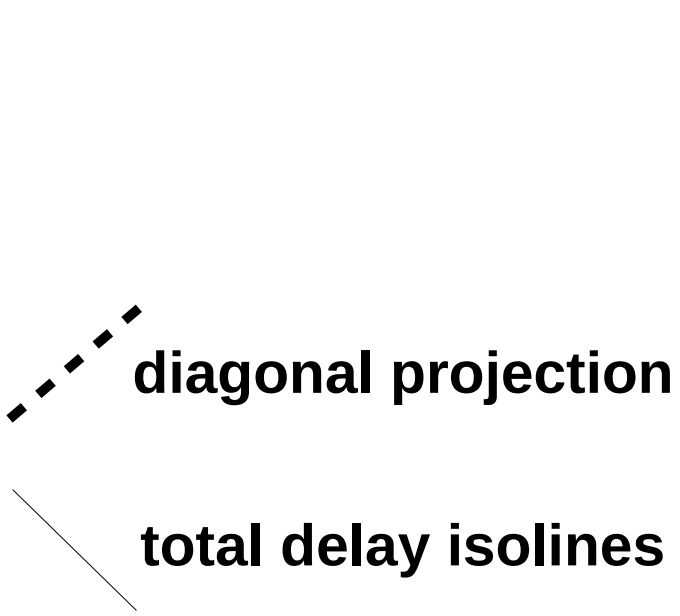
Asymmetry effect

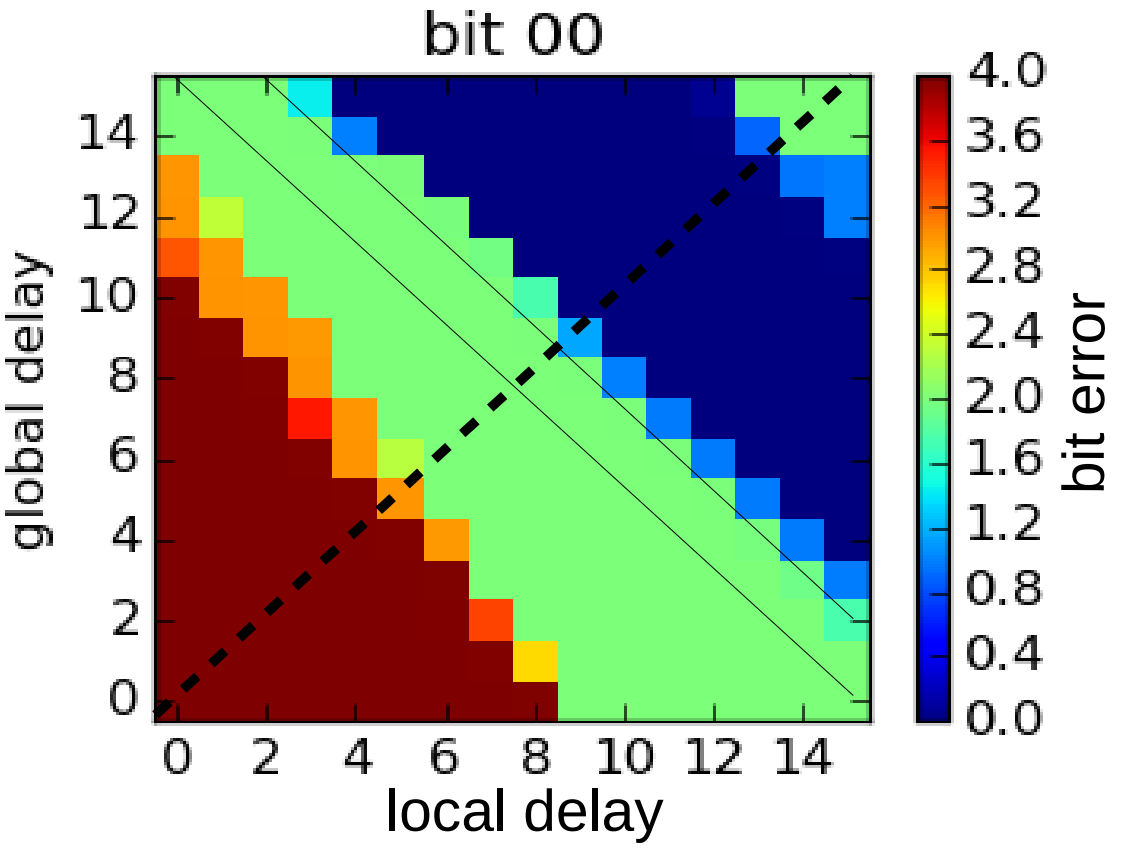


-> here: falling edge slower than rising edge,
at some delay point falling edges are already wrong,
while rising edges are still right (asymmetry)

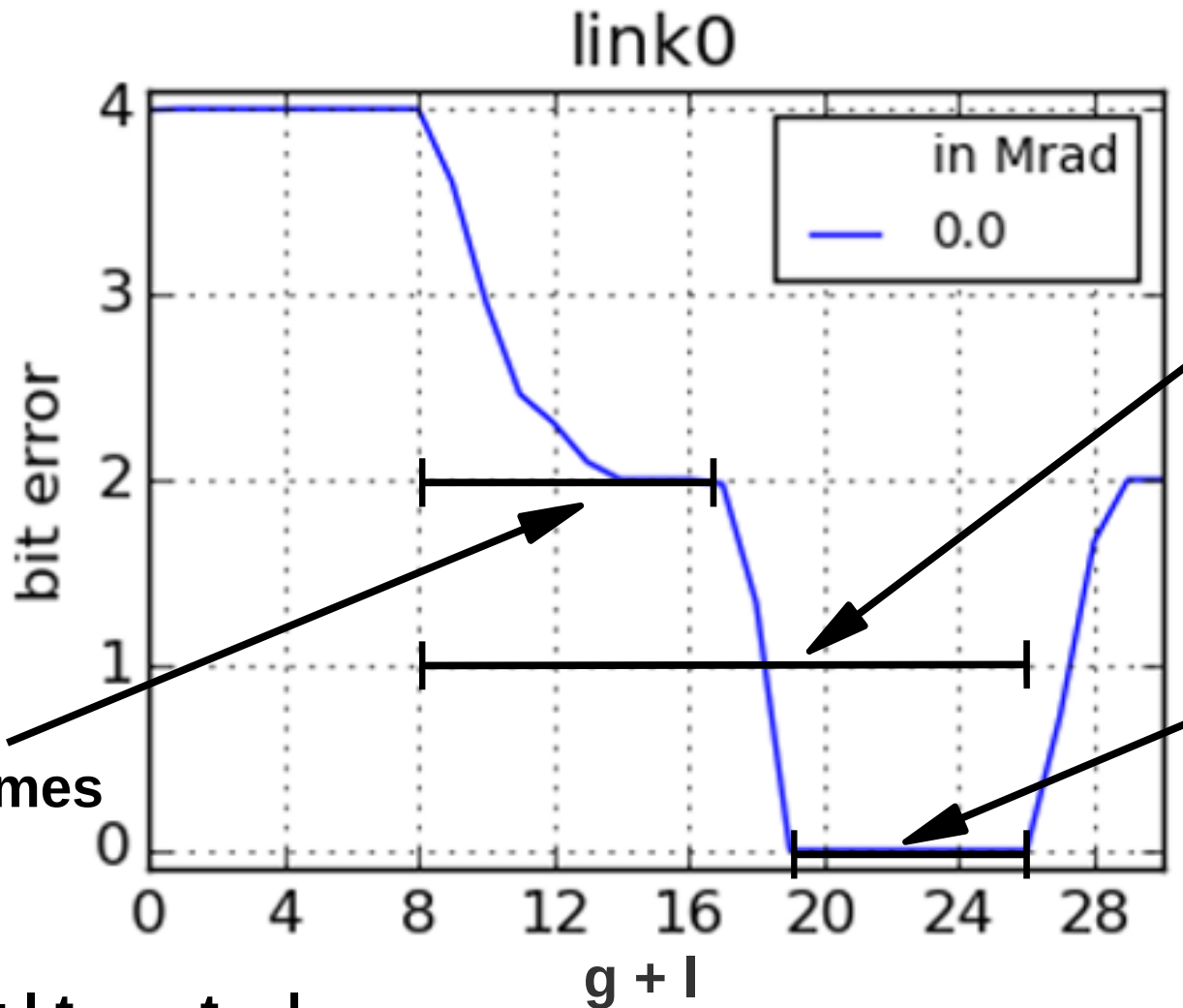
2D delay Scan

- **scan global and local delay settings**
- **compute bit errors for several readings**
- **(anti) diagonals have equal total delay**





Delay Scan



one clock period (~ 3.2 ns)

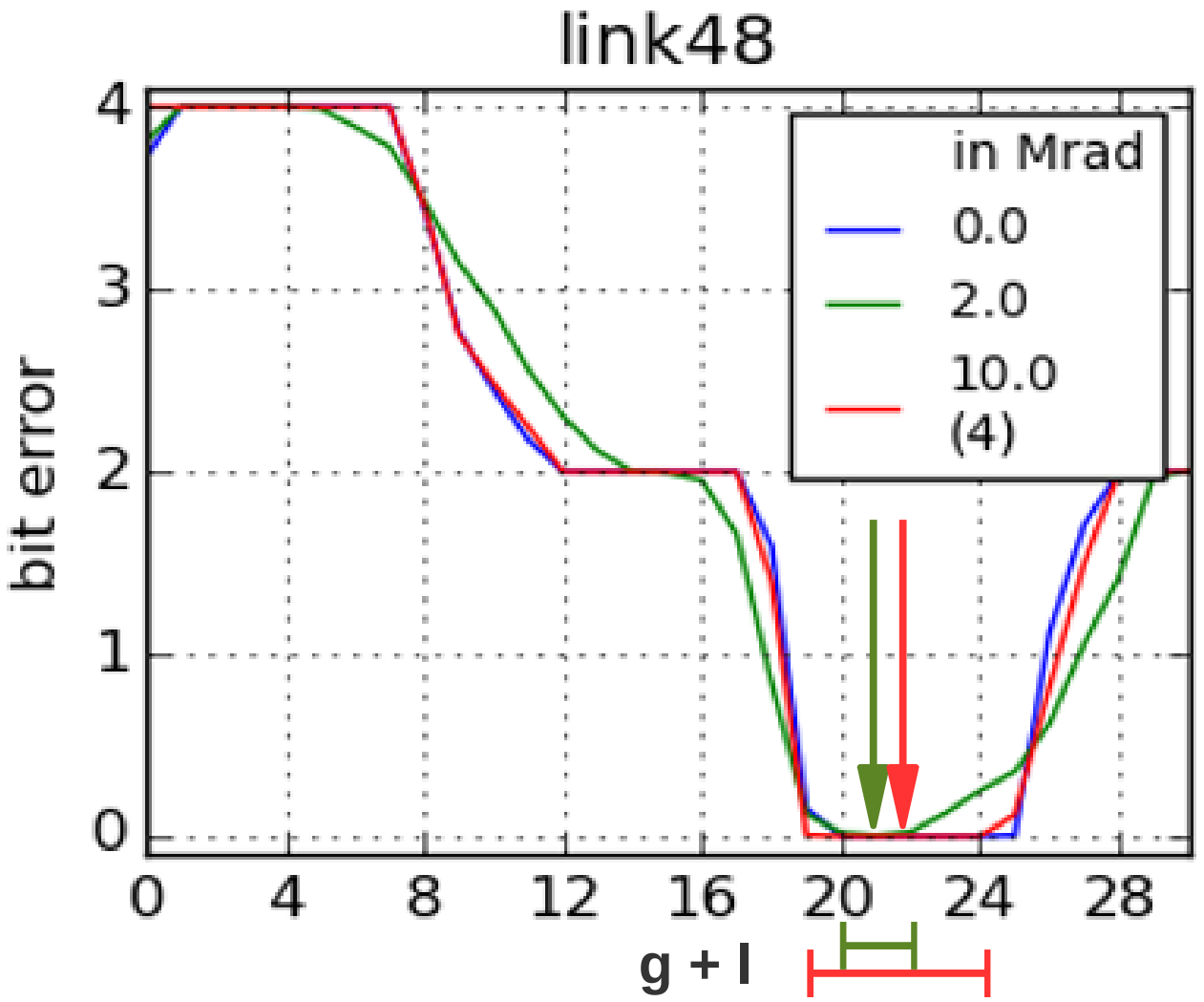
delay tolerance

difference of rise and fall times

asymmetry := | t_{fall} – t_{rise} |

g + l = total delay in # inverter units

Irradiation effects (typical link)



from 0Mrad to 10Mrad

- no change

@ 2Mrad

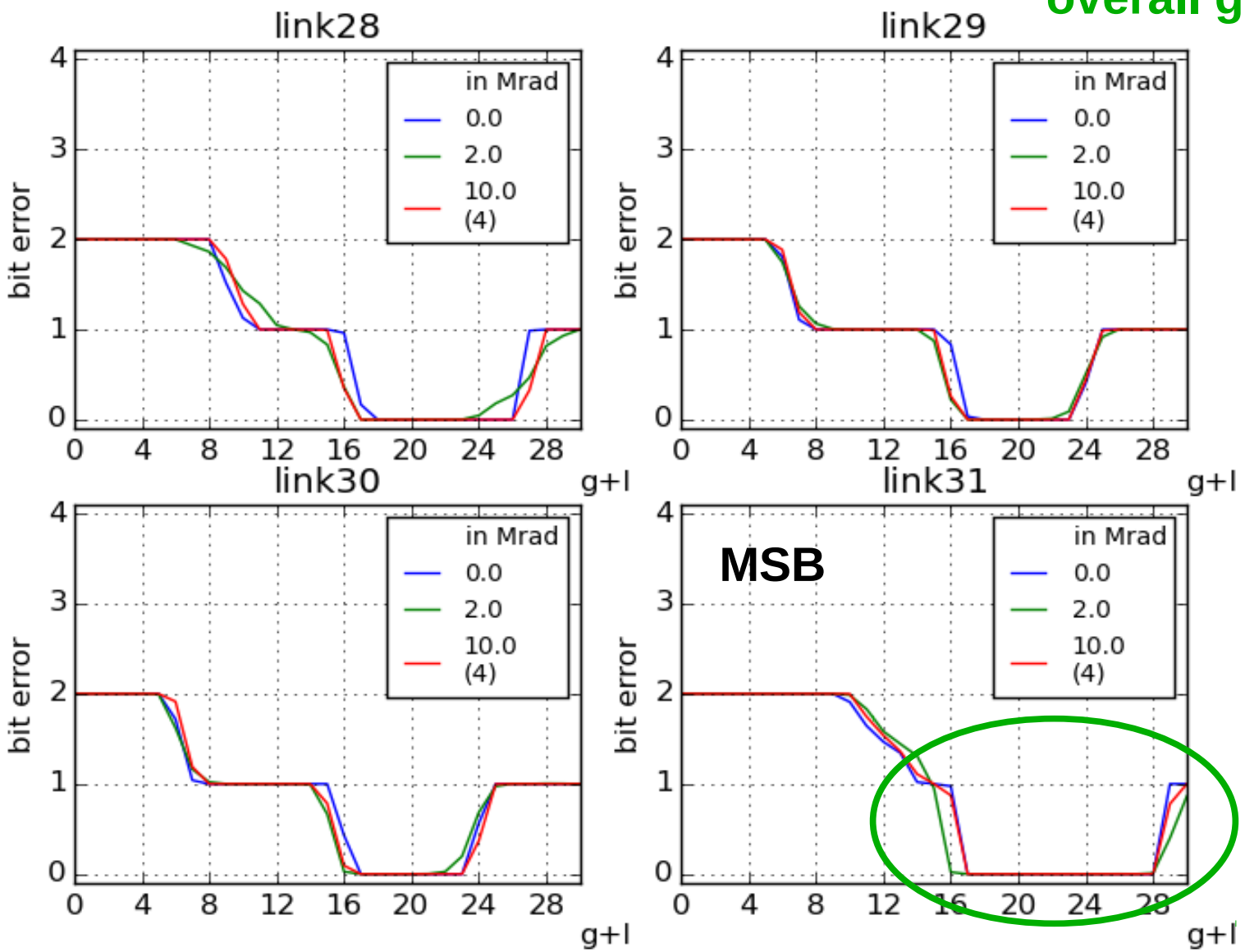
- delay tolerance shrinks

- asymmetry grows

- optimal delay shifted

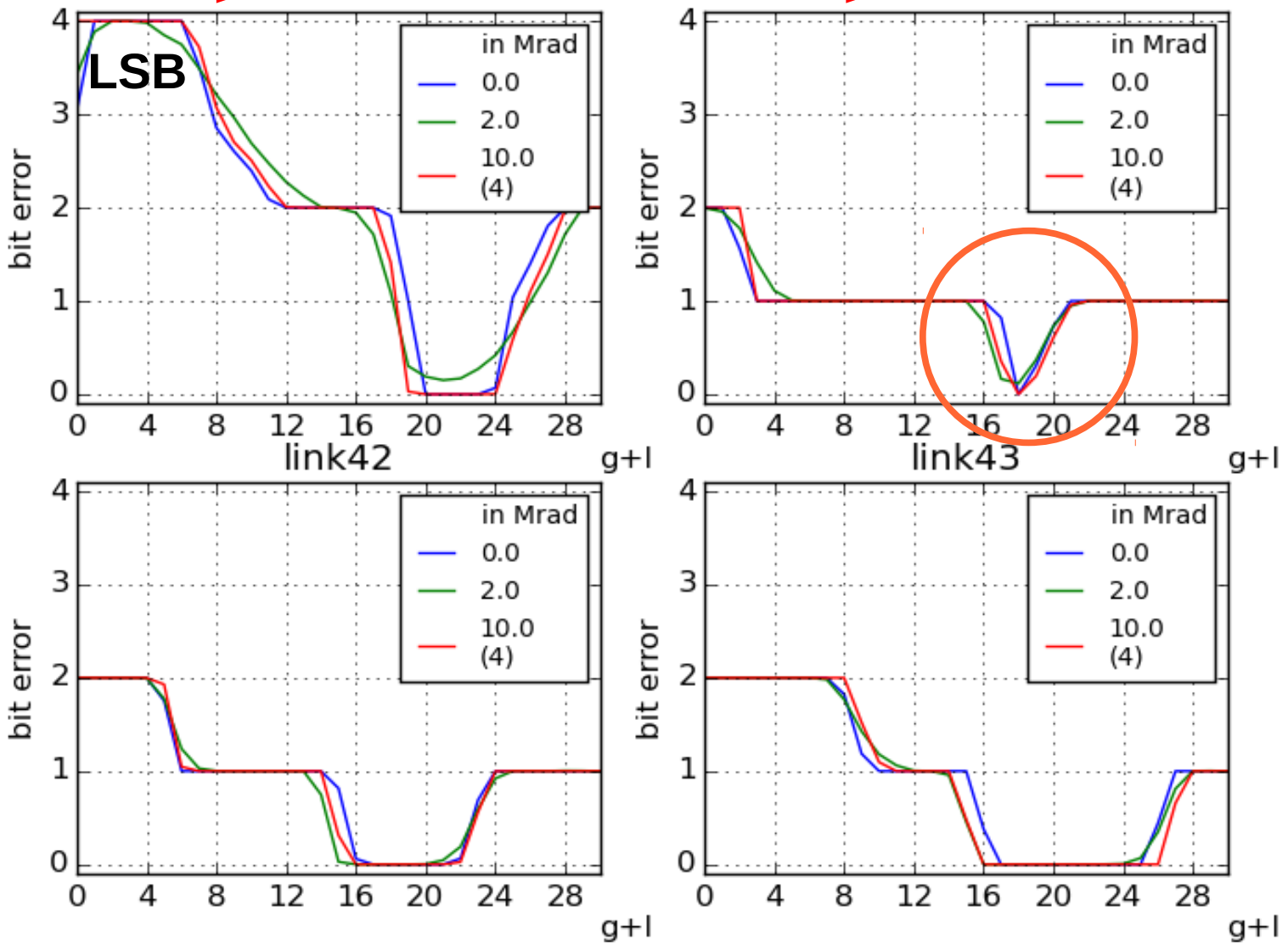
Delay scan
Variation between links

overall good link

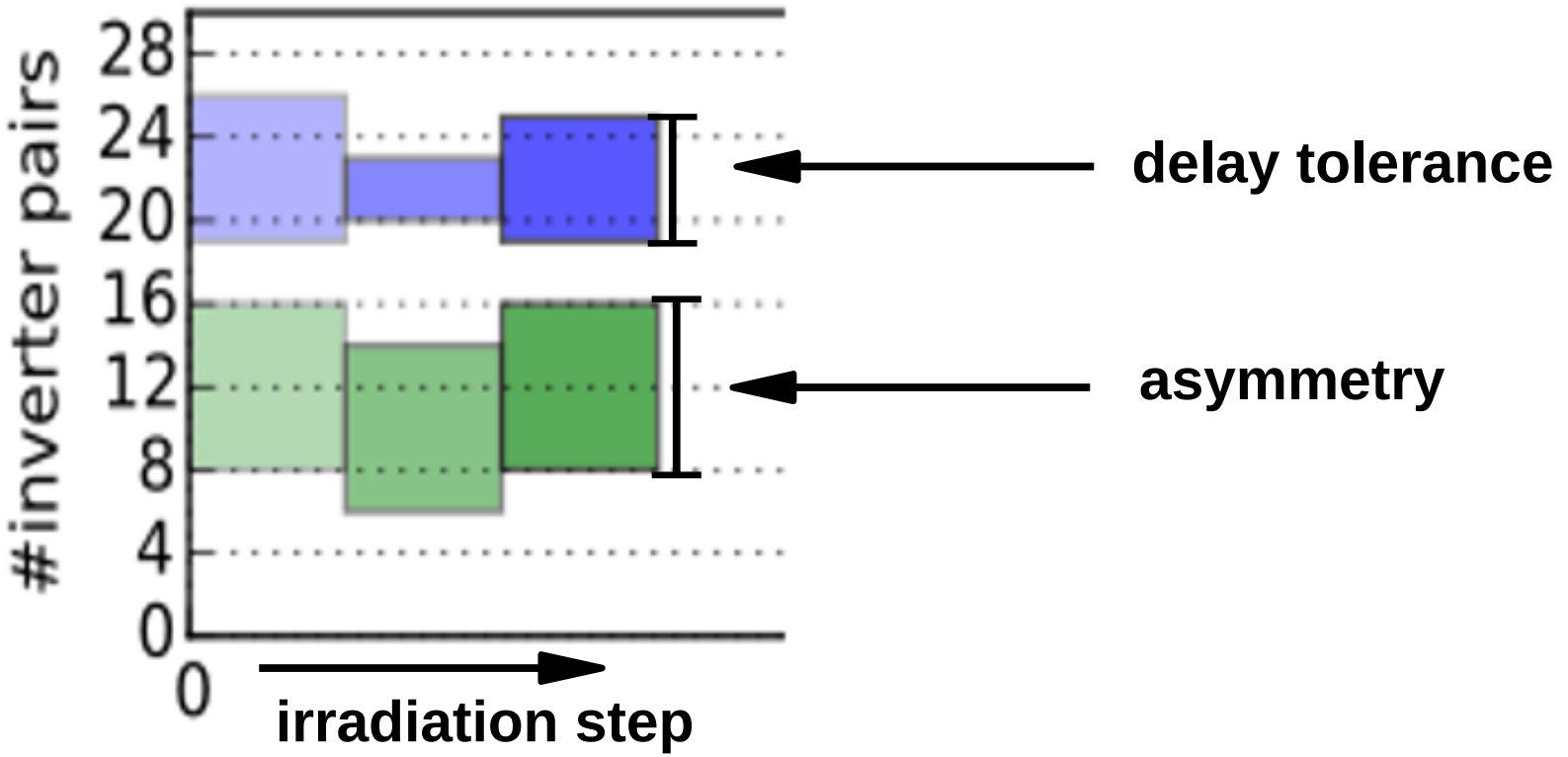


Delay Scans
Few links behave badly

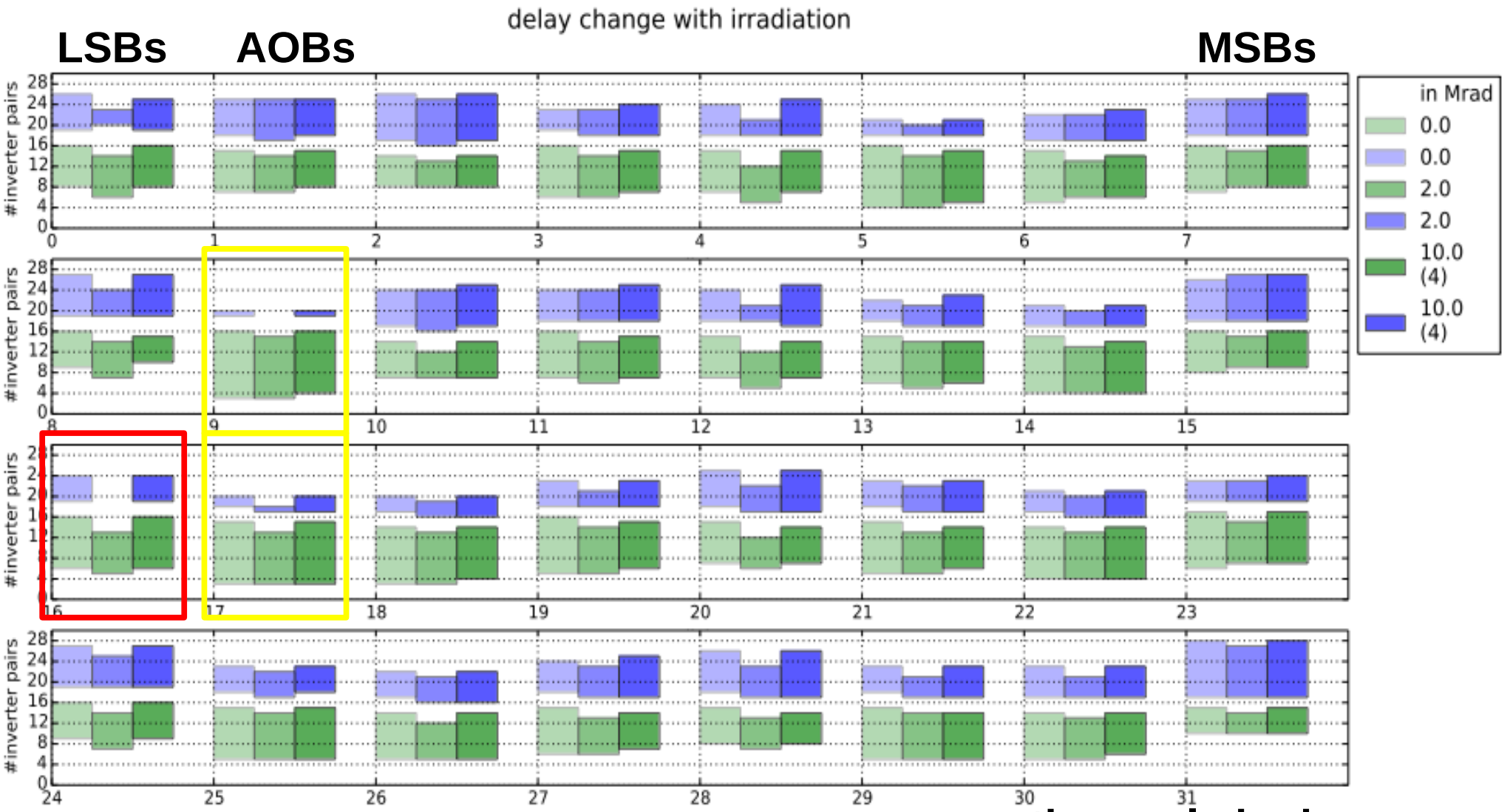
fails for 2 Mrad → link40 **fails for 2 Mrad** → link41



Delay Scans Analysis



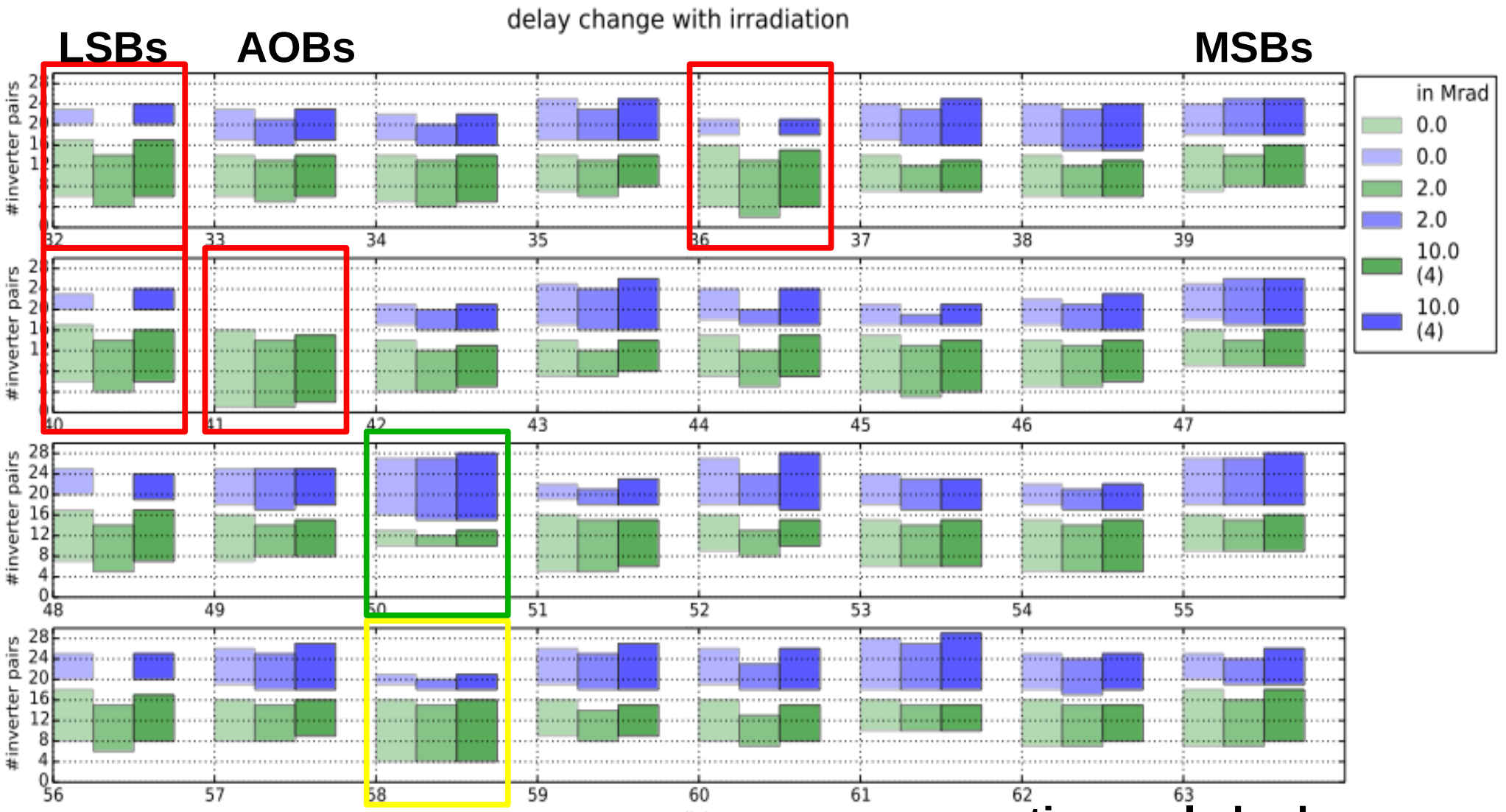
Tolerance + Asymmetry Irradiation Analysis



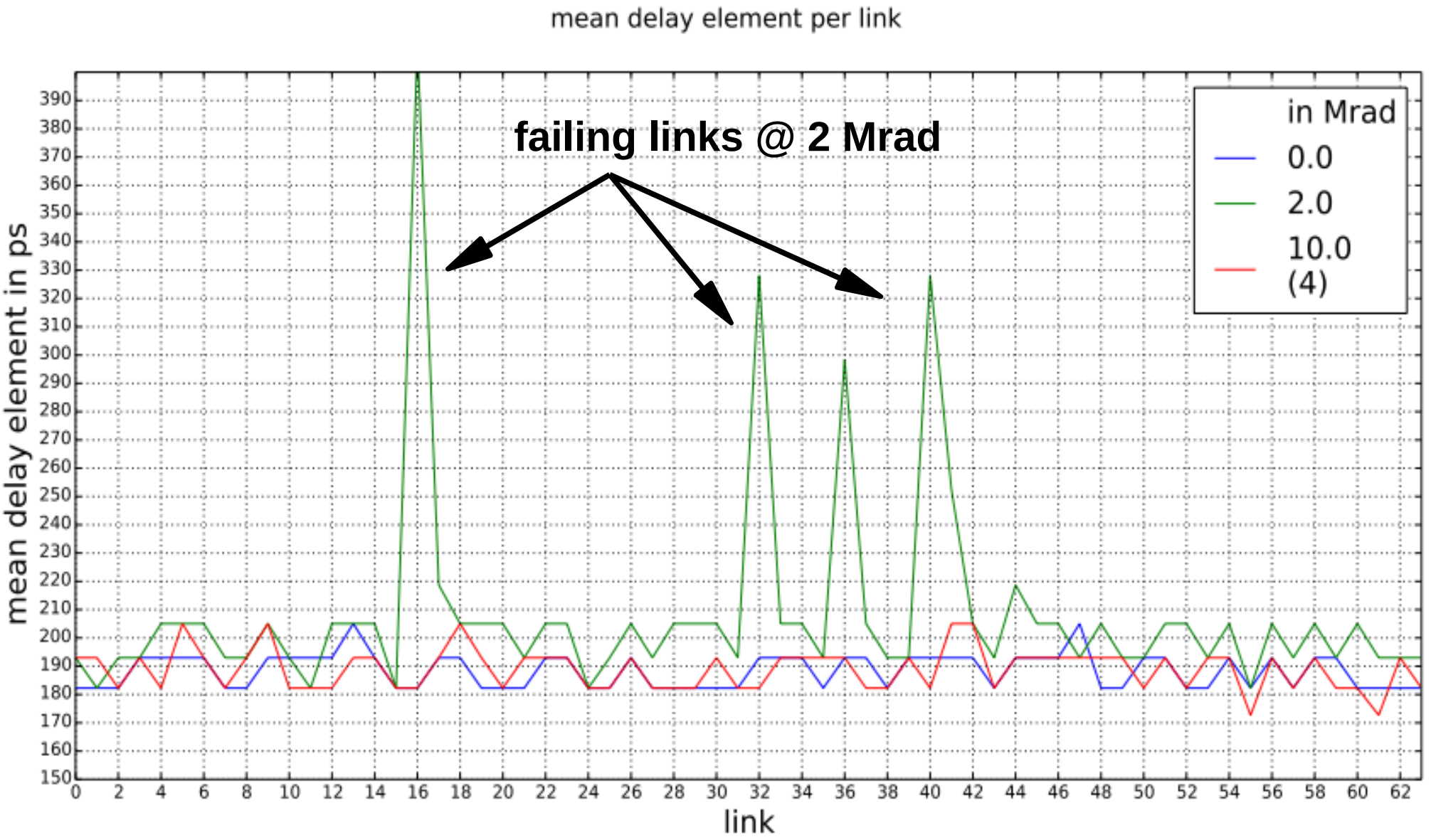
failing for 2 Mrad

continuously bad, but not failing links

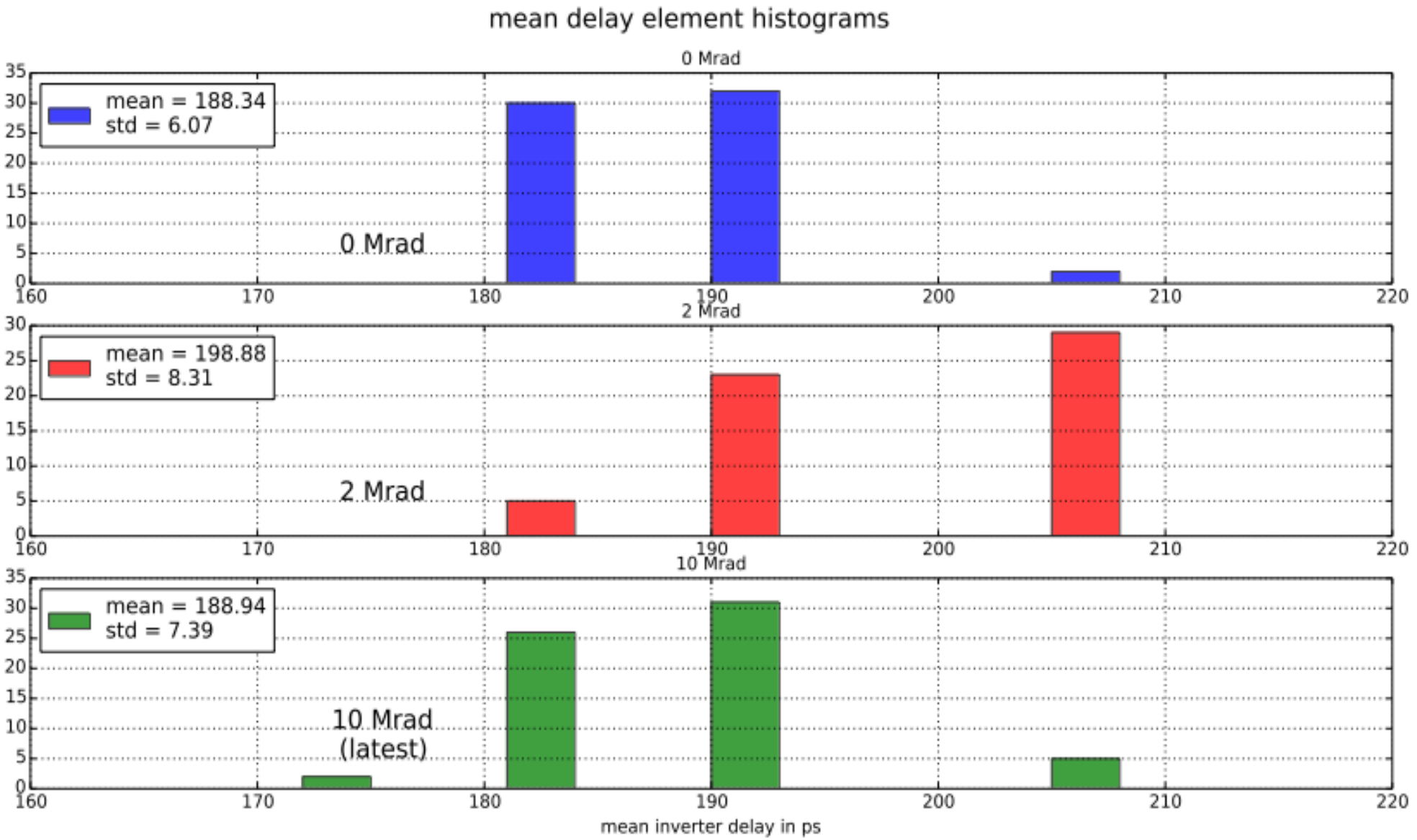
Tolerance + Asymmetry Irradiation Analysis



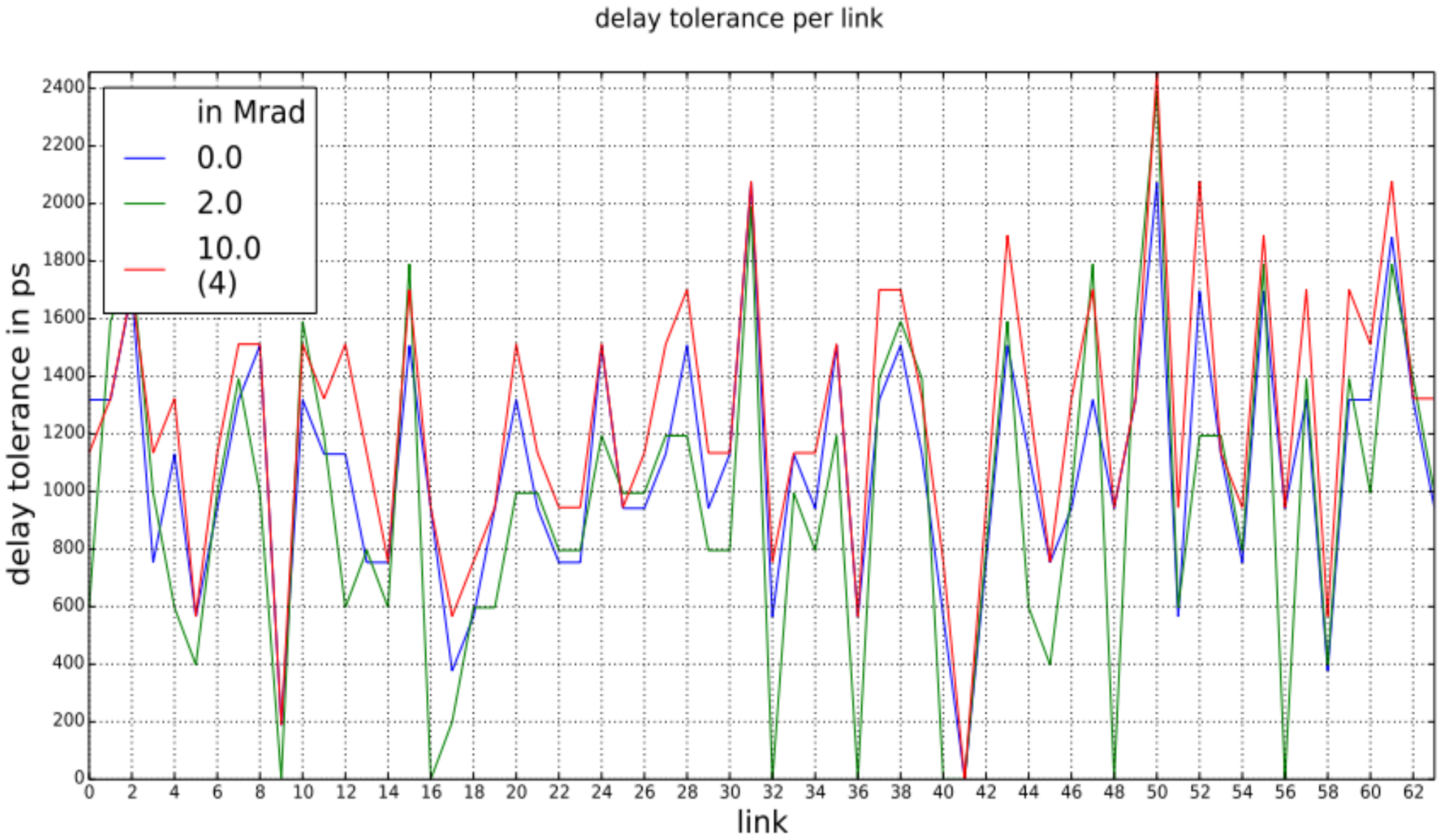
Delay Time Extraction



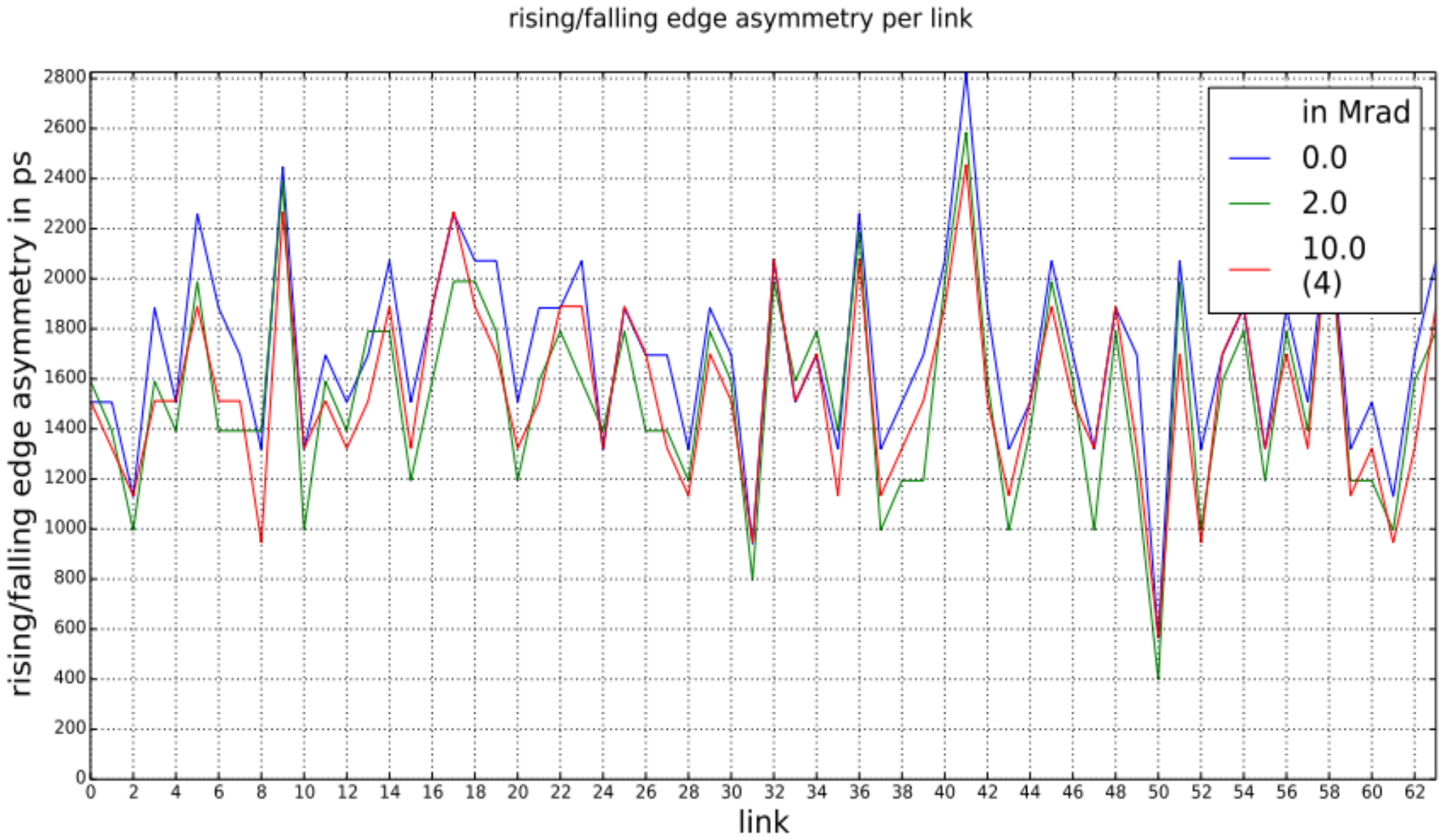
Delay Time Extraction



Delay Tolerance Extraction



Asymmetry Extraction

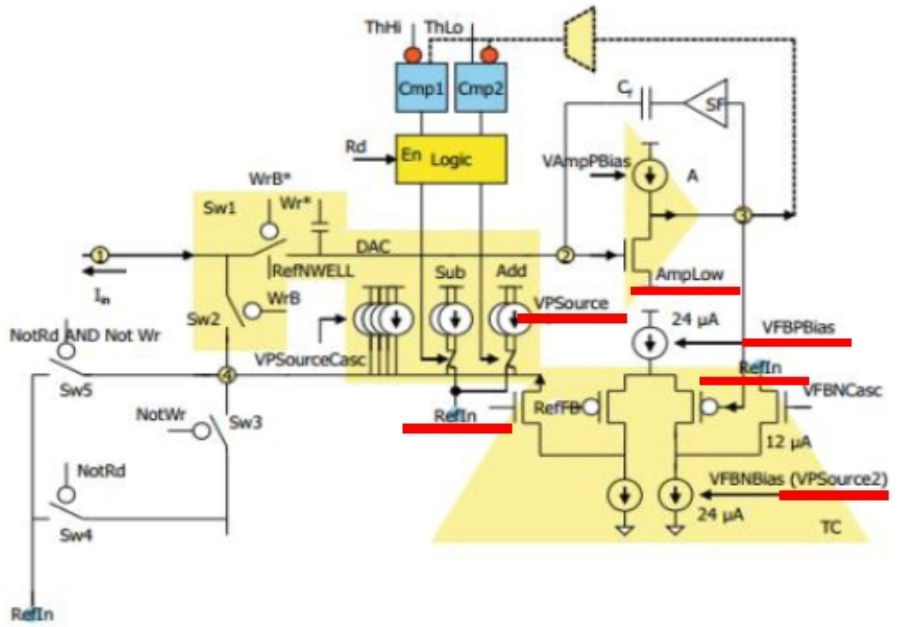


Part 2:

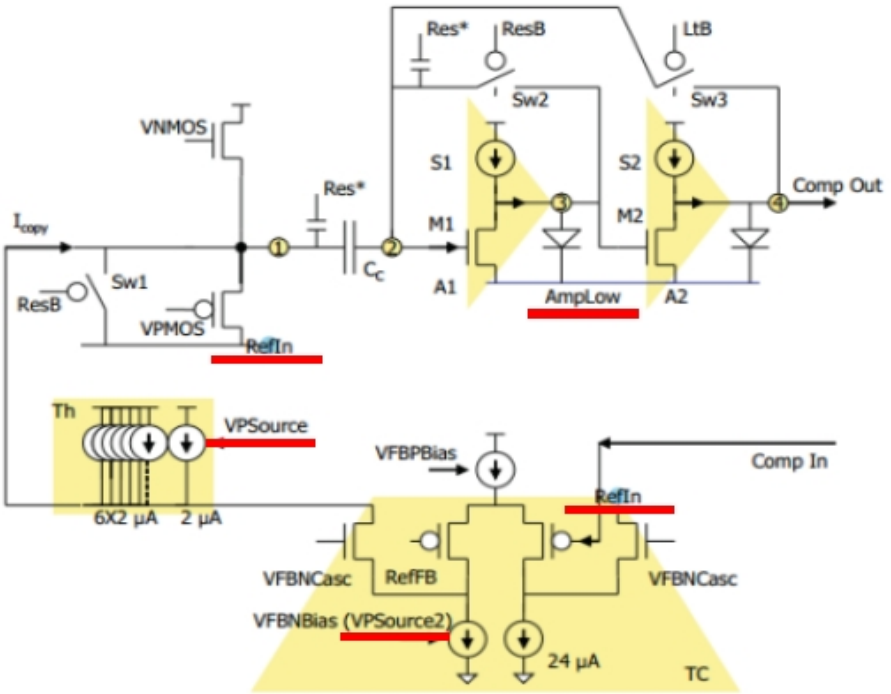
ADC Measurements

DCD parameter optimization

- Detailed scan over most important voltages and DACs for 8 ADC channels
- Scan over 256 ADC channels for nominal voltages and DACs



Current Memory Cell in the ADC



Comparator in the ADC

Scans & measurements

Gain 1: 'low gain' LSB = 115nA
Gain 2: 'high gain' LSB = 72nA

~10h measurements after each Irradiation step

	refin (Voltage)	amplow (Voltage)	ipsource (DAC)	ipsource2 (DAC)	ifbpbias (DAC)	gain	channels
refin vs. amplow	700 - 1100mV	200-600mV	105	100	90	1,2	8
ipsource vs. ipsource2	800mV	450mV	80-110	80-110	90	1,2	8
ifbpbias	800mV	450mV	105	100	60-110	1,2	8
allchannel	800mV	450mV	105	100	90	1,2	256
allchannel2	900mV	350mV	95	90	85	1,2	256

Scans & measurements

Scan 8 DCD channel to find good working point (noise/linearity)

	refin (Voltage)	amplow (Voltage)	ipsource (DAC)	ipsource2 (DAC)	ifbpbias (DAC)	gain	channels
refin vs. amplow	700 - 1100mV	200-600mV	105	100	90	1,2	8
ipsource vs. ipsource2	800mV	450mV	80-110	80-110	90	1,2	8
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allchannel	800mV	450mV	105	100	90	1,2	256
allchannel2	900mV	350mV	95	90	85	1,2	256

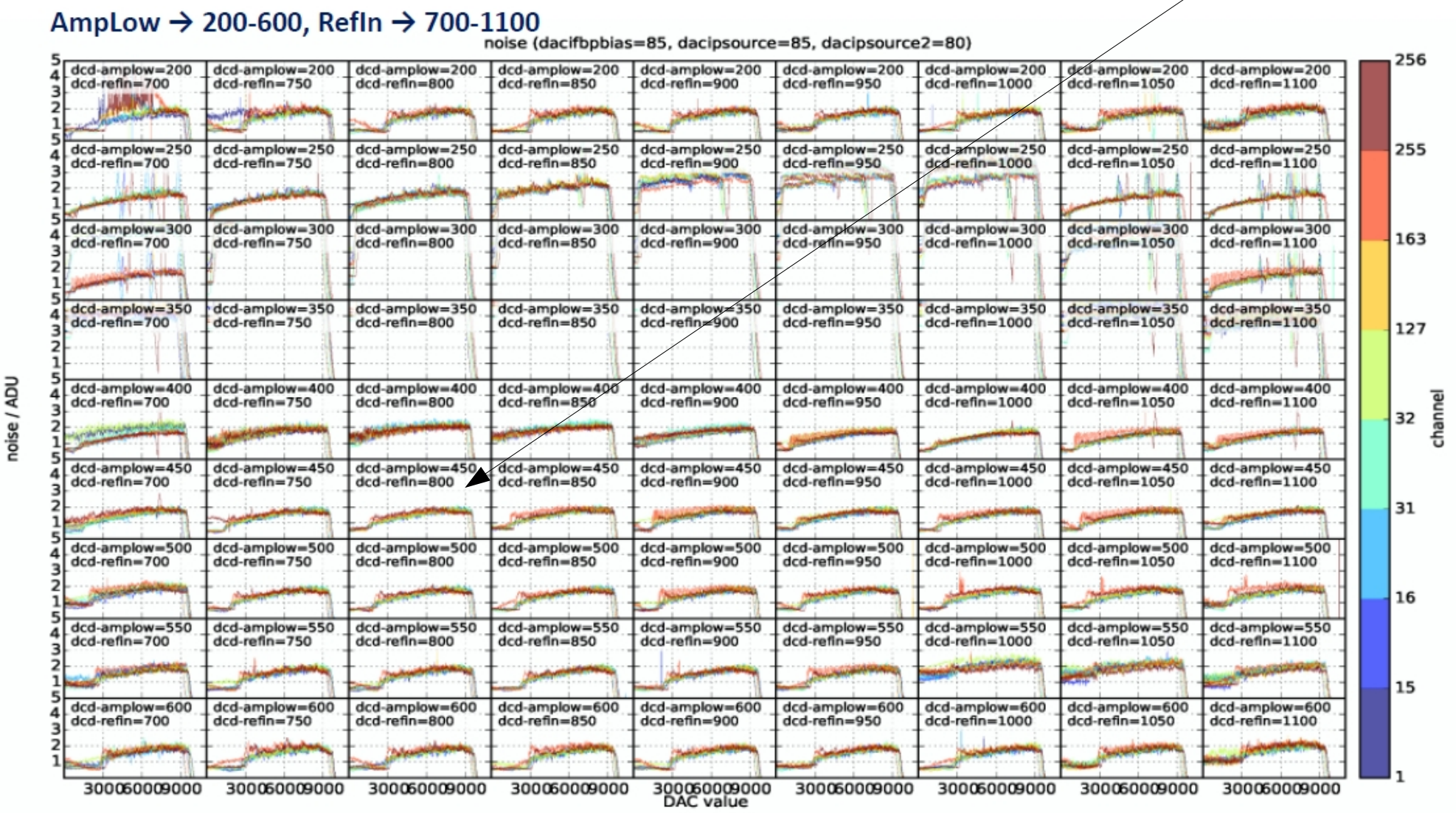
Scans & measurements

Scan all channels for two working points
:- allchannel1: baseline parameters before irradiation
:- allchannel2: optimized parameters after 0.75Mrad

	refin (Voltage)	amplow (Voltage)	ipsource (DAC)	ipsource2 (DAC)	ifbpbias (DAC)	gain	channels
refin vs. amplow	700 - 1100mV	200-600mV	105	100	90	1,2	8
ipsource vs. ipsource2	800mV	450mV	80-110	80-110	90	1,2	8
ifbpbias	800mV	450mV	105	100	60-110	1,2	8
allchannel	800mV	450mV	105	100	90	1,2	256
allchannel2	900mV	350mV	95	90	85	1,2	256

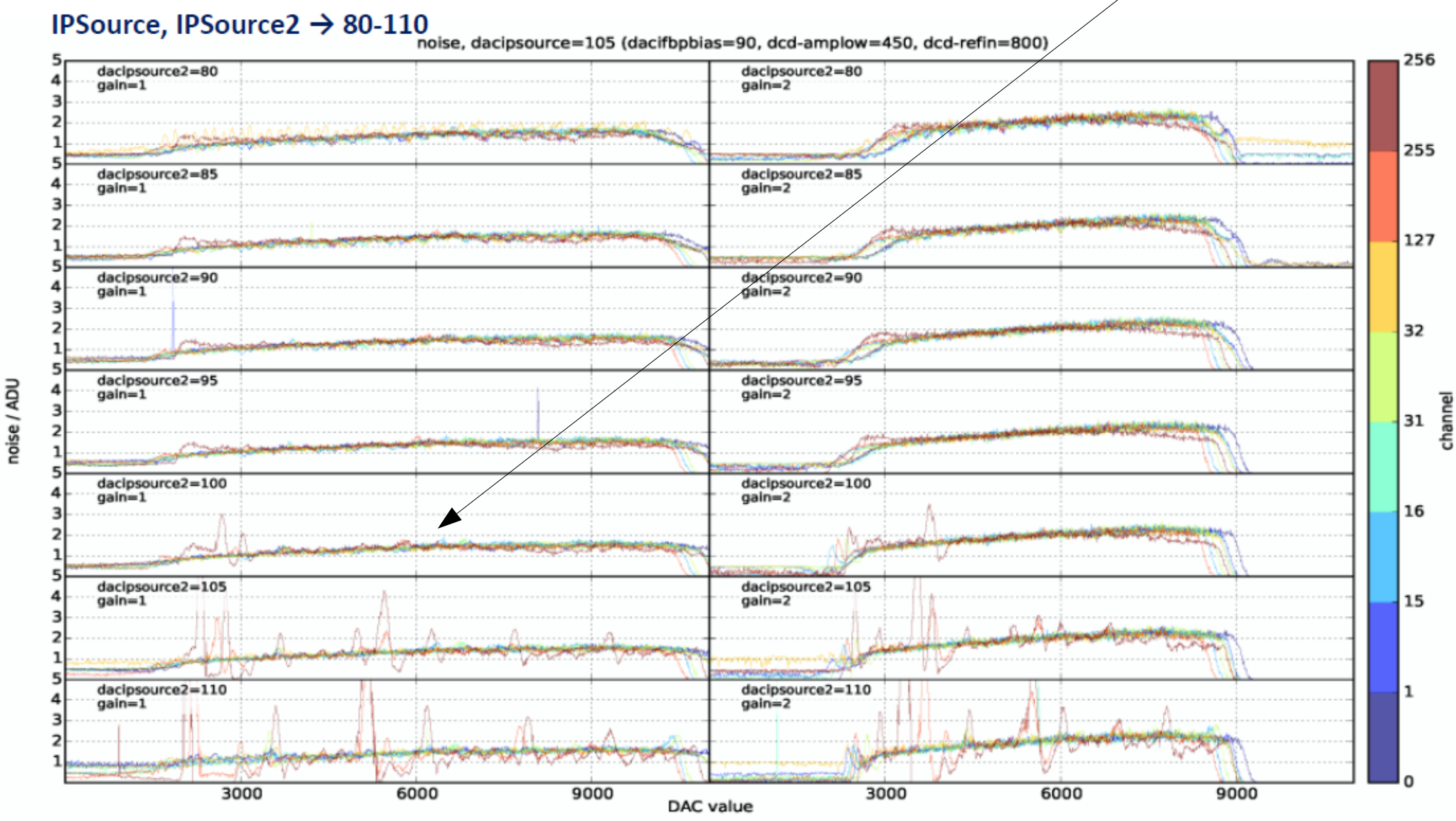
Refin vs. Amplow scan (before irradiation)

Selected point

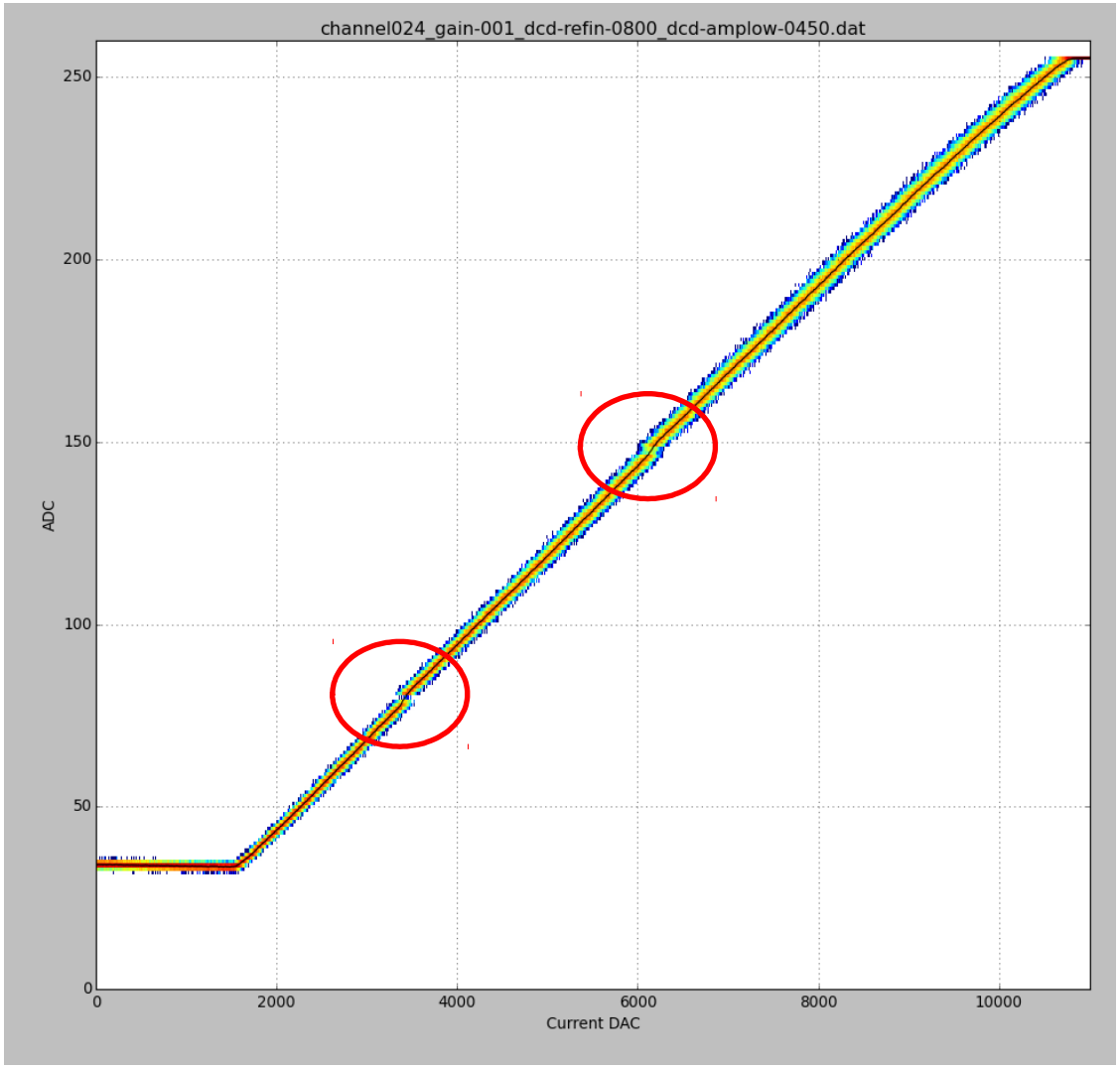


IPSource vs IPSource2 (before irradiation)

Selected point



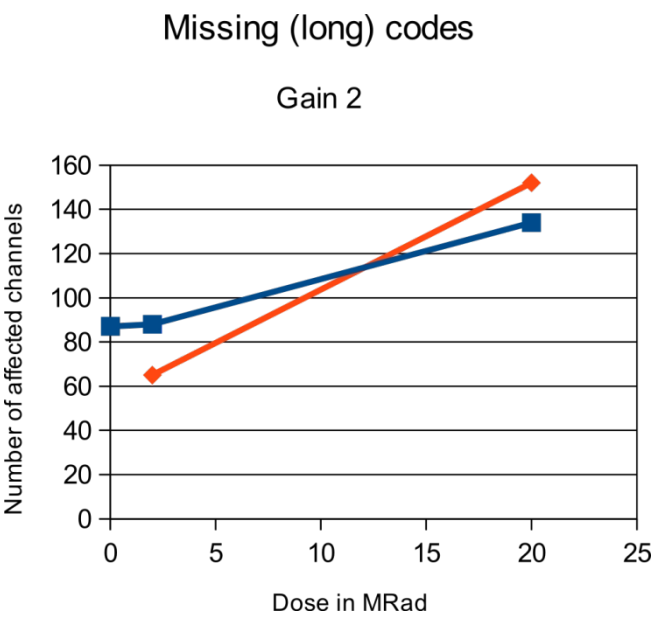
Missing (long) codes



Definition: One or more ADU codes occurred less than 20 times

→ genuine ADC problem

Missing (long) codes



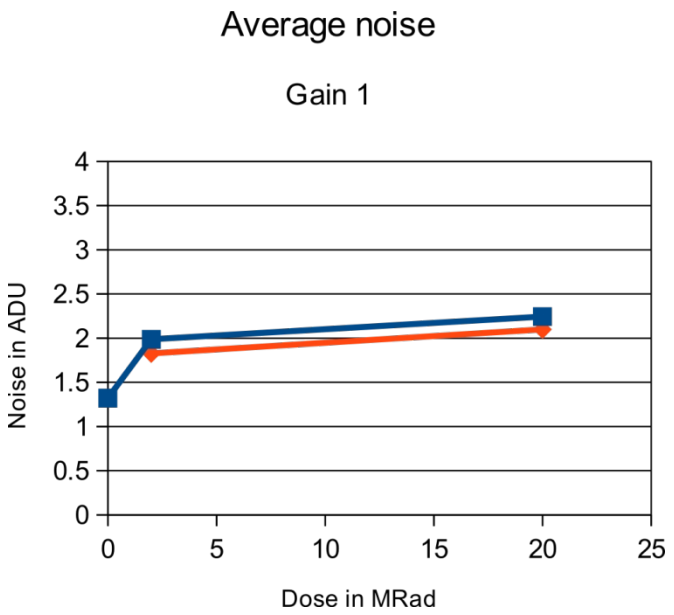
blue:= baseline parameters

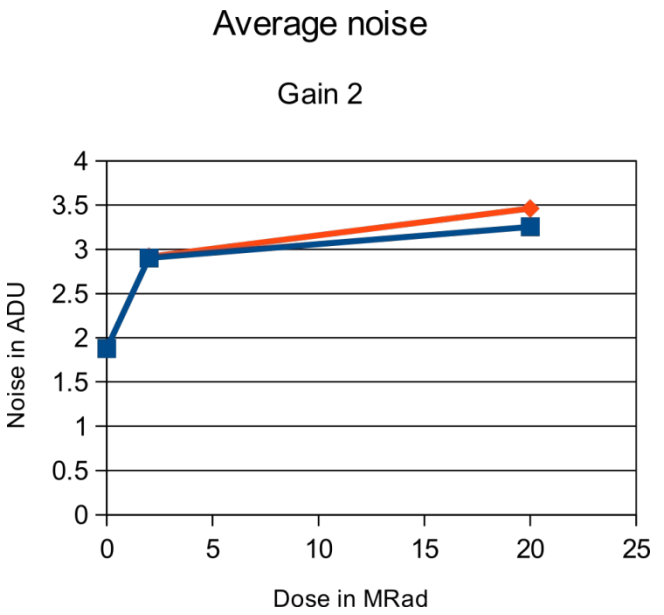
orange:= optimized parameters

:- more channels affected with more irradiation

:- absolute numbers strongly depend on DCD parameters.

Average ADC noise





:- Excluding ADC curves with communication problems

:- Excluding parts of ADC curves with long codes

:- Noise jumps from 0->2Mrad

:- Noise is rather flat for higher Irradiation steps

Conclusion – Delay scans

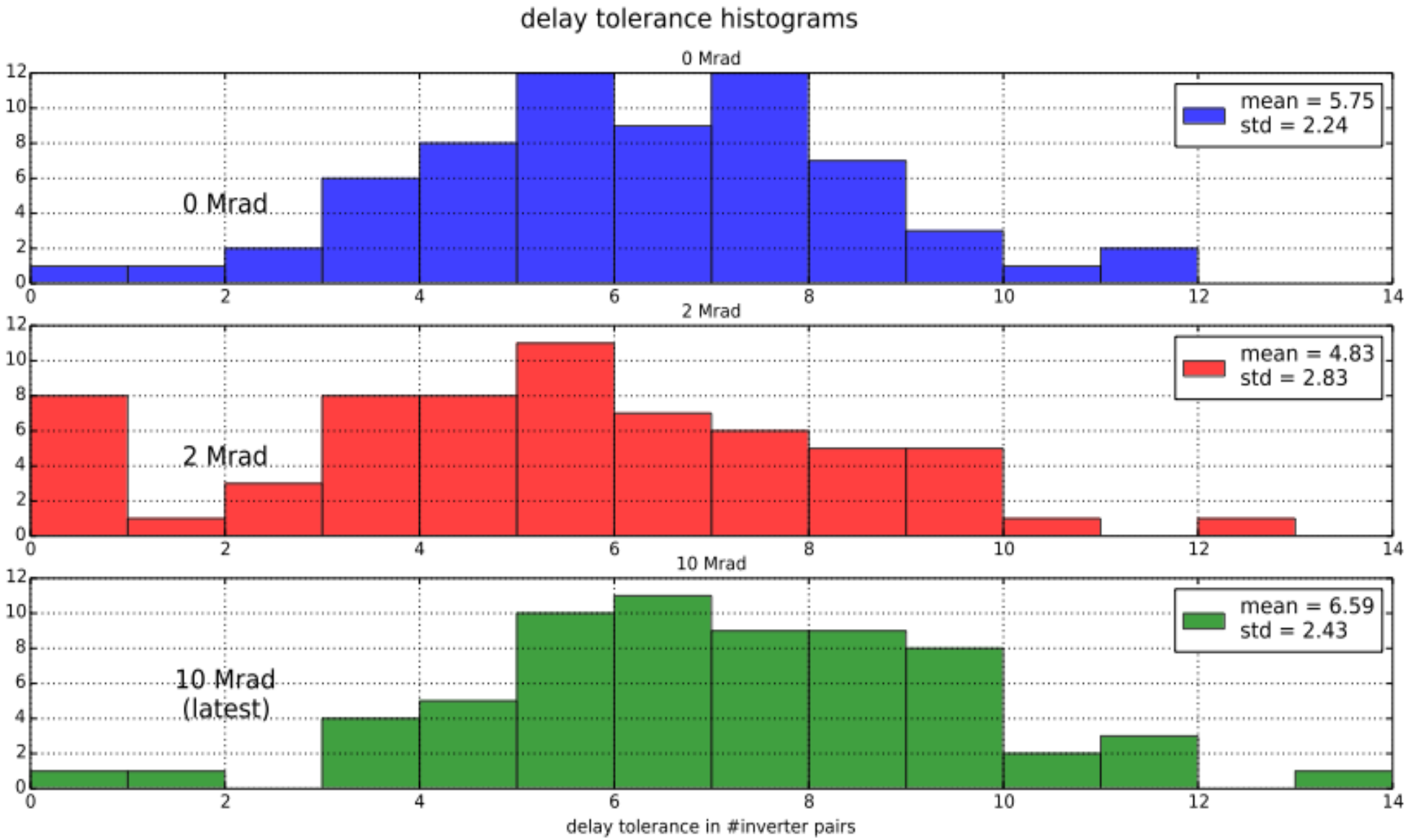
- Irradiation has almost no effect on delay times in DHPT
  - Mean delays time is 190ps @0Mrad and 10Mrad
  - Delays are homogeneous among links
- ~90% of data links show very little irradiation effect
  - Asymmetries and tolerances hardly change with TID
- 6 data links have no optimal delay at @2Mrad
  - These links recover until 10Mrad
  - Possibly irradiation effect (→ shift of transistor properties)

Conclusion – ADC curves

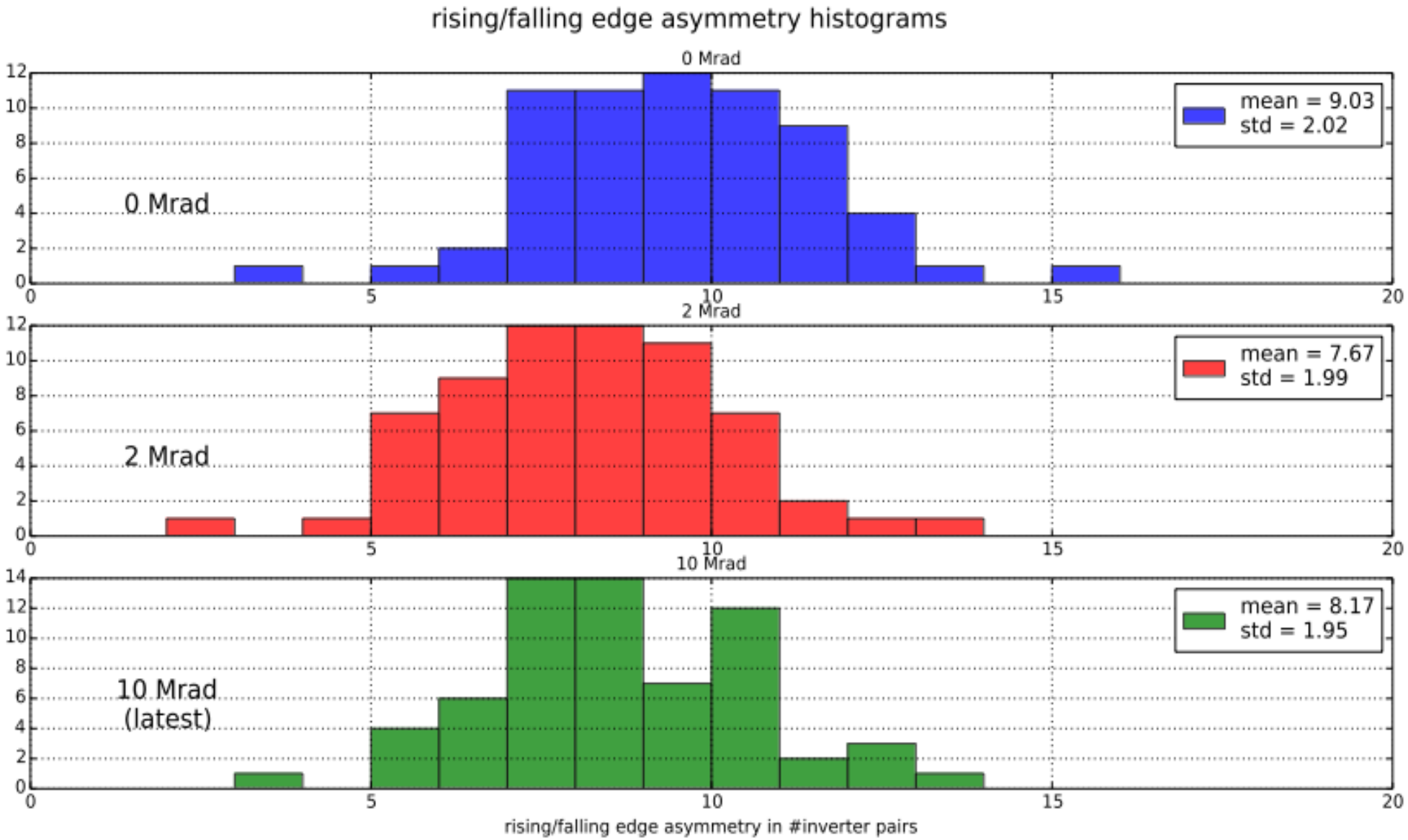
- Good DCD parameters found after all irradiation steps
  - 'Allchannel1' parameters only good <0.75Mrad
  - 'Allchannel2' parameters worked for 0.75-20Mrad
- ADC noise increases from 0->2Mrad but rather flat for higher irradiation steps.
- Number of channels with missing codes seems to increase slightly with irradiation.
- Results are still preliminary:
  - Discovered some setup problems
  - Hard to disentangle/quantify genuine ADC problems

BACKUP

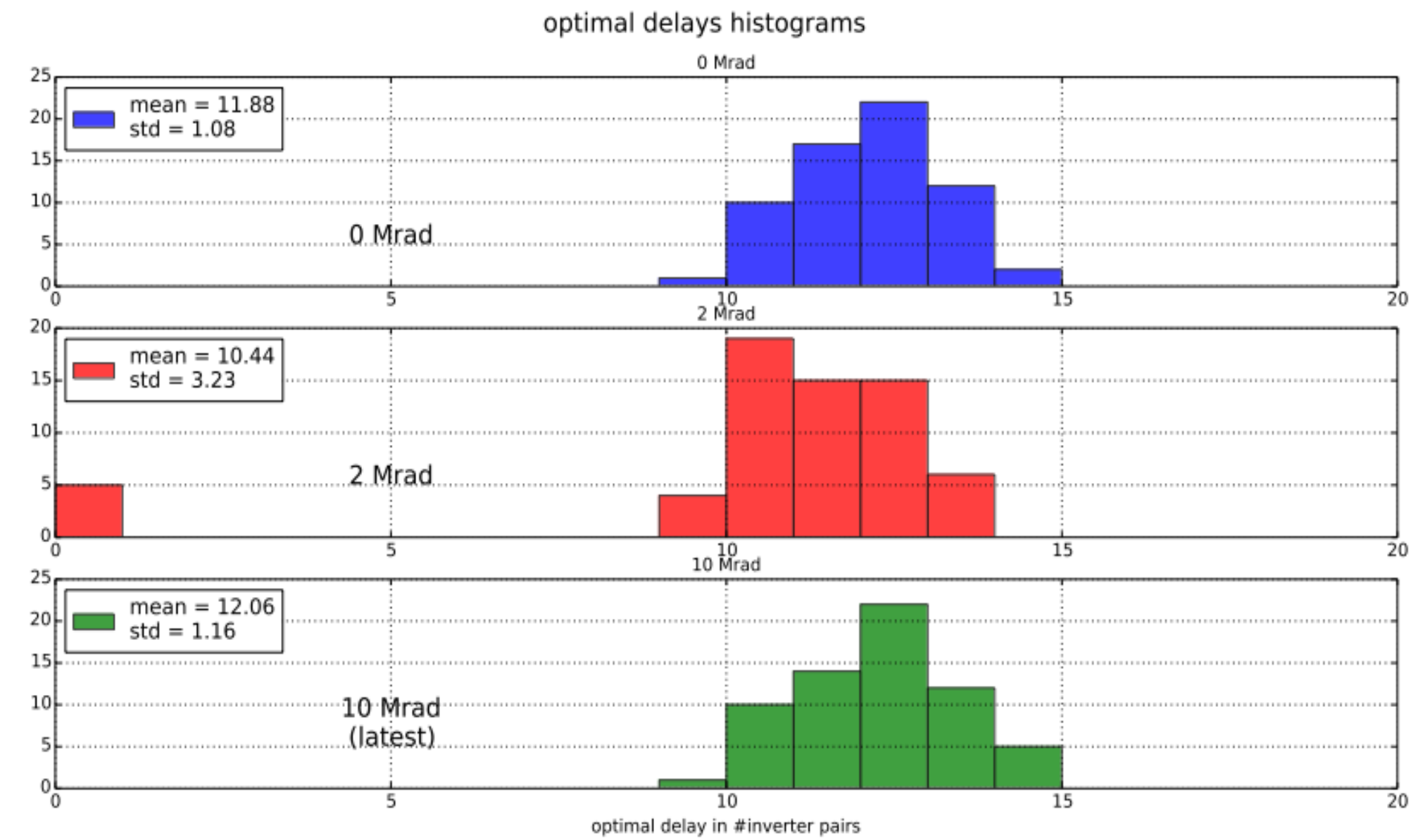
Delay Tolerance Extraction



Asymmetry Extraction



Optimal Delays



Current Consumption Log