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DHPT - Design Review

H. Krüger, Bonn University

July 15-16, 2015

Outline

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1. DCD – DHPT Interface
2. Response to the reviewers comments from the Oct ‘14 design review
3. DHPT 1.0 known issues / proposed enhancements
   - Serializer
   - CML driver
   - Data Receiver
   - Delay elements
4. SEU rates with neutrons
5. High Speed link
   - End-of-stave layout
   - Flex cable characterization

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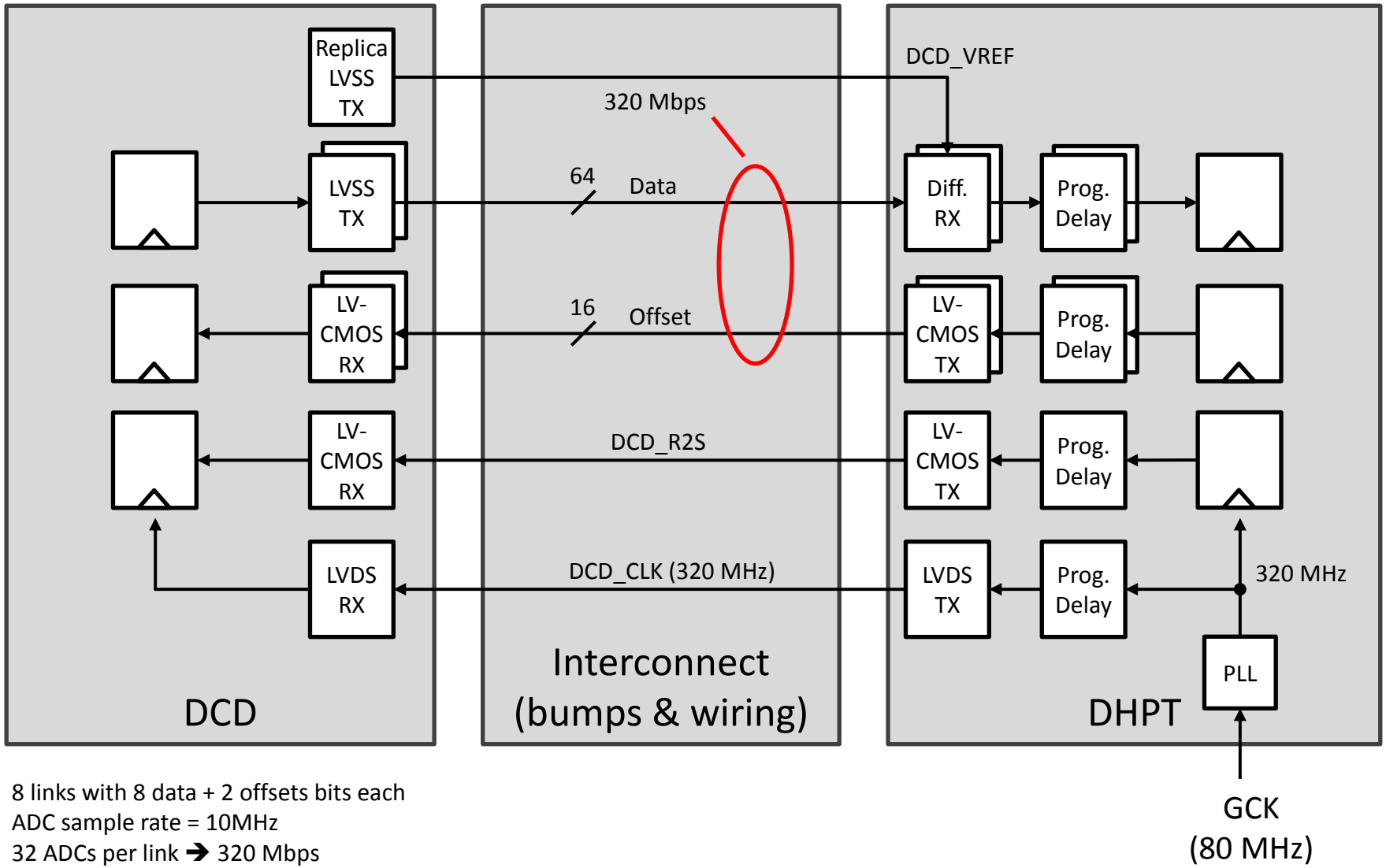
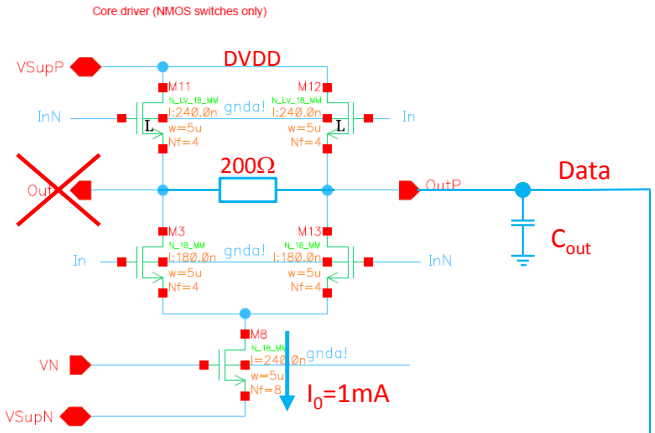
DCD- DHPT INTERFACE

DCD – DHPT Interface Block Diagram

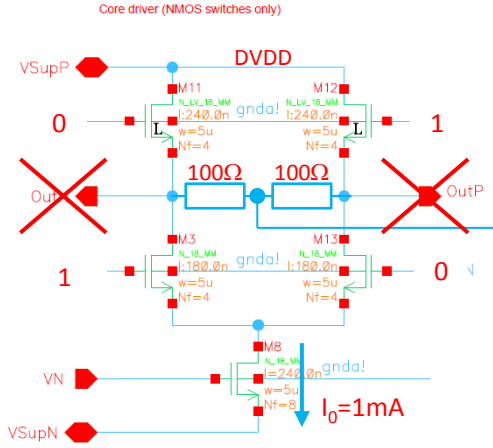


8 links with 8 data + 2 offsets bits each
ADC sample rate = 10MHz
32 ADCs per link ➔ 320 Mbps

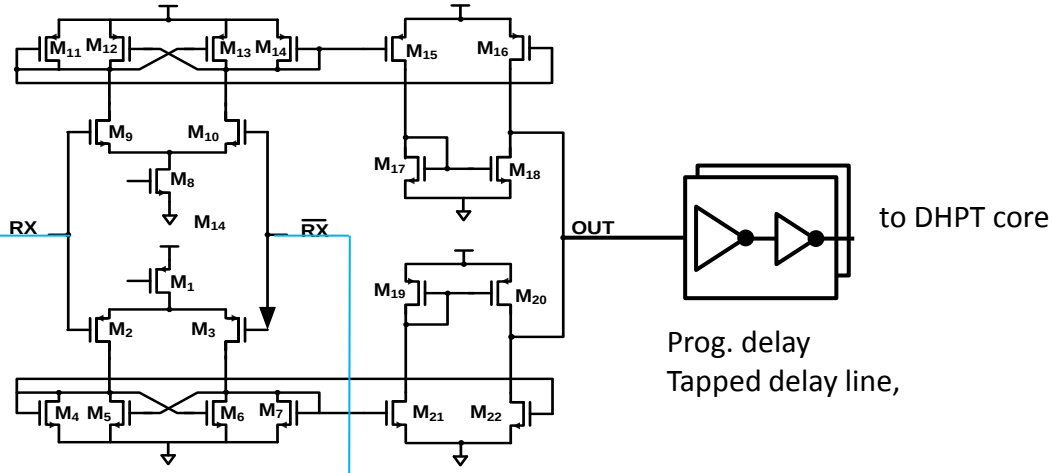
DCD – DHPT Data Transmission Schematic Details



DCD output driver



DCD output reference voltage generation



DHPT receiver

Prog. delay
Tapped delay line,

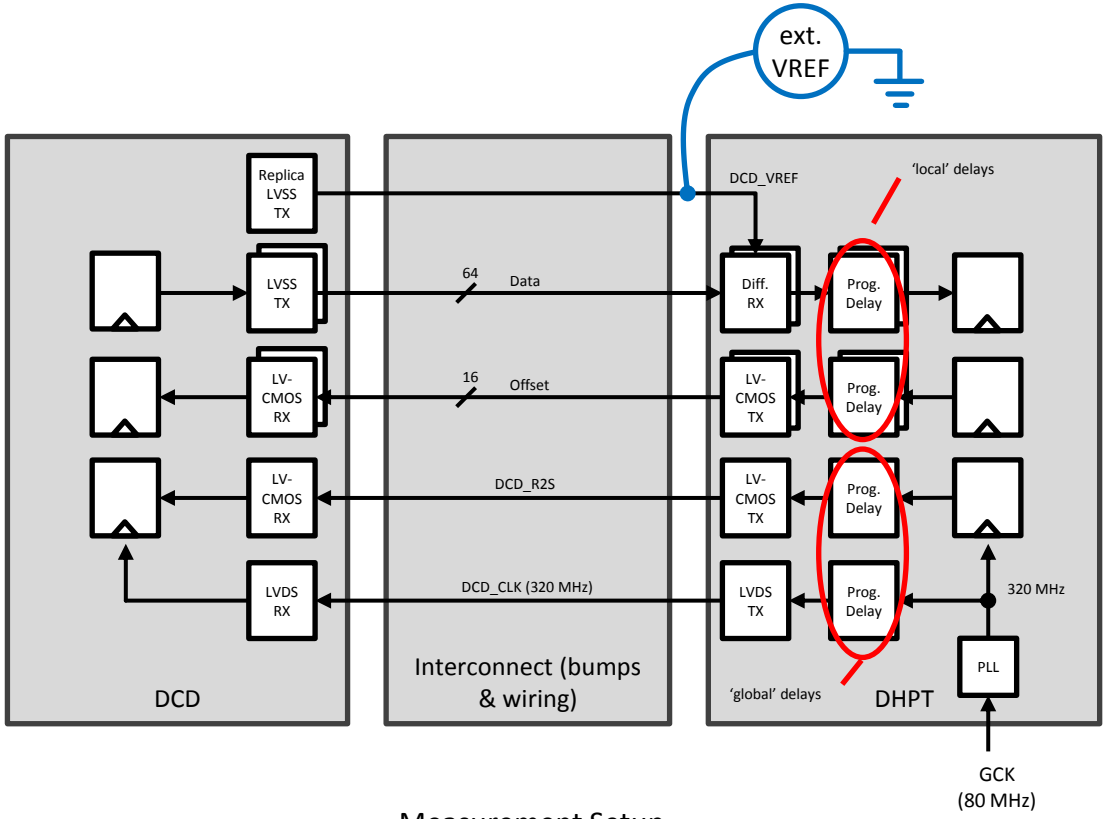
Data Link Synchronization

- DCD can produce a simple test pattern for synchronization of the data links

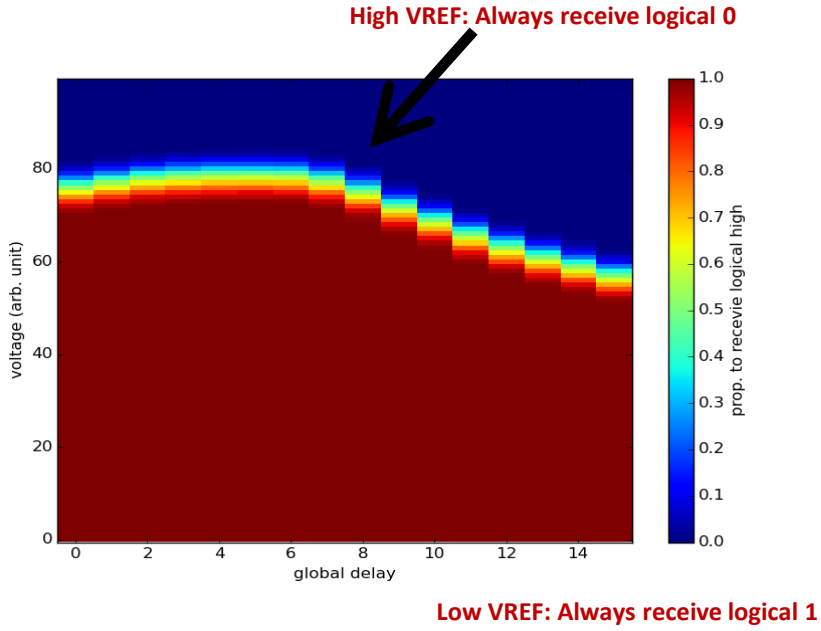
		Time (clock period) ≙ ADC channel																														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Bit line	0	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	1	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	2	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	3	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	4	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	5	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	6	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	7	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Data Line Waveform Analysis

- Combined reference voltage- and delay scan (no direct access to data lines)

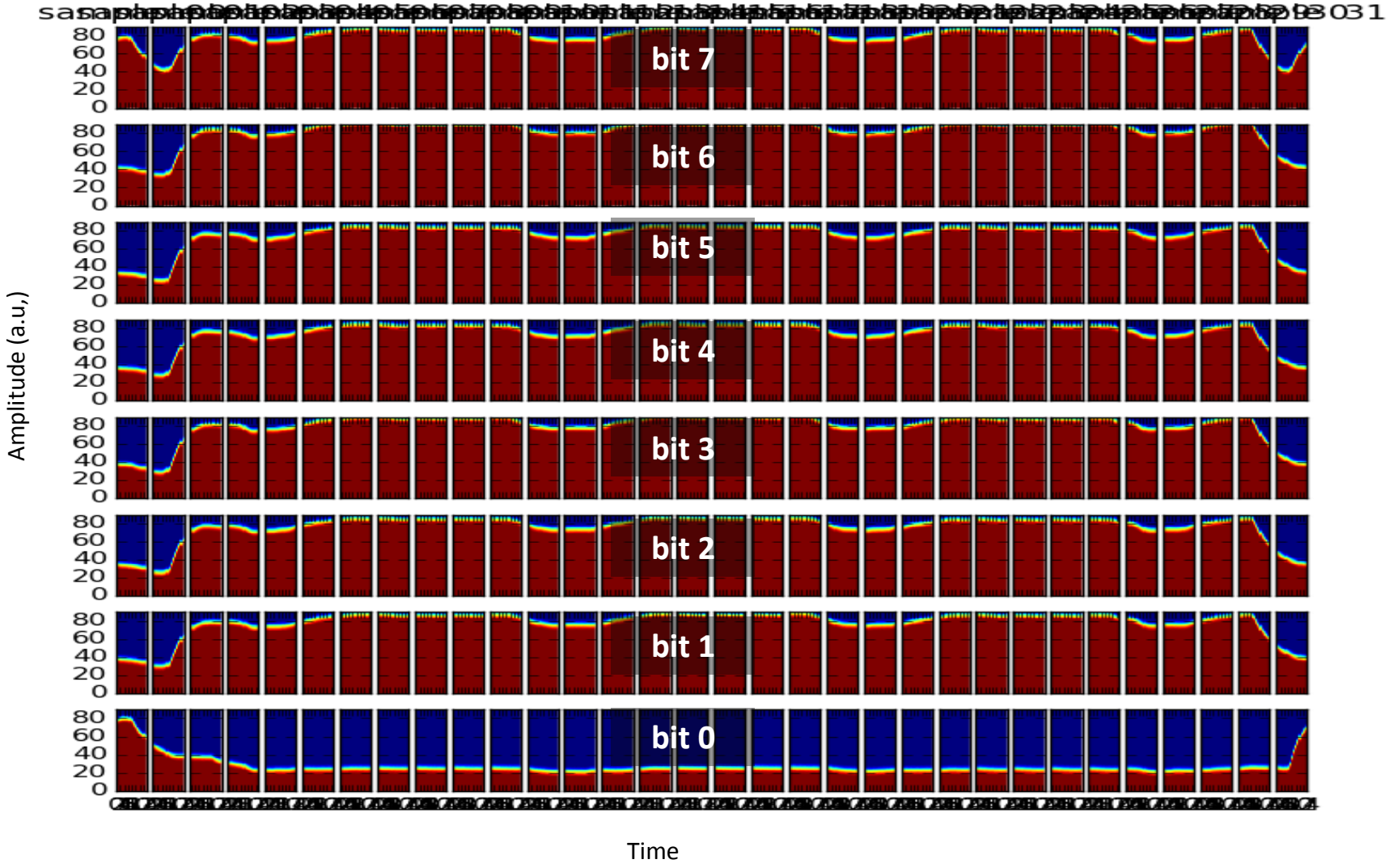


Measurement Setup

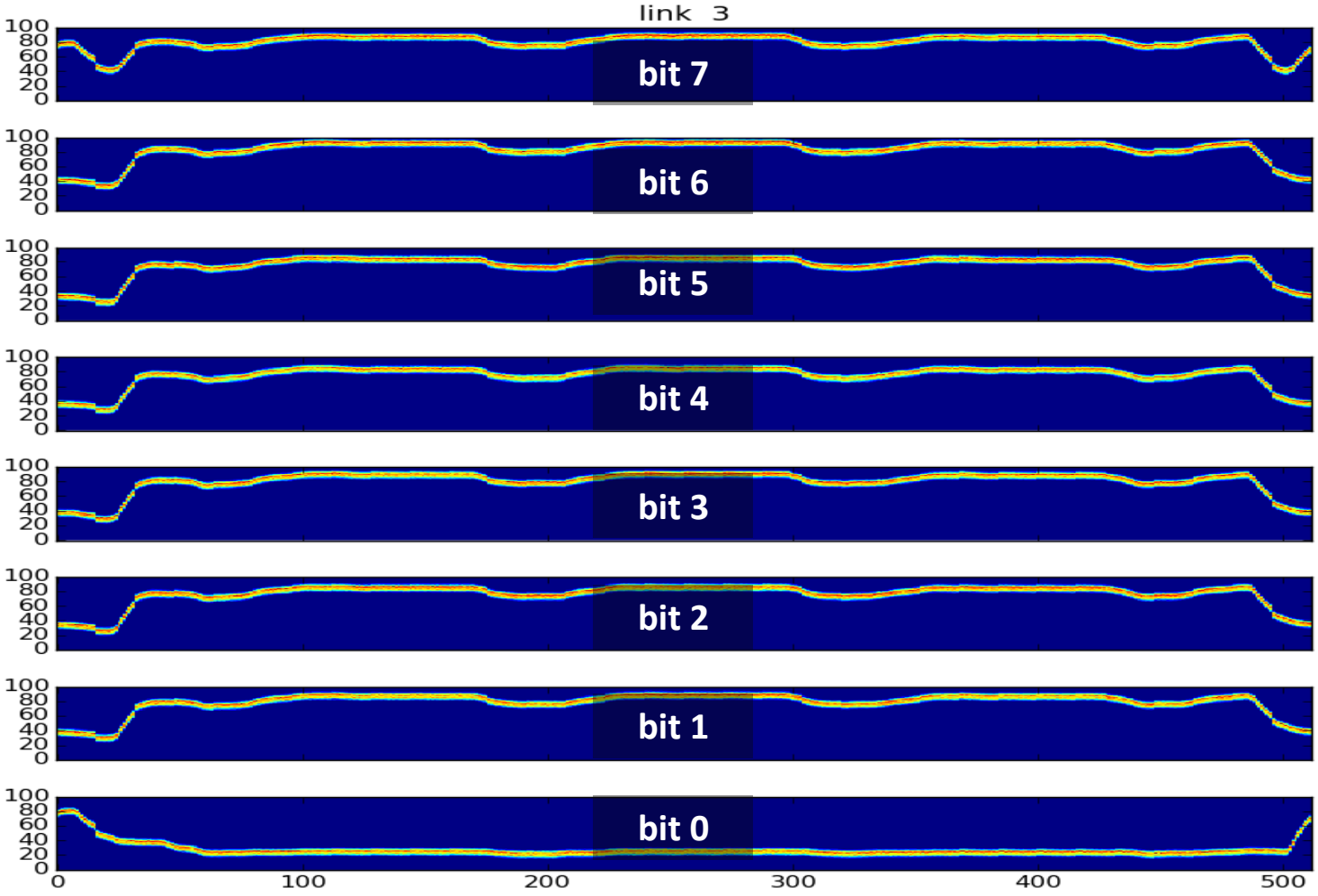


Typical scan result

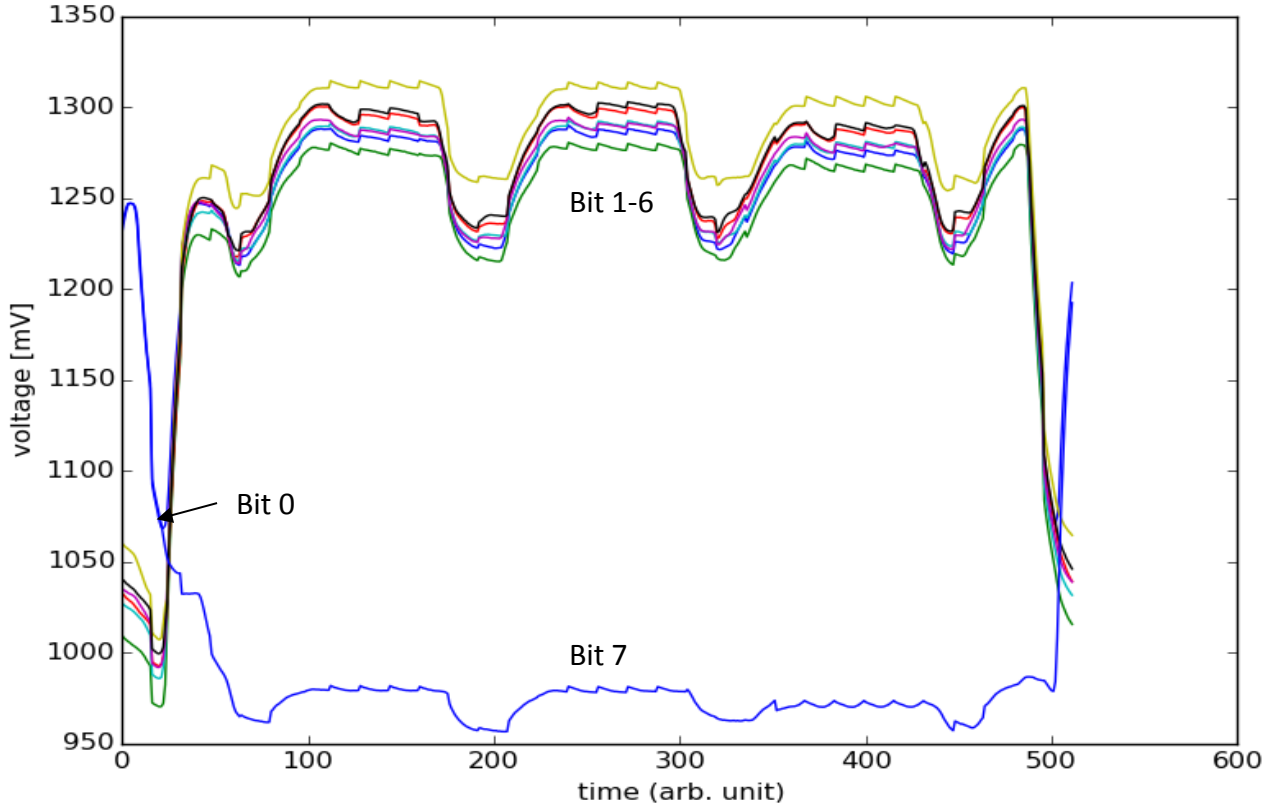
Probability Plots – Combination of all time slices



Differentiation of the Probability Plots

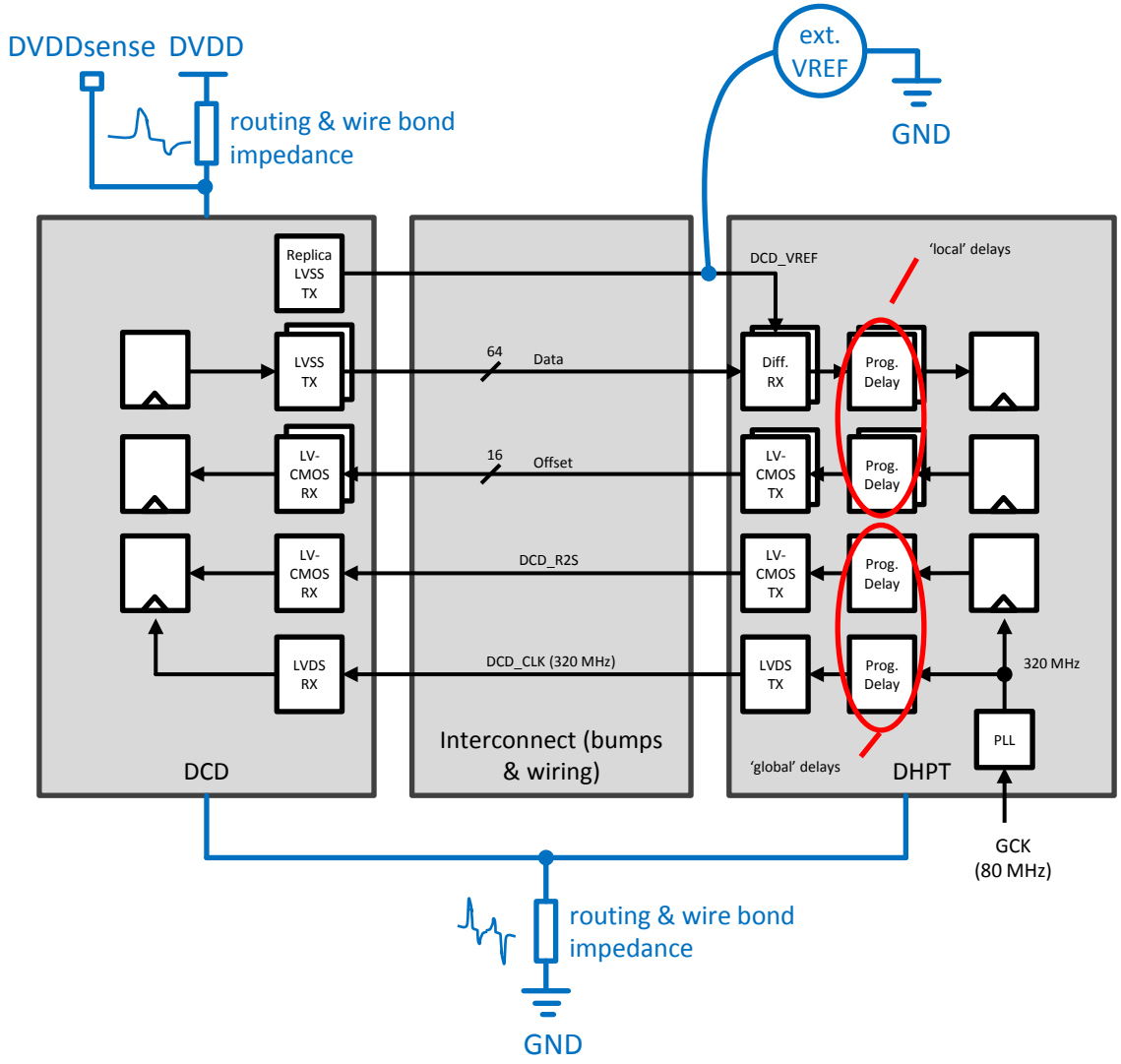


All Bit lines of one Link

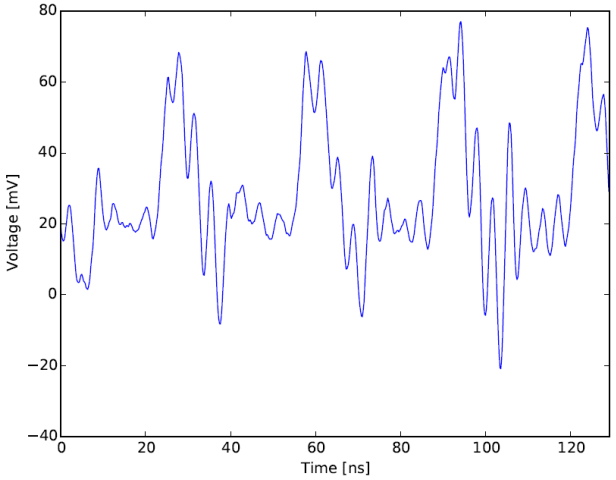


Bit line																															
	0	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	1-6	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	7	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

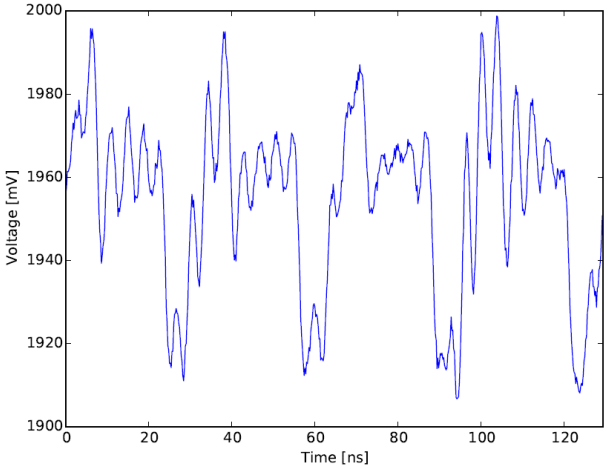
DCD_VREF external Control & Measurement



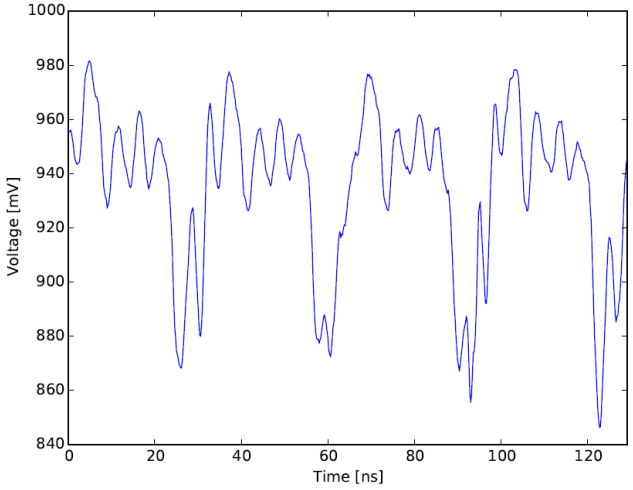
Measurement Artefacts



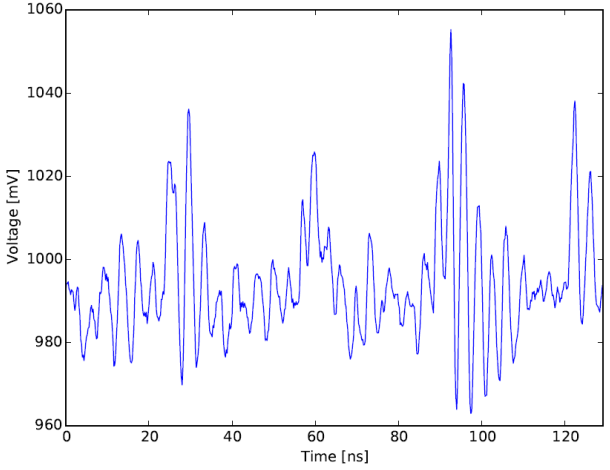
DVDD – DVDDsense



DVDDsense – GND



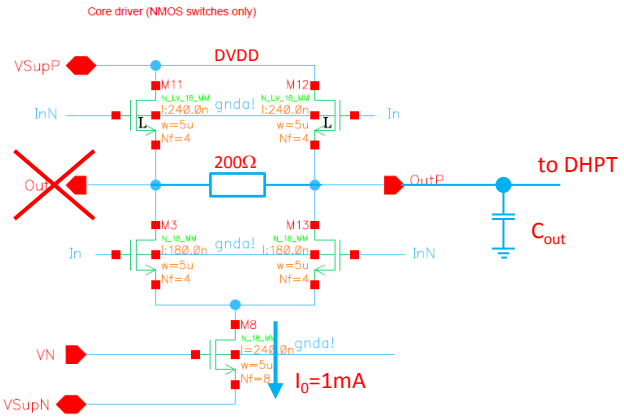
DVDDsense – DCD_VREF

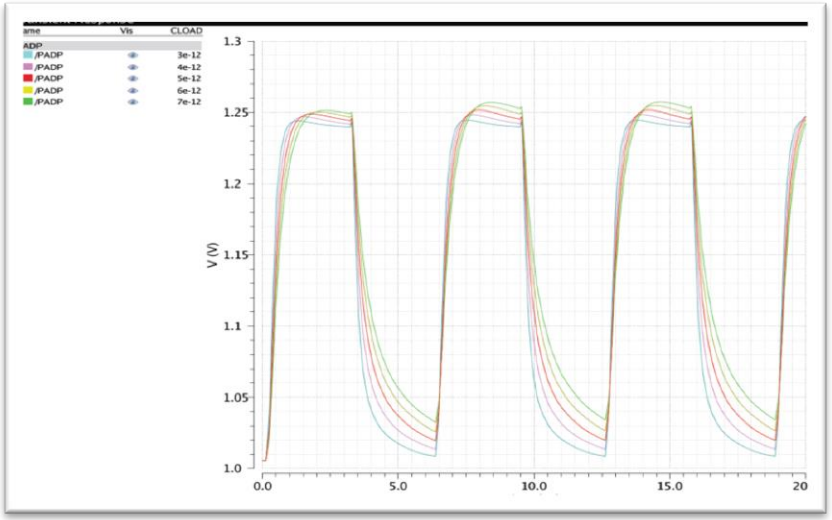


DCD_VREF – GND

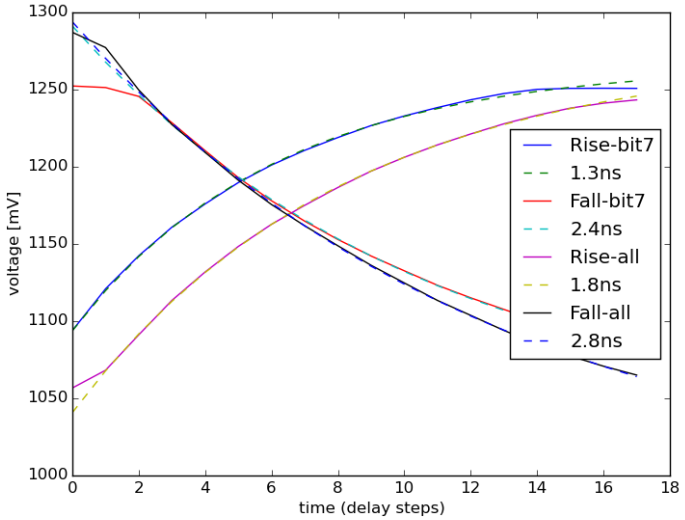
DCD output driver

- Schematic level simulation
  - capacitive load (C_{out}=3..7pF)





- Rise-/fall time extraction from Vref/deltaT scans



Interface Issues

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- Synchronization of data line critical
  - Little contingency for delay settings
  - Sensitive against TID
- Distortion of the duty cycle
  - Delay elements on DHPT
  - Hysteresis of the DHPT differential receiver (plus asymmetric rise and fall times of the DCD driver)
- Slow signals
  - Underestimated parasitic capacitance of wiring and pads
  - DCD driver output levels not adjustable and drive strength asymmetric

Design Changes

- Fix duty cycle distortion
  - Symmetric delay elements on DHPT inputs
  - DHPT differential receiver → remove hysteresis

  } See next chapters

- Make signal faster
  - Reduce parasitic capacitance of the DHPT input pads ($C_{PAD} \simeq 3$ pF dominated by ESD protection) → analysis/simulation started, pad layout change in progress
  - DCD output driver → Increase drive strength, make programmable (see Ivan's talk)
  - Changes of routing on PXD module ? (estimated $C_{line} \simeq 1$pF) TBD

Reviewers comments form Oct ‘14

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- Specifications for output loads and timing are needed for signals in Table 1 of the Manual. For such a complex device, a more comprehensive document many be required.

  A: Still missing, will be done (chip design experts are actively involved in the system test and module operation)

- Finer step TID testing, SEU testing. Channel masking and Overflow handling tests self-identified.

  A:
  - *TID test campaign previously done (results will be shown in other presentations)*
  - *SEU cross section measurement deemed to be reliable (see comments on later slides)*
  - *channel masking → ok*
  - *overflow handling → ongoing system tests*

Reviewers comments form Oct ‘14

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- Not clear who is doing what to provide further testing and by when

  A: Established weekly lab-meetings for detailed test planning and discussion of results

- A detailed model of the cabling needed to complete output driver redesign (Characterize the electrical properties of the external interconnects and cables).

  A: Cable driver is designed for maximum (programmable) drive performance for the given architecture (1 stage of pre-emphasis). Optimization work is related to the seen discrepancy between schematic level simulation and real performance (see later slides). The existing driver (DHPT 0.1 test chip) together with a mockup of the real cable connection is performing well (see slides about CML driver). However the routing of the high speed data lines on the module have been identified as sub-optimal and the layout of that region has been re-designed (see slides on the PXD module EOS layout in the backup)

Reviewers comments form Oct ‘14

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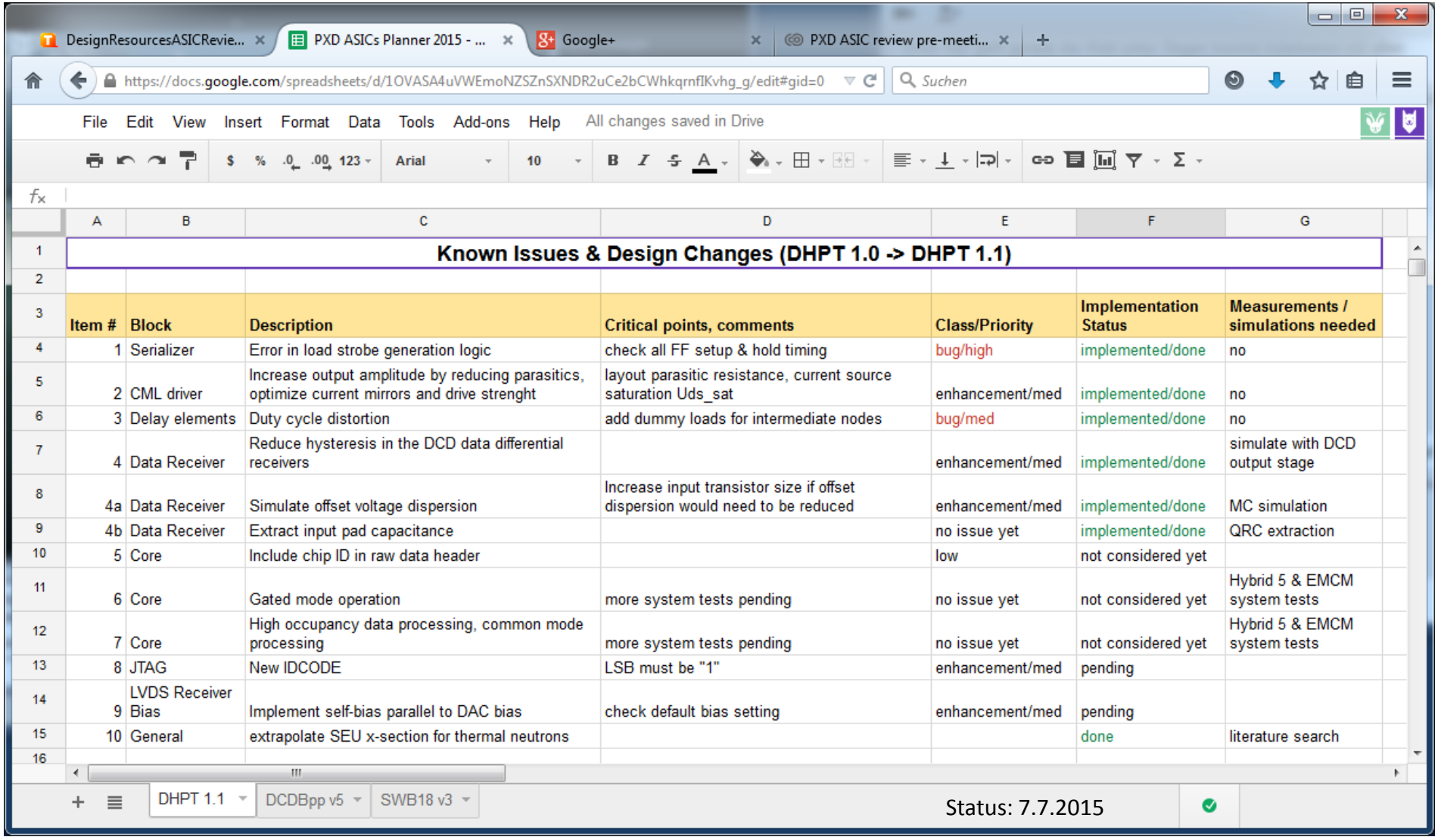
- June submission seems plausible given proposed testing schedule. A rigorous internal review of the proposed changes should be held prior to release for submission.

  A: Internal design review held in April ’15.

  Submission schedule
  - *Design review: July 15/16 (now)*
  - *August 26: tape-out (MPW, 12 weeks turn-around)*
  - *December: shipment of 100 parts*
  - *February 2016: DHPT 1.1 verified, reorder of additional parts (100-200 parts ship immediately)*
  - *April 2016: shipment of the remaining parts (all together 9 wafer sets).*

  KGD testing in Bonn and shipment of tested chips to HLL will start in February.

Known Issues & Design Changes (DHPT 1.0 -> DHPT 1.1)



Known Issues & Design Changes (DHPT 1.0 -> DHPT 1.1)

Item #	Block	Description	Critical points, comments	Class/Priority	Implementation Status	Measurements / simulations needed
1	Serializer	Error in load strobe generation logic	check all FF setup & hold timing	bug/high	implemented/done	no
2	CML driver	Increase output amplitude by reducing parasitics, optimize current mirrors and drive strenght	layout parasitic resistance, current source saturation Uds_sat	enhancement/med	implemented/done	no
3	Delay elements	Duty cycle distortion	add dummy loads for intermediate nodes	bug/med	implemented/done	no
4	Data Receiver	Reduce hysteresis in the DCD data differential receivers		enhancement/med	implemented/done	simulate with DCD output stage
4a	Data Receiver	Simulate offset voltage dispersion	Increase input transistor size if offset dispersion would need to be reduced	enhancement/med	implemented/done	MC simulation
4b	Data Receiver	Extract input pad capacitance		no issue yet	implemented/done	QRC extraction
5	Core	Include chip ID in raw data header		low	not considered yet	
6	Core	Gated mode operation	more system tests pending	no issue yet	not considered yet	Hybrid 5 & EMCM system tests
7	Core	High occupancy data processing, common mode processing	more system tests pending	no issue yet	not considered yet	Hybrid 5 & EMCM system tests
8	JTAG	New IDCODE	LSB must be "1"	enhancement/med	pending	
9	LVDS Receiver Bias	Implement self-bias parallel to DAC bias	check default bias setting	enhancement/med	pending	
10	General	extrapolate SEU x-section for thermal neutrons			done	literature search

DHPT 1.1 | DCDBpp v5 | SWB18 v3

Status: 7.7.2015

DHPT 1.0 known issues

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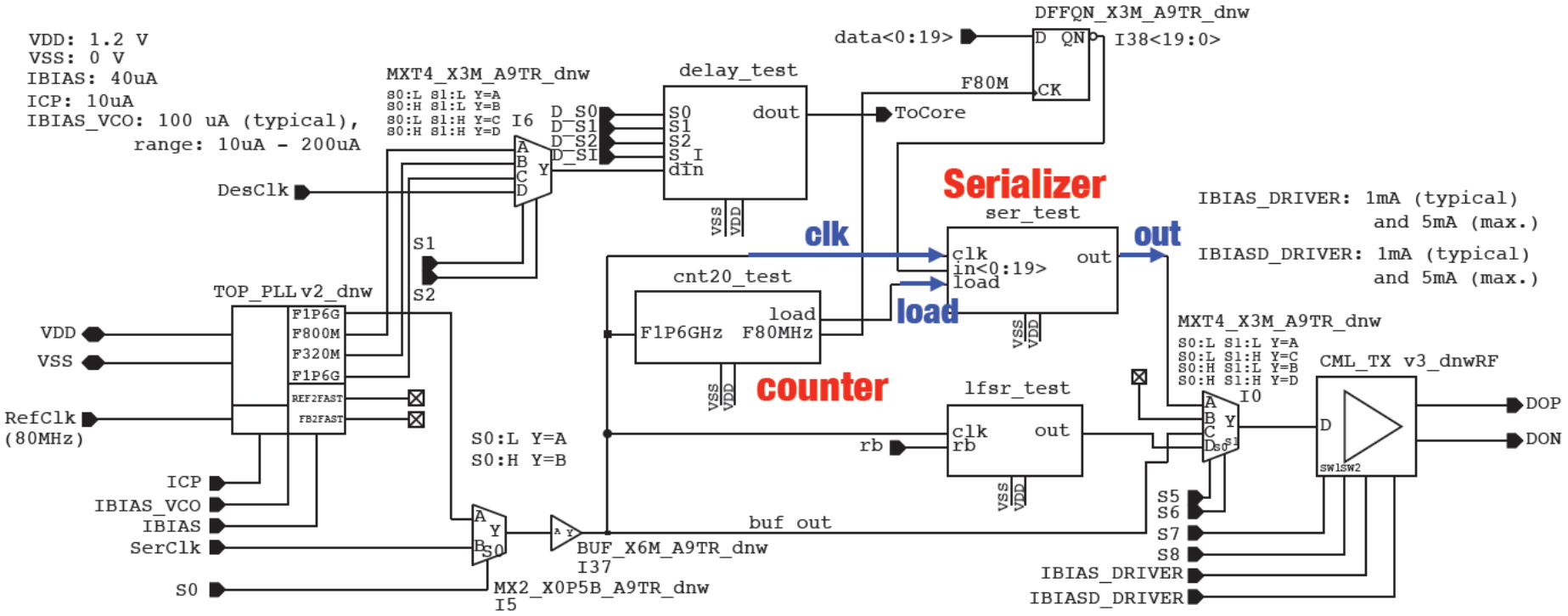
- Serializer: timing bug
- CML driver enhancement : reduce parasitic resistance
- Prog. delay elements issue: duty cycle distortion
- Data receiver robustness: duty cycle distortion with non-symmetric input edges

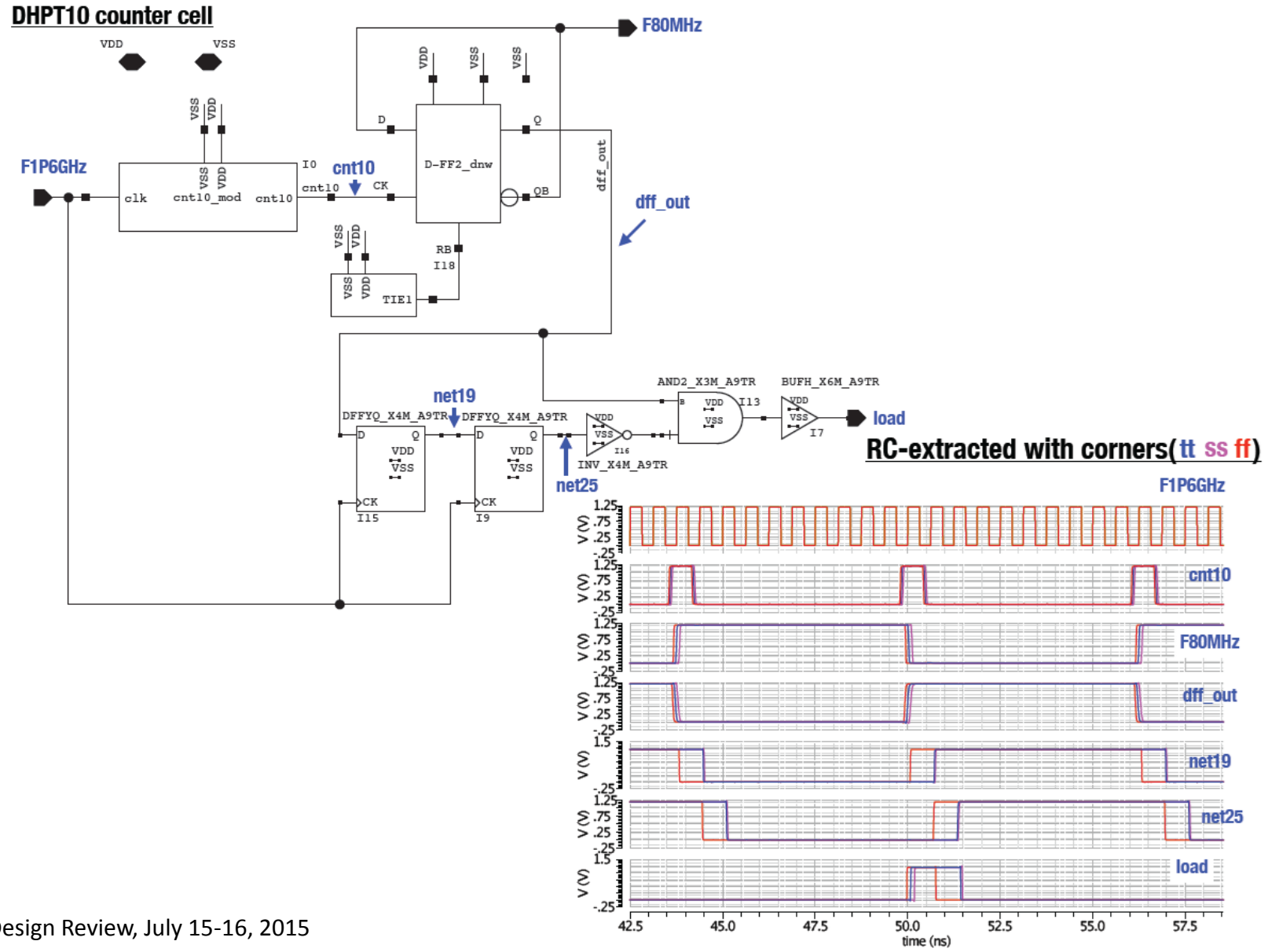
DHPT 1.0

SERIALIZER

PLL + SER Block Diagram



Load Strobe Generation (Counter)



Serializer Bug

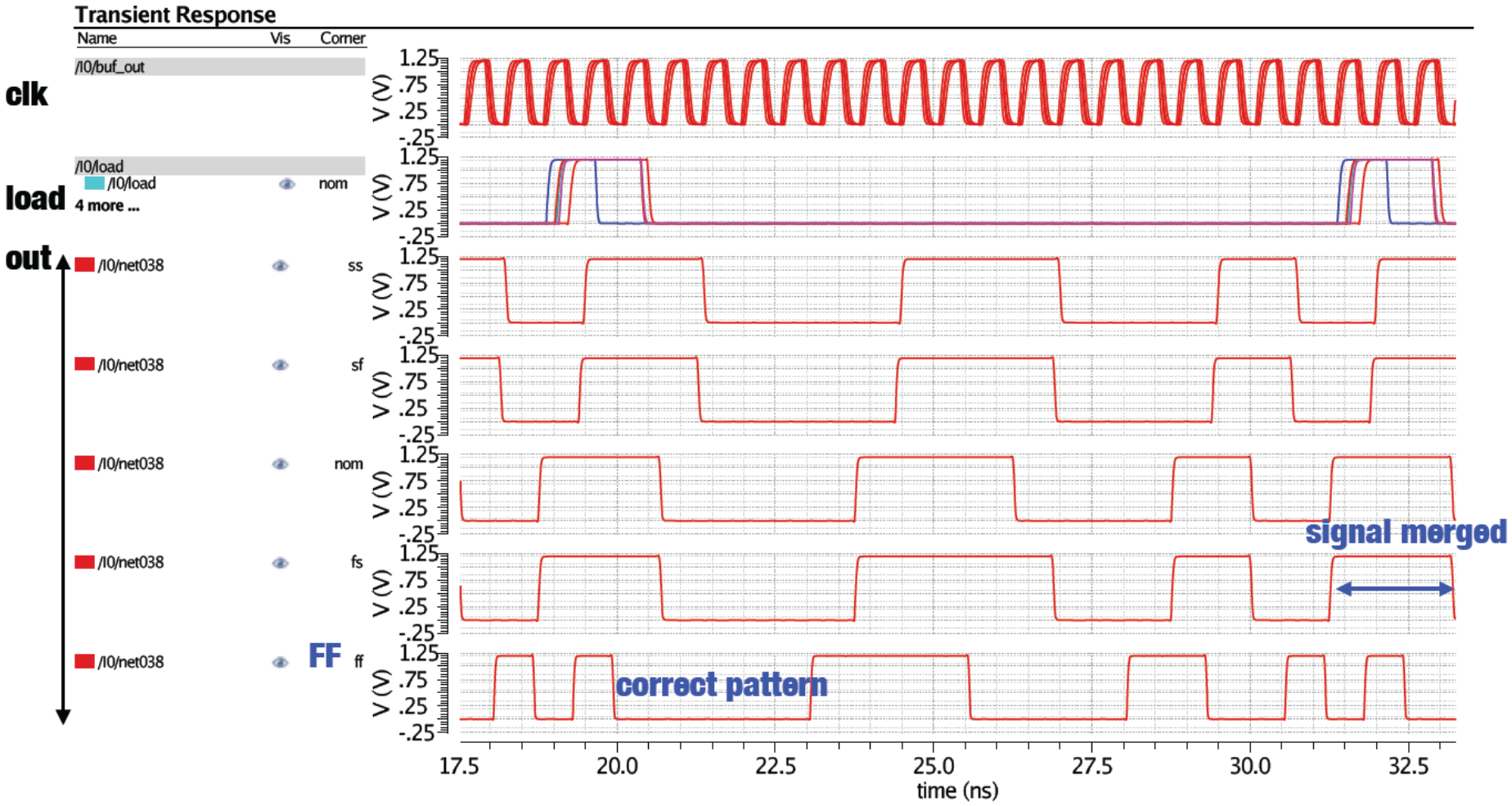
- Mistake made during extracting and simulating the layout with all process corners

- Serializer works, but VCC and/or GCK have to be adjusted:
  - GCK= 80 MHz → VCC = 1.6V (works but should not be applied for a long time)
  - GCK= 60 MHz → VCC = 1.4V (ok)

- Manufacturer test data ➔ wafer batch has „slow NMOS“ (too high threshold)

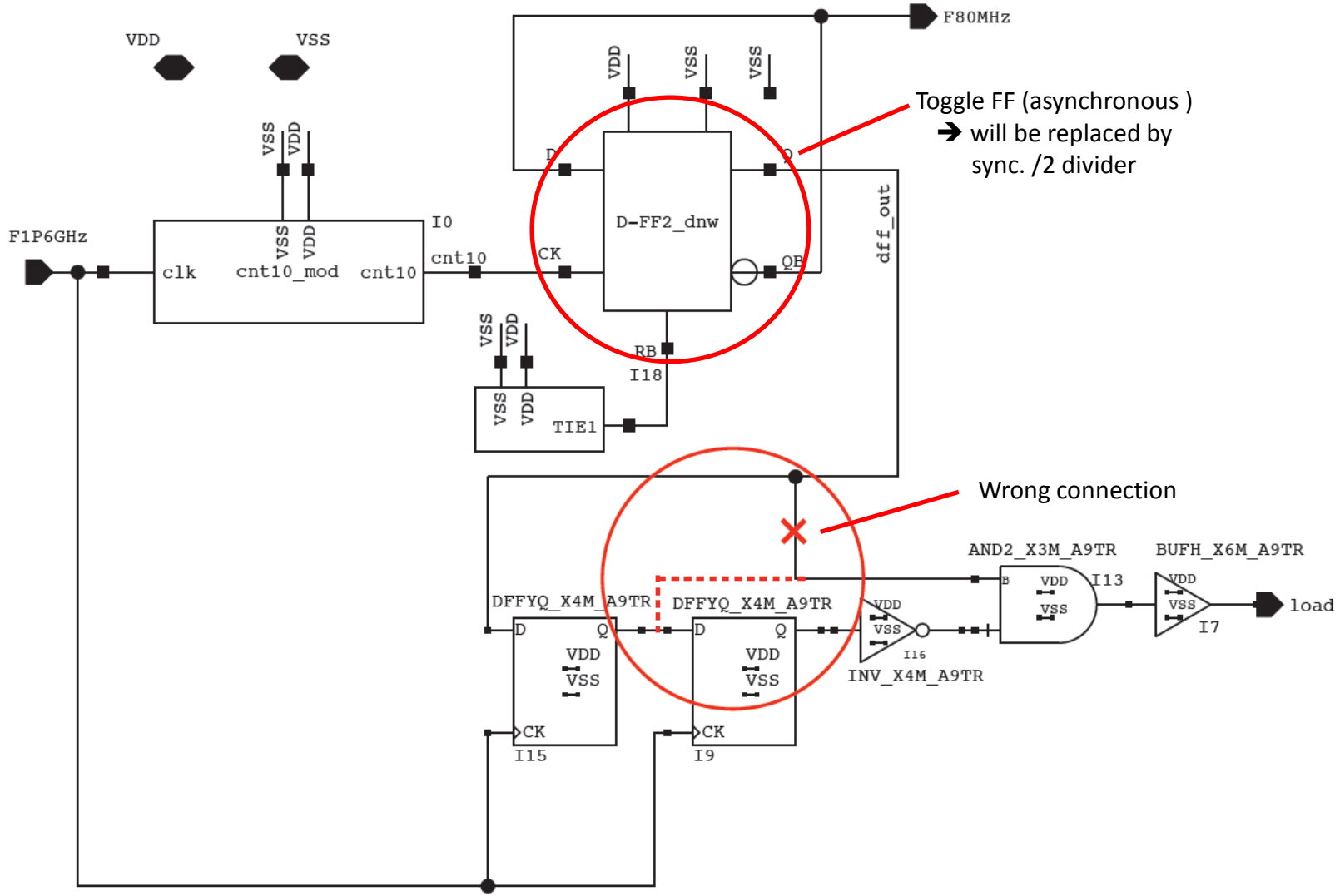
PARAMETER BY LOT:		SPEC LO	SPEC HI	MIN	MAX	MEAN	STD DEV
VTl_N4	(N/.3/.06/1)	0.300	0.490	0.368	0.490	0.423	0.029
Isof_N4	(N/.3/.06/1)	-1.400E-07	0.000	-8.958E-10	-3.833E-11	-2.339E-10	2.063E-10
Isat_N4	(N/.3/.06/1)	0.491	0.735	0.547	0.673	0.593	0.031

DHPT 1.0 Serializer Simulation

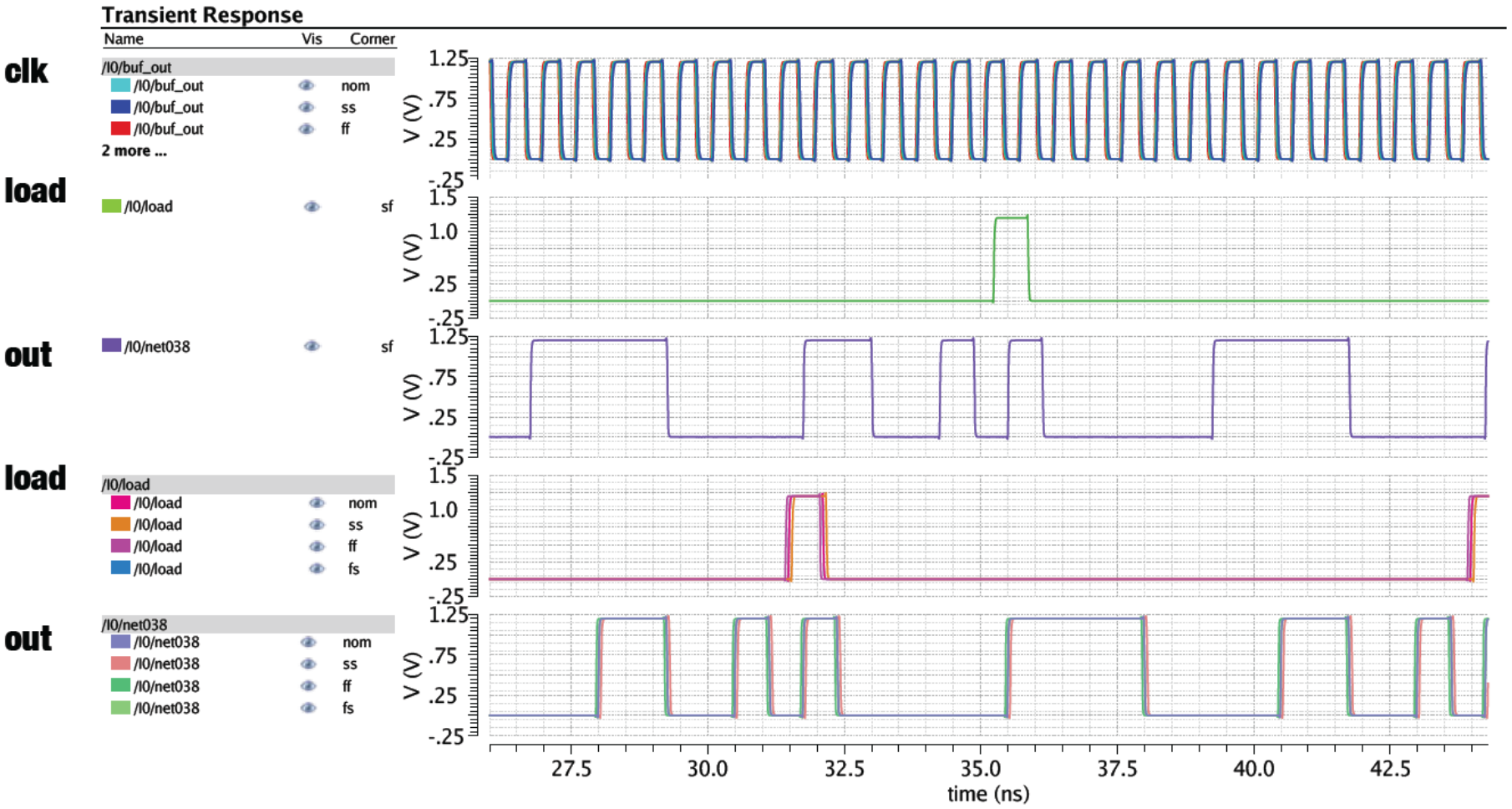


Timing of "load" is not provided correctly, except fast-fast corner.

Design Fix in the Counter Circuit



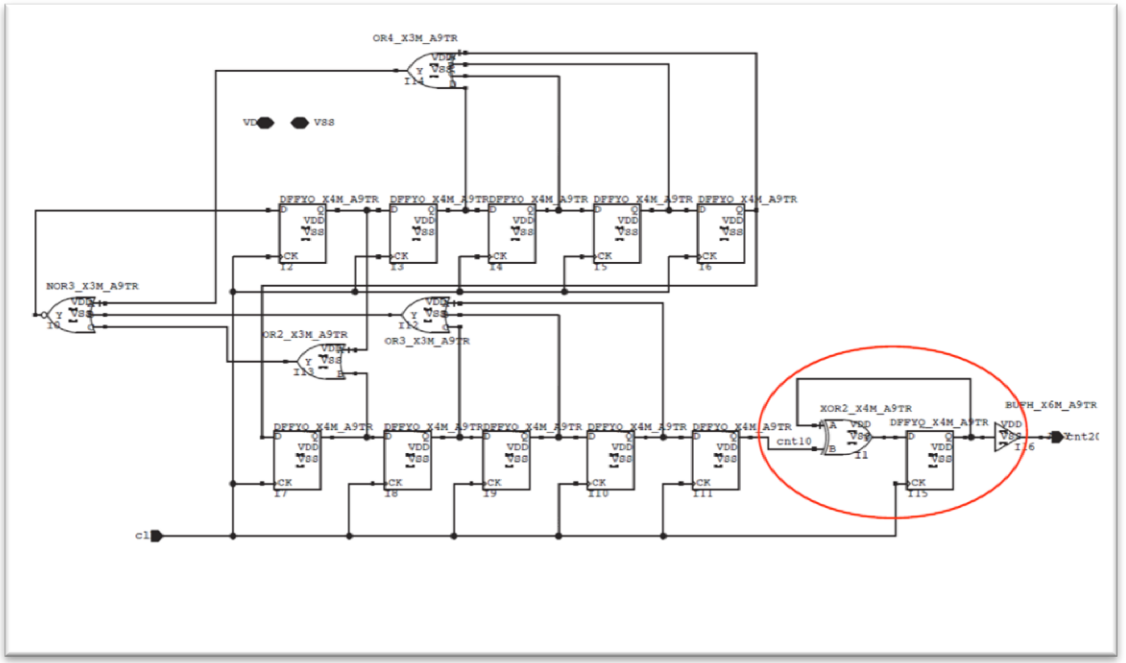
Serializer Simulation with Modification (DHPT 1.1)

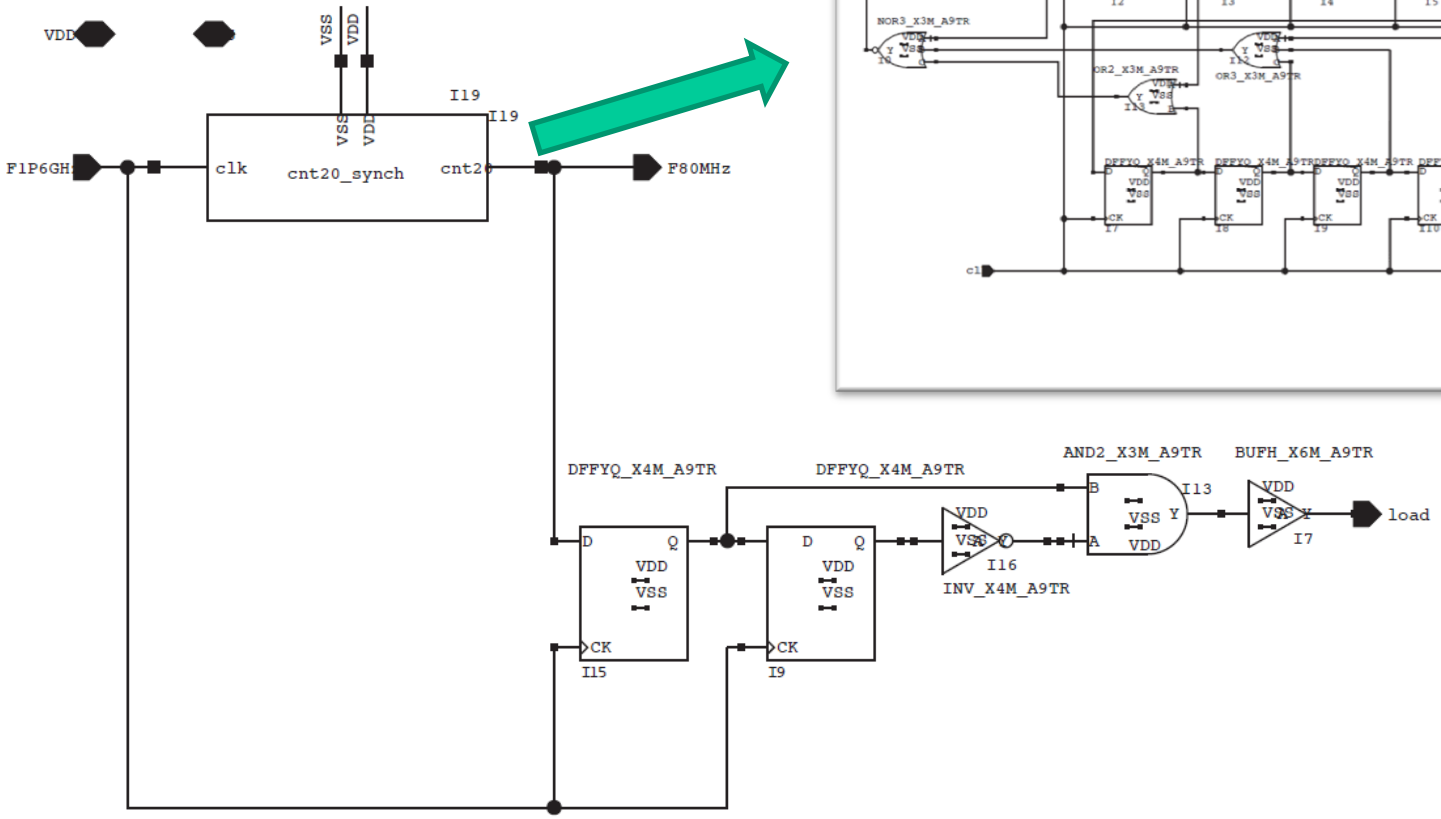


Correct pattern can be obtained with all corners.

New Serializer Load Strobe Generator

- Synchronous design





RC-extracted simulation with corners(tt ss ff)

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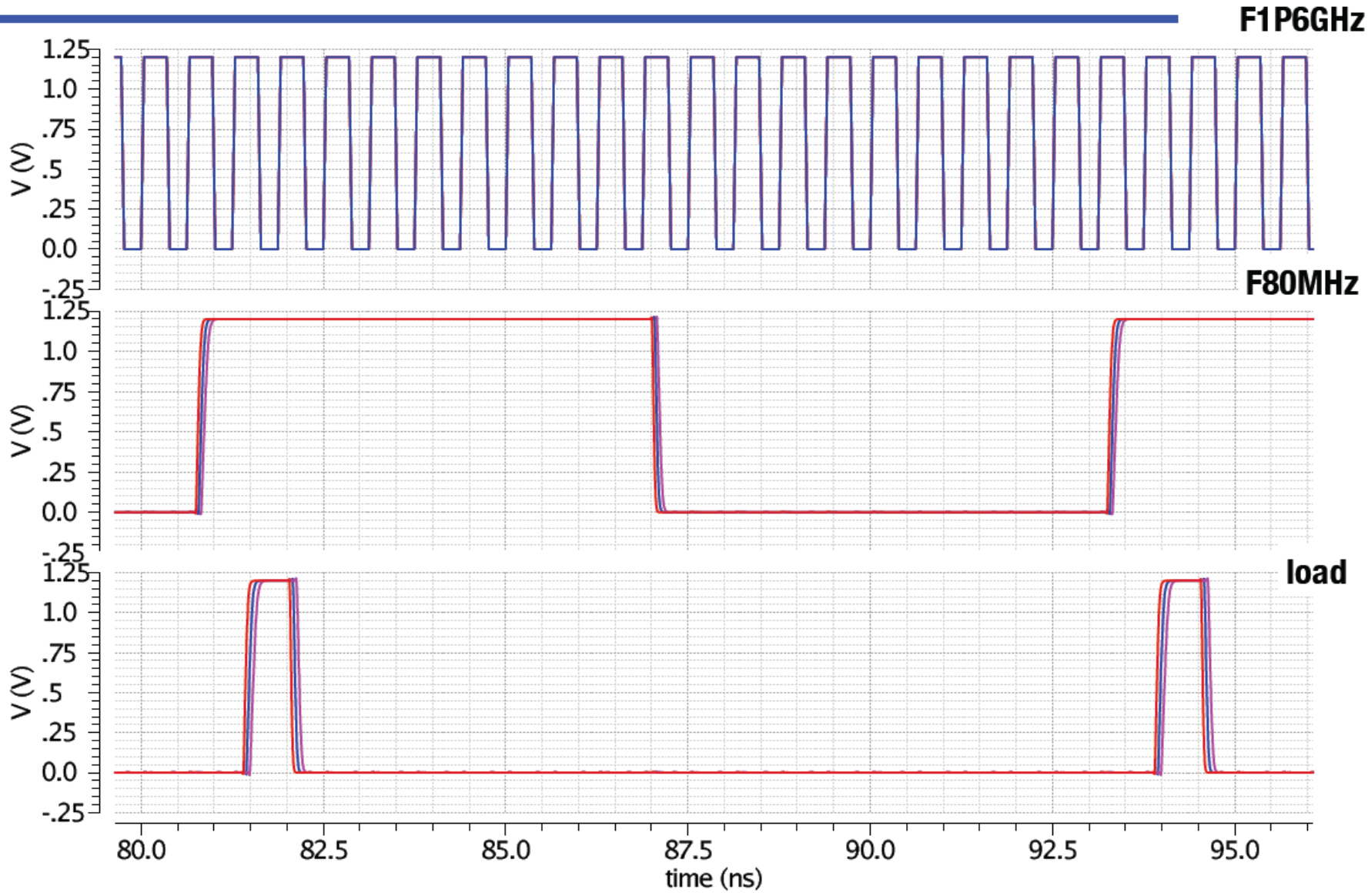

Serializer Re-design Status

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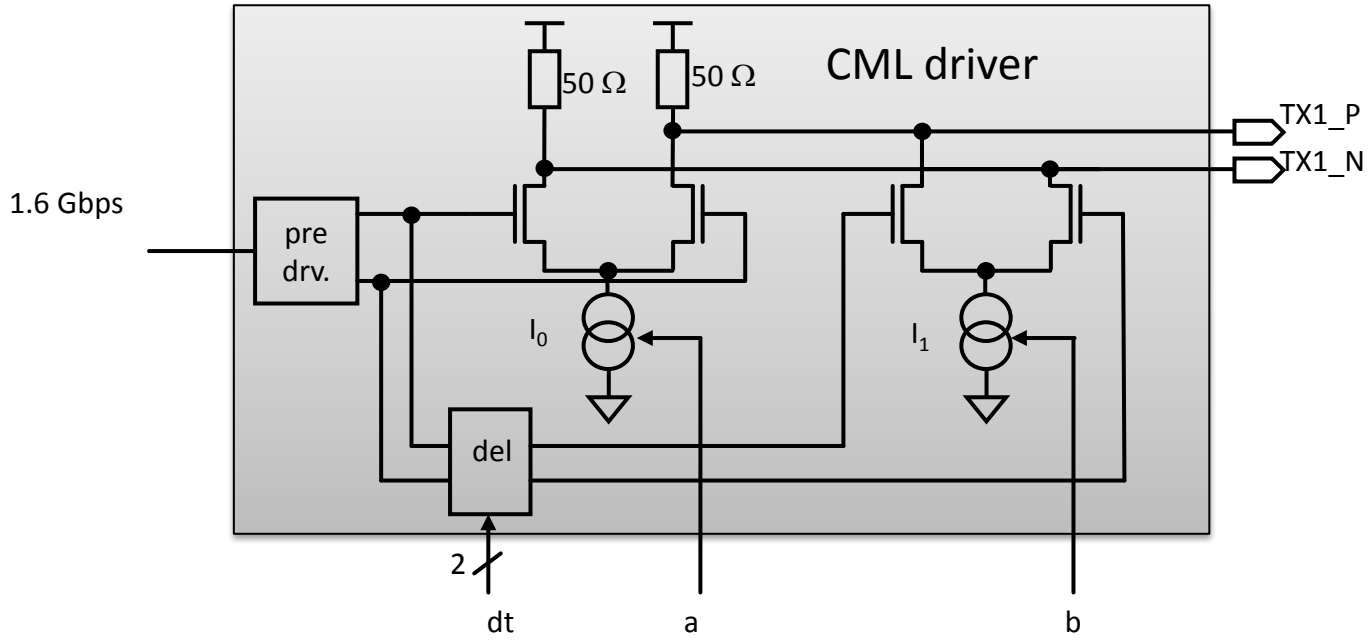
- Origin of the bug: **understood, reproducible**
- Design modification: **identified**
- Re-design on schematic level: **done**
- Re-design on layout: **done** (homeopathic change)
- Simulation of extracted netlist (all corners): **done**

DHPT 1.0

CML DRIVER

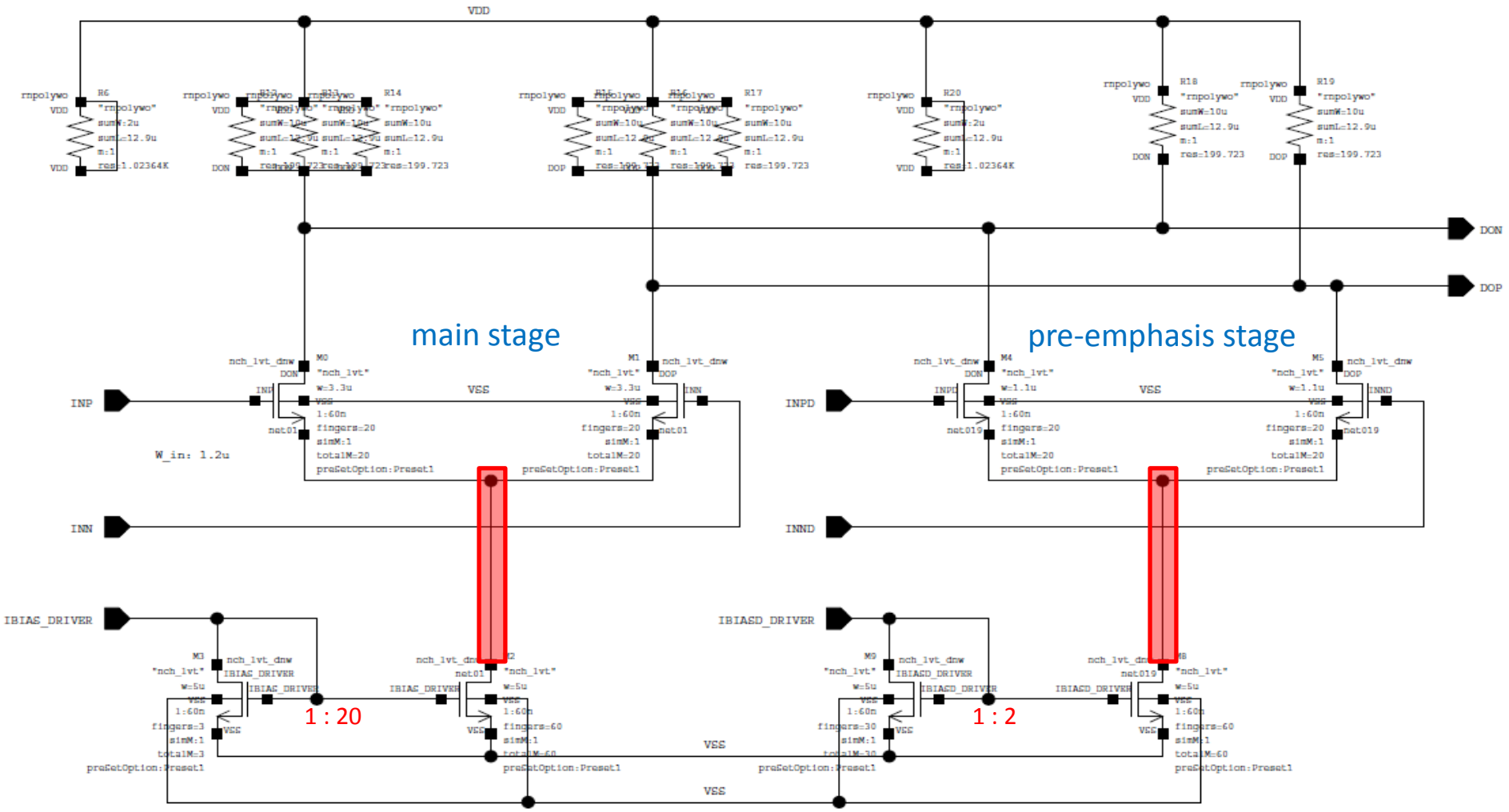
CML Driver

- Works fine, try to **enhance the performance** (output swing) to have a bit more safety margin



T. Kishishita

Driver Schematic



DHPT 0.1 – Test setup

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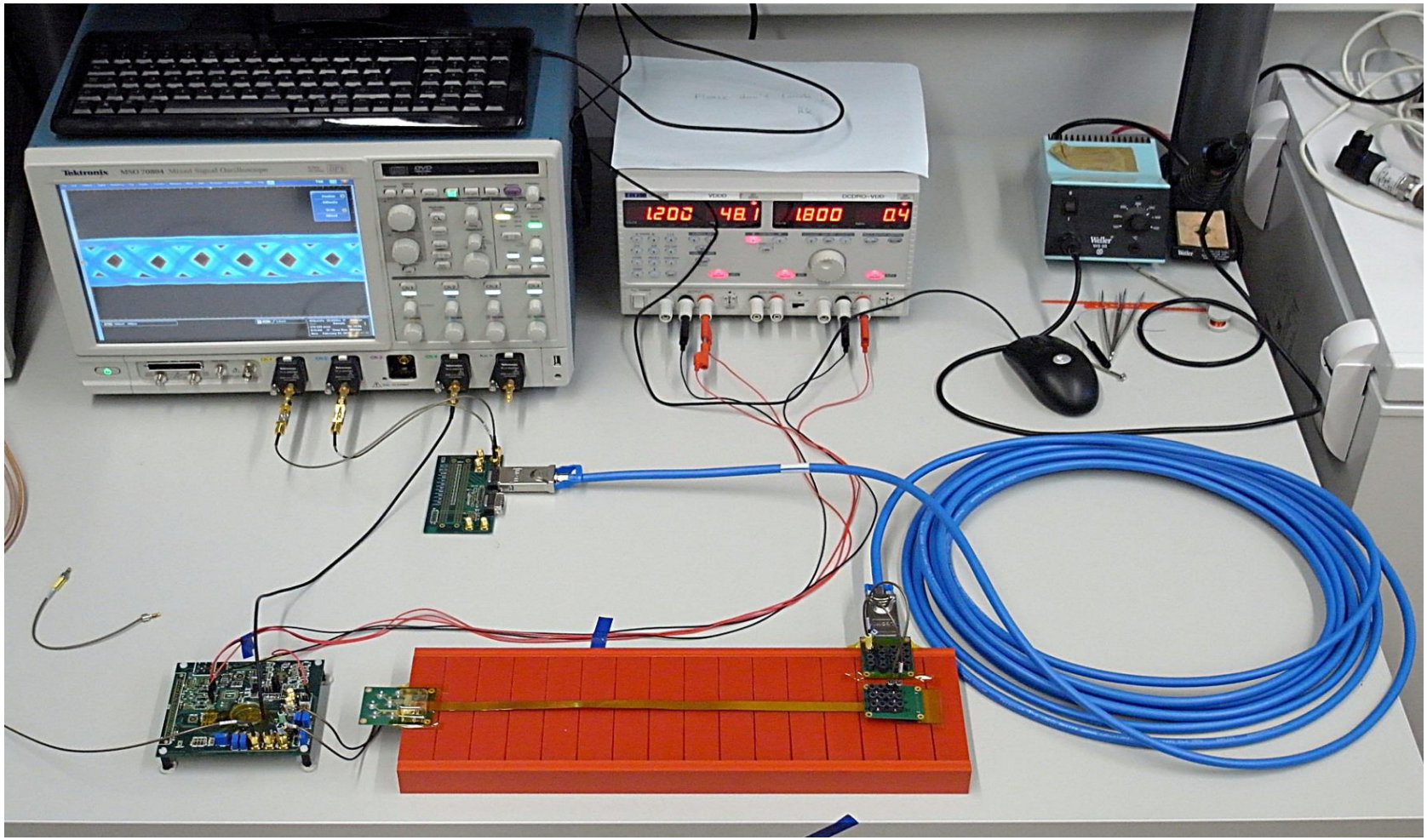
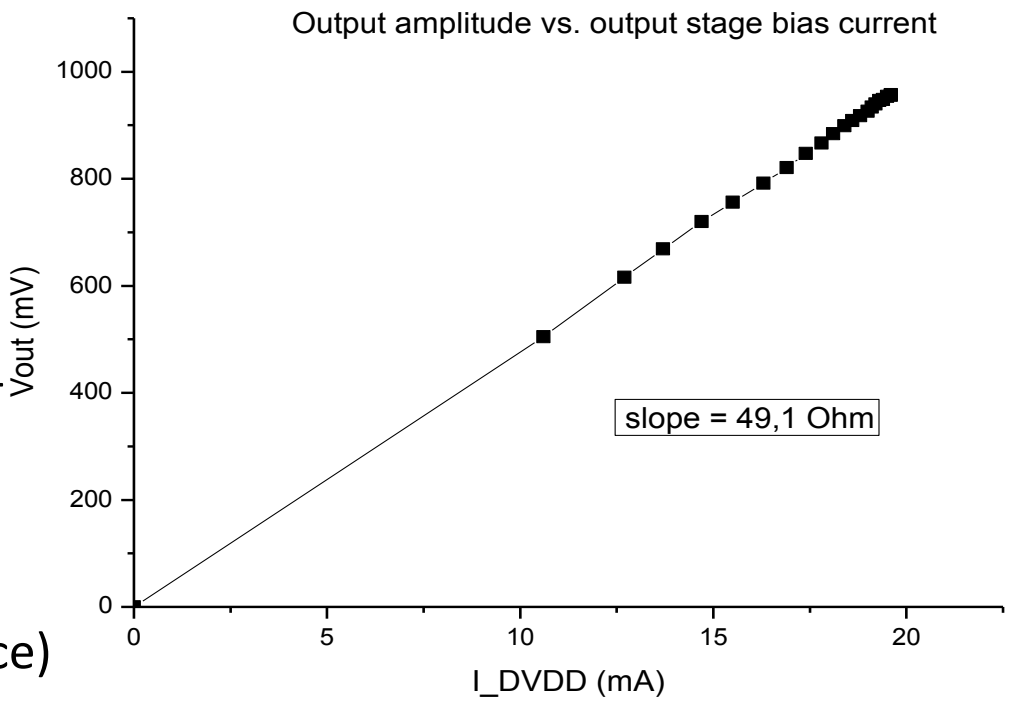


Differential Output Amplitude

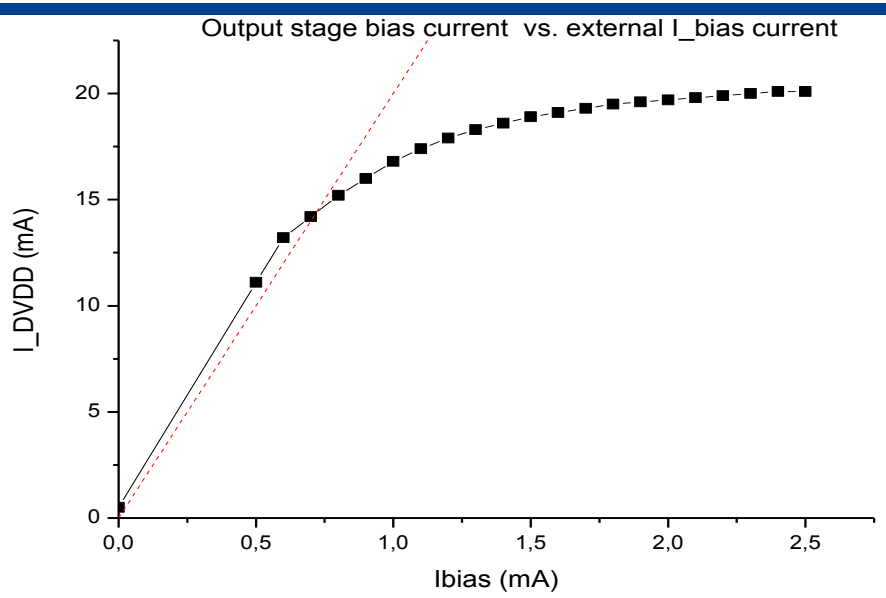
- Linear function of bias current (IBIAS_DRIVER)
- IBIAS_DRIVER ≈ I_DVDD
- Preemphasis off (IBIASD_Driver = 0)
- Effective output resistance: 49.1 Ohm
- DC output resistance: 55 Ohm
- ➔ ~3.5 Ohm Series resistance (chip wiring, bond wire, PCB trace)



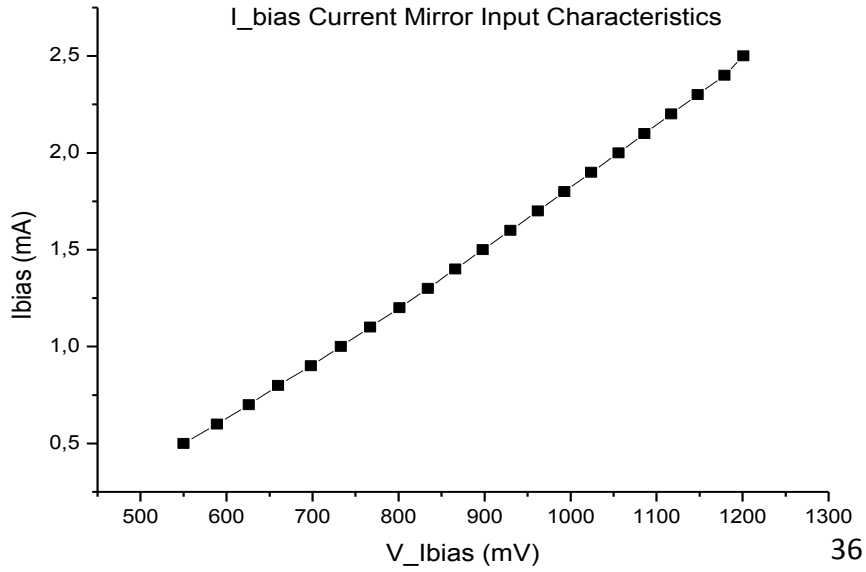
➔ Output resistance Ok

Main Output Current Mirror

- IBIAS_DRIVER current mirror
- Design value
  IBIAS_DRIVER/Ibias = 20
- Non-linear for Ibias > 0.7mA
  ➔ M2 not saturated?
- Drive current limited to 20 mA
  → $Vout_{max}$ = 957 mV

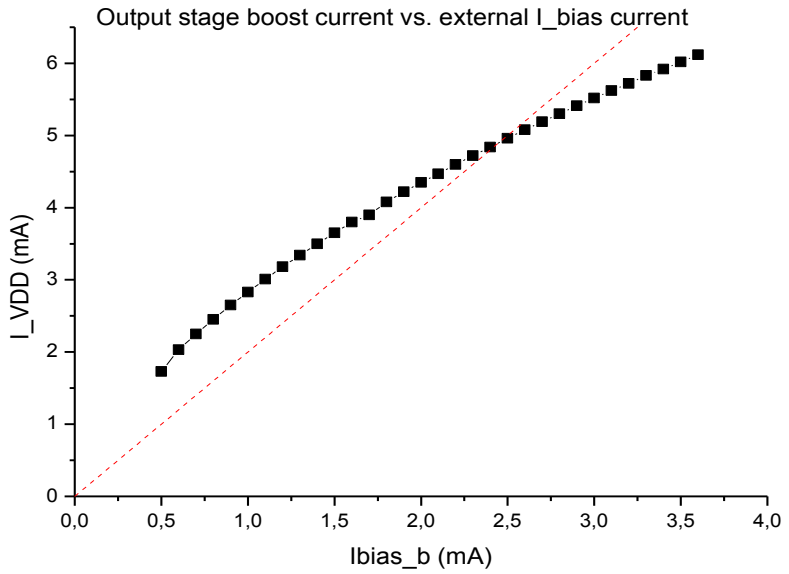


➔ Limited by current sink (M2) or switches M0/M1 (too high on resistance or parasitic wiring resistance)

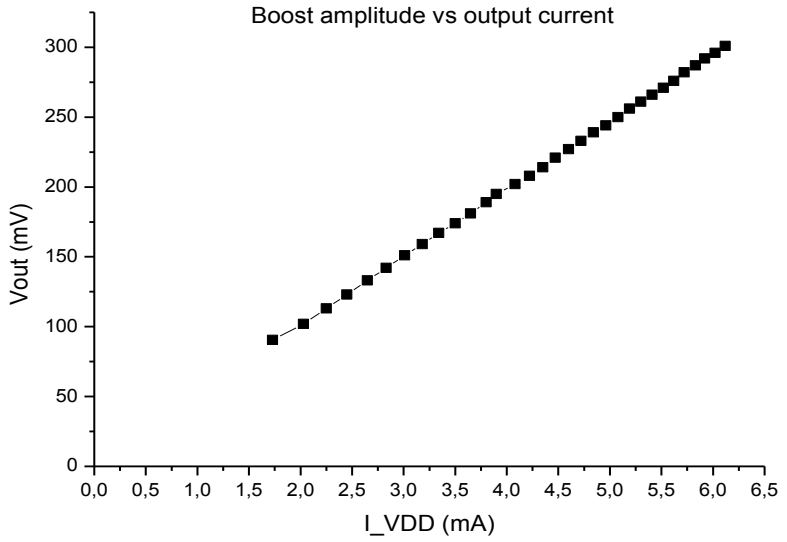


Boost Output Current Mirror

- IBIASD_DRIVER current mirror
- Design value
  IBIASD_DRIVER/Ibiasd = 2
- Fair linearity
- Drive current limited to 6.12 mA
  → $Vboost_{max}$ ~300mV



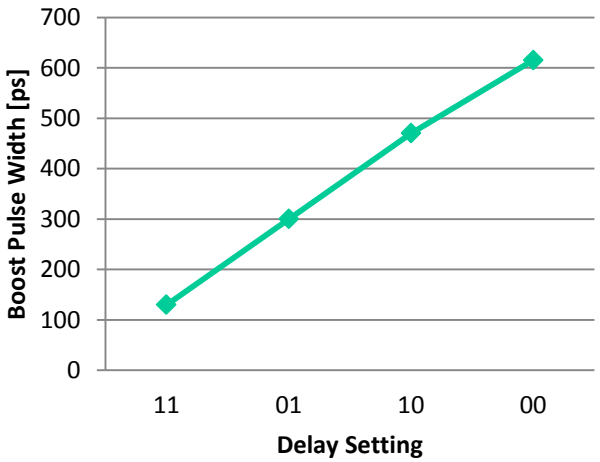
➔ Enhancement:
Make boost current sink M8 stronger

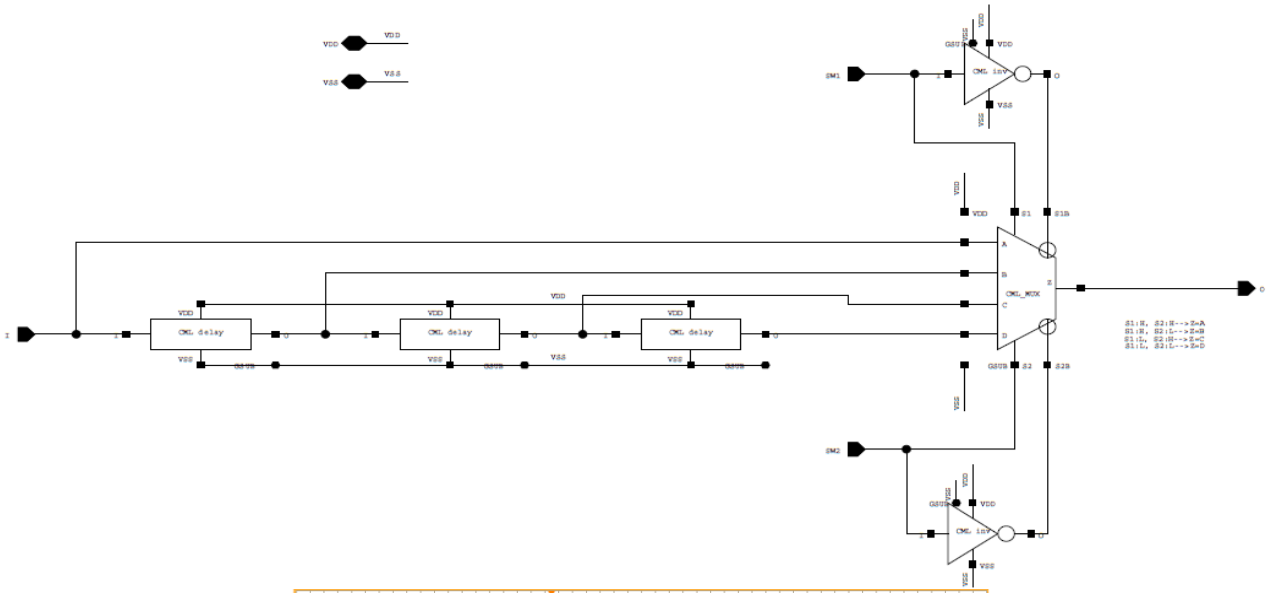


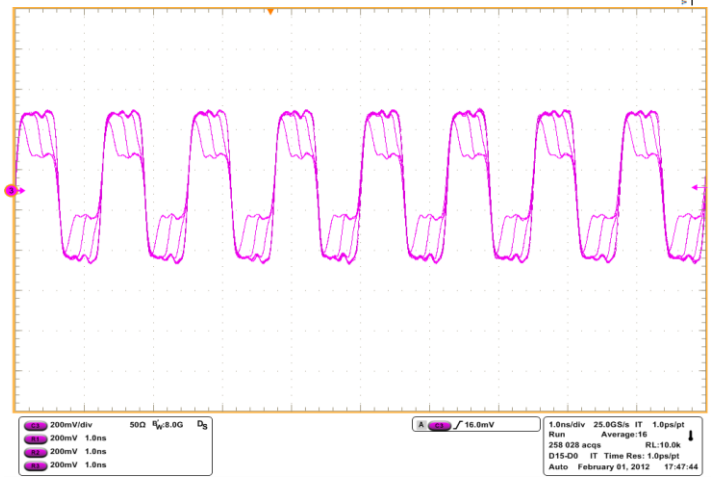
Delay Settings

Setting SW[1:0]	Pulse Width [ps]
11	130
01	300
10	470
00	615

➔ ~170 ps per delay buffer



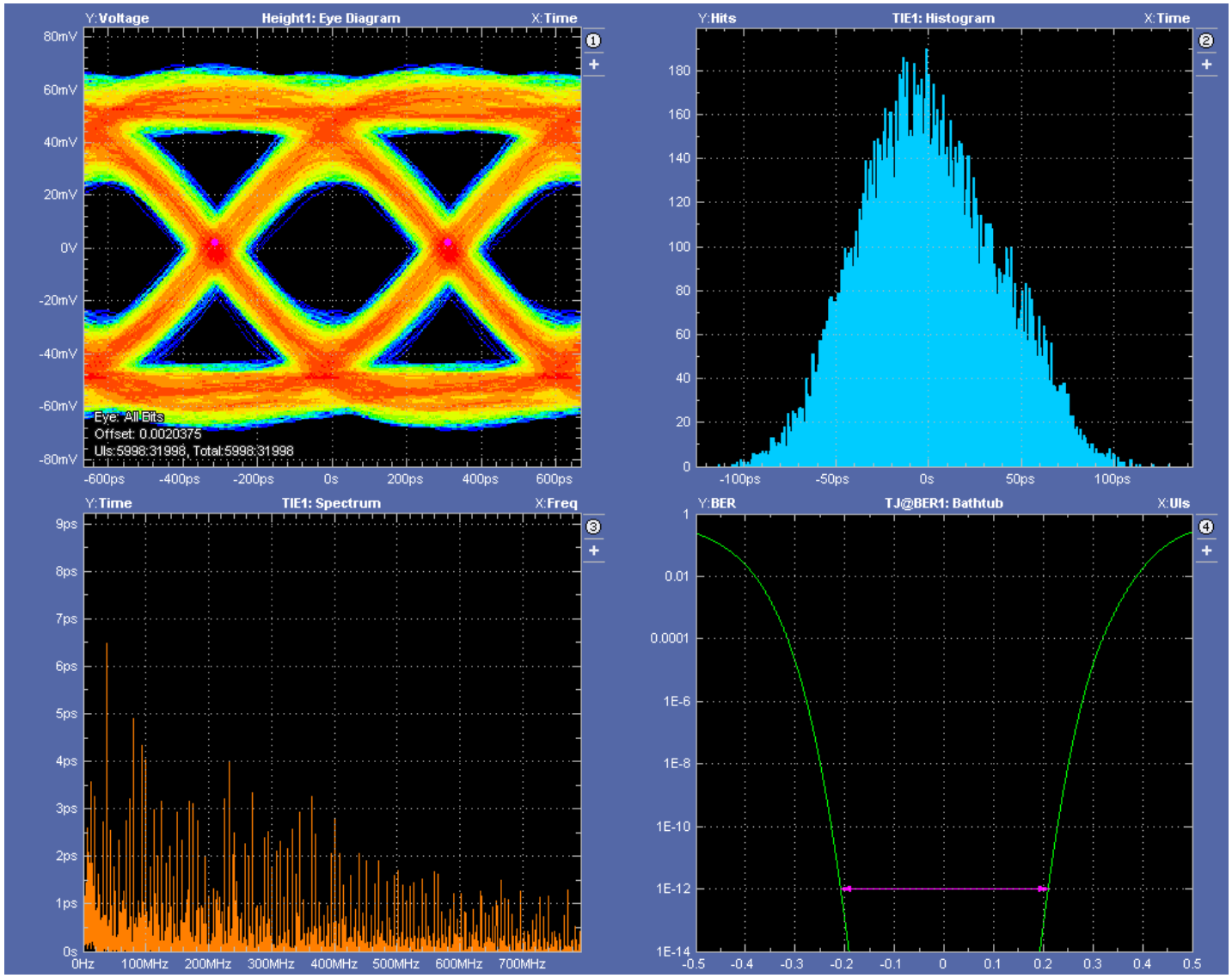




800 MHz clock, different delay settings

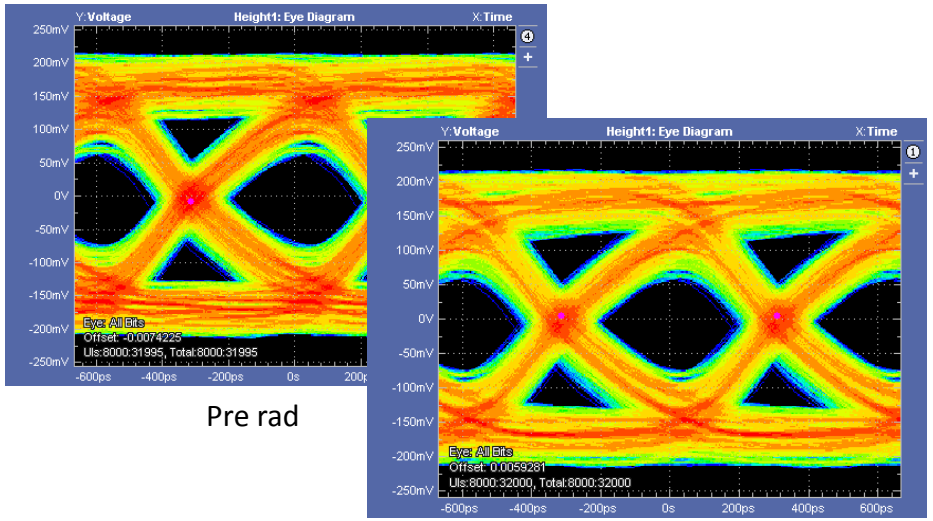
Signal Integrity Characterization

- 1.6 Gbps LFSR-8
- 30 cm kapton cable + 20m AWG26 twisted pair cable



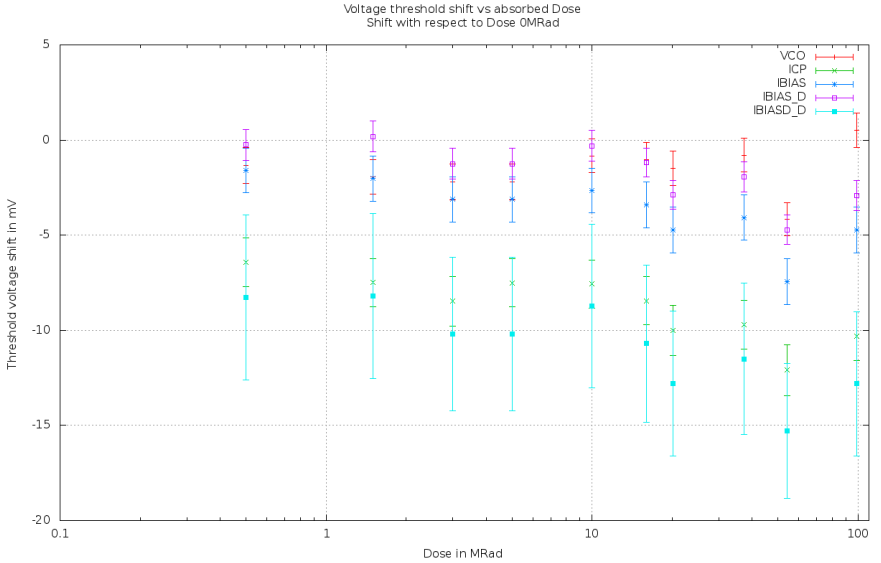
X-ray Irradiation

- TSMC 65nm TID tolerance:
  - V_{THR} shift (wide pMOS and nMOS only)
  - PLL + Gbit link performance
- Up to 100 Mrad (60keV X-ray tube, Karlsruhe)
- Dose rates: ~300 kRad/h (initial) → ~2Mrad/h (end)
- Annealing after each step: 80°C for 100 mir



Pre rad

100 Mrad



No TID induced degradiation observed up to 100 Mrad

DHPT10 CML TX
Main driver

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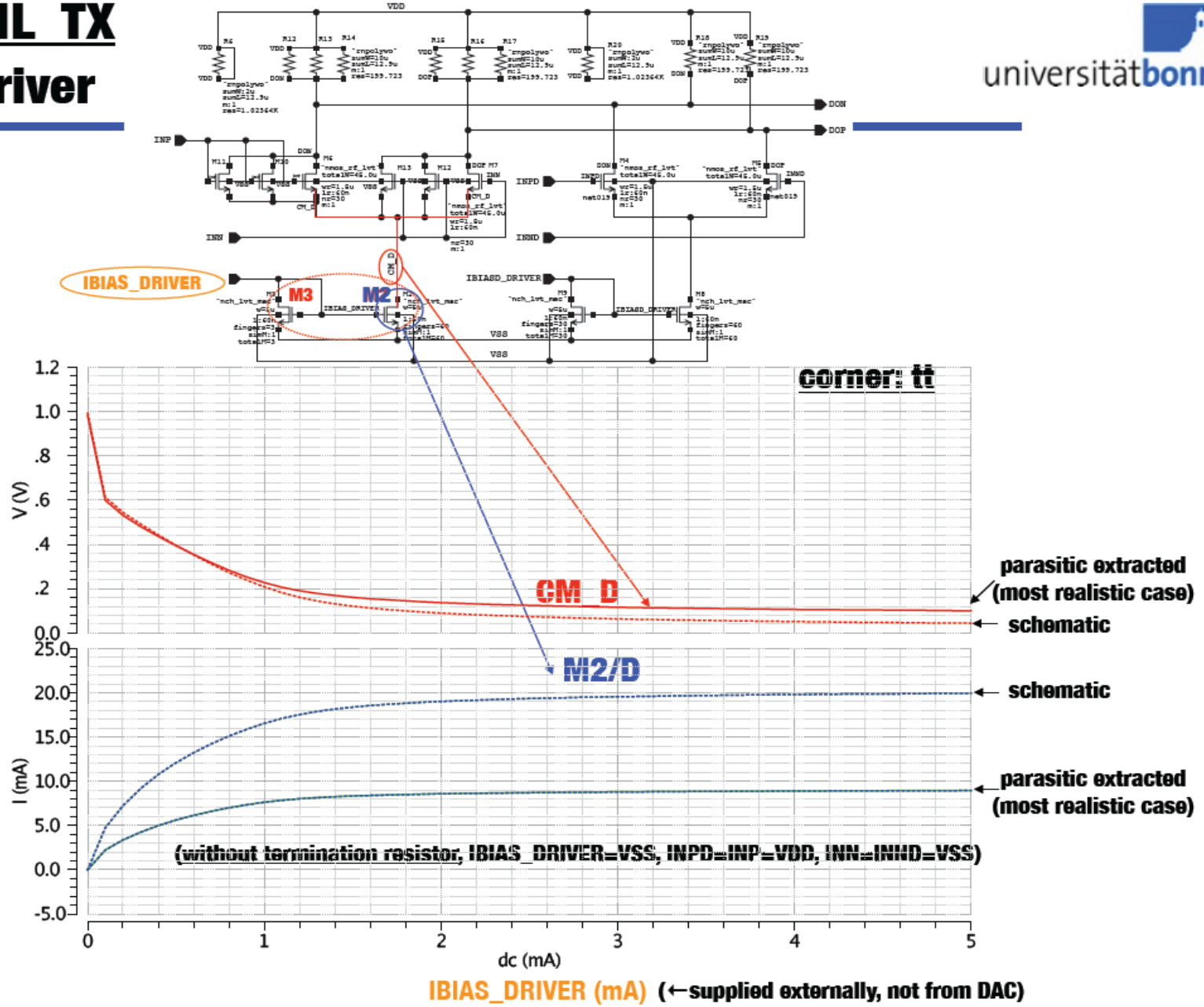
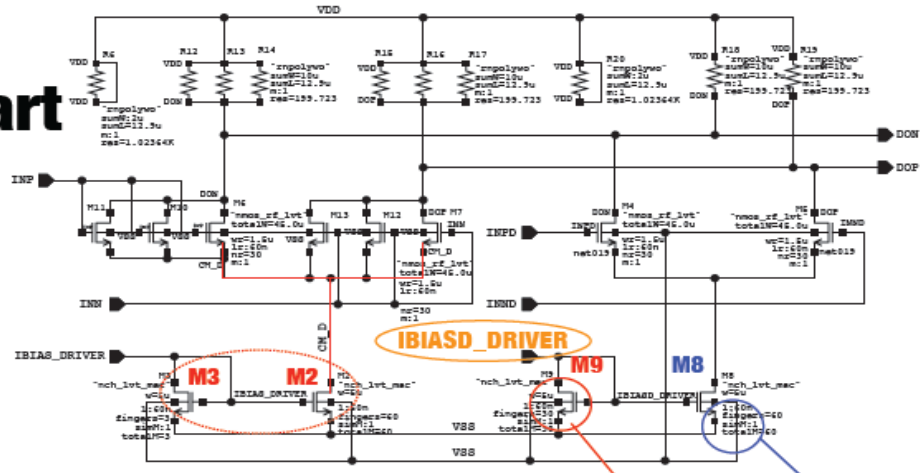


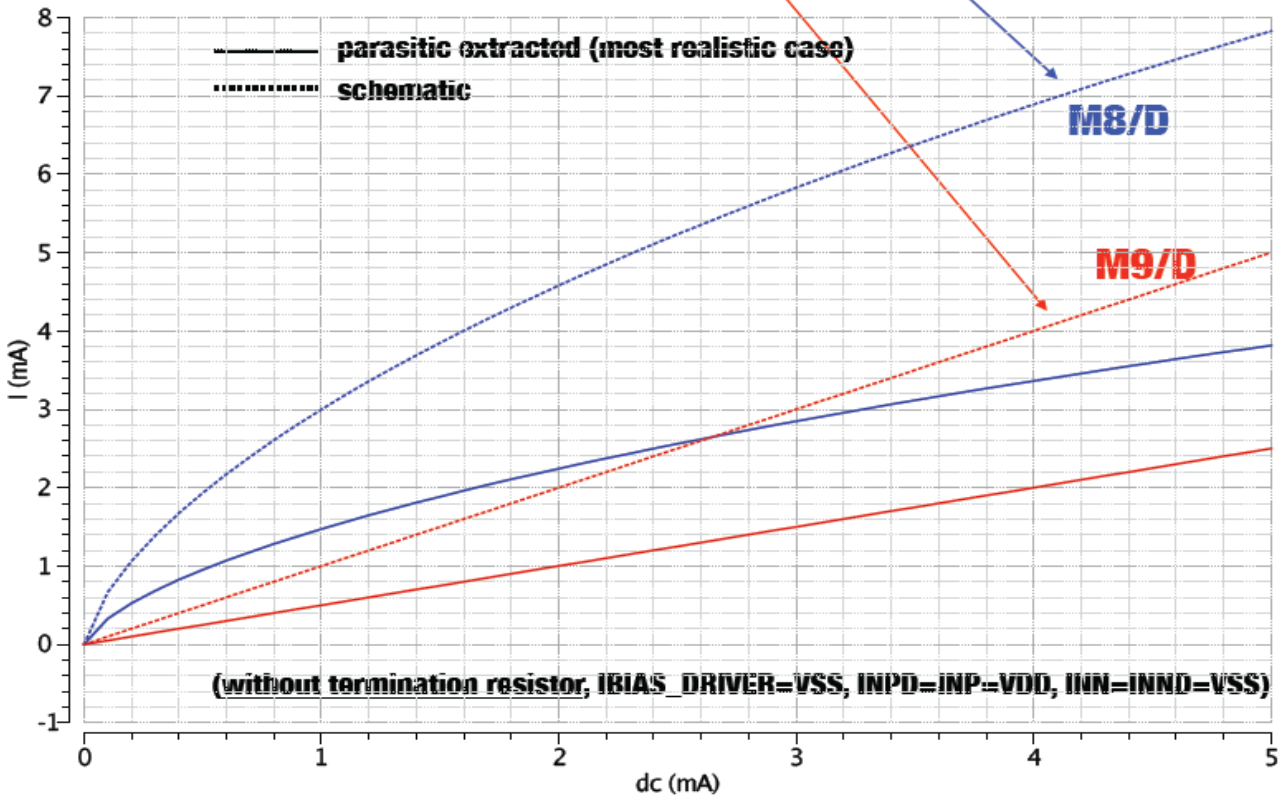
06.05.2015, T.Kishishita

DHPT10 CML_TX

Pre-emphasis part

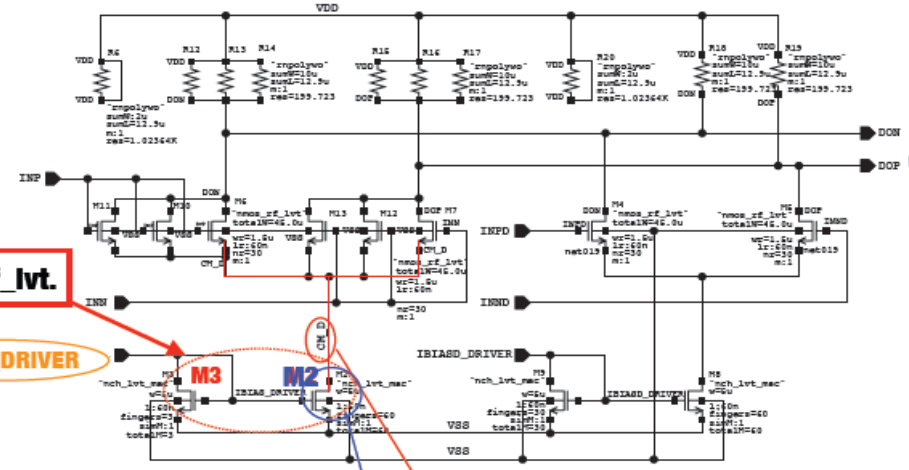


corner: tt



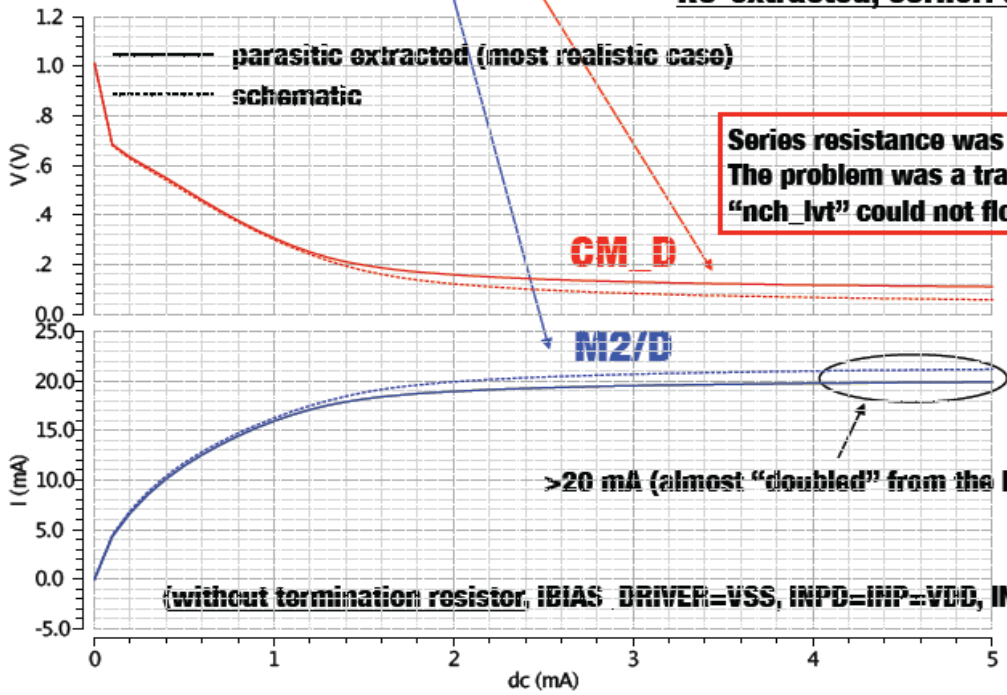
21.04.2015, T.Kishishita

Improved Design
Main driver



replaced from "nch_lvt" to nmos_rf_lvt.

RC-extracted, corner: tt



Series resistance was not a major problem.
The problem was a transistor type of the current mirror.
"nch_lvt" could not flow much current.

>20 mA (almost "doubled" from the DHPT10 design)

(without termination resistor, IBIAS_DRIVER=VSS, INPD=INP=VDD, INN=INND=VSS)

Improved Design
Pre-emphasis part

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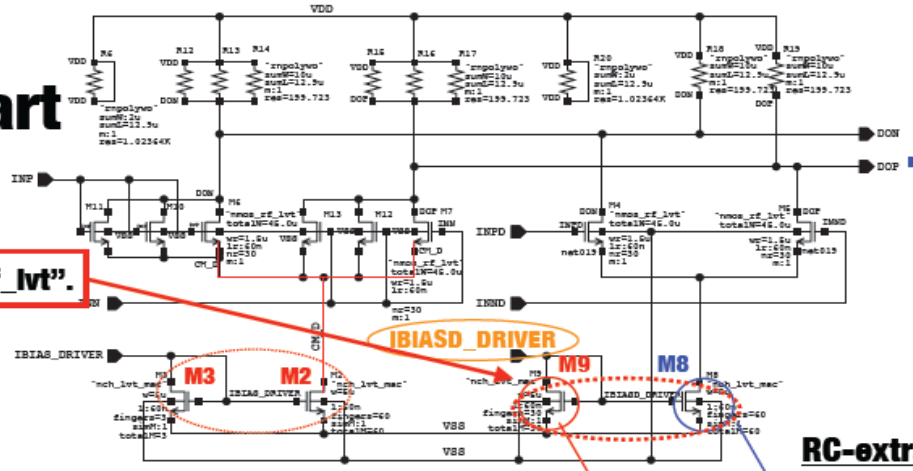
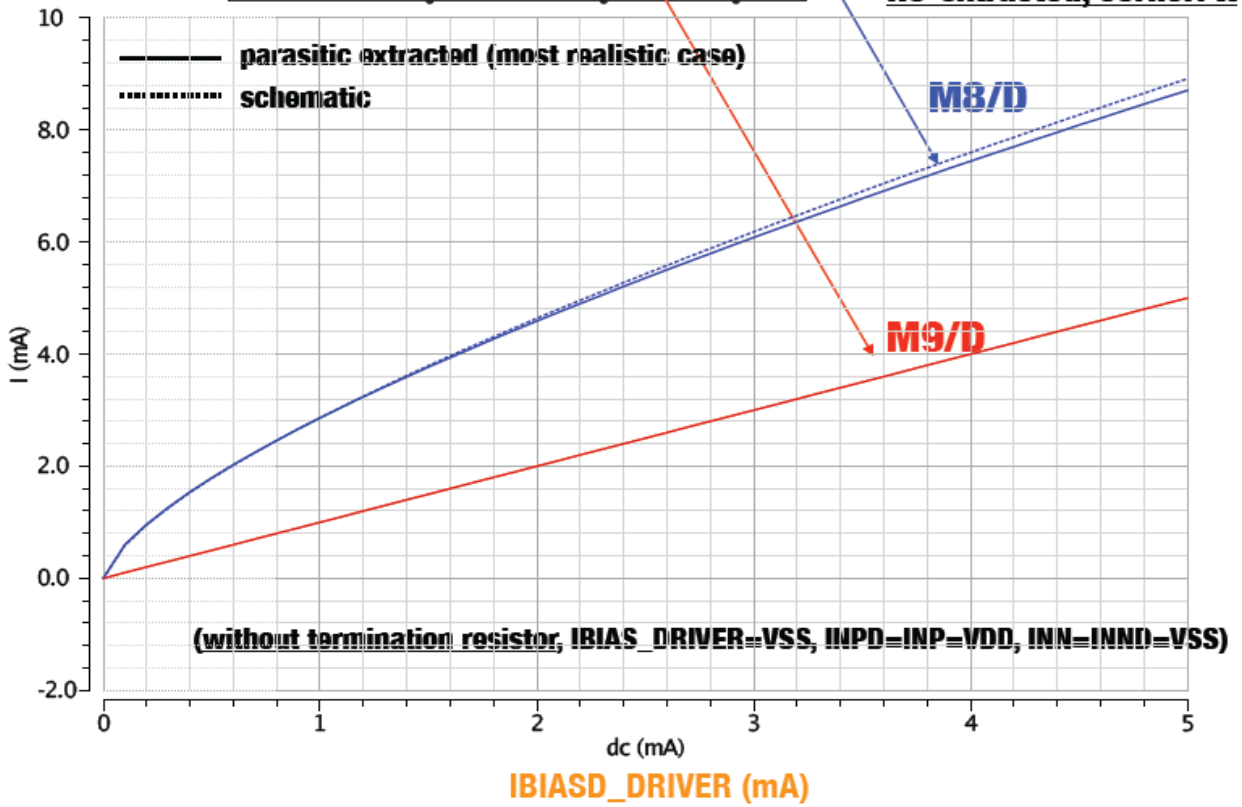
replaced from "nch_lvt" to "nmos_rf_lvt".



RC-extracted, corner: tt



21.04.2015, T.Kishishita

CML Driver Enhancements

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- Delay settings → Ok
  - minimum delay setting (SW[1:0]=11 → 130 ps) shows best eye diagram for long cables
  - Possible optimization: make delay steps a bit smaller (170 ps → 120 ps, 7 → 5 inverter per delay)

- Output amplitude
  - Signal amplitude on DHPT 1.0 less than expected
  - **Identified parasitic resistance within the NMOS current sources (wiring & vias) → changed to RF-Transistor layout**
  - Max. pre-emphasis level increased by 30%
  - Max. output amplitude almost doubled

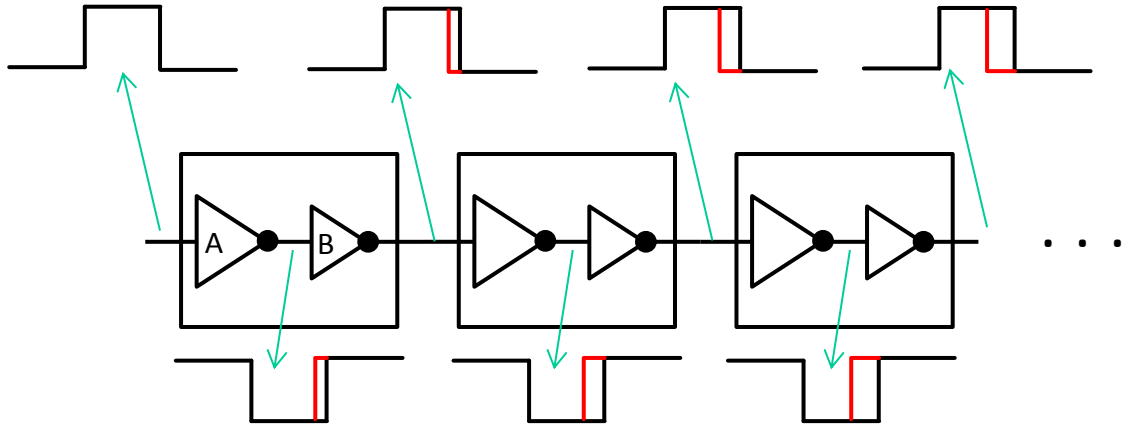
DHPT 1.0

DELAY ELEMENTS

Delay Element Issues

- Programmable delay lines made from std. cell delay elements (dual inverters)
- Inverter have usually unequal propagation delays for rising and falling edges (Asymmetry of PMOS-NMOS drive strength, process corners, W/L…)
- The **std. cell delay** elements consist of **alternating no-equal sized inverters**

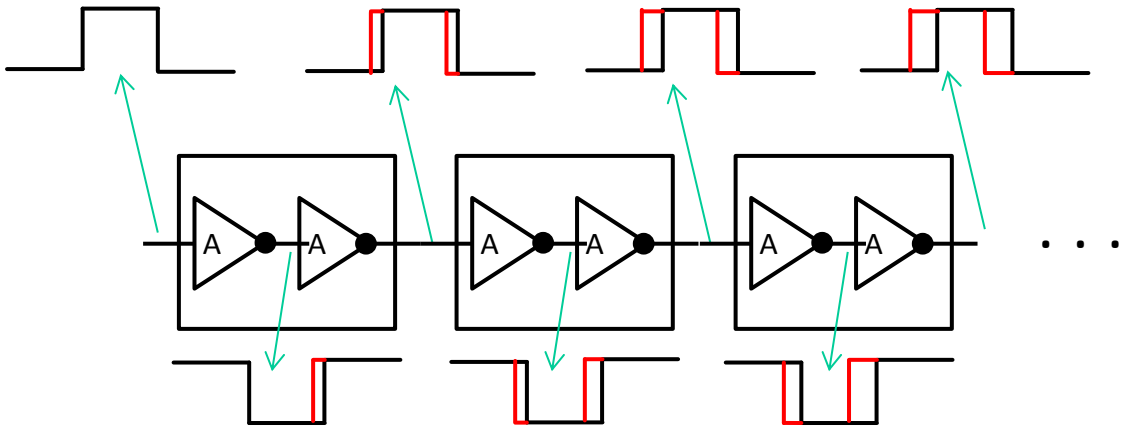
→The difference in t_{pd} for rising and falling edges for inverter A and B is <u>different</u>!



→ Duty cycle distortion increases (accumulates) with the number of delay elements used, i.e. the programmed delay time

Delay Element Issues cont.

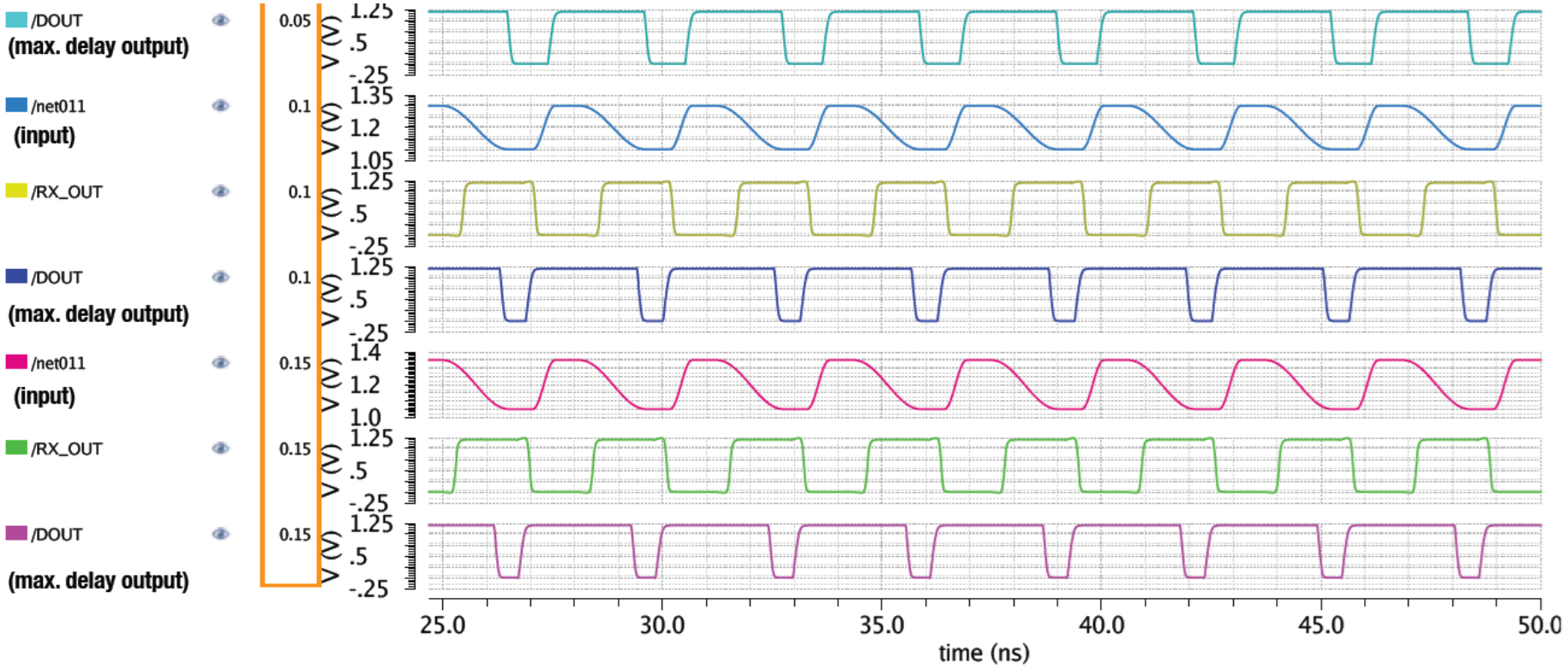
- If all **inverters in the delay chain are equal** (and the number of inverters is even), **no duty cycle distortion** occurs (differences in rising and falling edge propagation delay cancel out)



➔ Implemented new, custom made delays based on identical inverters

Duty cycle distortion

- Duty cycle distortion was overlooked during DHPT 1.0 sign-off



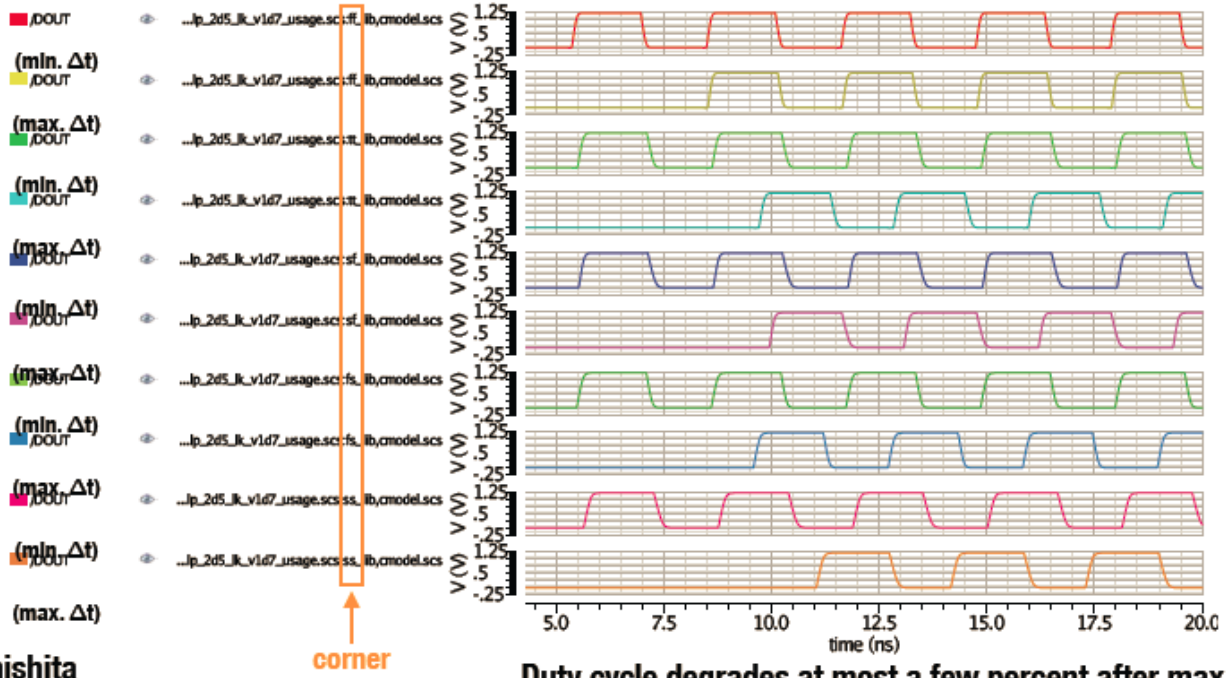
Delay Element Modification

- Custom delay elements made out of identical inverters

All corners covers 3.125 ns (←320 MHz).

Max. delay time with extracted model

	Δt	duty cycle (min. Δt)	duty cycle (max. Δt)
tt	4.20 ns	52.0%	53.3%
ff	3.15 ns	51.4%	52.2%
fs	4.10 ns	51.6%	51.8%
sf	4.43 ns	52.2%	54.9%
ss	5.42 ns	52.8%	54.9%



Duty cycle degrades at most a few percent after max. delay.

07.04.2015, T.Kishishita

Delay Element Re-design Status

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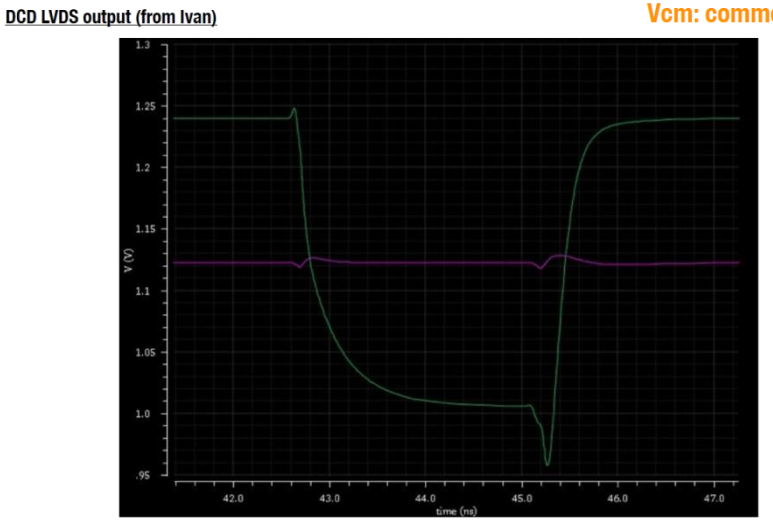
- Origin of the bug: **understood**, reproducible
- Design modification: **identified**
- Re-design on schematic level: **done**
- Re-design on layout level: **done**
- Simulation of extracted layout (all corners): **ongoing**

DHPT 1.0

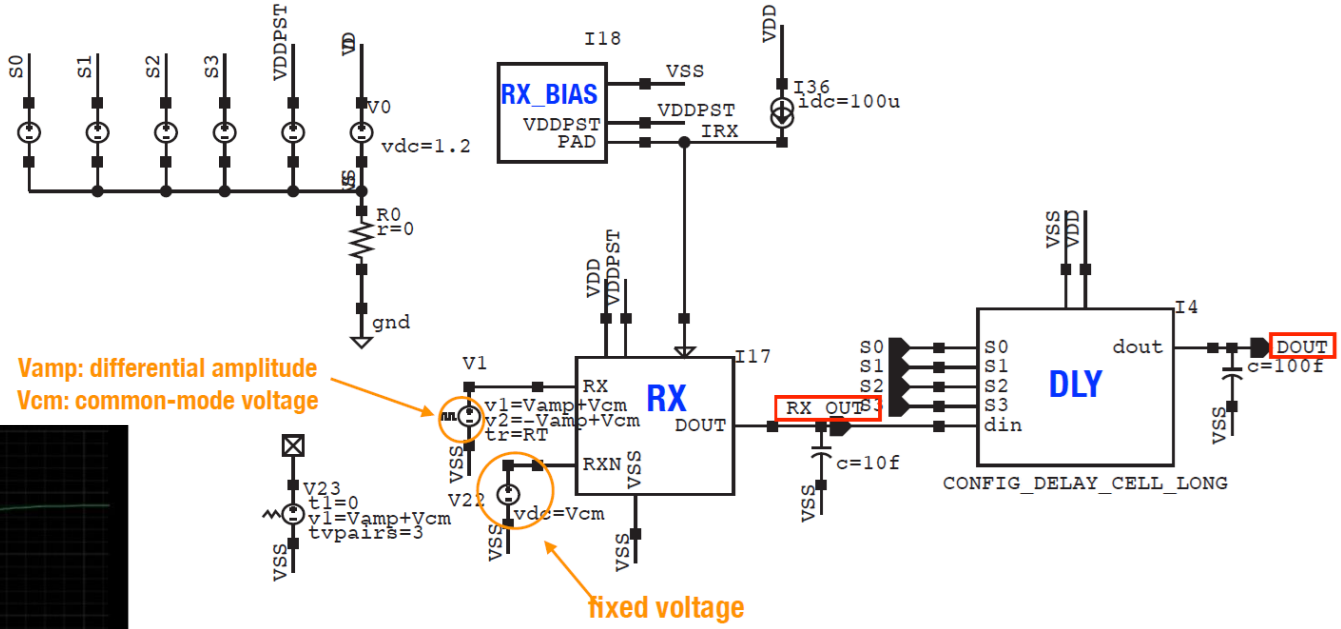
DCD DATA RECEIVER

DCD Data Receiver

- Single ended DCD data receivers based on LVDS receivers → low voltage single ended signaling (LVSE)



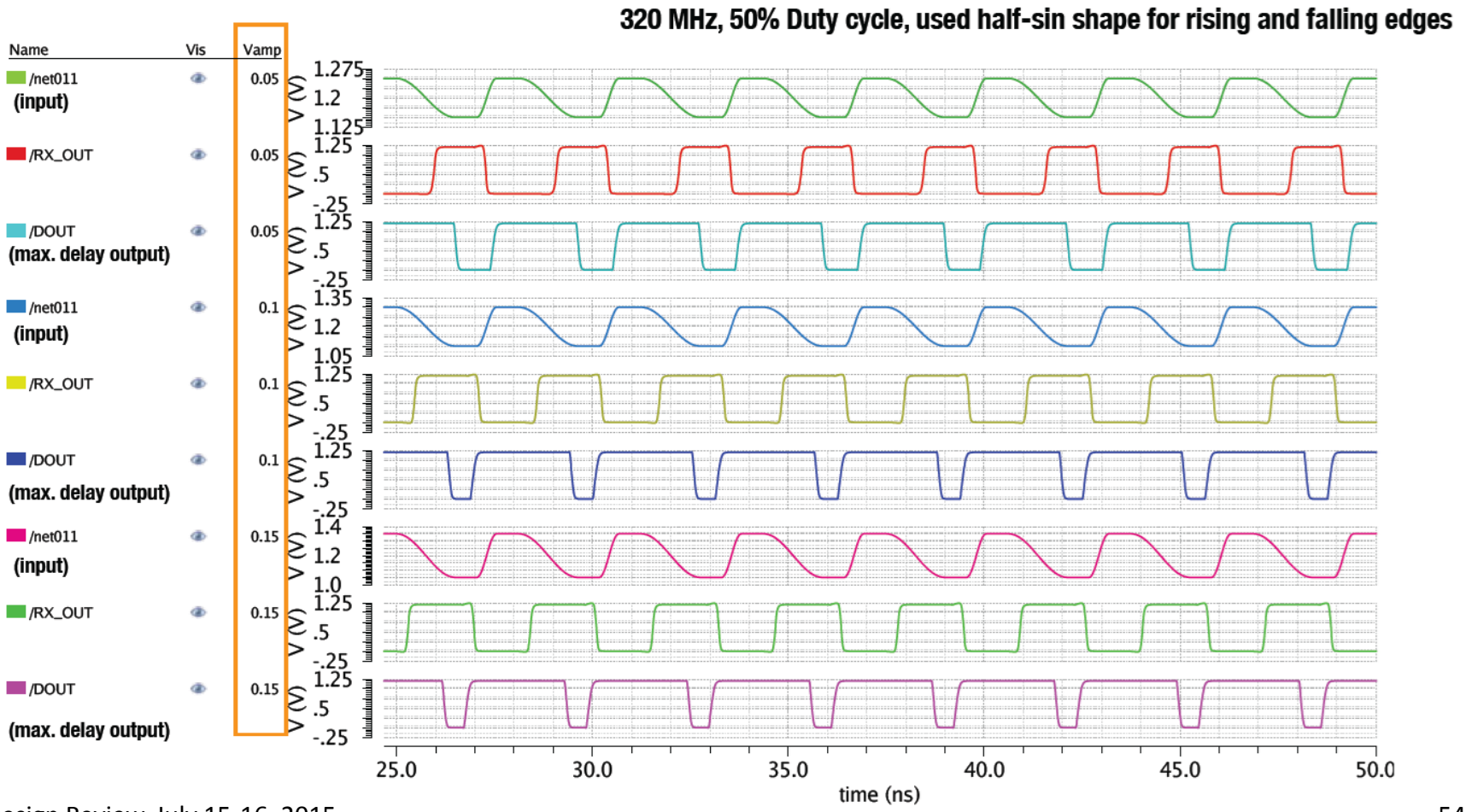
- the falling and rising edges with non-symmetrical shape
- differential amplitude of 120 mV



Duty cycle distortion

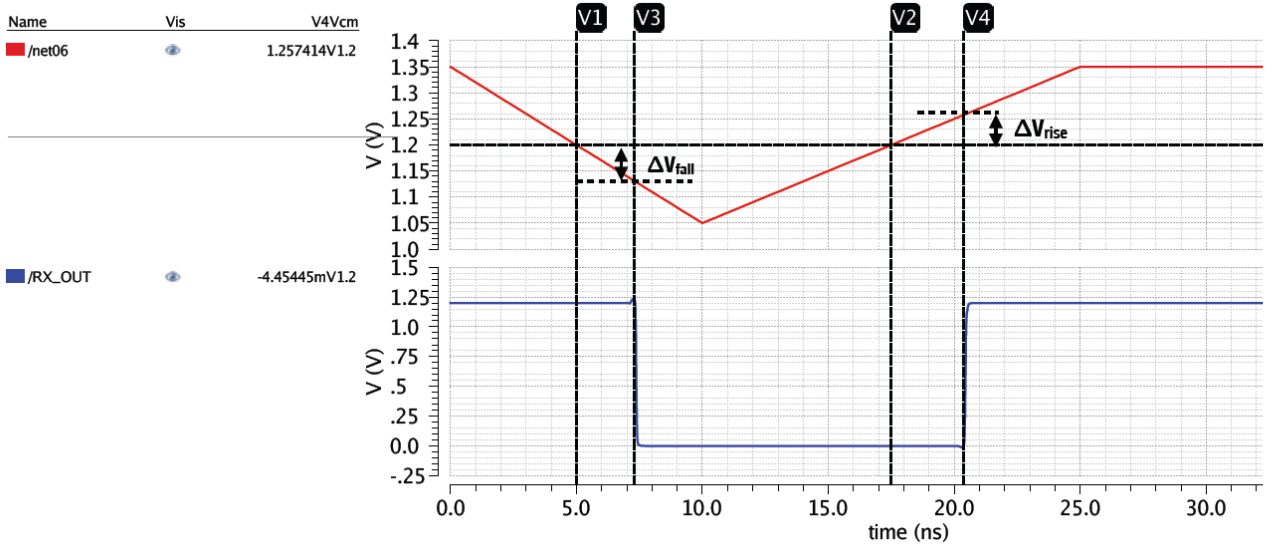
- Asymmetric rise- and fall time of the input signal (+ effect of hysteresis)
- Delay elements (see later slides)

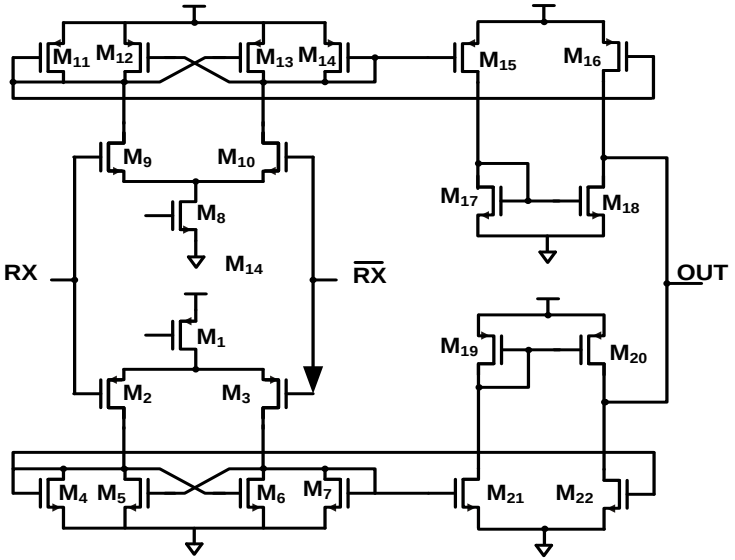
Dependence of the differential amplitude (Vamp, nominal corner)



LVDS Receiver (DHPT 1.0)

- LVDS RX with build-in hysteresis





Markers

	Vcm	V1	V2	V3	V4
x		5.0ns	17.4689ns	7.31256ns	20.3707ns
/net06					
/net06	1.2	1.2V	1.199378V	1.130623V	1.257414V
/RX_OUT					
/RX_OUT	1.2	1.2V	37.1315nV	1.22718V	-4.45445mV

	ΔVfall	ΔVrise
ff	55 mV	46 mV
fs	71 mV	57 mV
sf	68 mV	57 mV
ss	85 mV	68 mV

ΔV_{rise}=57 mV
ΔV_{fall}=70 mV (for nominal corner)

25.03.2015, T.Kishishita

P.2

LVDS Receiver Design Modification

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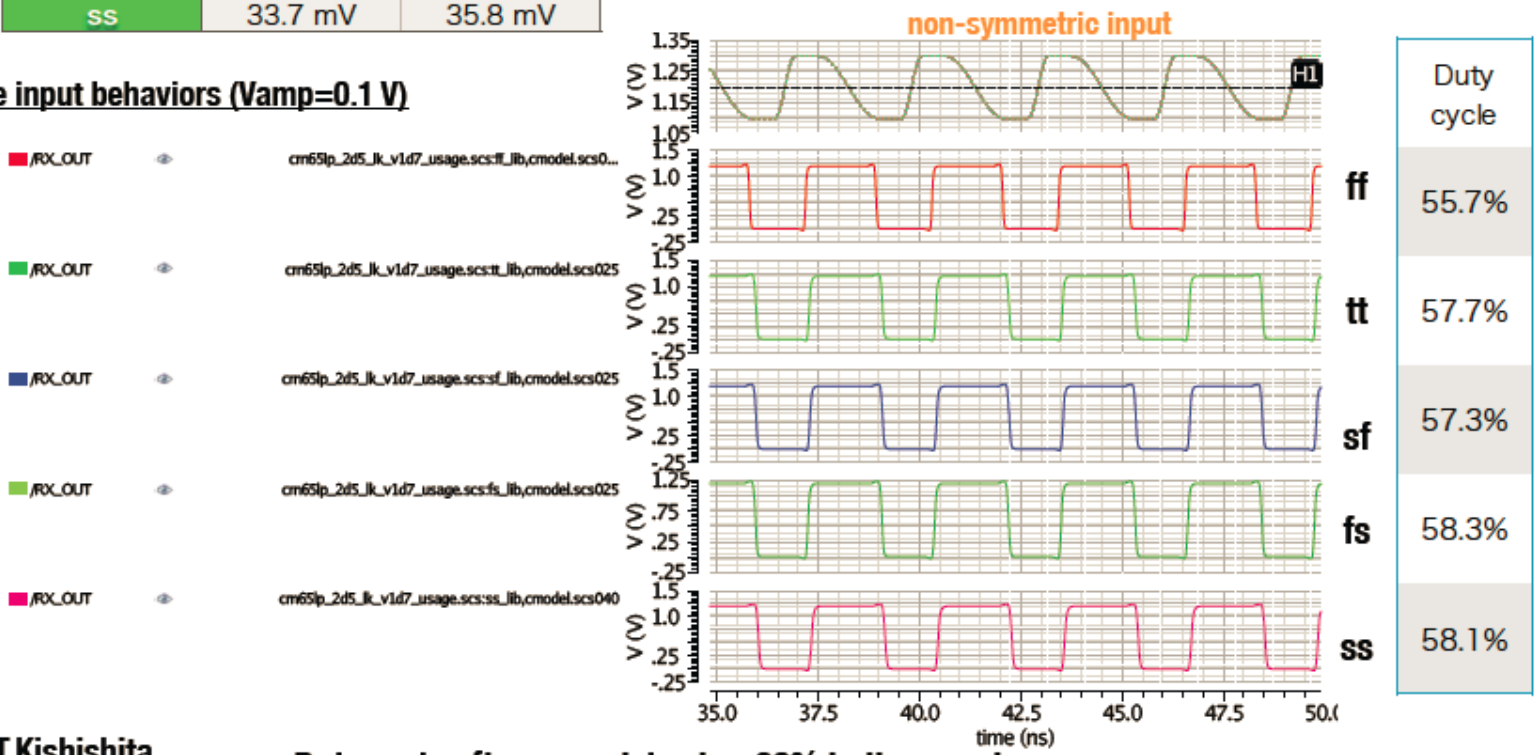
FET sizes and layout modified to reduce hysteresis (~50% of the current DHPT1.0 design).

Hysteresis values with extracted model

	ΔVfall	ΔVrise
tt	27.5 mV	34.4 mV
ff	19.8 mV	30.0 mV
fs	29.1 mV	33.4 mV
sf	26.3 mV	34.1 mV
ss	33.7 mV	35.8 mV

DCD-like input behaviors (Vamp=0.1 V)



07.04.2015, T.Kishishita

Duty cycle after max. delay is ~60% in the worst corner.

Data Receiver Re-Design Status

- Enhancement: Reduced (remove) the input hysteresis to be less sensitive to duty cycle distortion due to asymmetric rise- and fall time of the input signal → **done**

➔ **Suggested improvements of the DCD output signal**

  - Symmetric rise- and fall times
  - Higher signal amplitude

SEU Tolerance

- Cross section measured with 24 GeV pions
  - $\sigma_{SEU\_FF} = 0.64 \cdot 10^{-14} cm^2$
  - $\sigma_{SEU\_SRAM} = 9.7 \cdot 10^{-14} cm^2$
- Result is comparable with other data published for 65nm memory cells
- SEU rate extrapolated by assuming 10^4 neutrons s^{-1} cm^{-2}

Technology Node	Product Family	Neutron Cross-section per Bit(1)		
		Configuration Memory	Block Ram	Error
250 nm	Virtex	9.90×10^{-15}	9.90×10^{-15}	±10%
180 nm	Virtex-E	1.12×10^{-14}	1.12×10^{-14}	±10%
150 nm	Virtex-II	2.56×10^{-14}	2.64×10^{-14}	±10%
130 nm	Virtex-II Pro	2.74×10^{-14}	3.91×10^{-14}	±10%
90 nm	Virtex-4	1.55×10^{-14}	2.74×10^{-14}	±10%
65 nm	Virtex-5	6.70×10^{-15}	3.96×10^{-14}	±10%

From XILINX application note UG116

Memory type	Size	Cross section	Mean time between SEU per one chip	Mean time between SEU for whole detector	Refresh rate	Mitigation	Critical?
Raw data buffer	0.5 Mbit	σ_{SRAM}	~30 min	13 sec	20 us		
Pedestals	0.5 Mbit	σ_{SRAM}	~30 min	13 sec	~15 min	Humming code protection. Single SEU corrected every 20 us, Double SEUs are detected.	yes
Configuration Register	368 bit	σ_{FF}	490 day	3 day	No	Triple redundancy, protects against single SEU.	yes
Data processing logic	45 kbit	σ_{FF}	4 day	36min	20 us		

Low energy Neutron vs. High energy Pions

cross section for 14 MeV neutrons

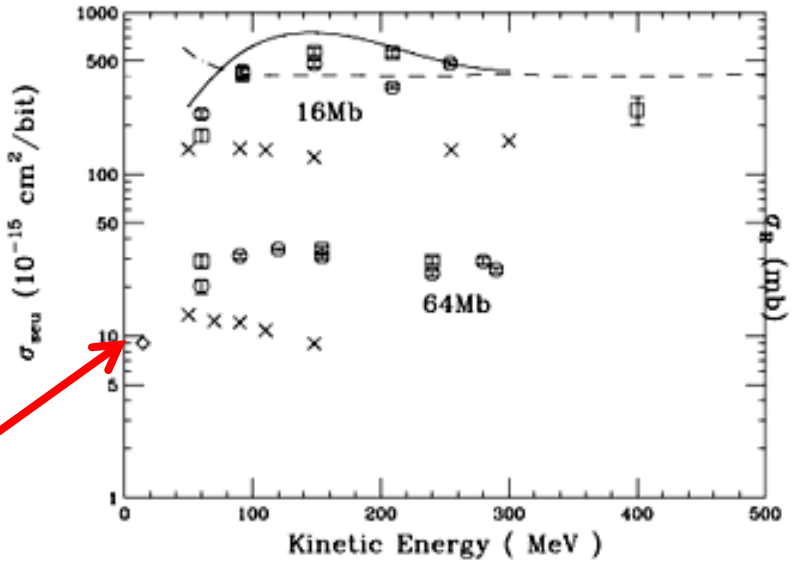
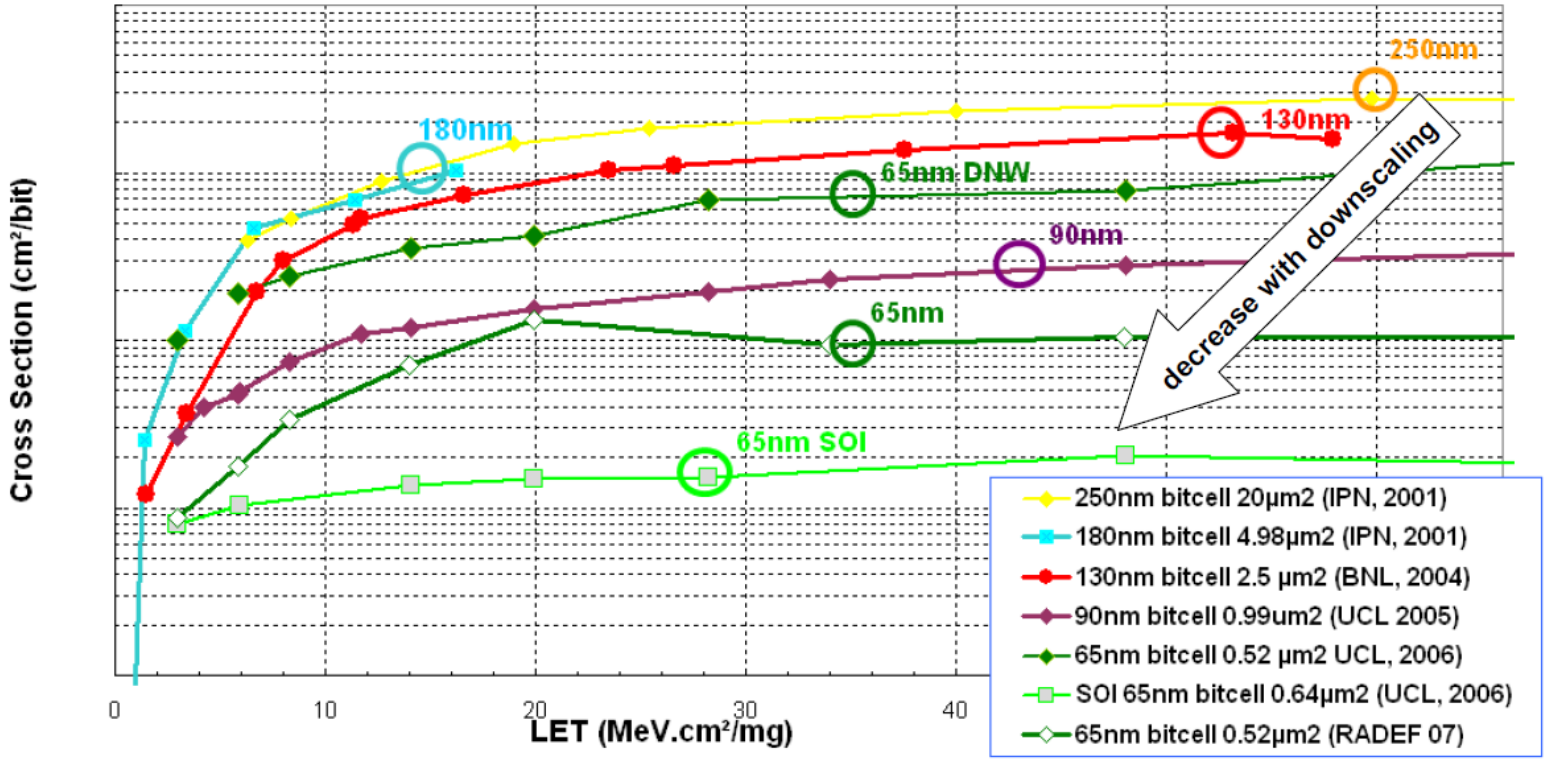


Figure 1. Crosses show measured cross sections for proton-induced SEU in 16 Mb and 64 Mb DRAM samples. The 16 Mb sample used the TEC technology. Squares show data for π^-, circles for π^+ for the same chip. The solid curve shows computed [8] π^+/π^- averaged reaction cross sections for ^{28}Si using the right hand scale. The pi-nucleon 3-3 resonance is prominent in the 16 Mb macroscopic device. The dashed curve shows proton reaction cross sections.[9] A single datum shows the cross section for 14 MeV neutrons.

R. J. Peterson, "Radiation-induced errors in memory chips" http://dx.doi.org/10.1590/S0103-97332003000200013

Heavy ions test results for commercial ST SRAMs in CMOS 250/180/130/90/65 nm



- **SEU cross-sections intrinsic reduction by 30× from commercial CMOS 250nm down to 65nm**
  - LET threshold unchanged
- **Moving from technology 250nm to 65nm naturally improves by 50× the SEU rate/bit/day**
  - estimations on XS here above with CREME96, GEO, minimum solar activity, 100mils Alu shielding

Publications on Neutron induced SEU cross section measurements compared to charged particles

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 56, NO. 6, DECEMBER 2009 3085

Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions

Brian D. Sierawski, *Member, IEEE*, Jonathan A. Pellish, *Member, IEEE*, Robert A. Reed, *Senior Member, IEEE*, Ronald D. Schrimpf, *Fellow, IEEE*, Kevin M. Warren, *Member, IEEE*, Robert A. Weller, *Senior Member, IEEE*, Marcus H. Mendenhall, *Member, IEEE*, Jeffrey D. Black, *Member, IEEE*, Alan D. Tipton, *Member, IEEE*, Michael A. Xapsos, *Member, IEEE*, Robert C. Baumann, *Member, IEEE*, Xiaowei Deng, *Member, IEEE*, Michael J. Campola, *Member, IEEE*, Mark R. Friendlich, Hak S. Kim, Anthony M. Phan, and Christina M. Seidleck

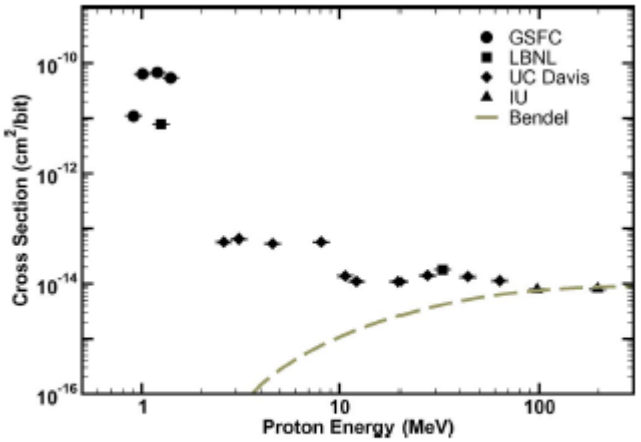


Fig. 1. Proton single event upset cross-section curve for a 65 nm bulk CMOS SRAM. Proton datasets with dramatic increases in cross section are not amenable to traditional rate prediction models; two parameter Bendel fit shown for comparison.

There is an **increase** in SEU cross section for low energy, charged particles because of the onset of direct ionization (high LET, dE/dx)

848 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 3, JUNE 2011

14 MeV Neutrons SEU Cross Sections in Deep Submicron Devices Calculated Using Heavy Ion SEU Cross Sections

Avner Haran, *Member, IEEE*, Joseph Barak, *Member, IEEE*, Leo Weissman, David David, and Eitan Keren

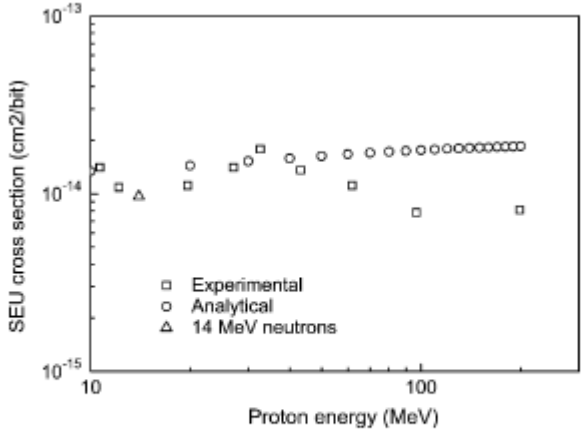


Fig. 6. Experimental proton cross section for the 65 nm SRAM presented in [10]. The fit for $E_p \geq 10$ MeV are calculated using the expressions in [14]. Also shown is the calculated cross section for 14 MeV neutrons.

There is **NO** increase in SEU cross section for low energy neutrons particles (no direct ionization , of course)

DHPT 1.0

DATA PROCESSING FUNCTIONAL VERIFICATION

Data Processing

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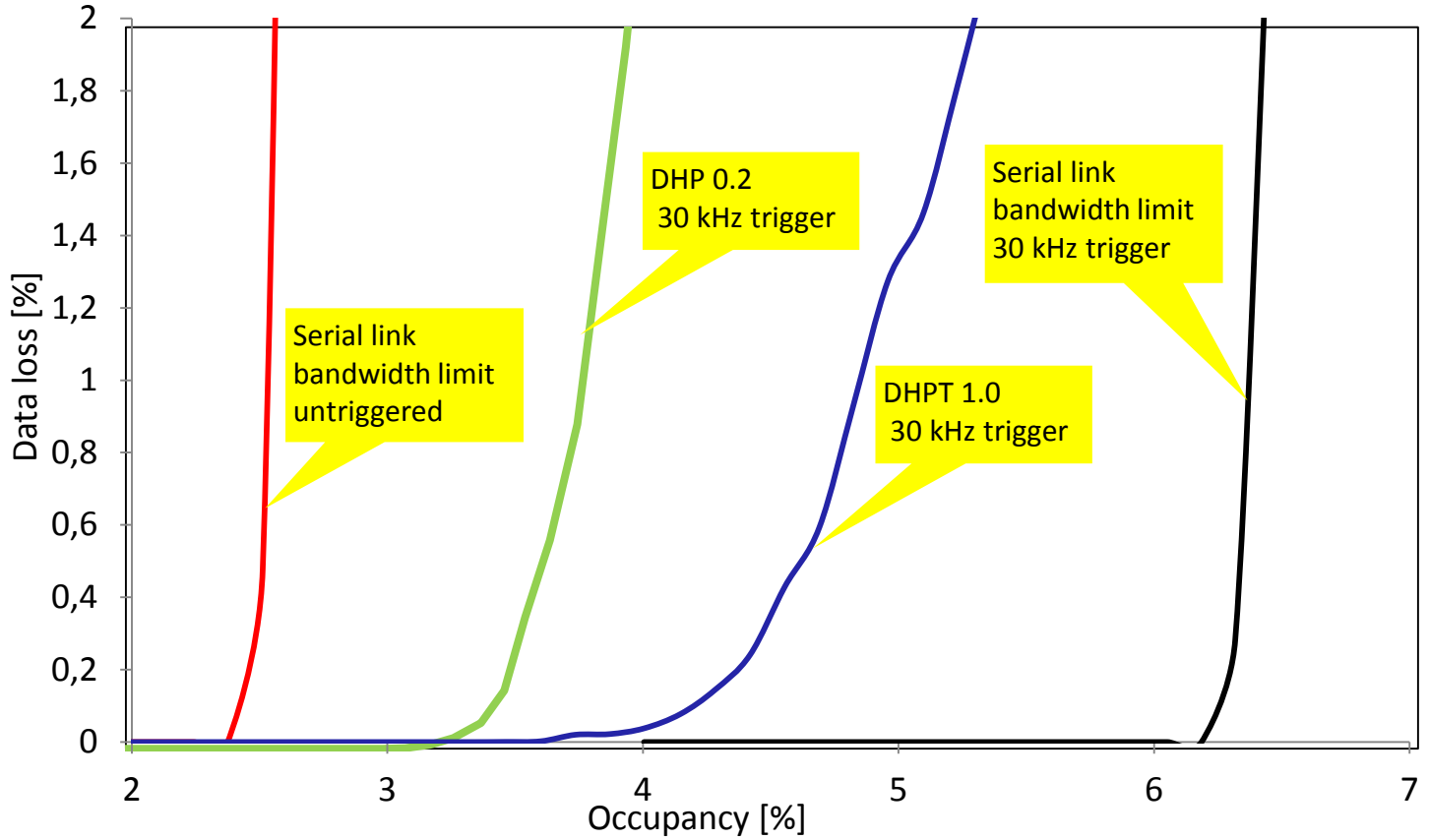
- So far no issues seen
- Things to look into in more detail:
  - Processing of high occupancy data
  - Gated mode
  - Power on configuration

➔ Need more system tests to assess the need of design changes

Expected DHPT 1.0 Data Losses

- FIFO 1: 64 FIFOs in front of the hit finder ➔ 256 words deep (DHP 0.2 → 16)
- FIFO 2: between hit finder and serializer ➔ 4096 word deep (DHP 0.2 → 512)



Data processing enhancements

➔ If not absolutely needed we would like to avoid the process of re-synthesizing the design (lot of work!!!)

What is really needed (no “nice to have” features)?

- Include Chip ID (JTAG programmable) in data header (needed?)
- Modifications for Gated Mode ?
- What else?

DHPT (System) Tests to be done

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- DHPT offsets → DCD
- DCD/DHPT (data, offset and JTAG) communication after TID damage - done
- High occupancy data processing - pending
- Gated mode – pending
- Triggering – pending
- Raw data transfer – done?
- JTAG timing (next DCD should follow the industrial standard wrt clock edges)
- SEU x-section for realistic neutron energy spectrum (calculate from 24 GeV proton data or re-measure) – done
- Power-up configuration Ok?
- …

Summary

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- Bugs / Enhancements of the full custom blocks
  - Serializer bug → fixed ✓
  - CML driver enhancement -> ongoing (✓)
  - Delay element issue → fixed, layout work in progress (✓)
  - Data reciever robustness → fixed, layout work in progress (✓)
  - Input pad optimization for low capacitive load – in progress
- Digital (data processing) enhancements
  - To be discussed
- Sytem test, system test, system tests!

DHPT 1.1 Production

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- TSMC 65nm MPW submissions costs
  - 12 mm^2, one wafer (100 chips) included: 59 TUSD + 12 TUSD for bumping ➔ 52 TEUR
  - Extra 12“ wafer (100 chips): 9 TUSD (7TEUR)
  - Two MPW runs per month, turn-around ~12 weeks

- DHPT 1.1 production
  - MPW + 9 extra wafers (1000 chips)
  - Extra wafers to be ordered after successful verification

BACKUP

DHPT 1.0

COMMAND TIMING

Notes on DHP Command Timing and Format

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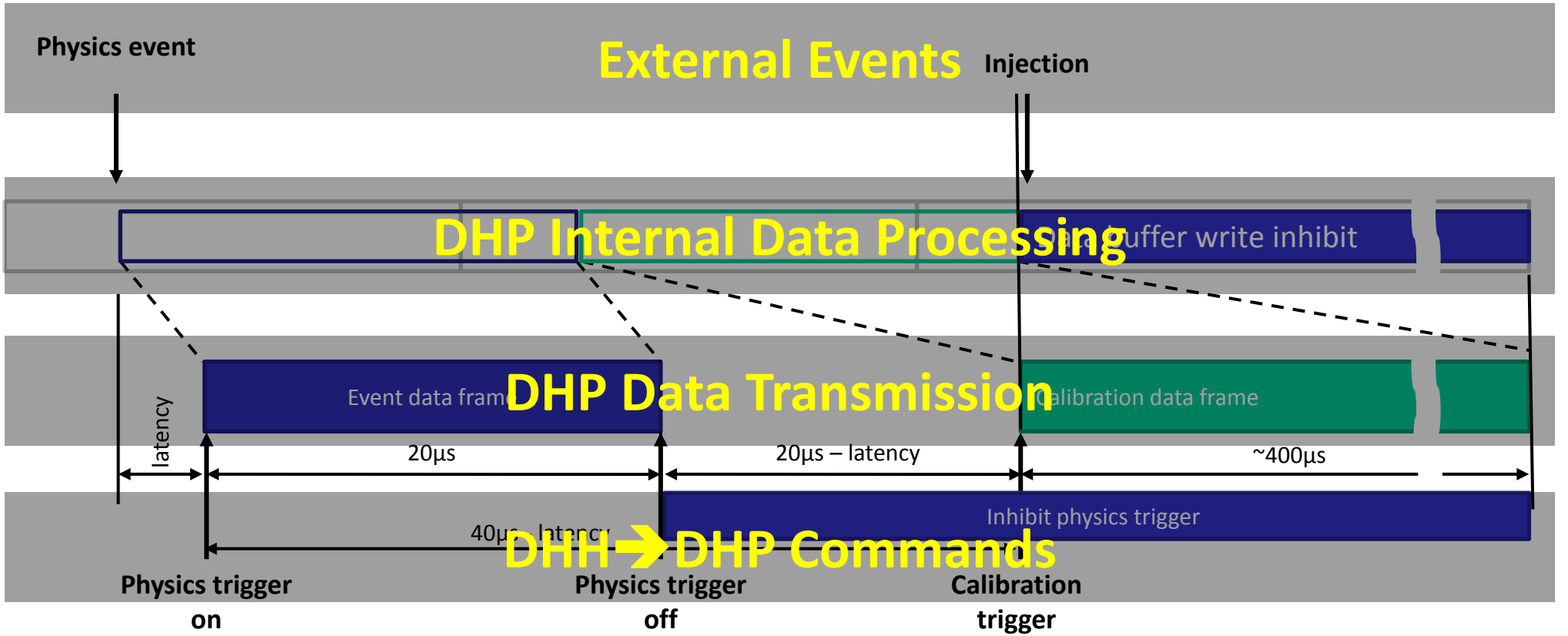
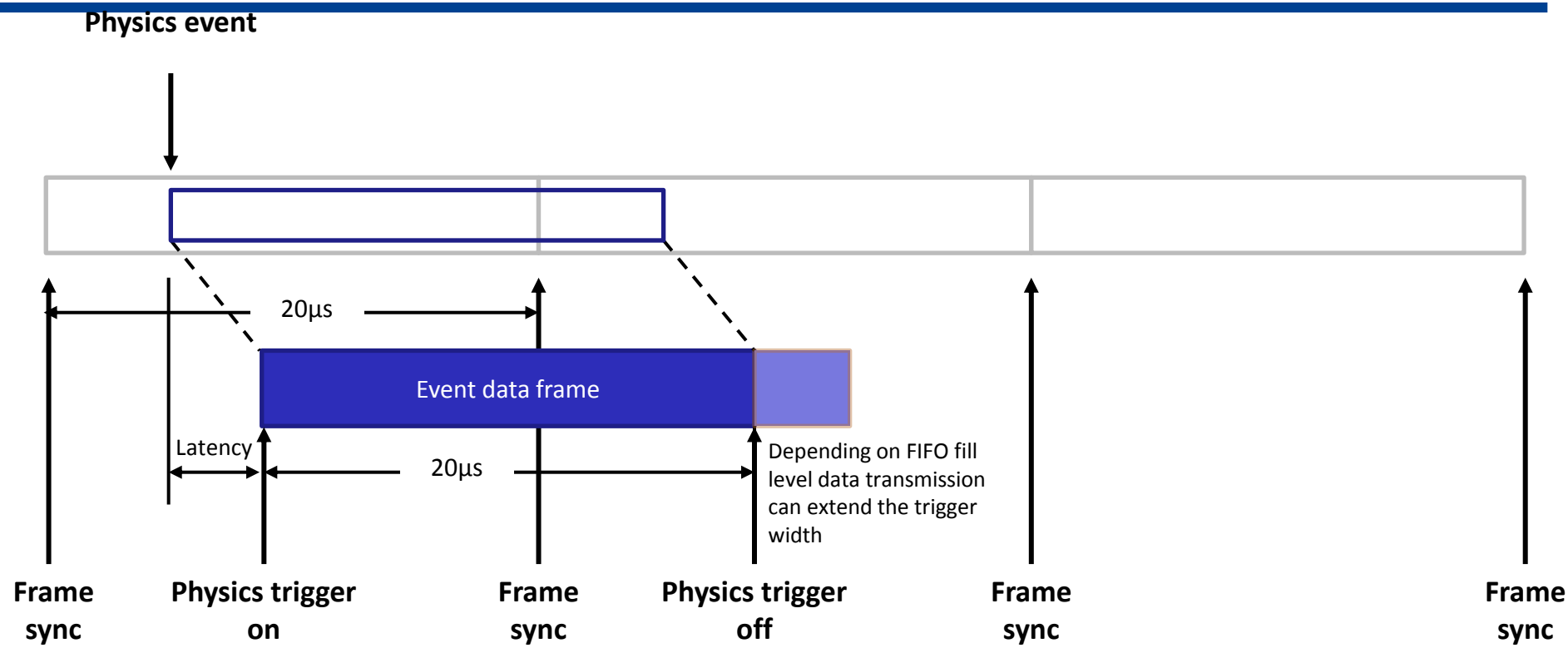
- **One control word per row period** is send synchronized to the DHP clock GCK (76.35 MHz)
- The control word (8 bits) transmits **four independent commands**: <RST|TRG|VTO|FSYNC>
  - RST: Reset, level sensitive, pulse width selects different reset modes
  - TRG: Physics trigger, level sensitive, pulse width selects raw data frame size
  - VTO: Veto (gated mode), level sensitive, selects veto sequence while on
  - FSYNC: Frame sync, edge sensitive
- The state of every command is encoded in two bits (Manchester code)
  - <10> = on
  - <01> = off
- Two additional control words are accepted (broken Manchester code)
  - <00 01 11 01> synchronization sequence, **should be used as IDLE**
  - <11 10 00 FSYNC> CALTRG (mem_dump): calibration data trigger, edge sensitive, allows simultaneous FSYNC command transmission
- The command latency in the DHP core is in the order of a few GCK cycles

Explanation of the Timing Diagrams

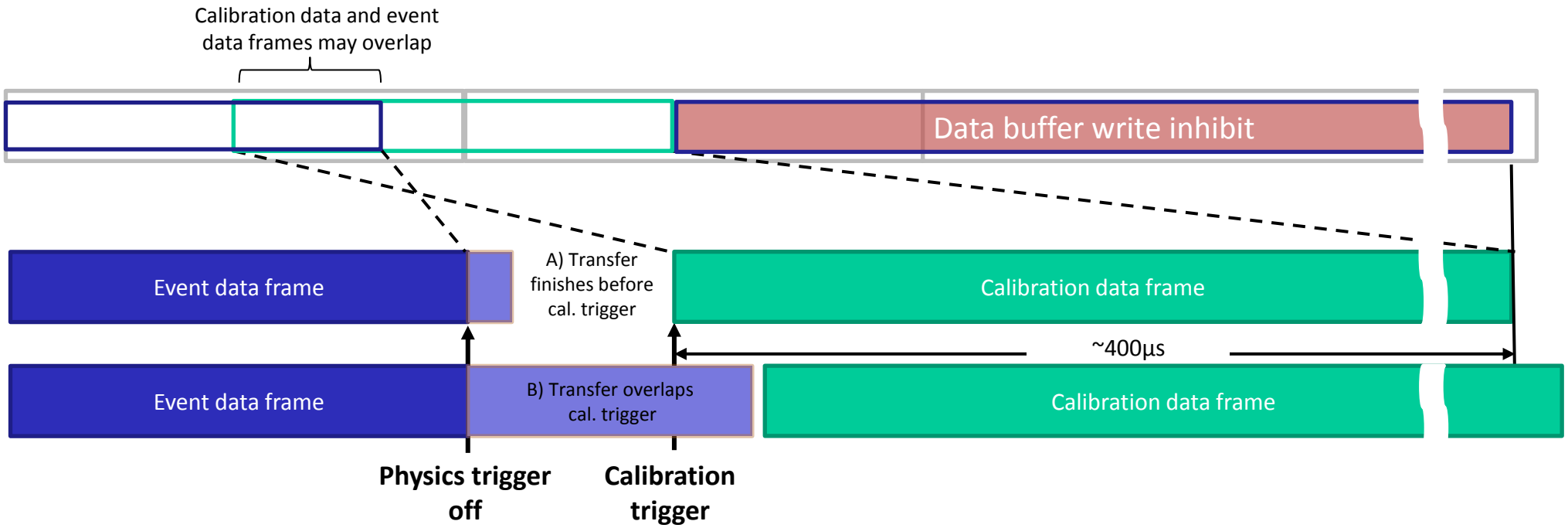


DHP timing for triggered data taking



- The transmitted *Event data frame* starts with hits from [row_m, raw data $frame_n$] and ends with [row_{m-1}, raw data $frame_{n+1}$]
- The row index m is a function of the phase between *trigger* and *frame sync*
- The trigger command is level sensitive and its width selects the size of the raw data frame to be processed
- The default width is 1536 GCK cycles (8 GCK cycles/row · 192 rows/frame)

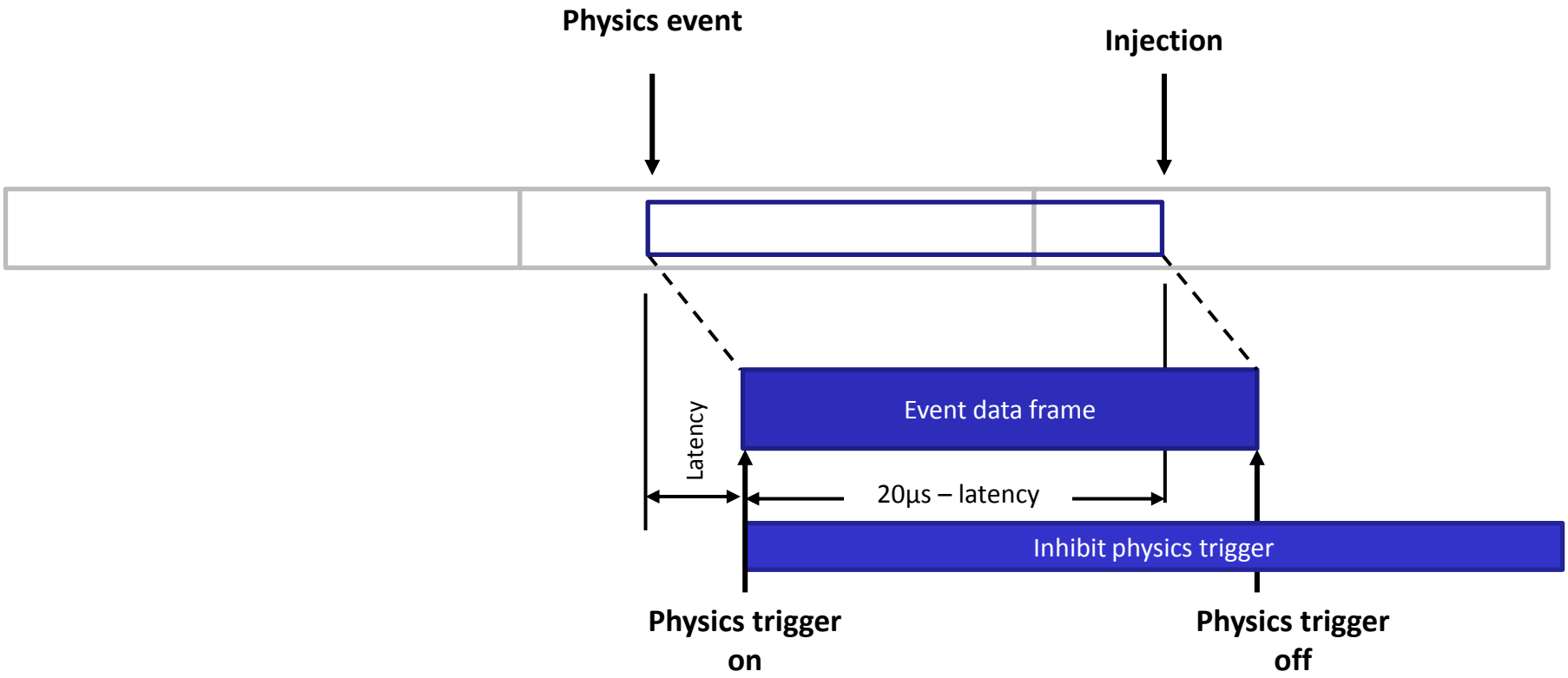
DHP timing for calibration data taking



- The calibration trigger can be send any time within a frame period
- If the previous event data transmission is not yet finished (case B), the calibration data transmission will be put on hold until the FIFOs are flushed. In some cases remaining event data still might be send after the calibration data frame (**not recommended**).
- The transmitted *Calibration Data Frame* is re-sorted and always starts with [row_0, raw data $frame_{n+1}$] and ends with [row_{max}, raw data $frame_n$]
- Programmable row_{max} and defines the raw data buffer size to transmit (default m= 191)

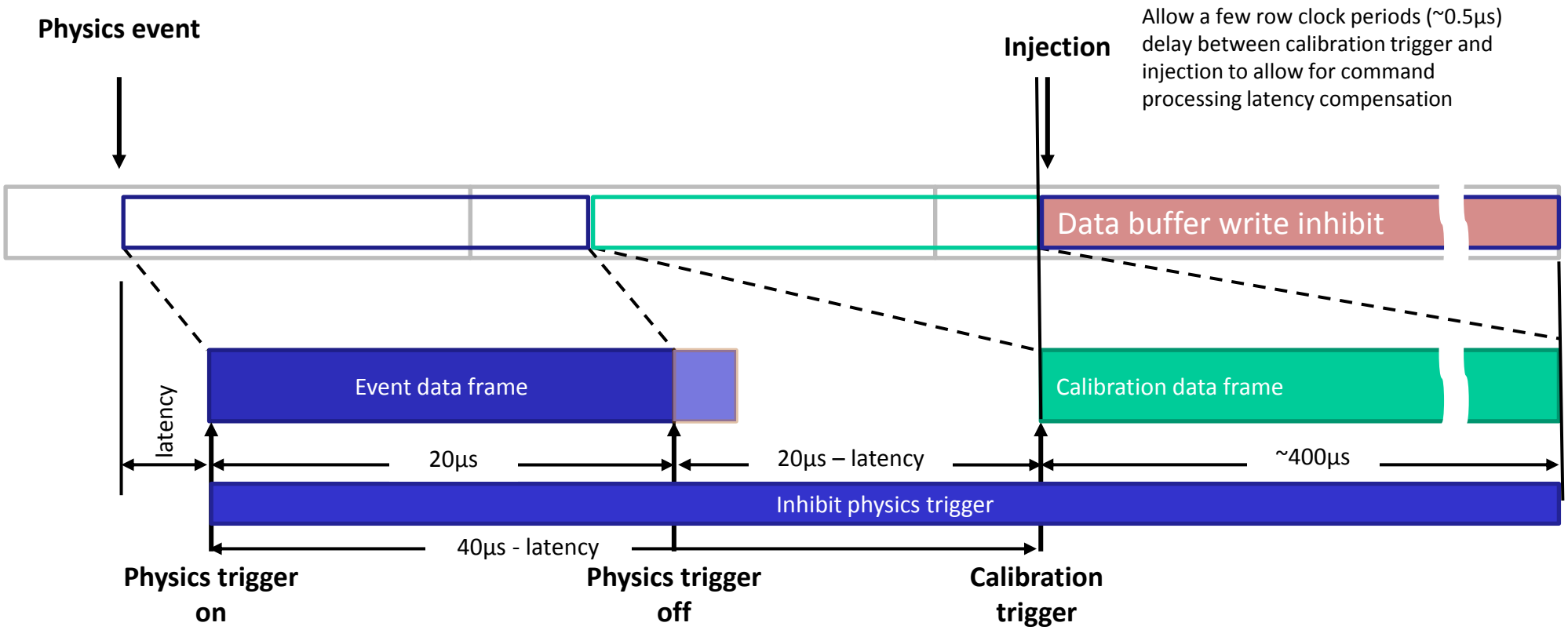
For better readability periodic *frame sync* commands are omitted in this and the following drawing s

DHP timing for injection sequence w/o calibration data taking



The suppression of physics triggers should start **20µs – latency** before the injection starts.

DHP timing for injection sequence with calibration data taking



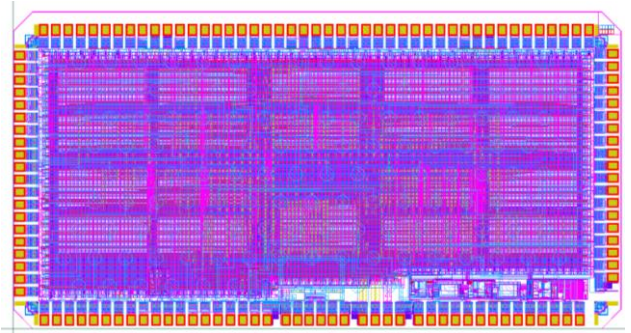
- The suppression of physics triggers should start **40µs – latency** before the injection starts.
- Calibration trigger should only be send if the previous event data transmission has finished

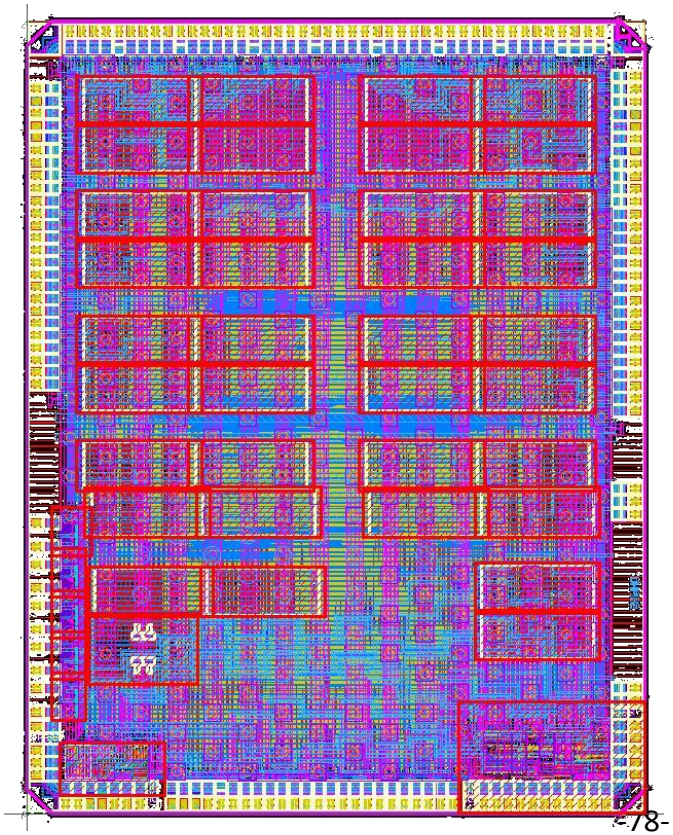
Data Handling Processor – Design History

Started with **IBM 90nm technology** in 2010

- DHP 0.1
  - Half size prototype, 2 x 4 mm^2, C4 bumps
  - Basic digital data processing
  - PLL (1.6 GHz) + High speed serial link
  - ➔ Successful verification

- DHP 0.2 (sub. mid of 2011)
  - Full size chip, 3.2 x 4.3 mm^2
  - Full data processing, added switcher sequencer and bias generators
  - Improvements in link performance (pre-emphasis), buffer size, and data format
  - ➔ Successful tests & system operation (some issues with max. speed of CMOS clock output)

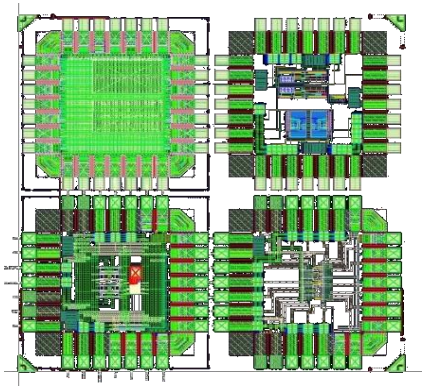




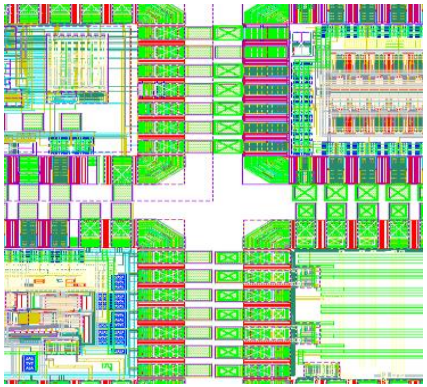
Data Handling Processor – Design History

Forced to abandon 90nm IBM process ➔ chosen **65nm TSMC**, started with small **prototype chips to verify full custom blocks** and rad. hardness performance

- DHPT 0.1 (Oct. 2011)
  - PLL (1.6 GHz)
  - High speed TX (CML driver)
  - Bias generators (U Barcelona)
  - Memory SEU test structures



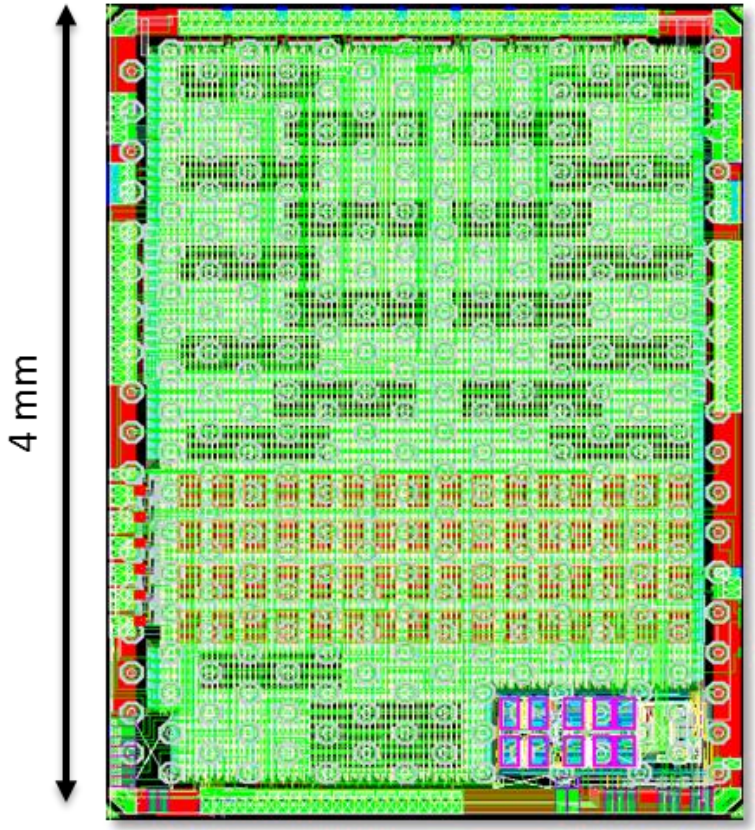
- DHPT 0.2 (June 2012)
  - LVDS RX & TX
  - Temperature sensor (U Barcelona)



Data Handling Processor – Design History

First **full size 65nm chip** submission (DHPT 1.0) after internal design review

- DHPT 1.0 (Aug. 2013)
  - Full size chip
  - Includes all pre-verified full custom blocks
  - Footprint & electrical compatible to DHP 0.2
  - Improved memory & processing resources wrt. DHP 0.2



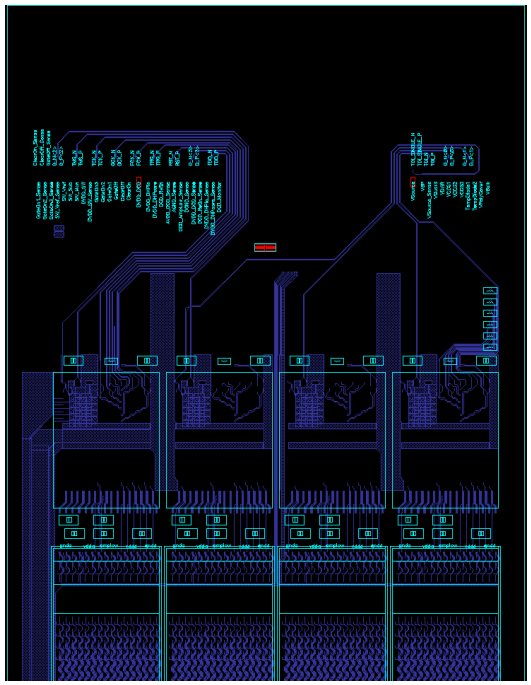
Data handling processor DHPT 1.0

DHPT 1.0 – PXD 9 Module

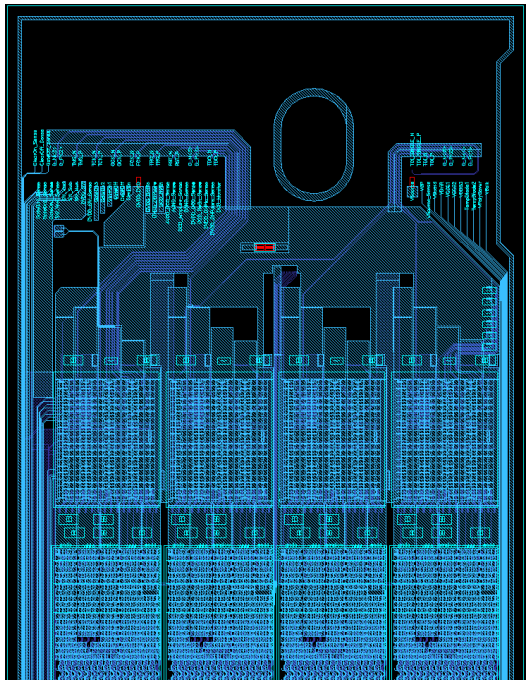
HIGH SPEED DATA LINE ROUTING

End of Stave Layout (EMCM & PXD9)

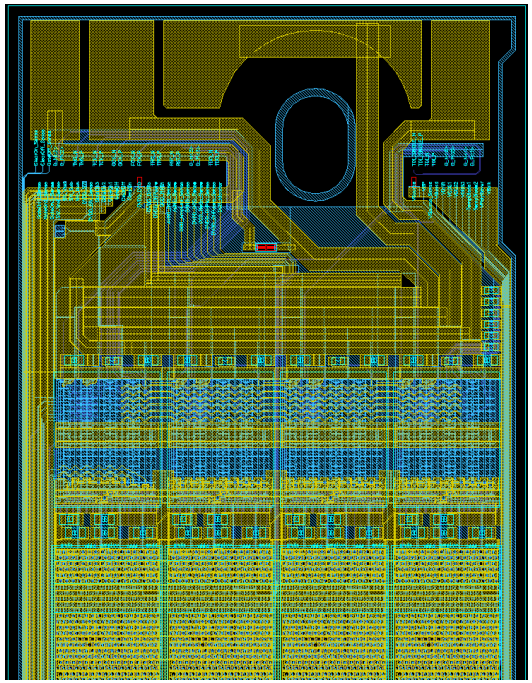
- Routing layers
  - Al1 (aluminum) → Signal routing
  - AL2 (aluminum) → Power supply distribution, wire bond pads, reference plane for high speed links
  - Cu (copper) → Power supply distribution & under bump metallization
- EMCM Layout:



AL1



AL1 + AL2



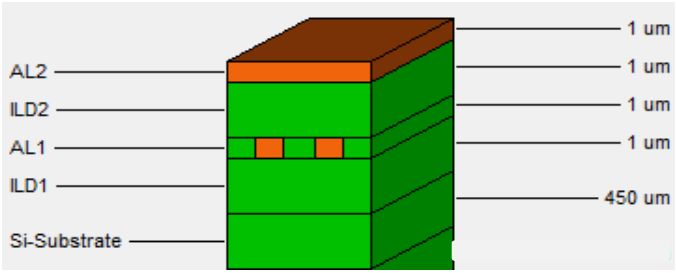
AL1 + AL2 + Cu

End of Stave Layout Details

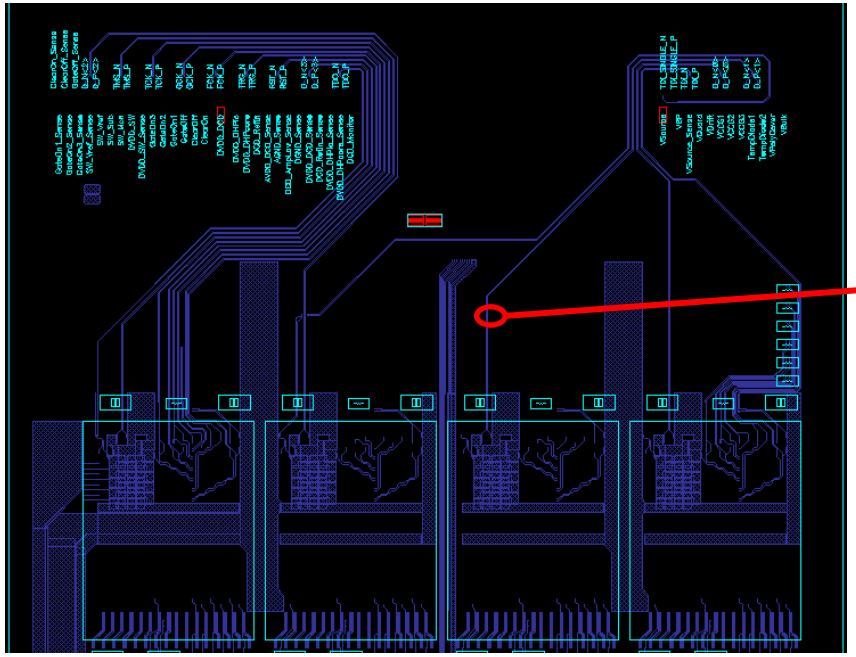
- Layer stackup (up to Al2)

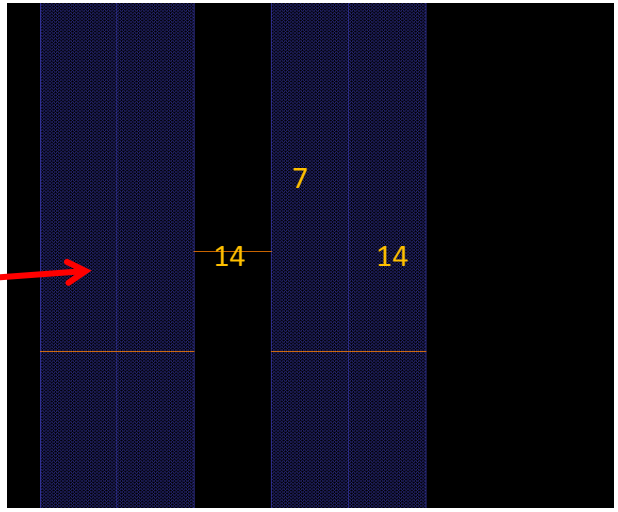
Layer Name	Type	Usage	Thickness um	Er
AL2	Metal	Plane	1	<Auto>
ILD2	Dielectric	Substrate	1	3.9
AL1	Metal	Signal	1	<Auto>
ILD1	Dielectric	Substrate	1*	3.9
Si-Substrate	Dielectric	Substrate	450	11

* minimum dimension HyperLynx can handle is 1µm



- Routing Details (Al1)

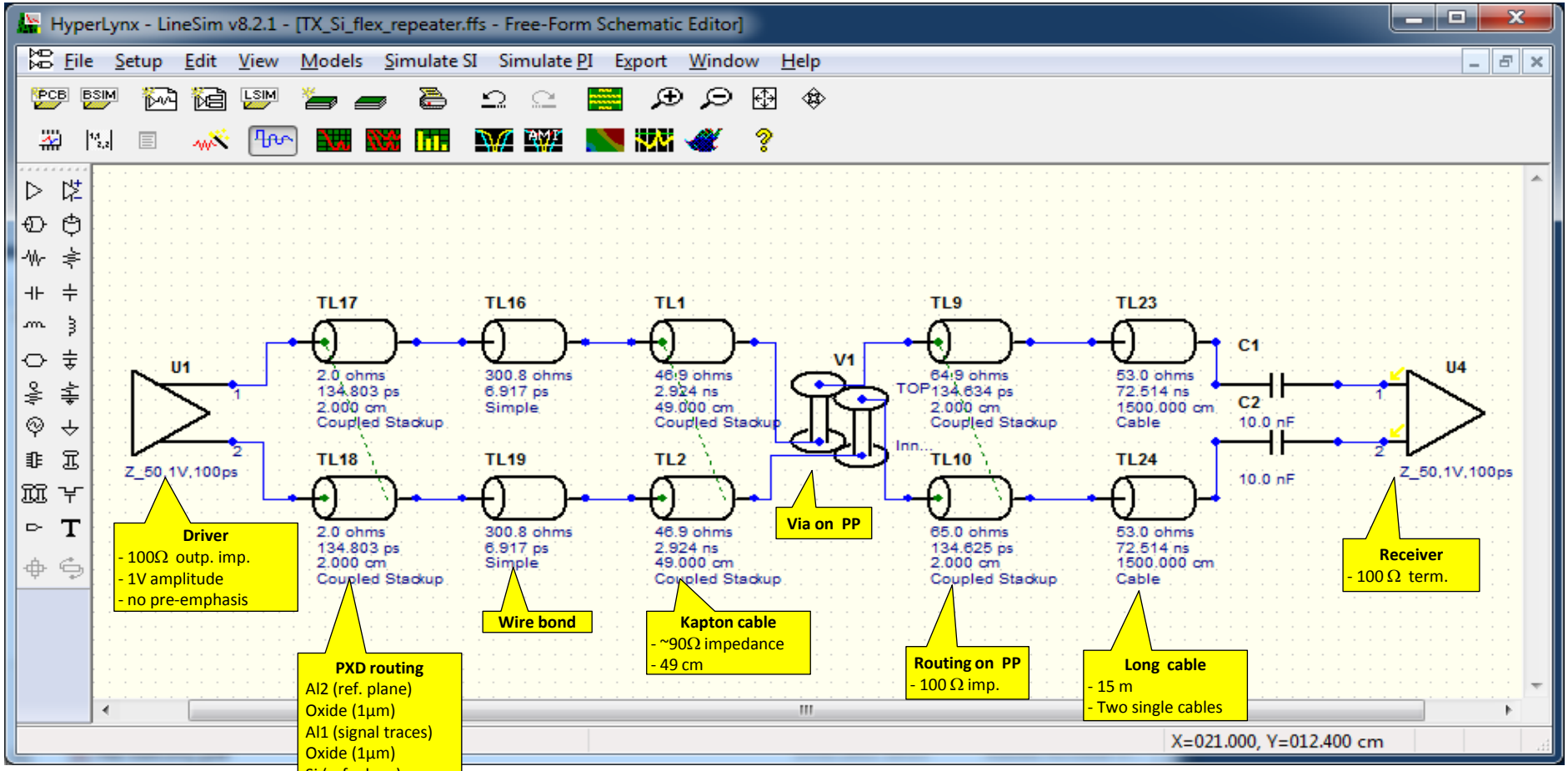




Diff. lines design values:
Width = 14µm (over etching → 12µm)
Spacing = 7µm (over etching → 9µm)

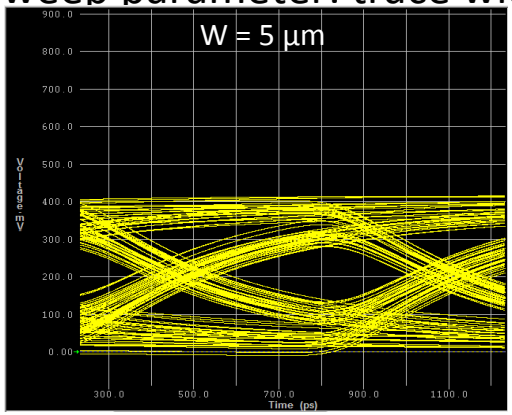
Simulation Environment

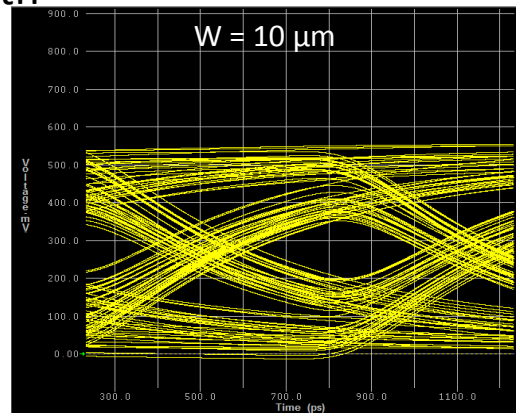
- Simulation tool: HyperLynx (➔ PCB signal integrity, not optimized for VLSI routing…)
- Model: Coupled lines on individual layer stacks for PXD and Kapton-cable, simple cable model for Infiniband cable (not TWP but two separate 50 Ohm cables)

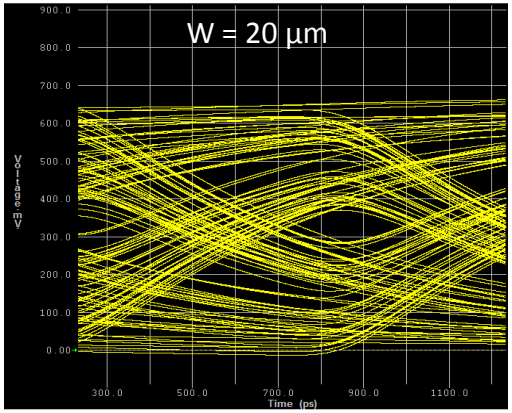


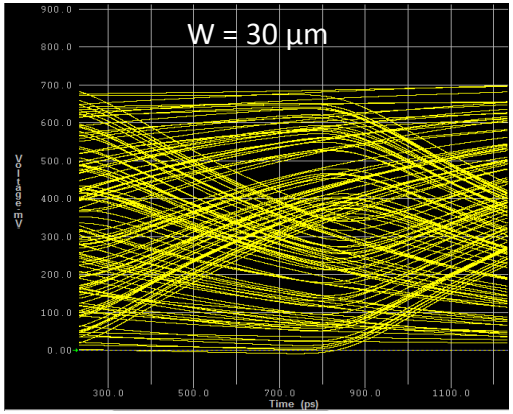
Simulation Results – Current Layout

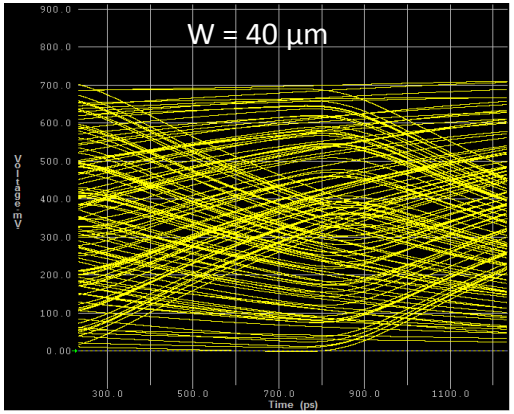
- Signal: 1.6 Gbps PRBS-7, no pre-emphasis
- Stackup: 1µm SiO_2 separation between signal and reference plane
- Sweep parameter: trace width

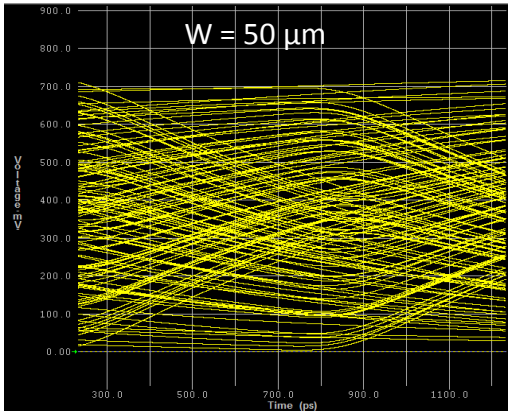






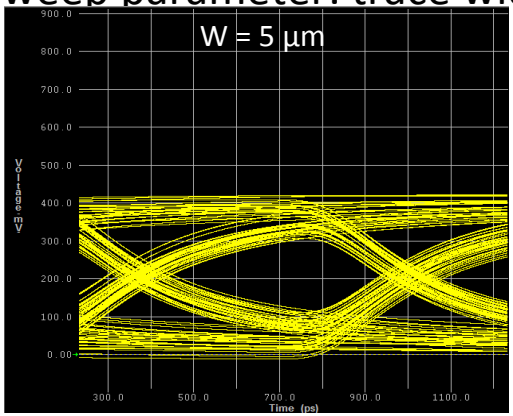


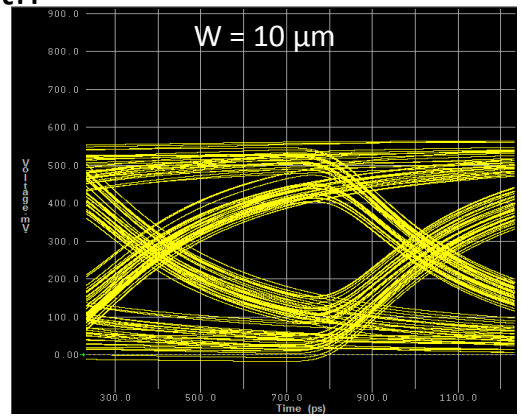


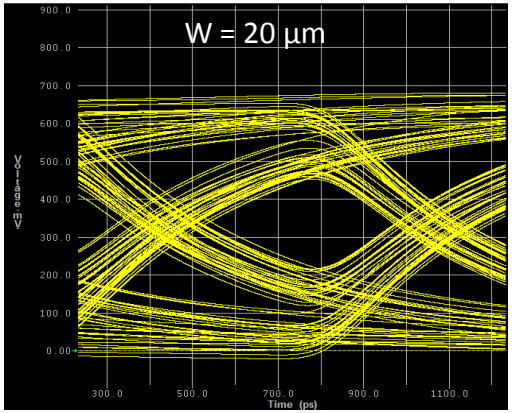


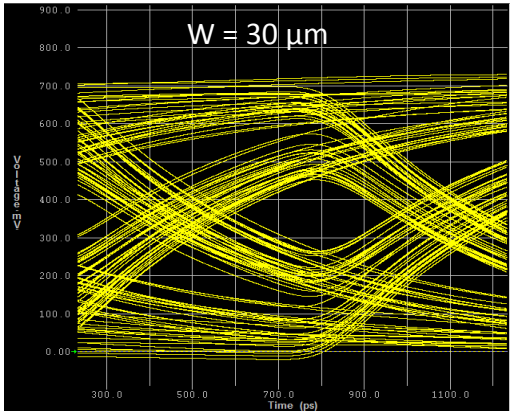
Simulation Results – Modified Layout

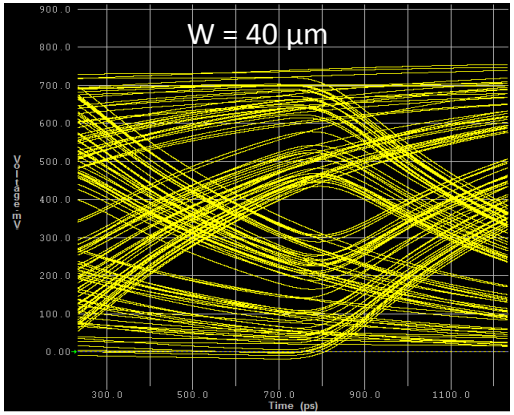
- Signal: 1.6 Gbps PRBS-7, no pre-emphasis
- Stackup: **2µm SiO_2** separation between signal and reference plane
- Sweep parameter: trace width

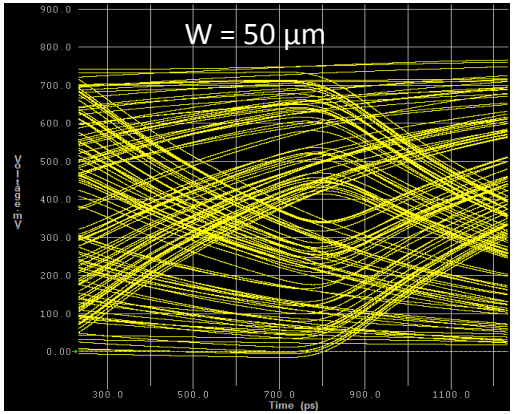












Simulation: EOS + Kapton Cable

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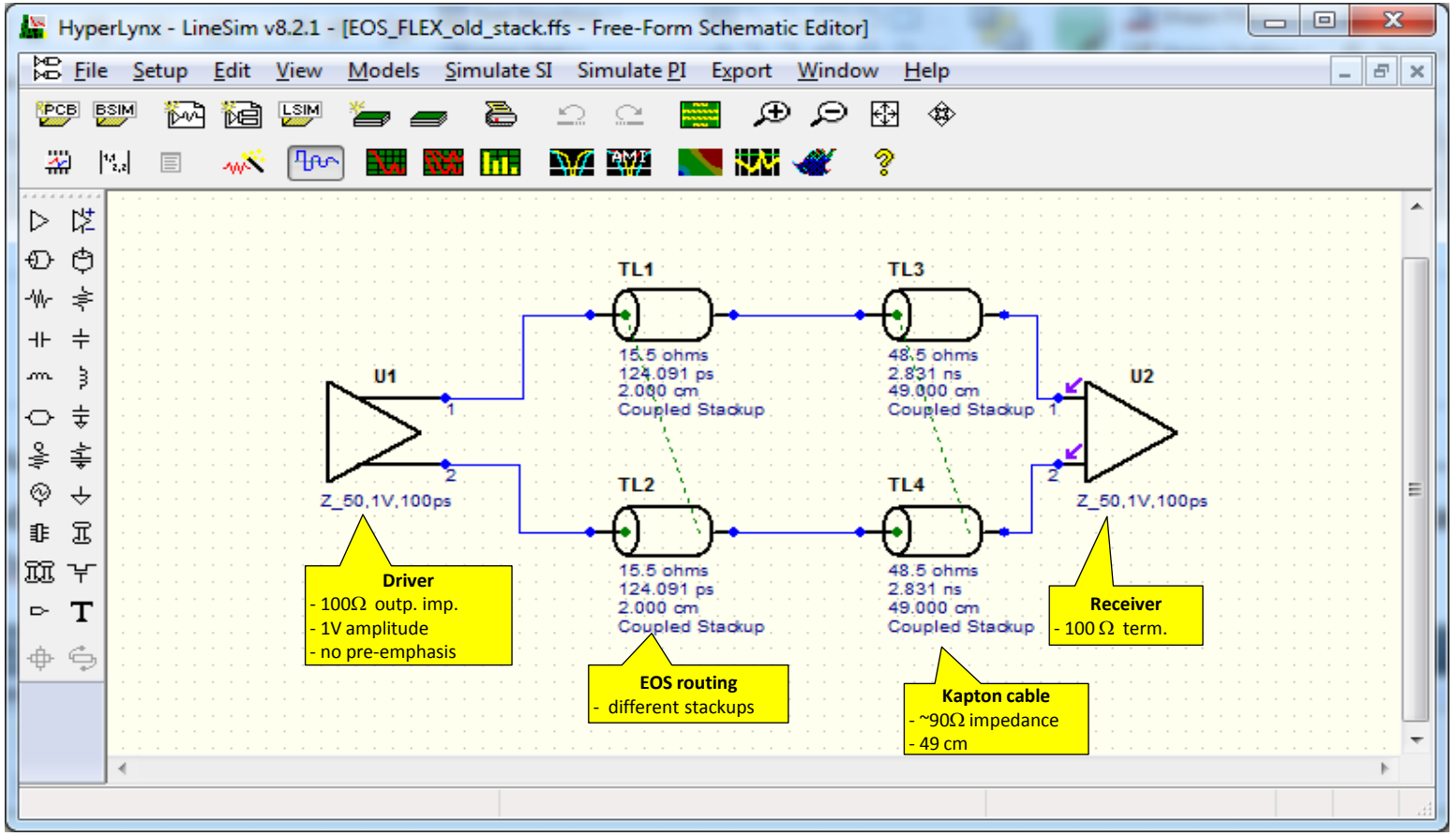
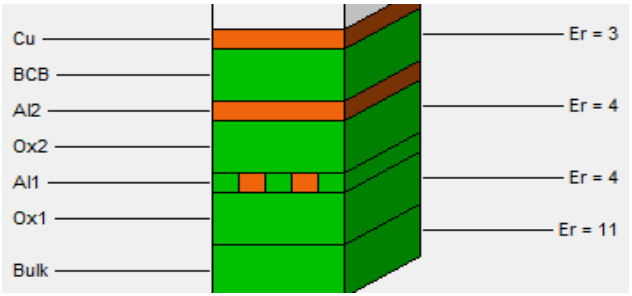
Simplified test-bench

- No long TWP cable, no wire bonds, vias, or connectors
- Ideal driver, 1.6Gbps PRBS-7, no pre-emphasis

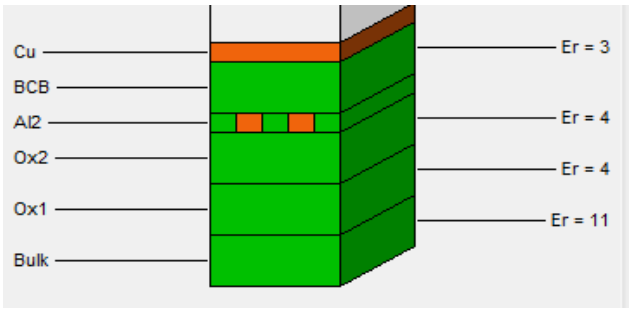


EOS Stackup Options

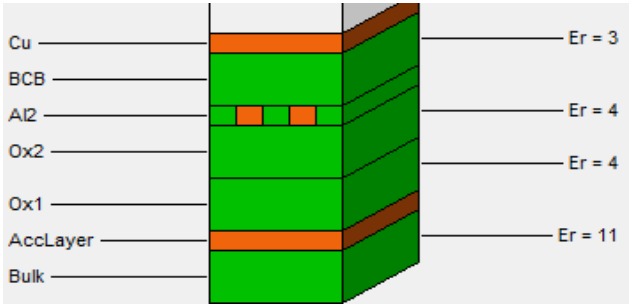
A. Original stackup
   - **Routing on Al1**
   - Top reference plane Al2
   - Bottom reference plane: Si bulk



B. Modified stackup
   - **Routing on Al2**
   - Top reference plane: Cu
   - Bottom reference plane: Si bulk



C. Modified stackup (worst case)
   - Routing on Al2
   - Top reference plane: Cu
   - Bottom reference plane: conduction layer between bulk on oxide (ideal acc. layer)



➔ Simulation tool cannot handle **resistive layers** for reference planes (**real accumulation** layer between Si bulk and oxide)

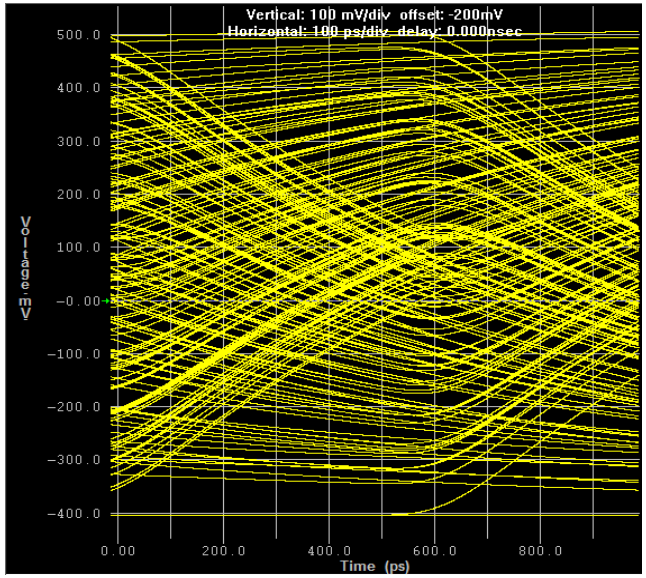
Simulation Results

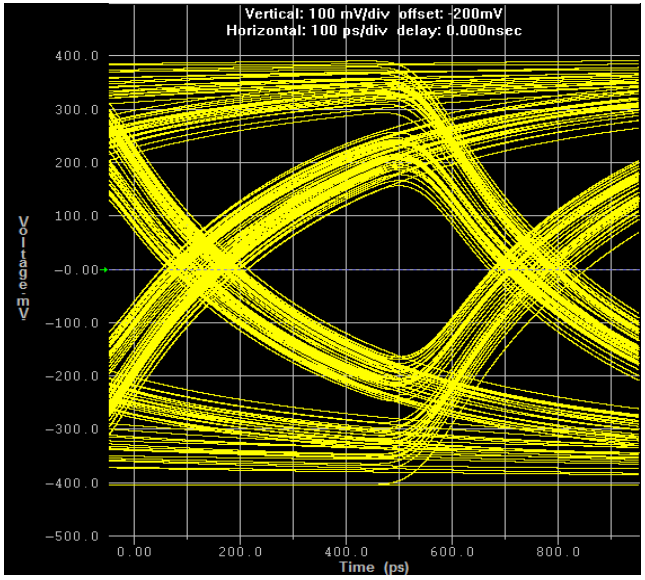
- EOS and kapton cable only (no long TWP)
- no pre-emphasis
- trace width: 30µm

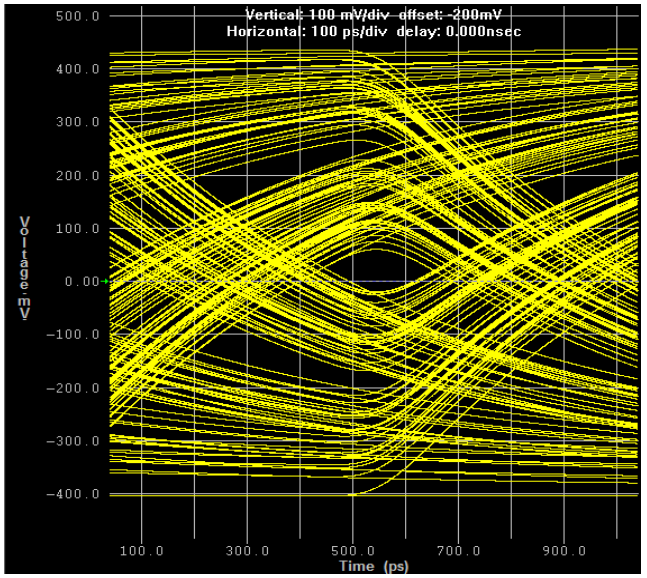
A. Original stackup
- Routing on Al1
- Top ref. plane: Al2
- Bottom ref. plane: Si bulk

B. Modified stackup
- Routing on Al2
- Top ref. plane: Cu
- Bottom ref. plane: Si bulk

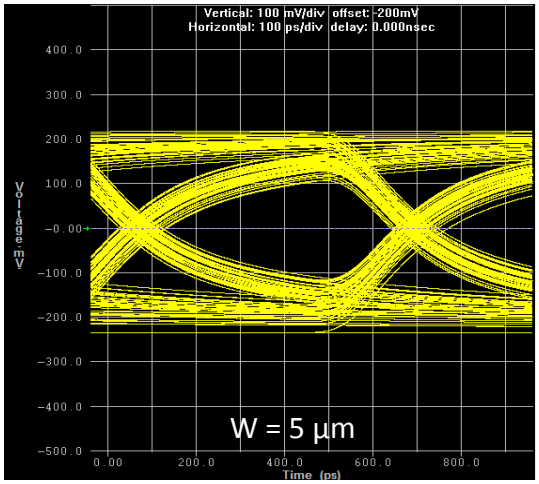
C. Modified stackup (worst case)
- Routing on Al2
- Top reference plane: Cu
- Bottom ref. plane: conductive layer between Si bulk and oxide

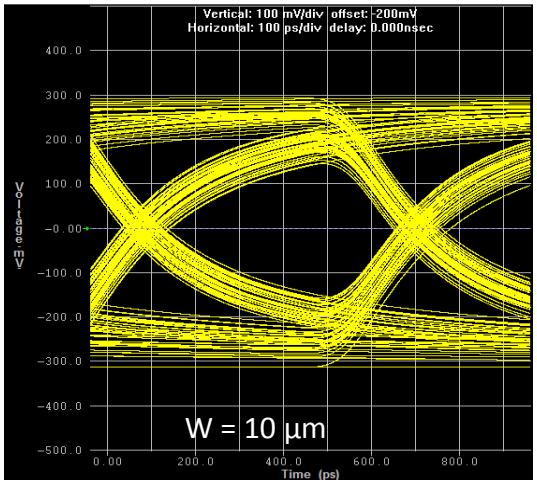


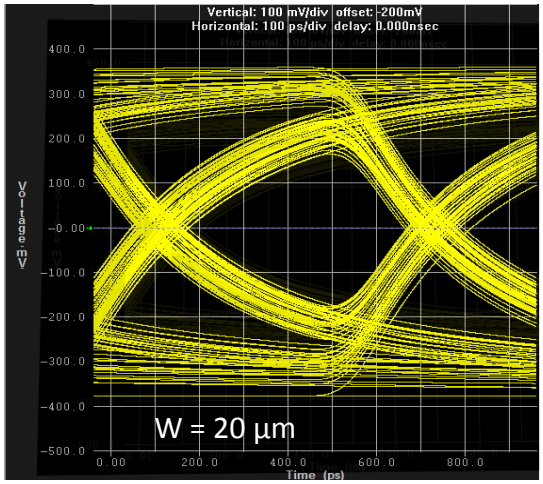


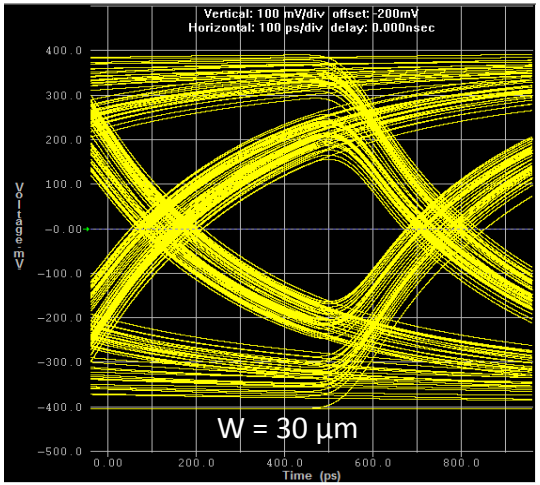


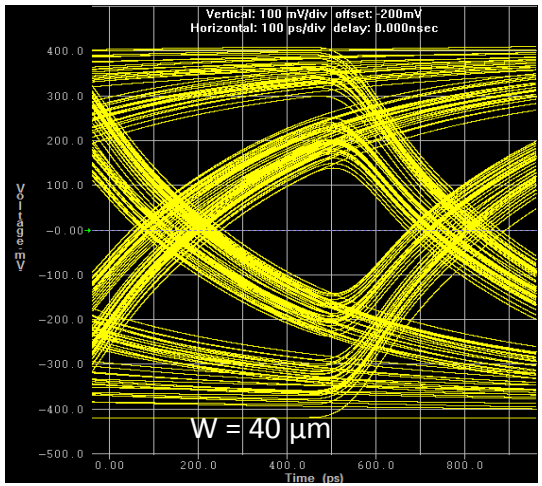
Modified Stackup B)

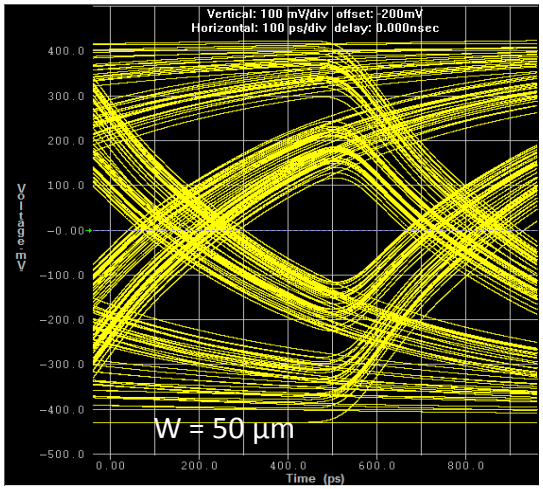












TML Parameters

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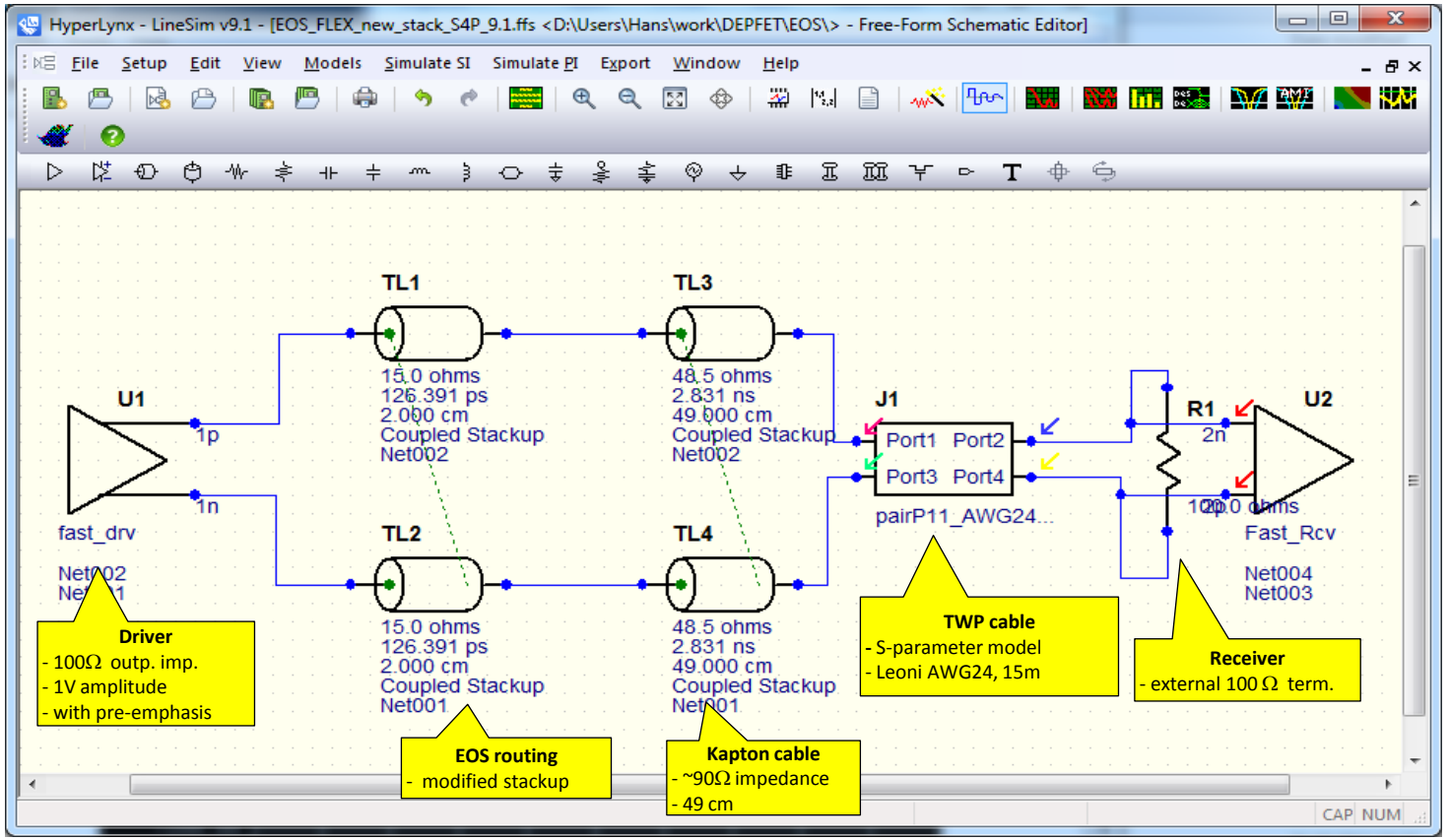
Width [µm]	Z_{DC} [Ω]	$Z_{0\ diff}$ [Ω] Al1 routing	$Z_{0\ diff}$ [Ω] Al2 routing
5µm	107	42	83
10µm	54	26	58
20µm	27	15	37
30µm	18	11	28
40µm	13	8.6	23
50µm	11	7.2	19

- (Reminder) ideal case: $Z_{DC} = 0\Omega$, $Z_{0\ diff} = 100\Omega$
- Signal traces on Al1 or Al2 layer: 1µm thick, 2 cm long, 10µm spacing

Simulation: EOS + Kapton Cable + TWP Cable

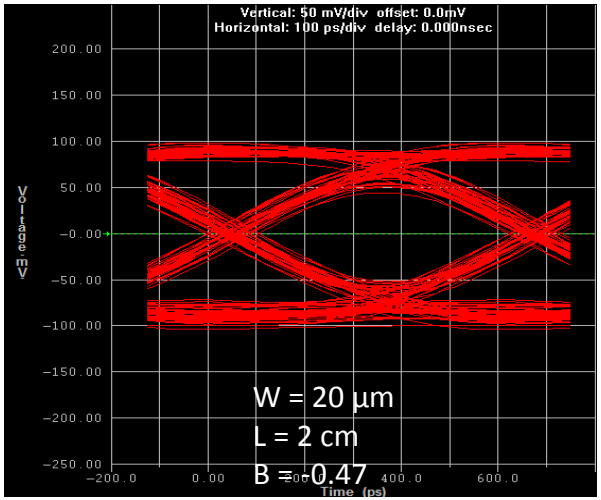
Simplified test-bench

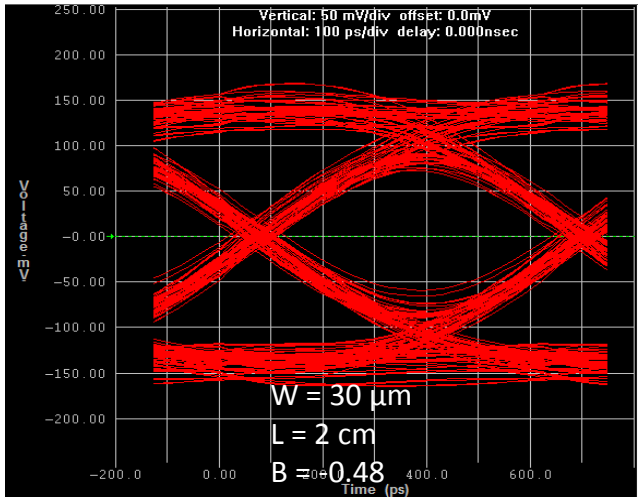
- no wire bonds, vias, or connectors
- TWP cable (15m): measured S-parameter form 24 AWG cable
- Ideal driver: 1.6Gbps, PRBS-7, **with** pre-emphasis: A = 1, B = […], dt = 625ps (fixed)

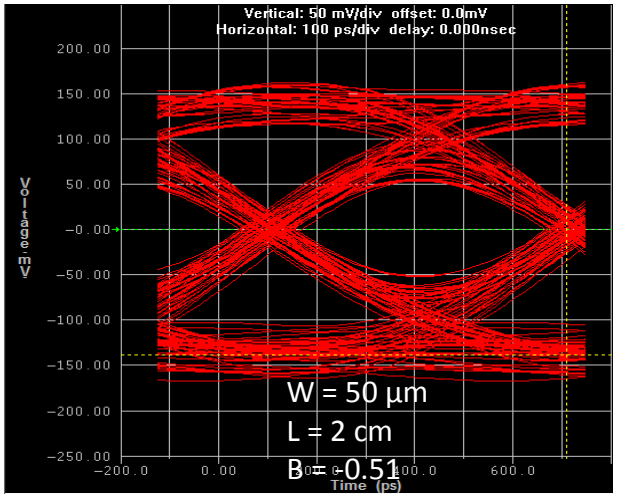


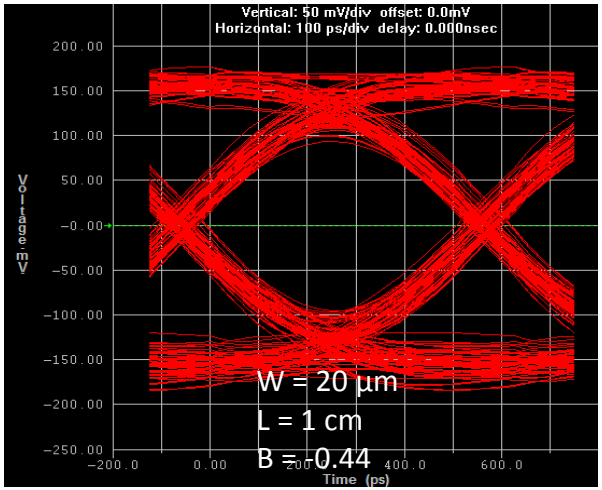
Simulation Results

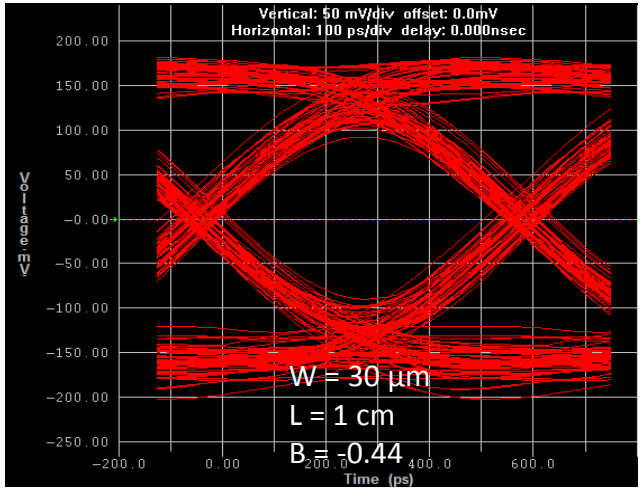
- EOS (modified stackup) + kapton cable + 15m TWP
- Ideal driver with pre-emphasis: A = 1, B = -[0.47…0.52], dt = 625ps (bit period)

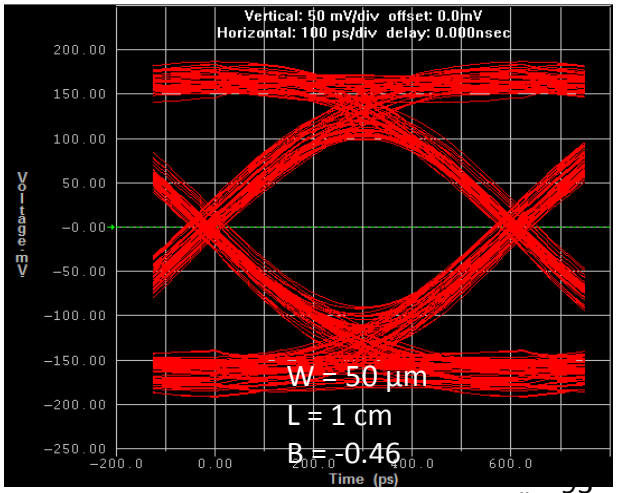






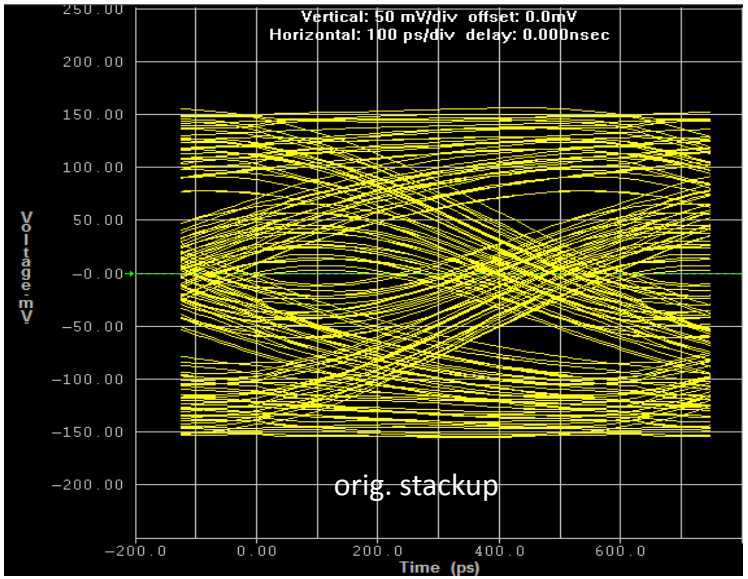


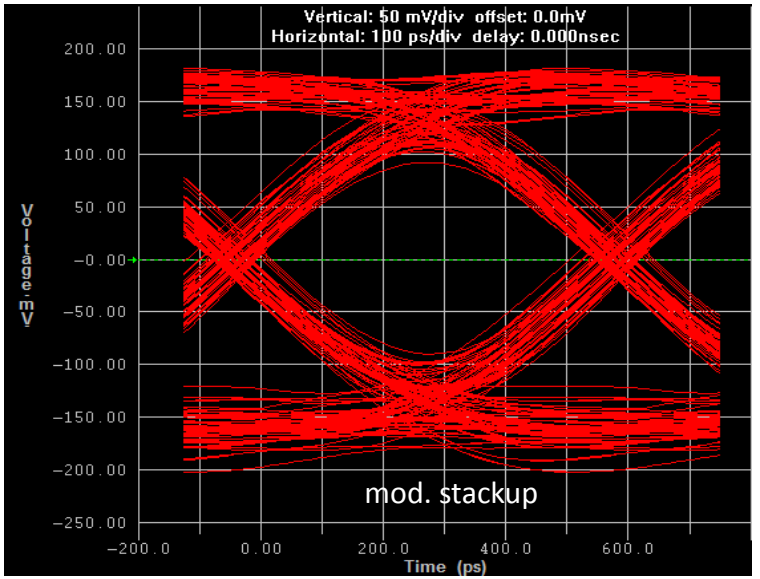




Original vs. modified EOS Stackup

- EOS + kapton cable + 15m TWP
- trace width: 30µm
- Ideal driver **with pre-emphasis**: A = 1, B = 0.48 , dt = 625ps (bit period)





Conclusion

- **Low TML impedance** (<< 100 Ω) on EOS due to strong capacitive coupling between metal layers
- The impedance mismatch is close to the driver and the **propagation delay** on the EOS (~150ps) is **in the order of the signal rise time**

➔ Increase of **signal dispersion** (i.e. additional high frequency attenuation due to **capacitive loading** of the driver)

Implemented design changes (EMCM → PXD9)

- **Move high speed link traces from AL1 to AL2 (less capacitance)**
- **Increase trace width from 14µm to 30µm (less DC resistance)**
- **Cu as reference plane**

TWP Cable Modeling

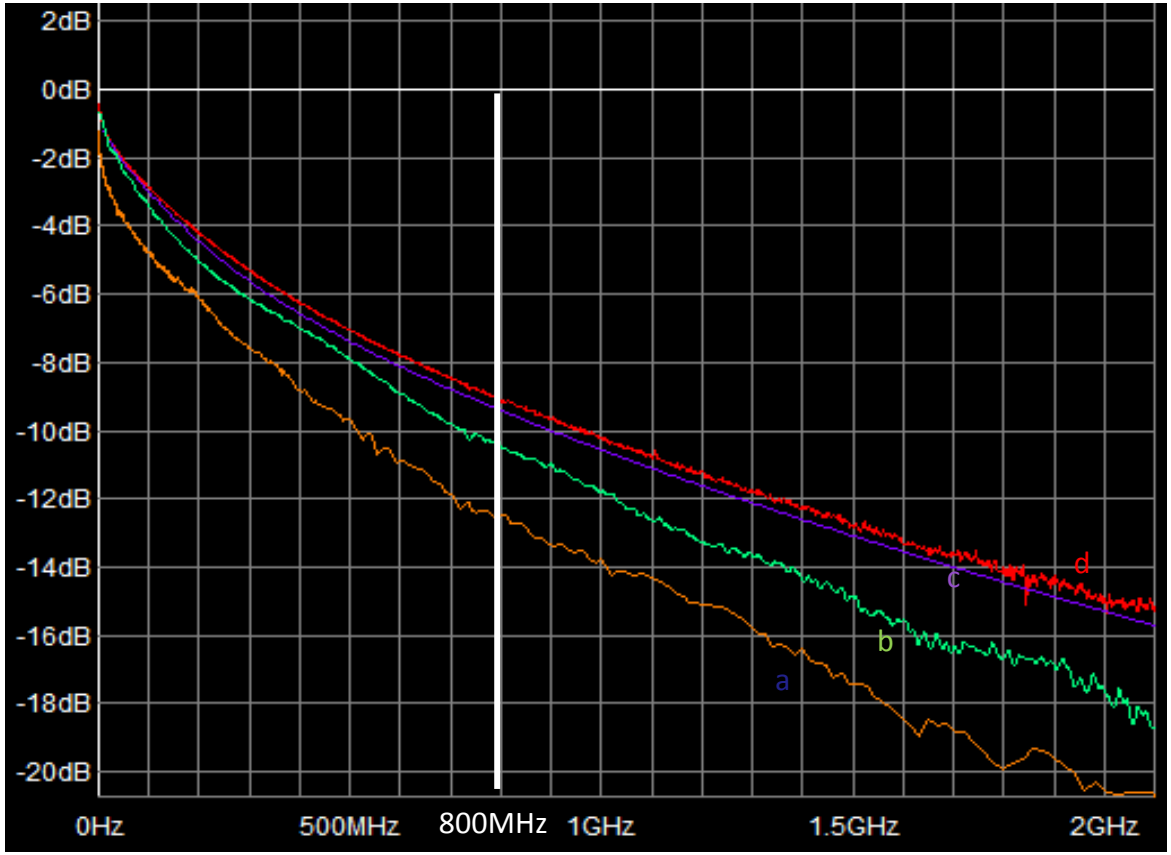
- Transfer curves extracted from **measured S-parameter** data
- 24AWG cables, different vendors, different measurements:

a) Meritec?, 12m, forced bends (S-parameter data from MPP)

b) Leoni, 15m (S-parameter data from **own measurement**)

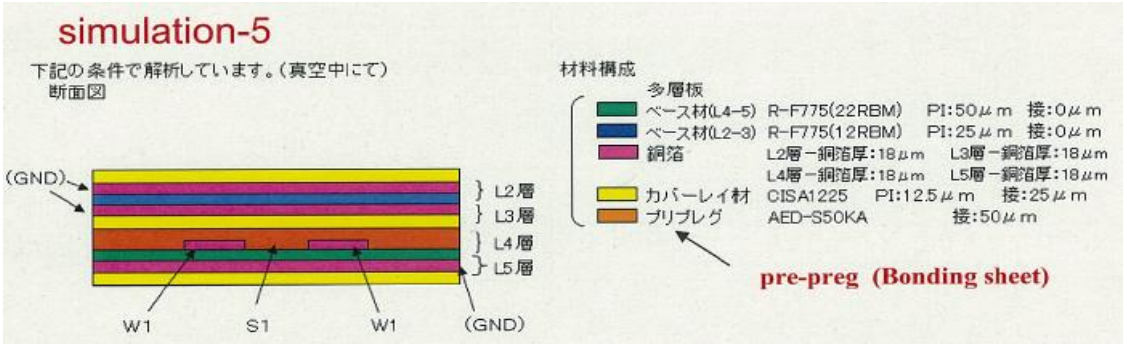
c) Leoni, 15m (S-parameter data from manufacturer)

d) Meritec, 15m (S-parameter data from manufacturer)



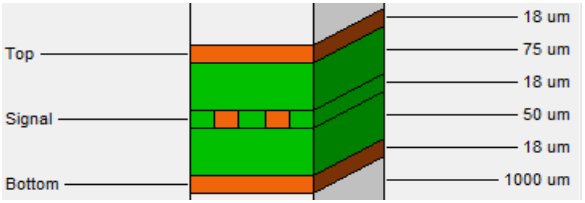
Flex Stackup (Tayio V2.1)

- Stackup data from Tayio
  - W = 75µm
  - S = 125µm



- Stackup used for simulation
  - W = 70µm
  - S = 130µm

  (assuming 2.5µm over etching)?

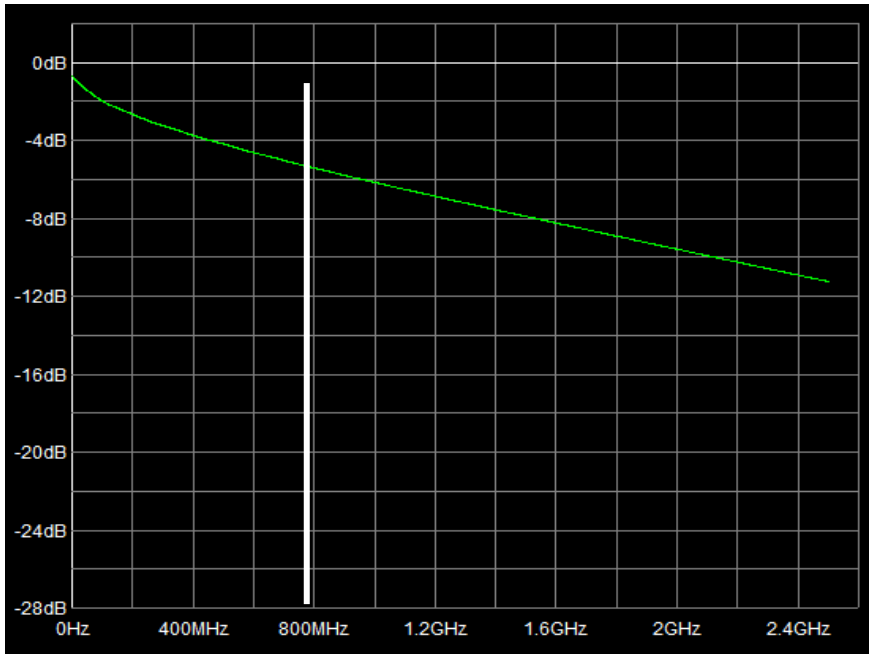


Top	Metal	Plane	18	<Auto>	Copper	<Auto>
	Dielectric	Substrate	75	3.2		0.02
Signal	Metal	Signal	18	<Auto>	Copper	<Auto>
	Dielectric	Substrate	50	3.2		0.02
Bottom	Metal	Plane	18	<Auto>	Copper	<Auto>

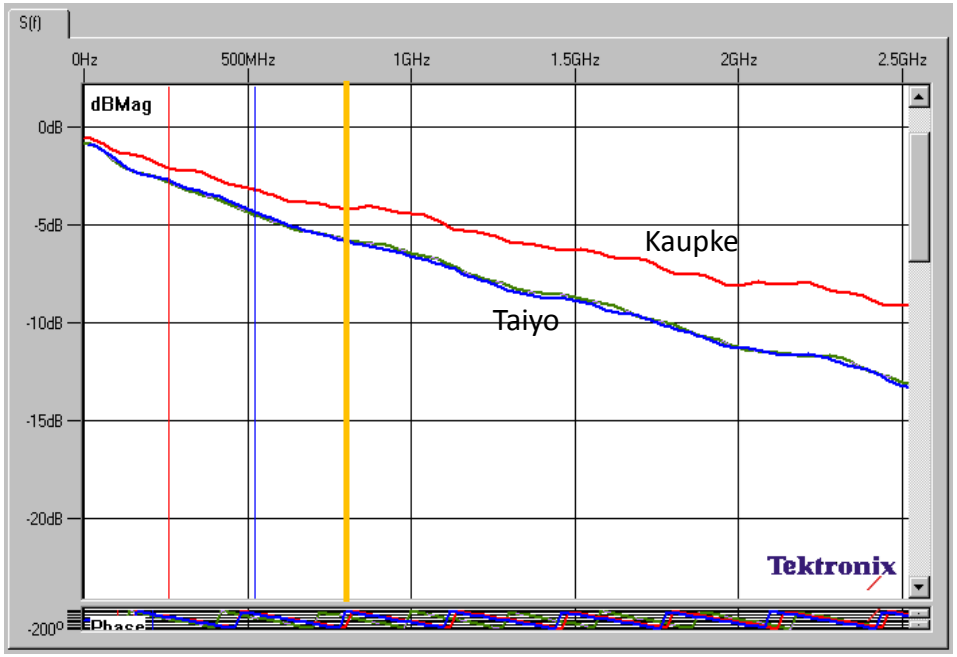
Flex Cable Modeling

- Transfer functions of the Tayio cable (V. 2.1, 49cm)

Simulated flex stackup



Measured TDT data



- Measurement and simulation in good agreement:

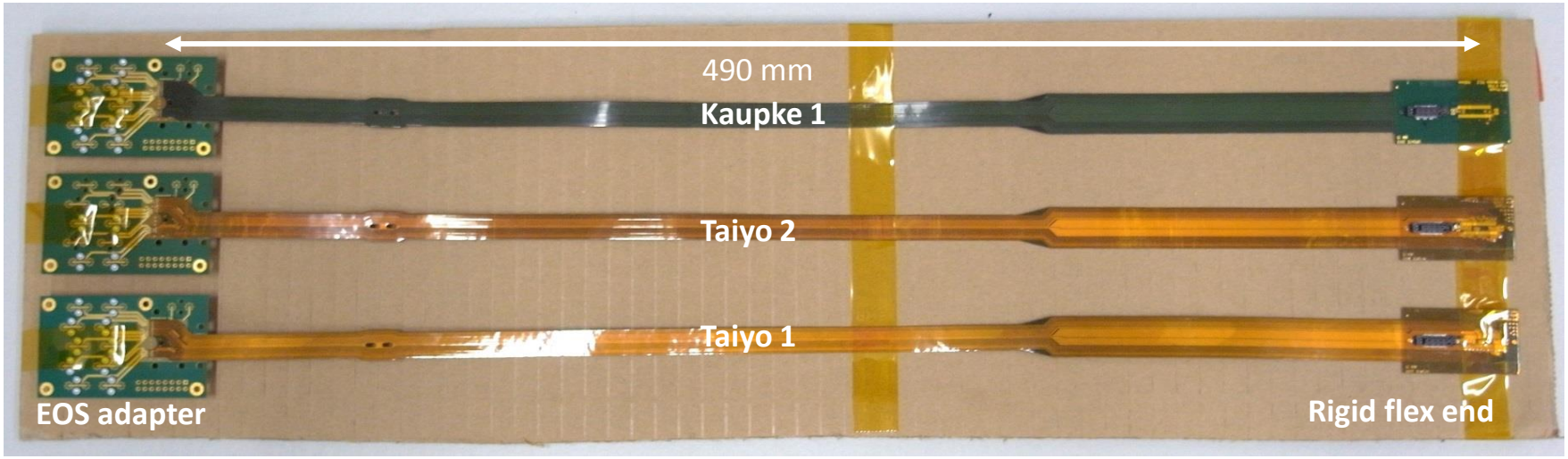
	Attenuation @ 800 MHz	R_{DC}	$Z0_{diff}$
Simulation	5.8dB	6.7Ω	86Ω
Measurement	5.4dB	7.6Ω	89Ω

PXD

FLEX CABLE CHARACTERIZATION

Flex Cable Prototypes

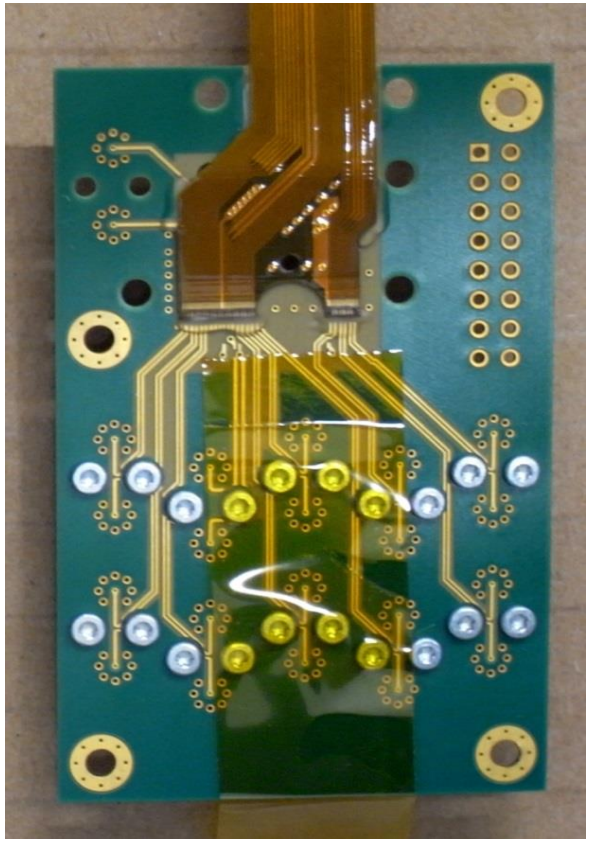
- Same design (MPI) produced by two different manufacturers (Taiyo, Kaupke)
  - length: 490mm
  - layers: 4
- Two productions by Taiyo (identical design data, V2.1)
- Kaupke design data with smaller via hole (0.2mm instead of 0.35mm, V2.2)
- Kaupke and Taiyo apparently use different layer stacks (see measurement data)



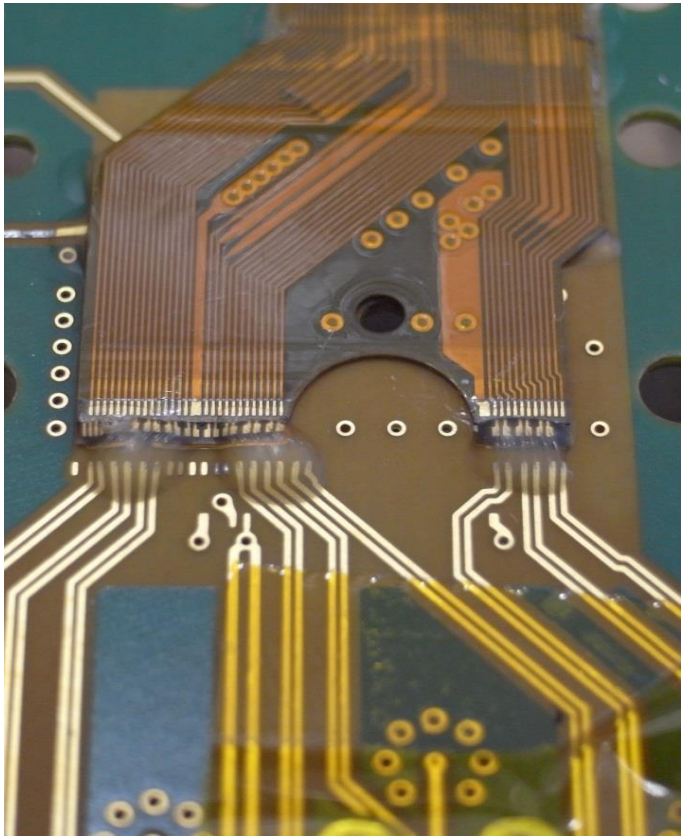
Flex cable prototypes with EOS adapter boards

Flex Cable – Module Side

- Adapter PCB to connect micro coax cables to the flex cable
- Two 25µm Al wire bonds per line, potted



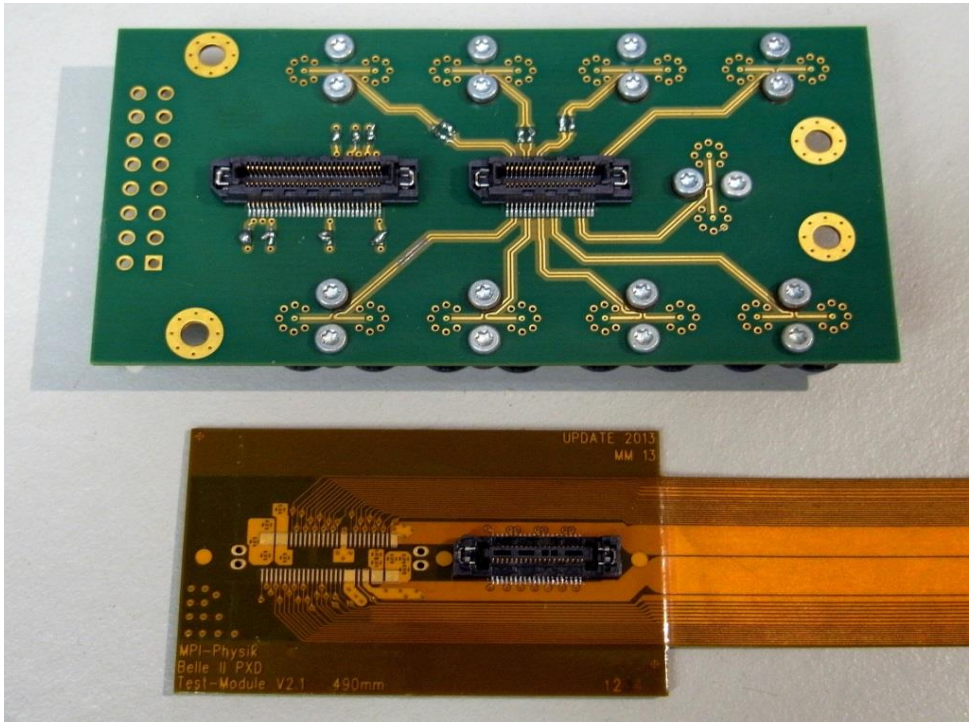
Flex adapter PCB, soldered and wire bonded to flex cable

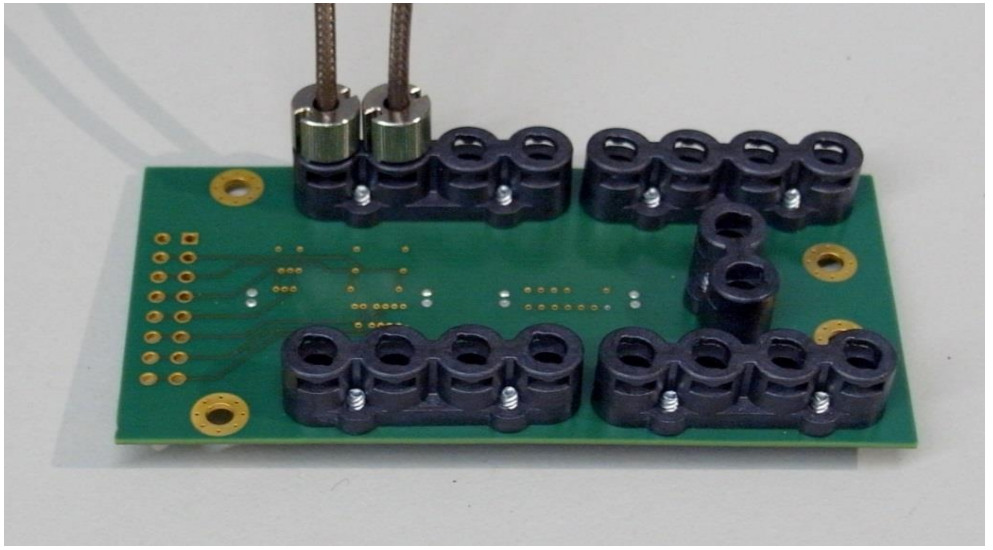


Wire bond detail

Flex Cable – Patch Panel Side

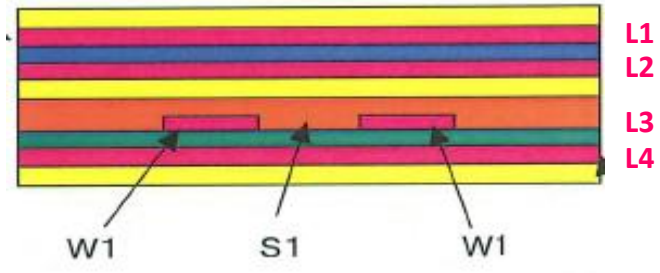
- Adapter PCB to connect micro coax cables to the rigid patch panel



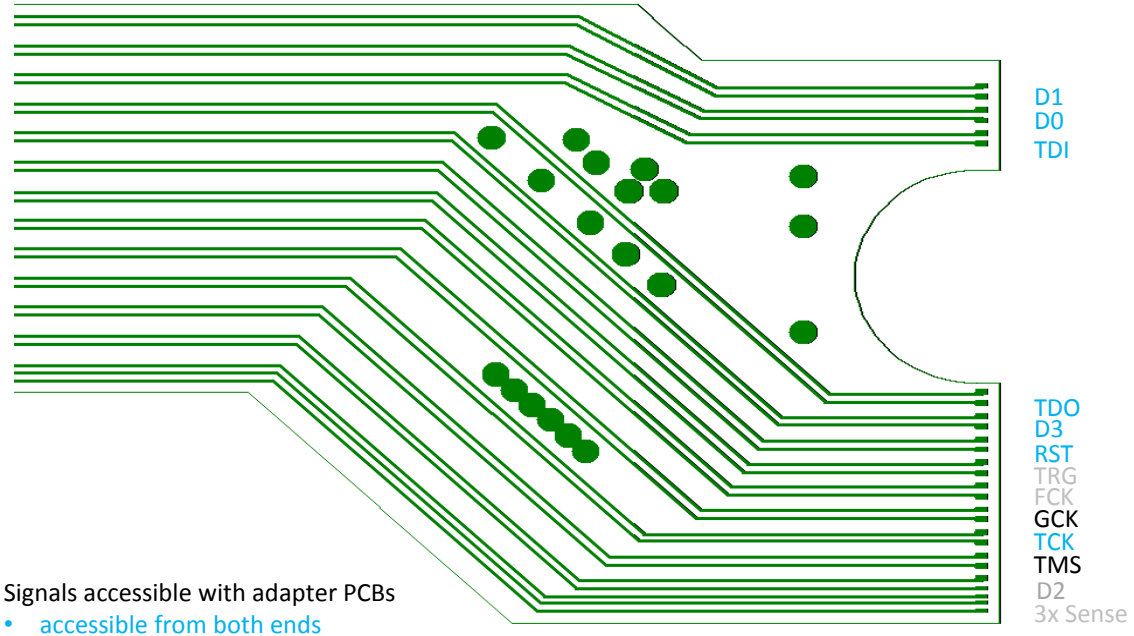


Design Details

- Impedance controlled differential pairs (most critical for Gbit link data lines D[3:0])
- Design goals
  - 100Ω diff. impedance (± 10Ω)
  - low DC resistance (< 8Ω)
  - good x-talk immunity



Layer stack (cross section), width (W) and spacing (S) of diff. lines on layer 3



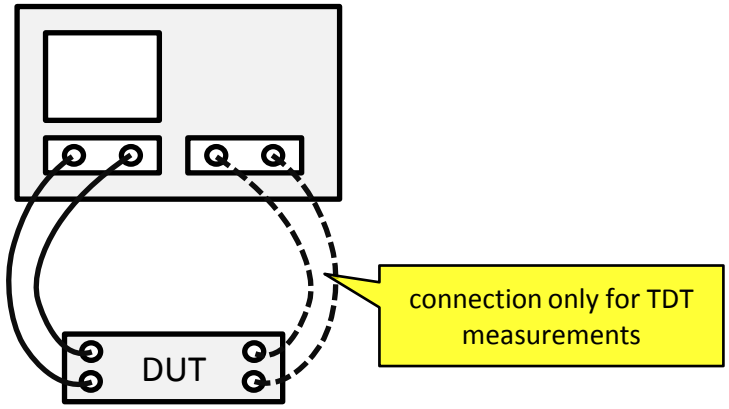
Signals accessible with adapter PCBs
- accessible from both ends
- accessible from module side only
- not accessible

Flex cable layout at module side, layer 3 shown only

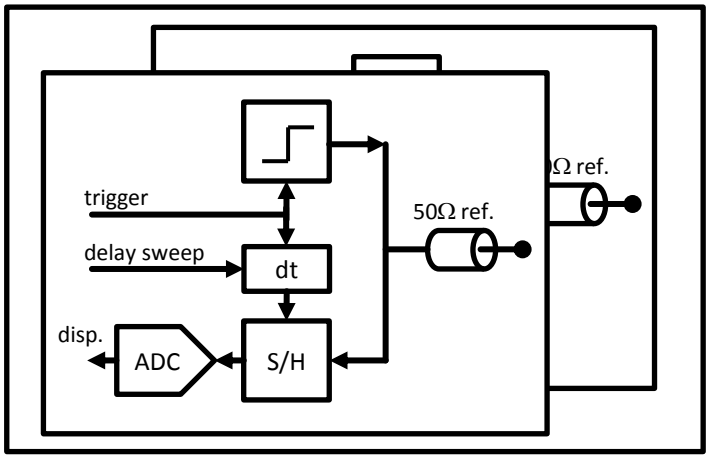
Measurement Methodology

- Digital Sampling Oscilloscope (DSA)
  - Very high input bandwidth (up to 30GHz)
  - Precision sample & hold at inputs
  - High resolution delay sweep of S&H trigger (sub ps)
  - Low speed, high resolution ADC (14 bit, 200ksps)

➔ Very accurate amplitude and timing resolution (works for periodic signals only)



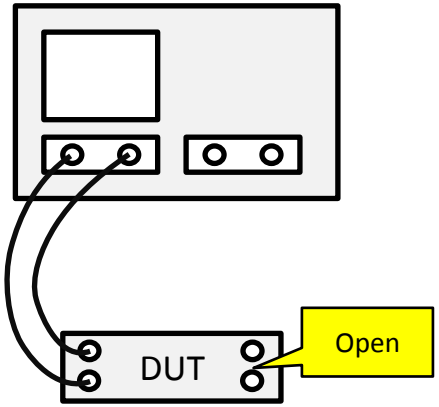
DSA with two dual channel TDR / Sampling modules connected to DUT with differential lines

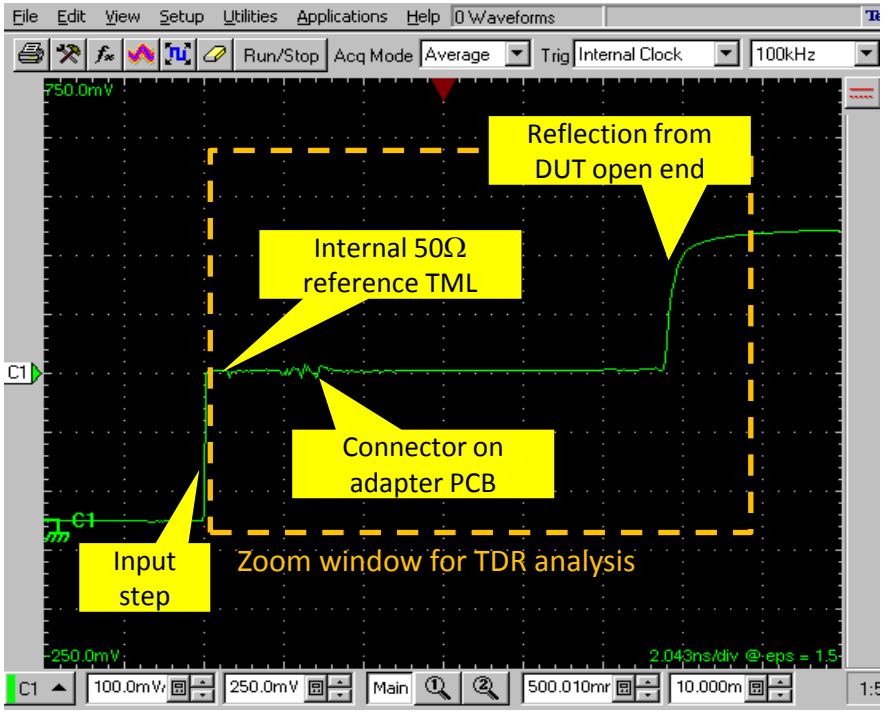


Dual channel TDR / Sampling module (step voltage generator and sampling stage can be activated independently)

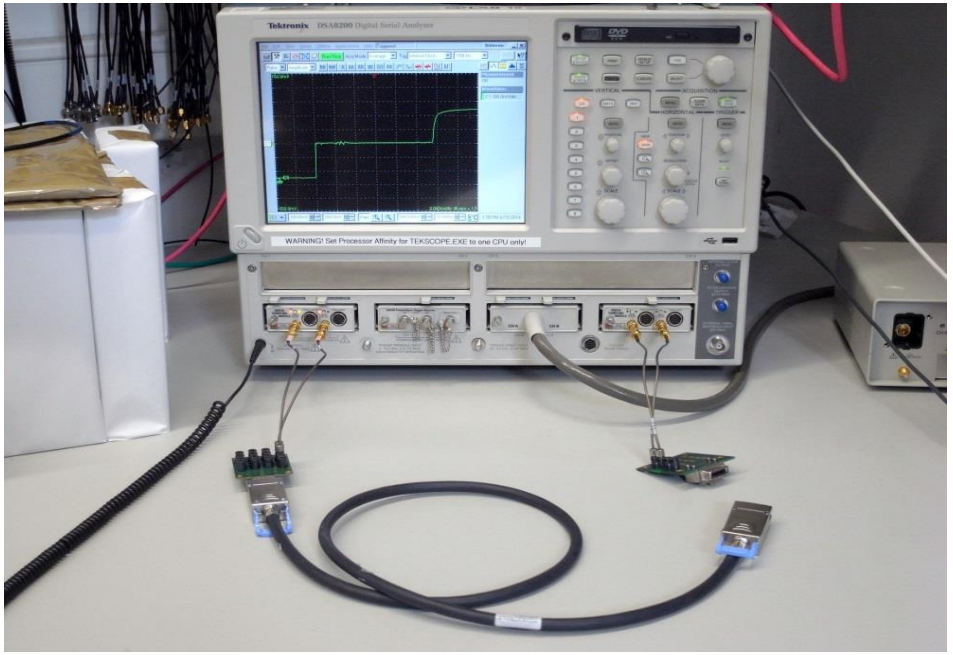
Time Domain Reflectometry (TDR)

- **Same TDR module** generates a voltage step and samples the reflected waveform
- Amplitude of reflected wave is proportional to the **impedance** along the DUT: $V_r(t) \propto Z(x)$





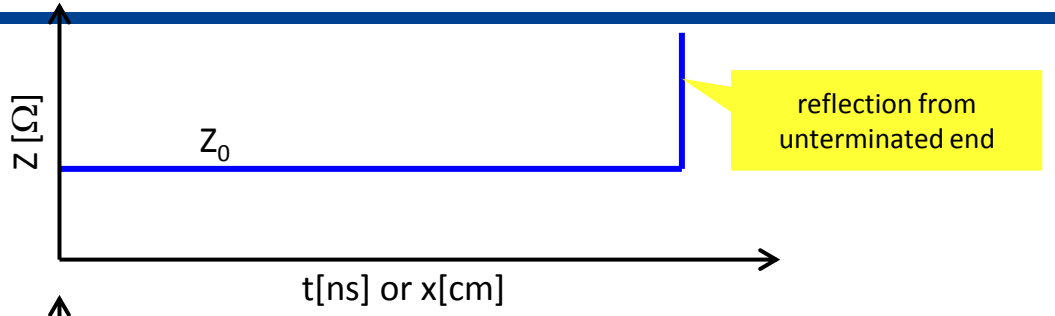
Measured TDR waveform



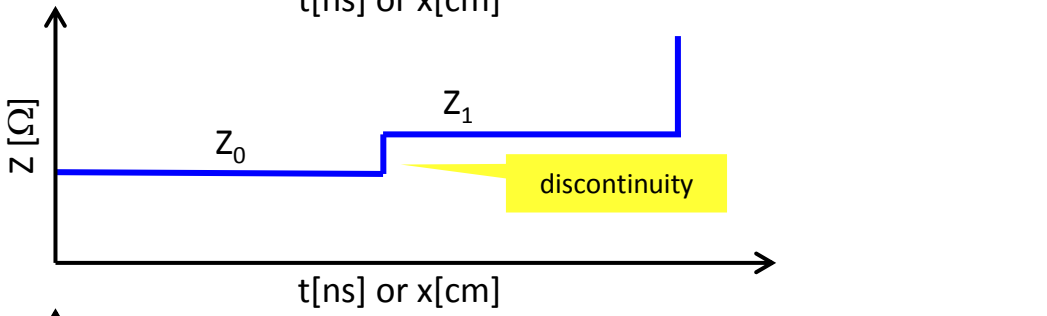
TDR setup with 1m Infiniband cable as DUT

How to interpret TDR Data

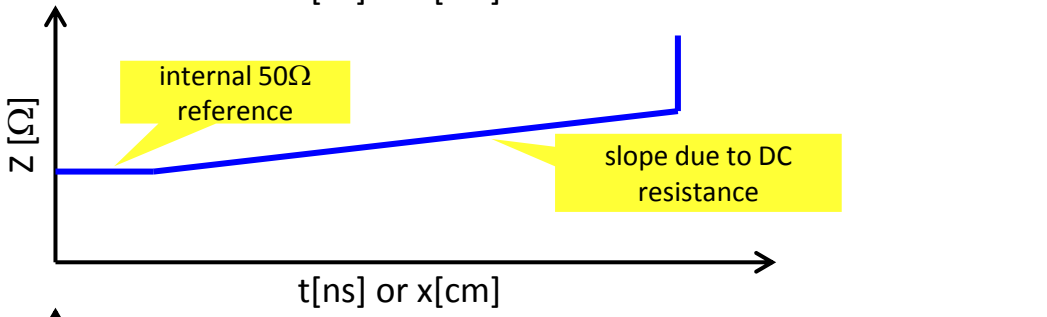
- Ideal transmission line



- TML with change in impedance

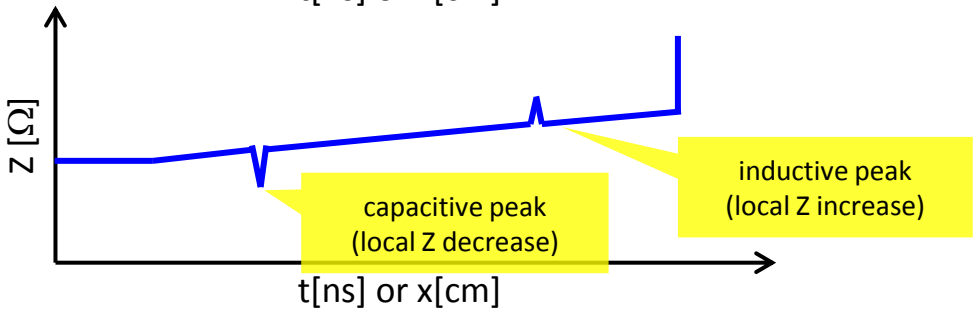


- TML with finite DC resistance



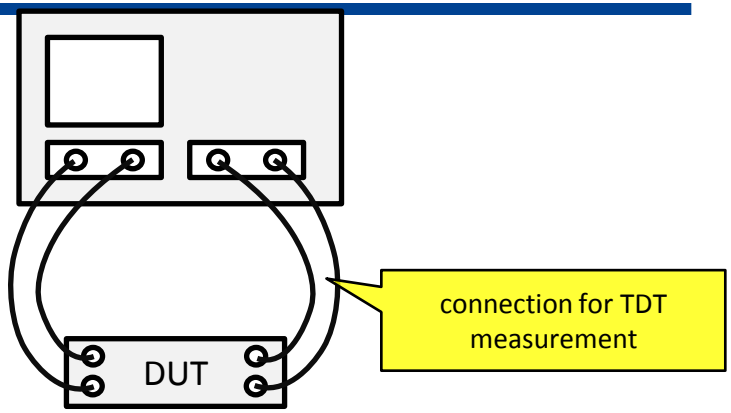
- TML with distortions

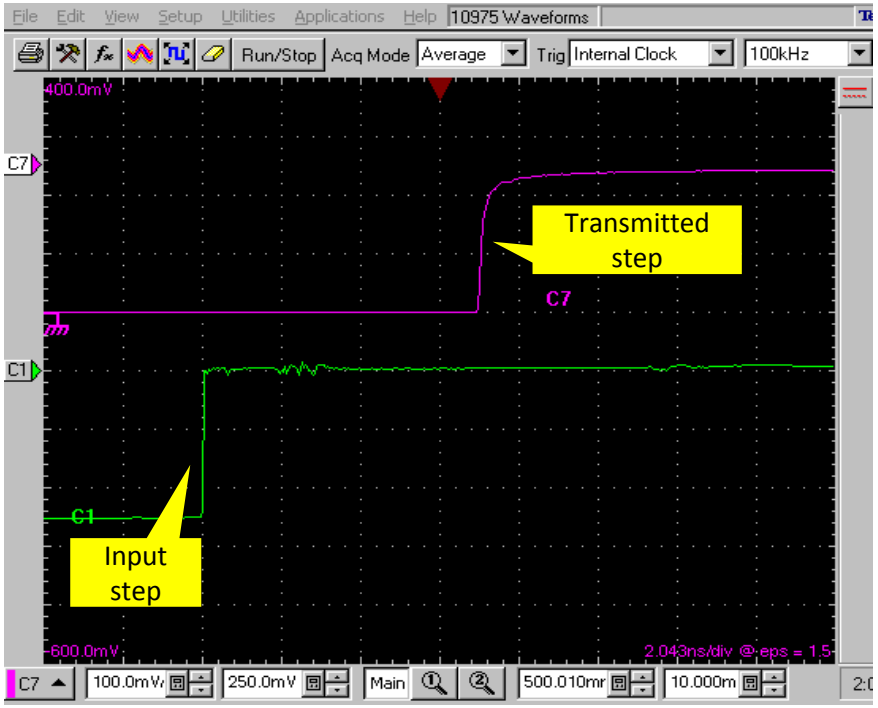
$$Z_0(x) = \sqrt{\frac{L'(x)}{C'(x)}}$$



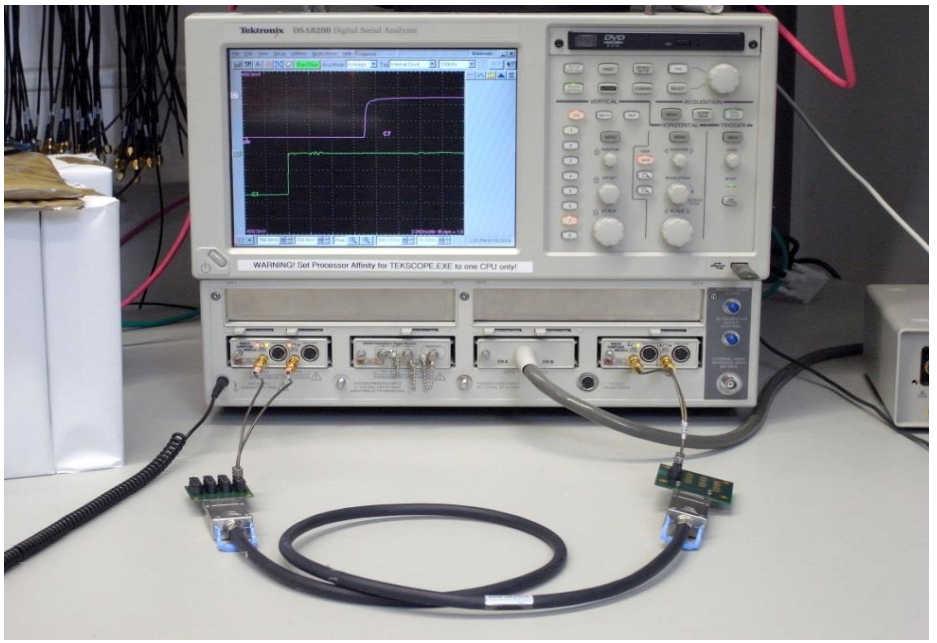
Time Domain Transmission (TDT)

- **One TDR module** generates the voltage step and the **second one samples** the transmitted waveform
- Analysis of input and output step functions yield the **transfer function *H(s)*** of the DUT





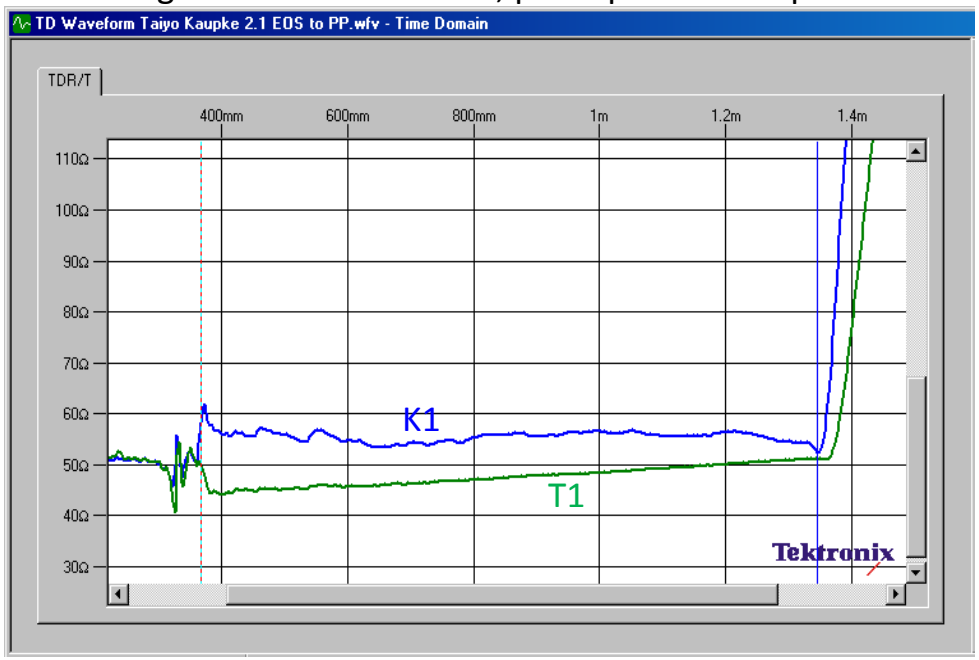
Measured TDT waveform



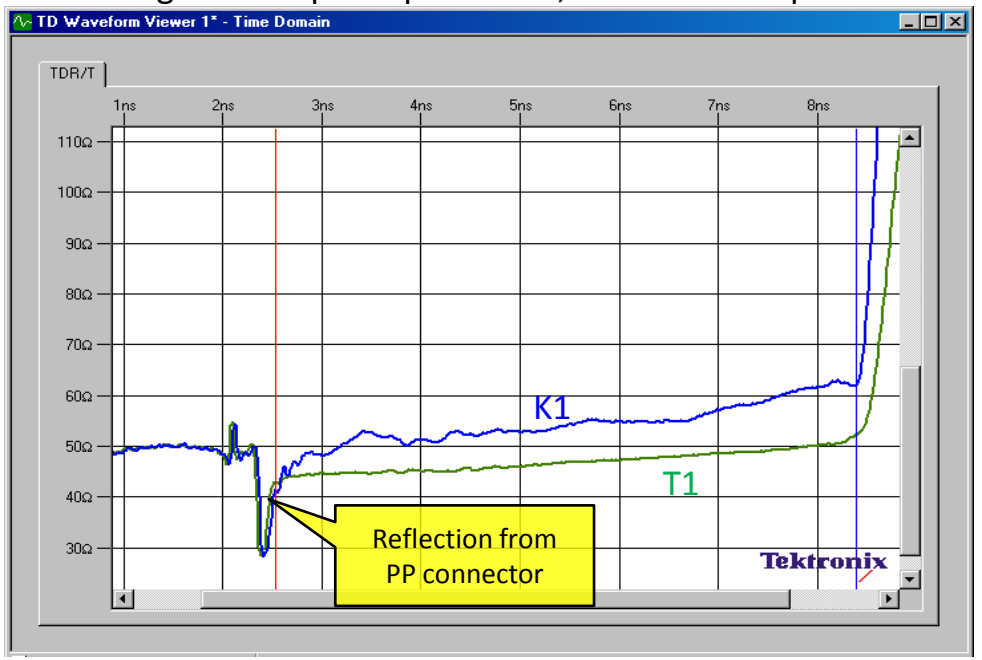
TDT setup with 1m Infiniband cable as DUT

Impedance Measurements (TDR)

Signal from module side, patch panel side open

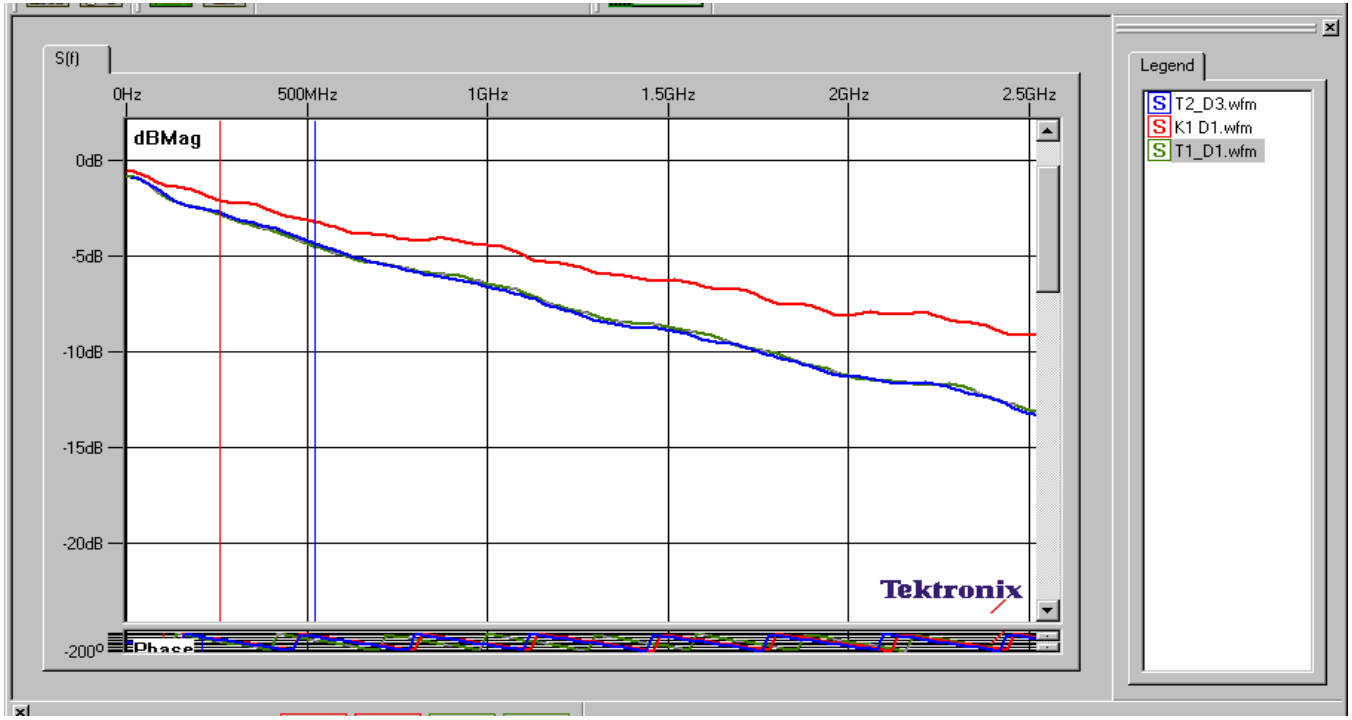


Signal from patch panel side, module side open



DUT	Diff. line impedance	Dielectric constant	Comment
T1 (Taiyo)	89Ω	3.1	Impedance constant along the cable
K1 (Kaupke)	90 - 116Ω	2.8	Impedance increases towards the module side of the cable

Attenuation Measurements (TDT)

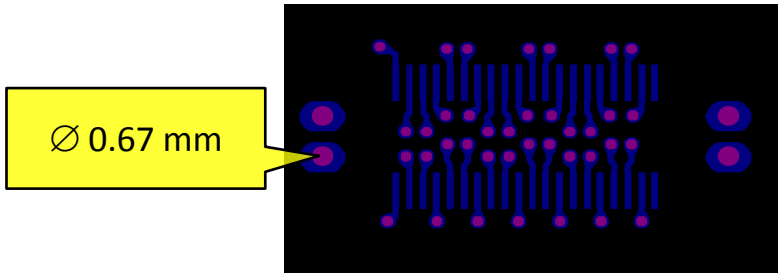


DUT	DC resistance (from DVM)	Attenuation @ 800 MHz	Attenuation @ 1.6GHz
T1 (Taiyo)	7.64Ω	5.75dB	9.03dB
K1 (Kaupke)	6.78Ω	4.19dB	6.55dB

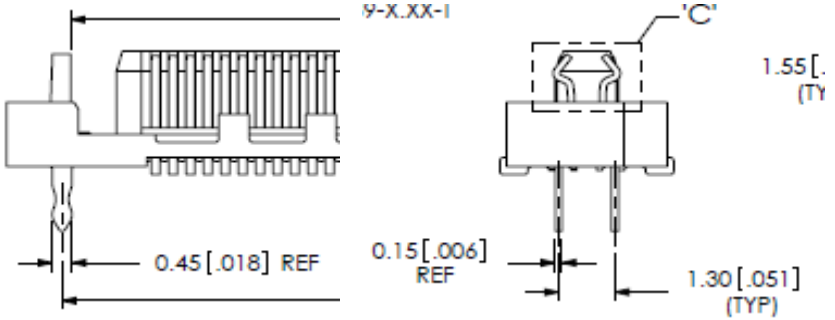
Proposed Design Improvements

- Poor alignment of data and power connectors (SAMTEC ST4) on patch panel
- Mounting holes diameter on PCB (0.67mm) much larger than connectors alignment pins dimension (0.45mm x 0.15mm)

➔ Recommendation: Reduce hole size to 0.5mm



Footprint in current design

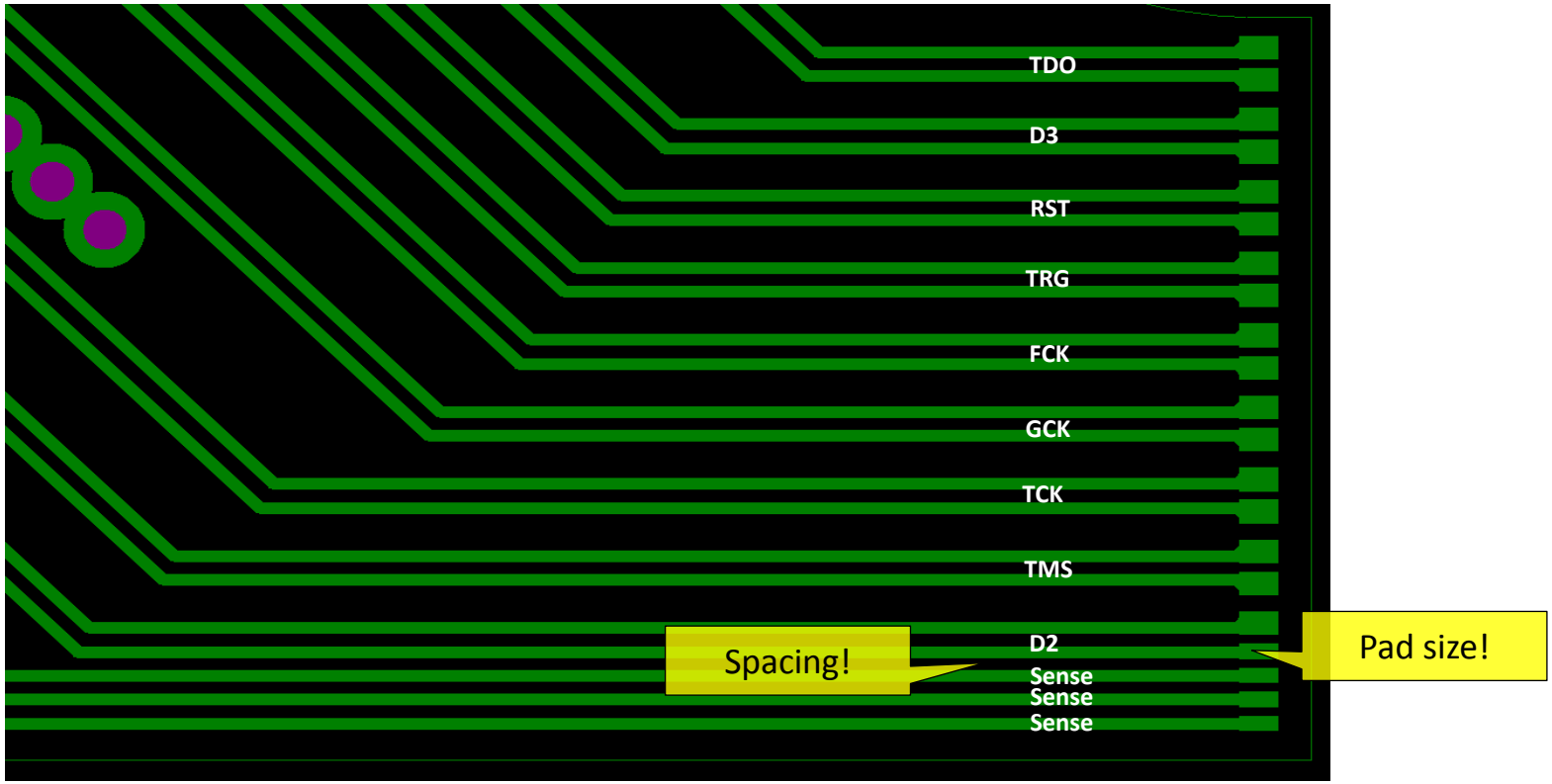


Samtec data sheet

Differential Lines Routing Details

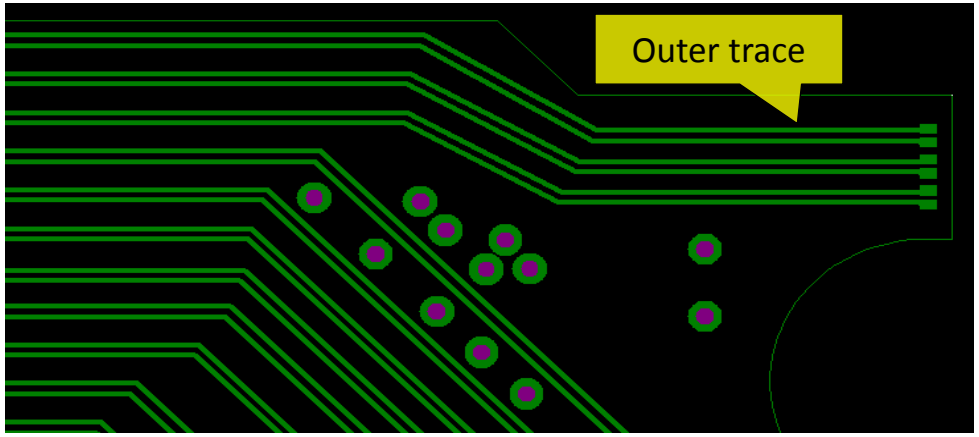
- D2 differential lines with little spacing to adjacent sense lines

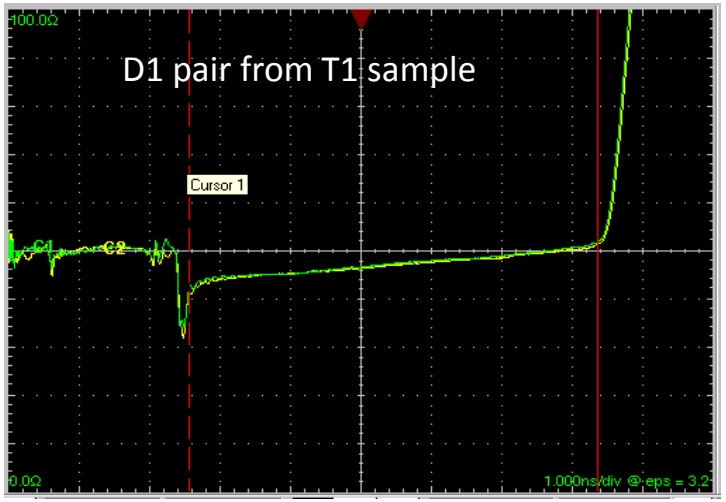
➔ Increase spacing between D2 and sense lines (remove RST and FCK lines)



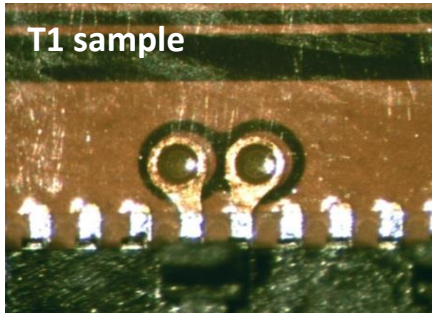
Differential Lines Routing Details

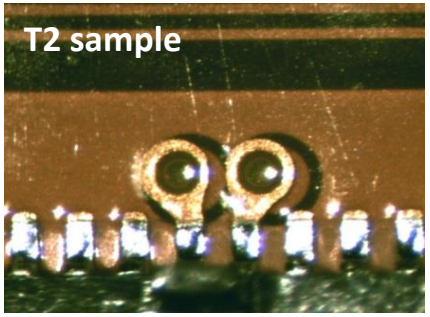
- Lines routed at the edge are critical



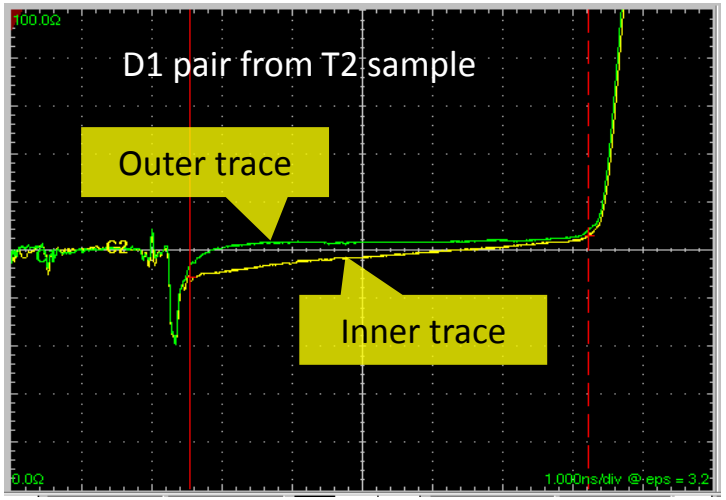


- Layer misalignment?



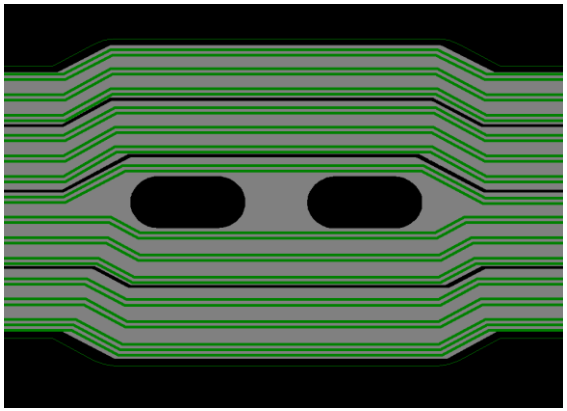


Zoom to PP data connector

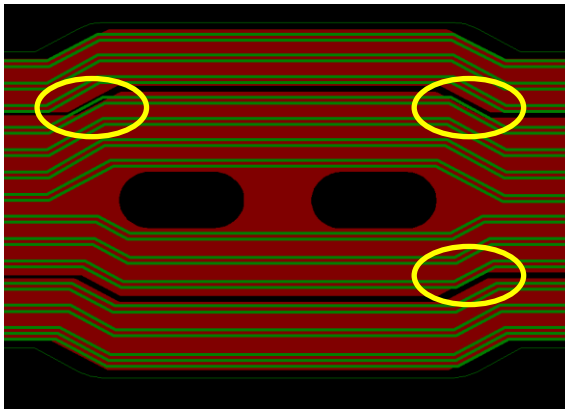


Differential Lines Routing Details

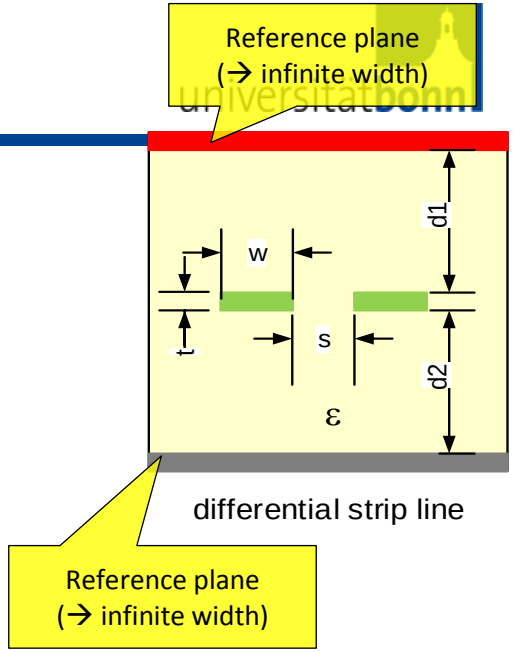
- Non optimal alignment between ground planes and signal lines



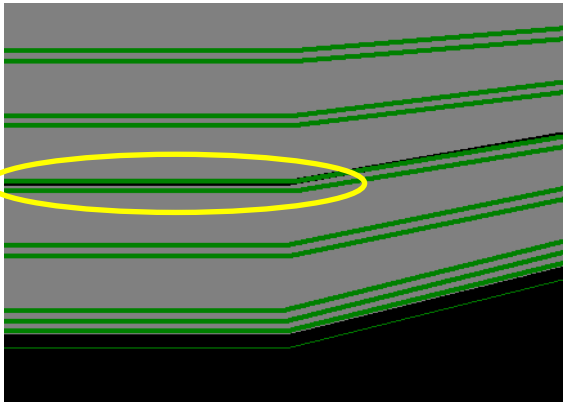
Signal layer vs. layer 4 plane (ok)



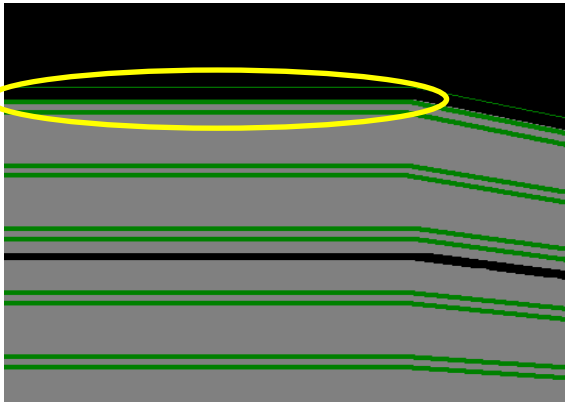
Signal layer vs. layer 2 plane (bad)



- Signal lines too close to the ref. plane edge or split between planes



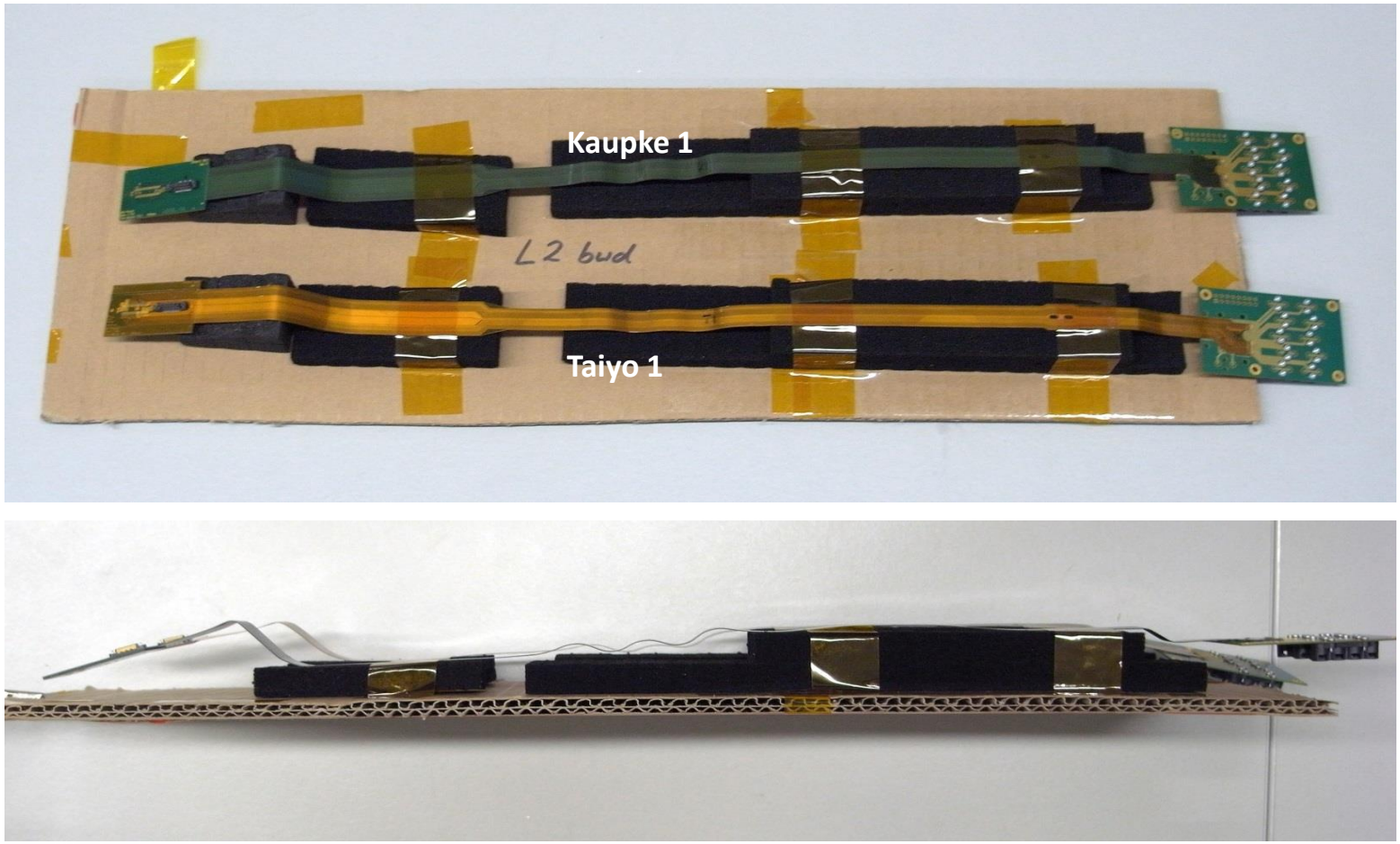
Diff. pair split between planes (bad)



Diff. pair too close to edge (bad)

Similar details on patch panel and module connector region

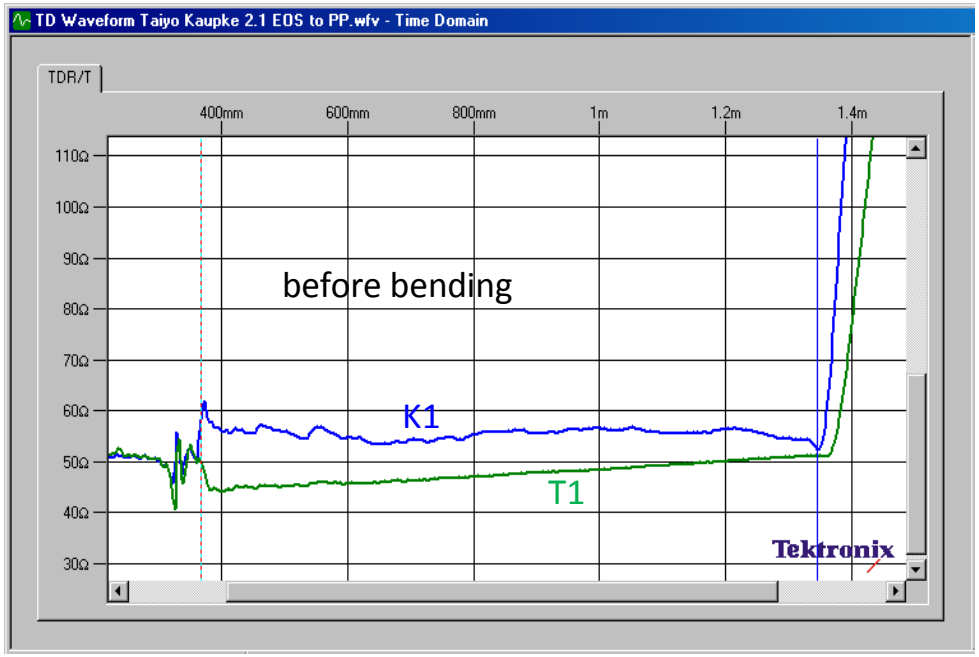
Cable Bending

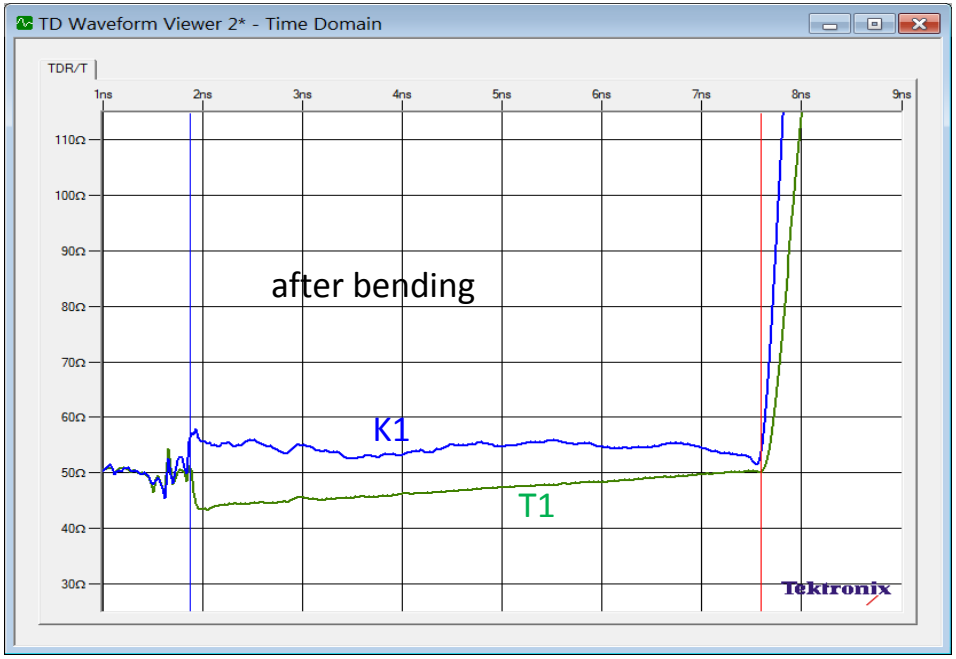


- The K1 flex is keeps the shape nicely, while T1 flex, being less rigid, tends to loose the pre-bends slightly

TDR before and after Bending

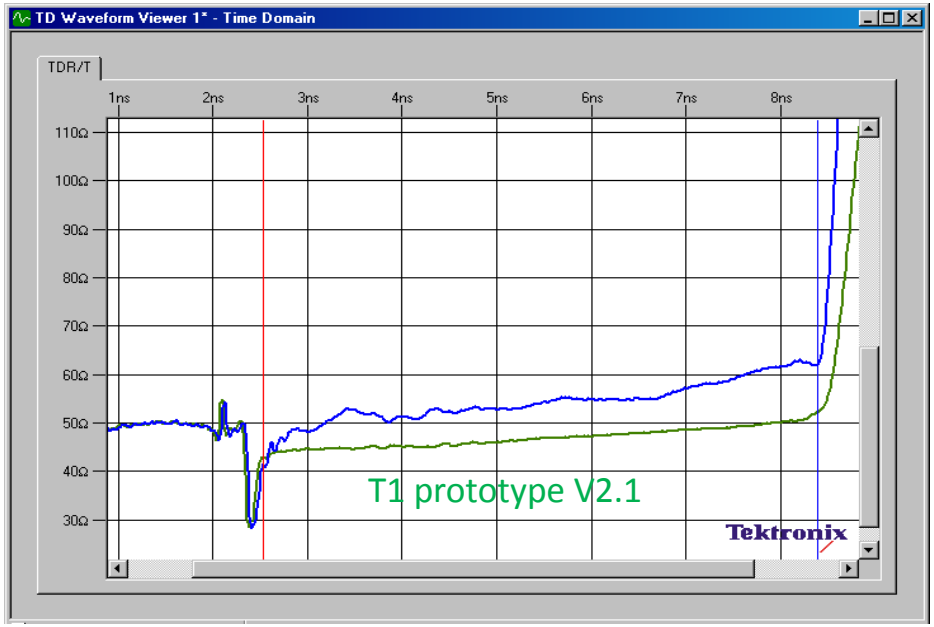
Signal from module side (D3), patch panel side open

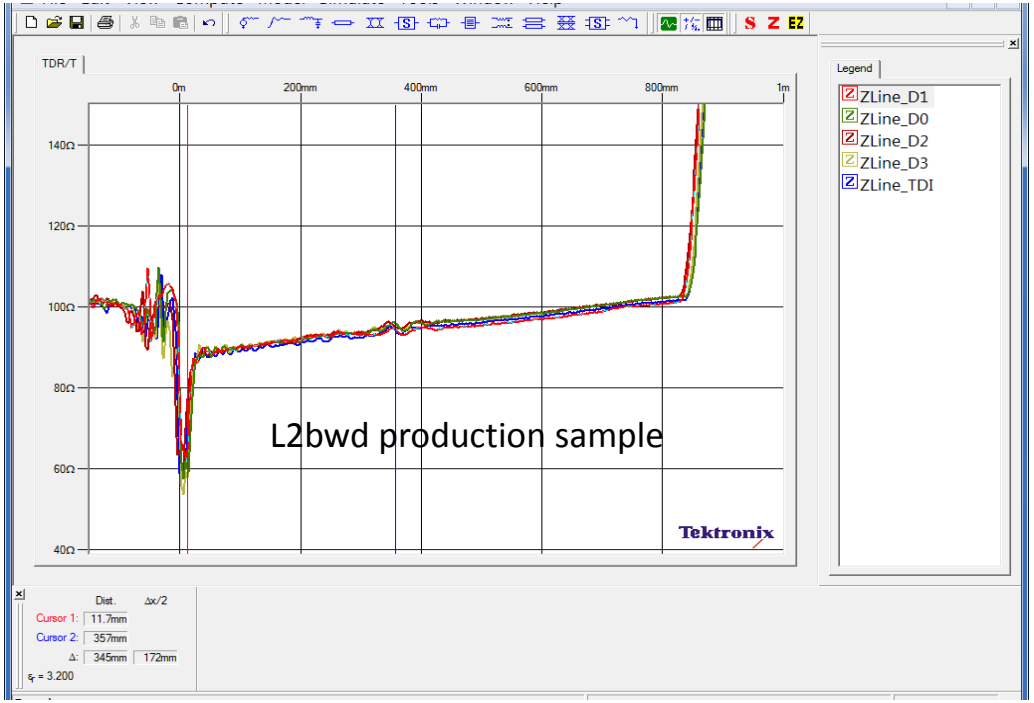




- TML impedance is not influenced by cable bending

First Production Sample “L2bwd”





- Production sample “L2bwd” (very similar to prototype “T1”)
  - Z_0 ~ 90 Ω
  - R_{DC} ~9 Ω
- No Impedance distortion for lines running close to the cable outline (TDI)

Summary

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- Taiyo prototypes
  - T1 and T2 samples have very similar electrical properties
  - Z_0 = 89Ω, R_{DC} = 7.6Ω
  - ε_r = 3.1
  - Attenuation @ 800MHz = 5.8dB

- Kaupke prototype
  - Z_0 = 90-116Ω (changes along cable), R_{DC} = 6.8Ω
  - ε_r = 2.8
  - Attenuation @ 800MHz = 4.2dB

➔ Kaupke seems to use a different layer stack (cable more rigid and slightly thicker)
  - Less attenuation
  - Higher impedance
  - Lower ε_r

Summary II

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- Full cable setup (flex + PP + short TWP + PP + long TWP) needs to be evaluated to assess the overall signal integrity

- High frequency damping (skin effect, dielectric losses)
  - can be partially compensated by pre-emphasis (DHP) and equalization on the receiver side (DHH/FPGA)

- Absolute TML impedance
  - Kapton cable layer stack and line geometry

- Impedance discontinuities (**Pre-emphasis does not compensate this!**)
  - Analyze TDR measurements and check critical PCB layout regions (edges, connectors, vias etc.)