PXD Gated Mode

ASIC Review Meeting

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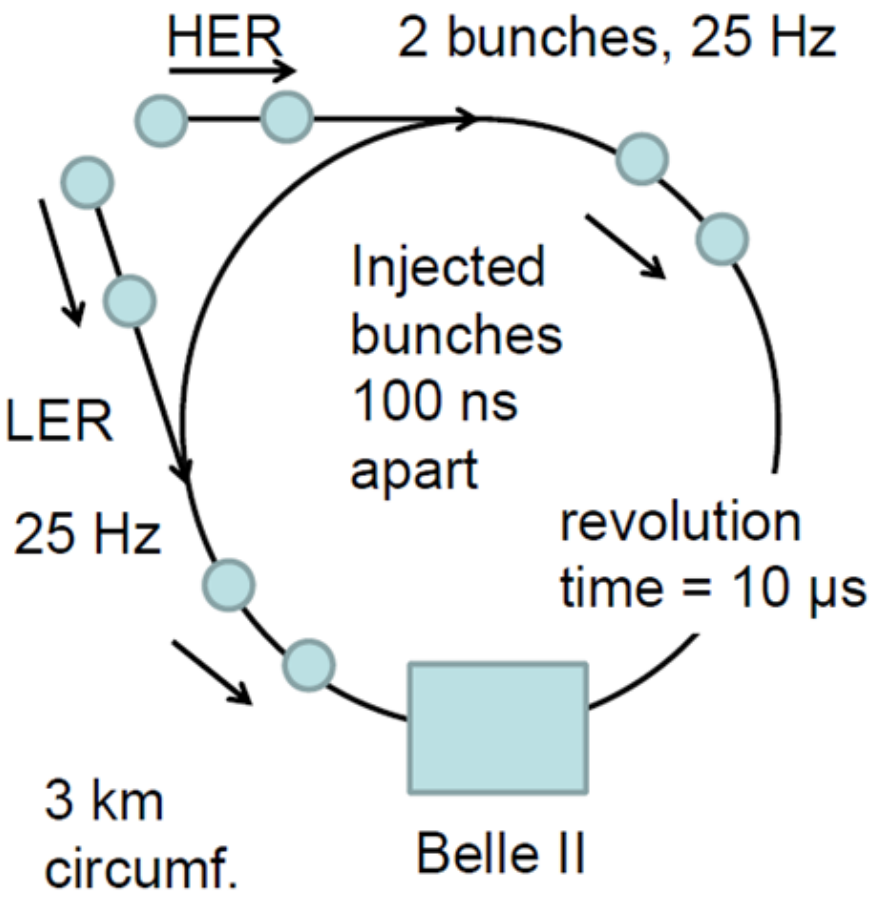
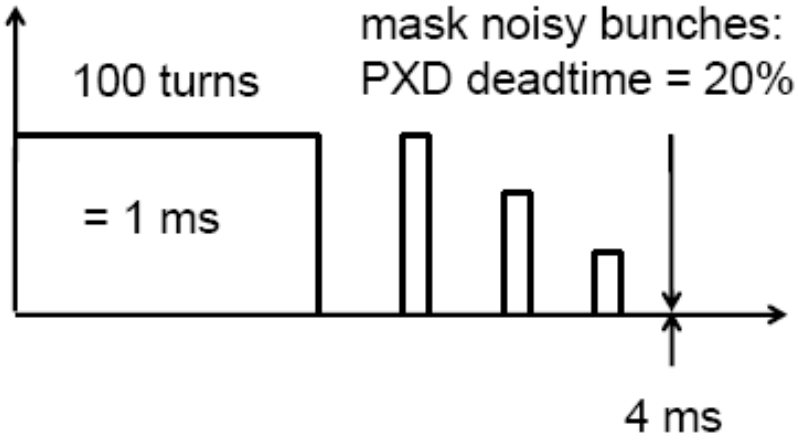
On behalf of the DEPFET collaboration

Outline

- Why is the Gate Mode necessary?
- Summing up of the mechanism how we get into the Gate Mode
  - DEPFET voltages
  - System overview
  - DHPT change of the SW sequence (block diagram of the DHPT logic)
  - SW which control signals are important?
- How long will the Gated Mode block an individual layer and what does this mean to the 2-layer PXD?
- Description of the test with the various ASICs/Test setups
  - DHPT with Probe Card
  - SW, DCDPP and small PXD6 matrix with Hybrid 4
- Outlook for the system test with EMCM and later PXD9-pilot
  - Integration of the DHE
  - Measurement of the SW output waveform
  - Response of small PXD6 matrix
- Summary

Injection Scheme of SuperKEKB



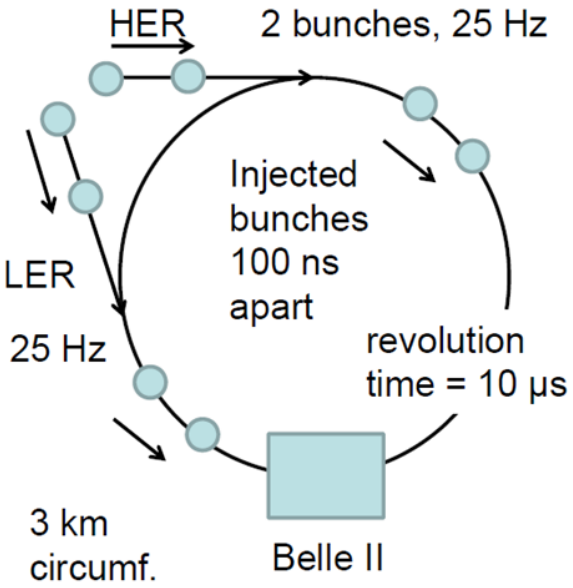


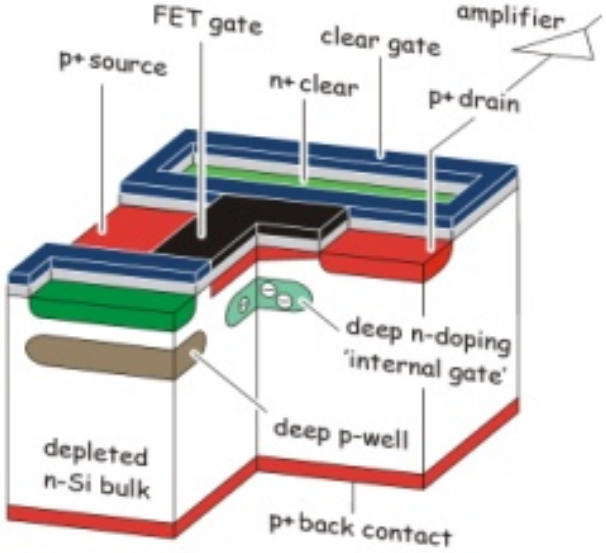
4ms for cooling mechanism

=> Loss of particles (‚noisy' bunches)

→ How to gate DEPFET pixels during bunch injection?

Principle of the DEPFET gated-mode

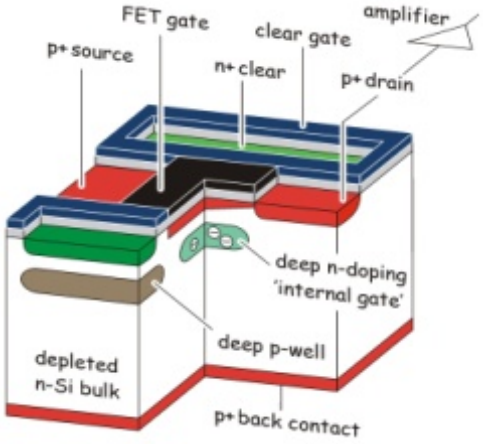




- "Noisy bunches" create (junk) electrons within the PXD detector
- These junk electrons have to be removed while the number of stored electrons in the internal Gate should **not** be changed!

Principle of the DEPFET gated-mode

- Applying appropriate voltages to **Clear** and **Gate** one can apply an electronic shutter:
  - Clear pulse to all pixels during the noisy bunch injection (every 10µs, ΔU = 15V)
  - Keep the Gate in the off state (+5V)



Two questions (sensor related):

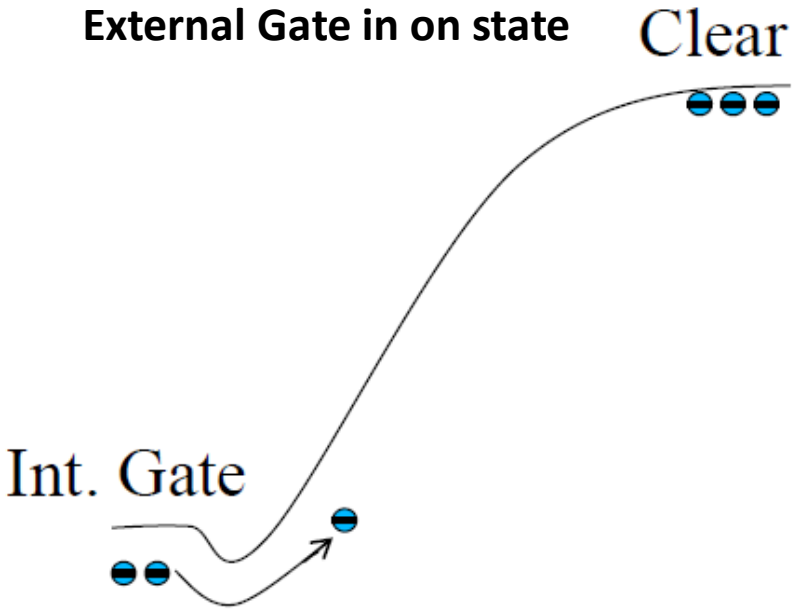
1) Can we protect charge in the internal Gate from being cleared?

2) How much of the junk charge will arrive in the internal Gate?

Selectivity of the Clear Process

Real Clear

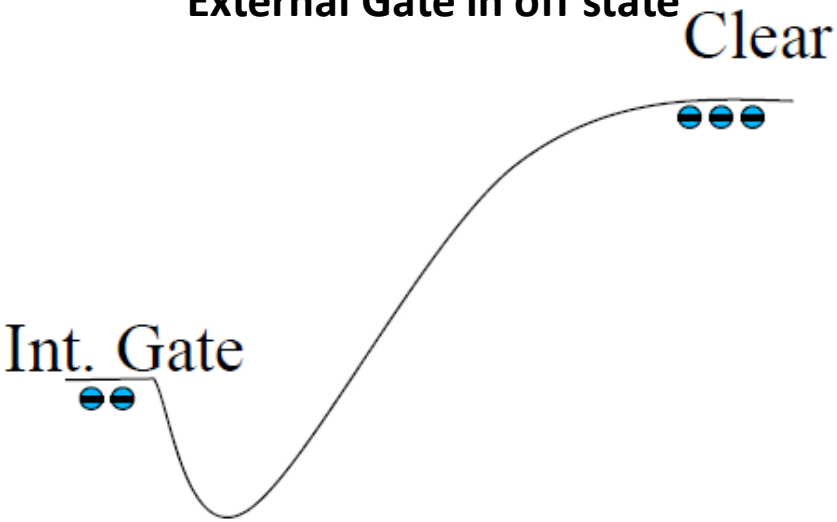
External Gate in on state



Electrons can overcome the small potential barrier by thermionic emission.

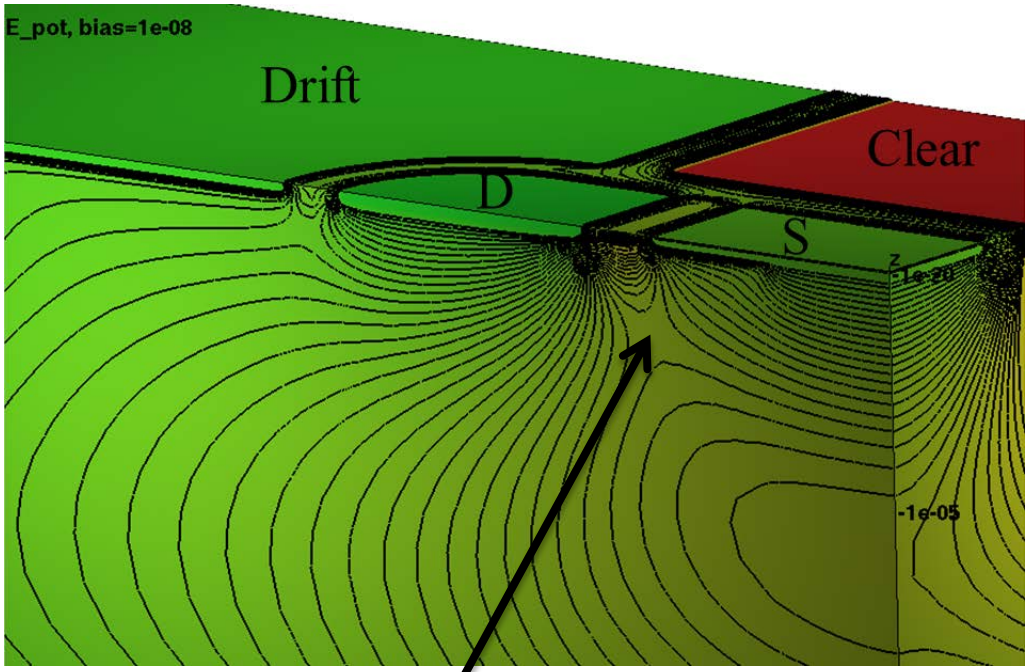
Suppressed Clear

External Gate in off state



→ The difference is due to the applied voltage at the external Gate.

Shielding of the Internal Gate

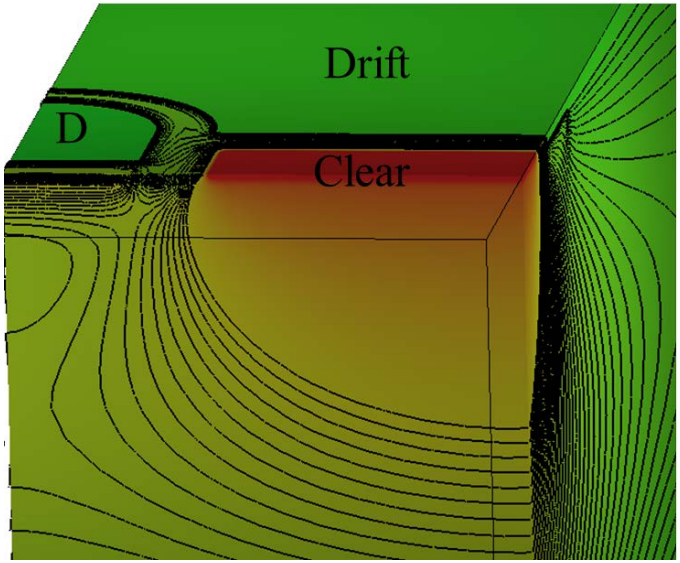


Clear region is much larger than internal gate

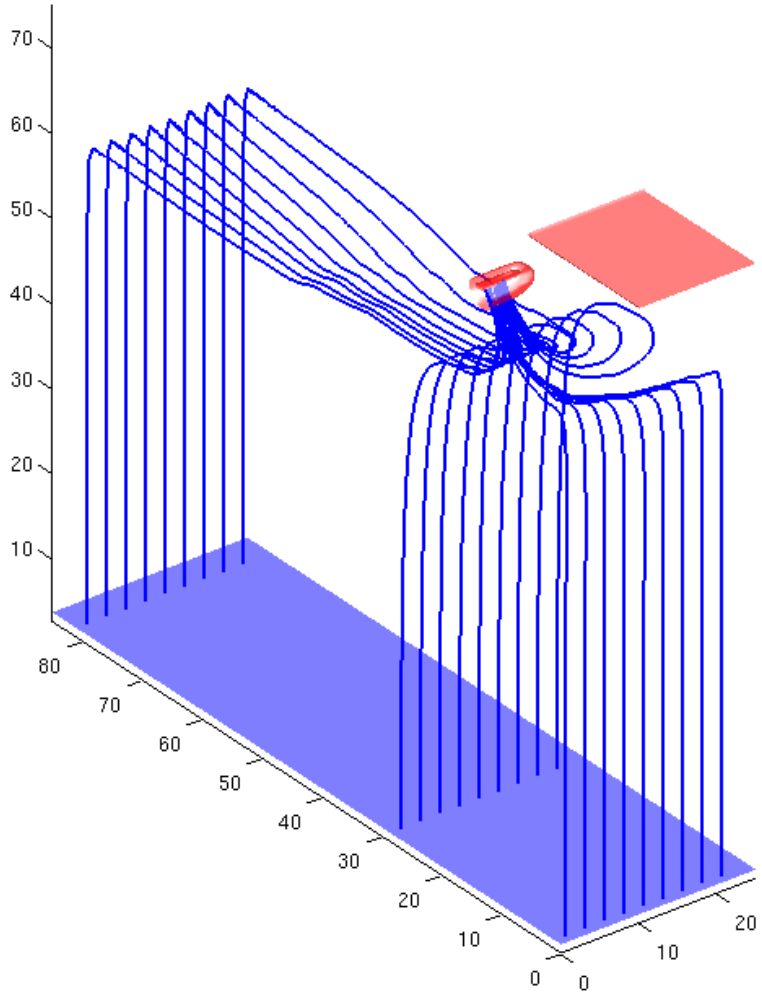
→ Good for dumping electrons into the clear

Potential barrier
→ Caused by the reach through of the drain to the source

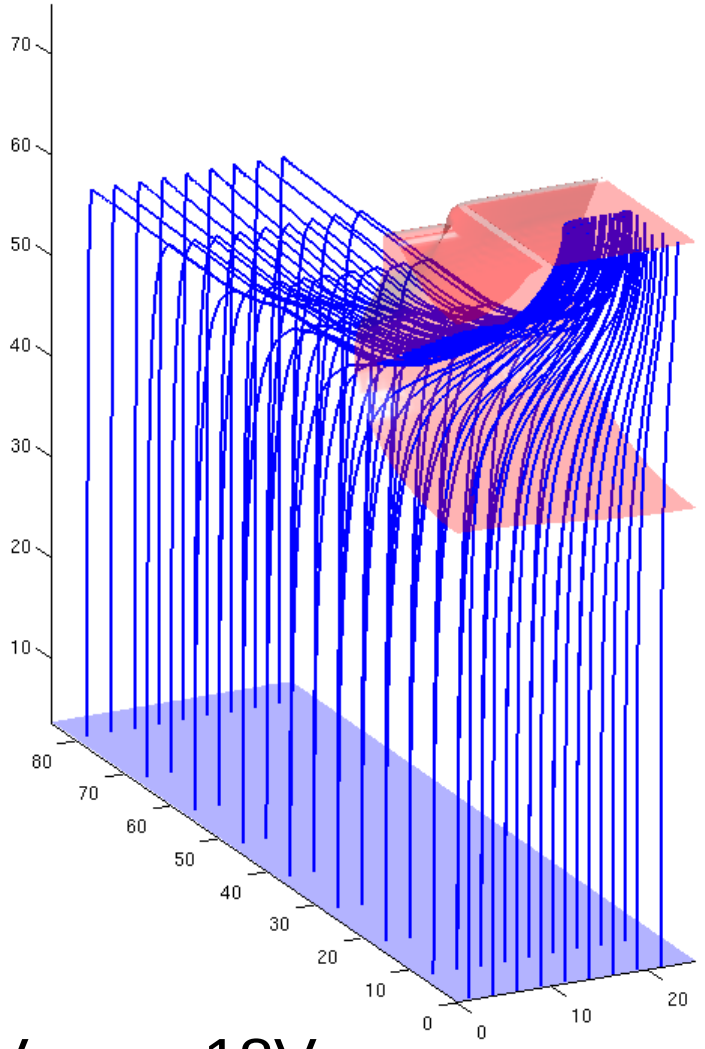
First results: No additional electrons in the Int. Gate @Vclear=18V



Shielding of the Internal Gate



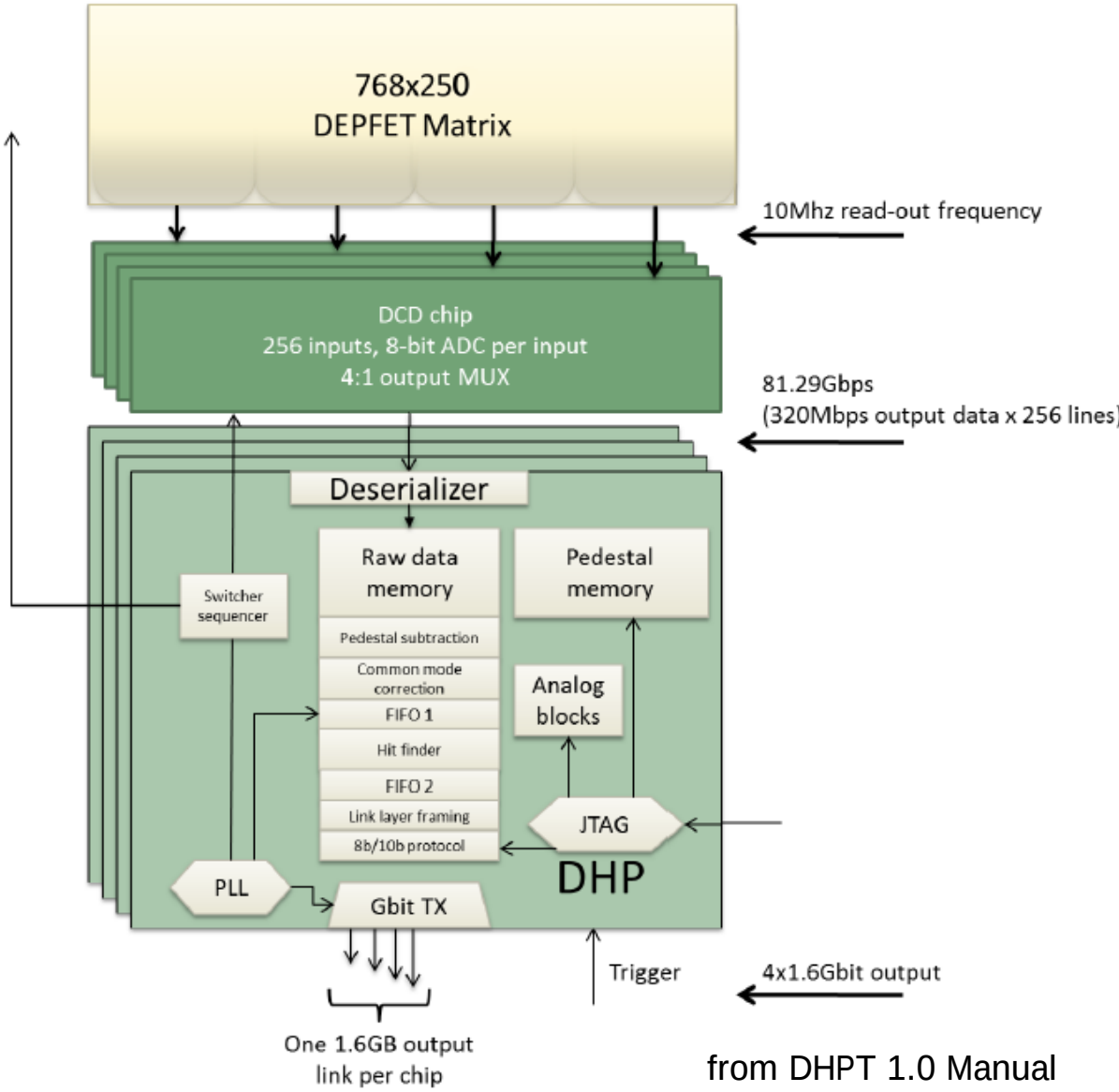
V_{Clear} = 3V



V_{Clear} = 18V

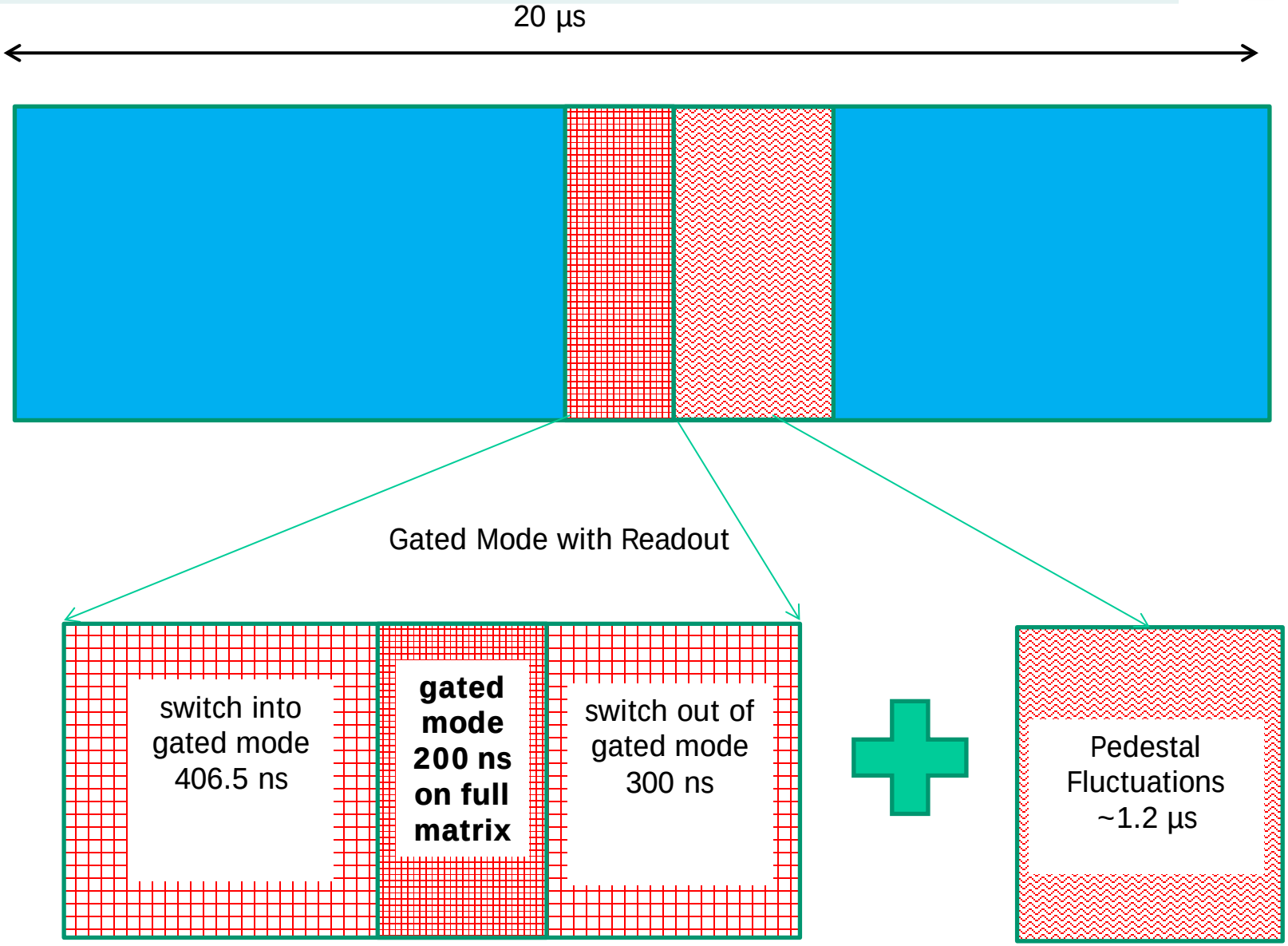
System Overview during Gated Mode

- DCDPP and DHPT operate as normal, including DCD clocking, pedestal correction with 2-bit DAC)
- SWB applies ClearOn voltage to all (except of one) rows + GateOff voltage to all (except of one) rows
- Different modes of operation during Gated Mode: with and with-out Read-out
- Even if the mode “Gated Mode with Read-Out” is chosen, data are not to be transmitted by DHPT
  - large shift of the pedestal currents which cannot be compensated
  - DHE puts Trigger signal to low during Gated Mode so there is nc problem with high occupancy during this time



from DHPT 1.0 Manual

How long will the Gated Mode block an individual layer?



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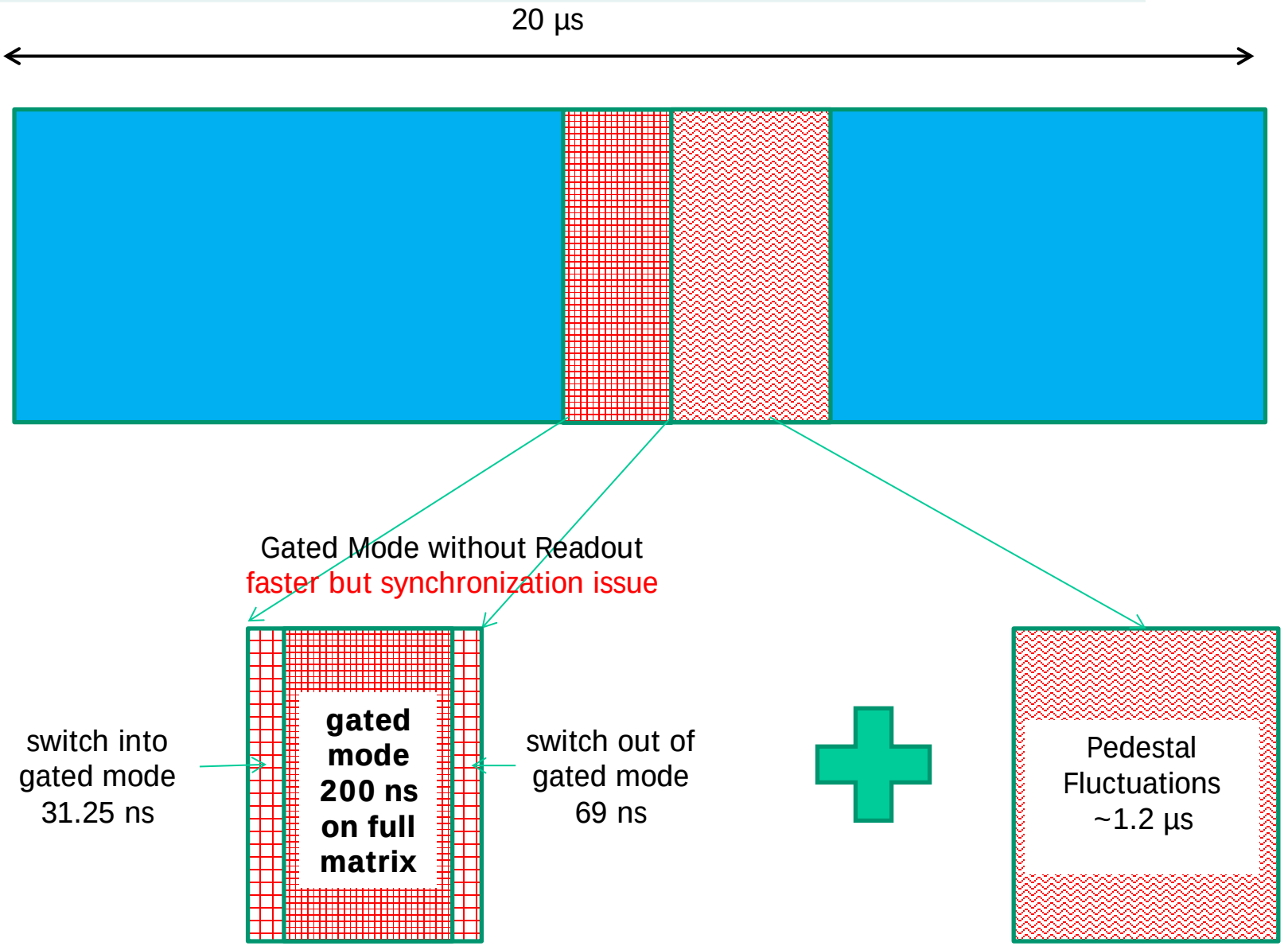


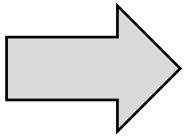
How long will the Gated Mode block an individual layer?

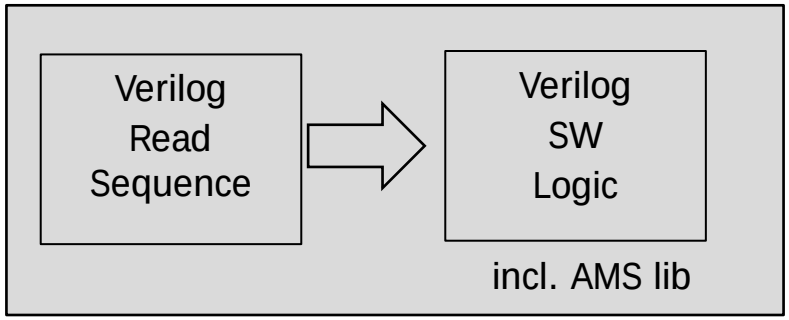
Gated mode without read-out

- Example of the SW sequence to “jump” to the correct row after the Gated Mode

Python program generate SW Sequence

SW_Frame	SW_Clear	SW_Gate	SW_CLK
o	0	1	0
0	1	0	1

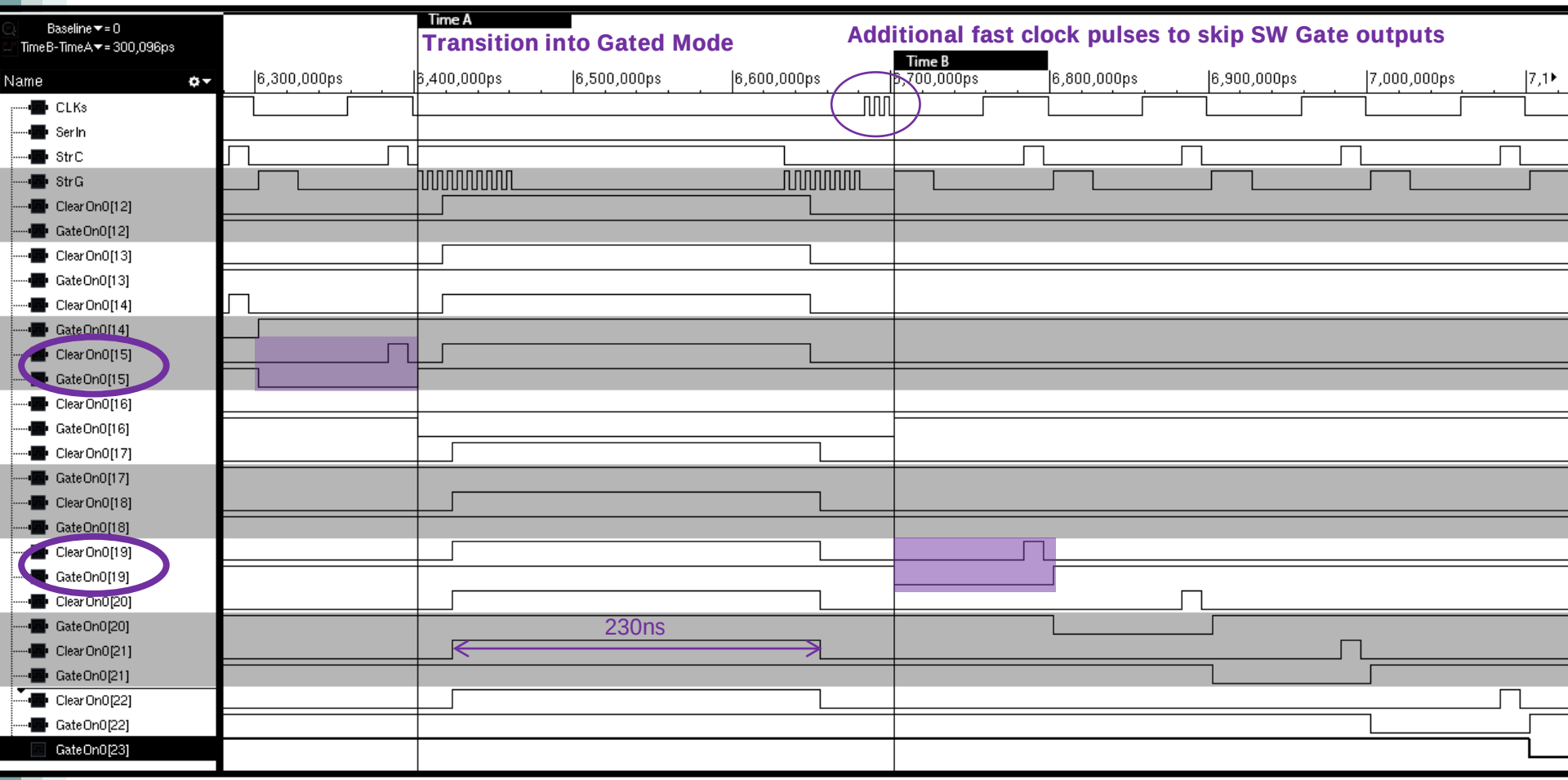




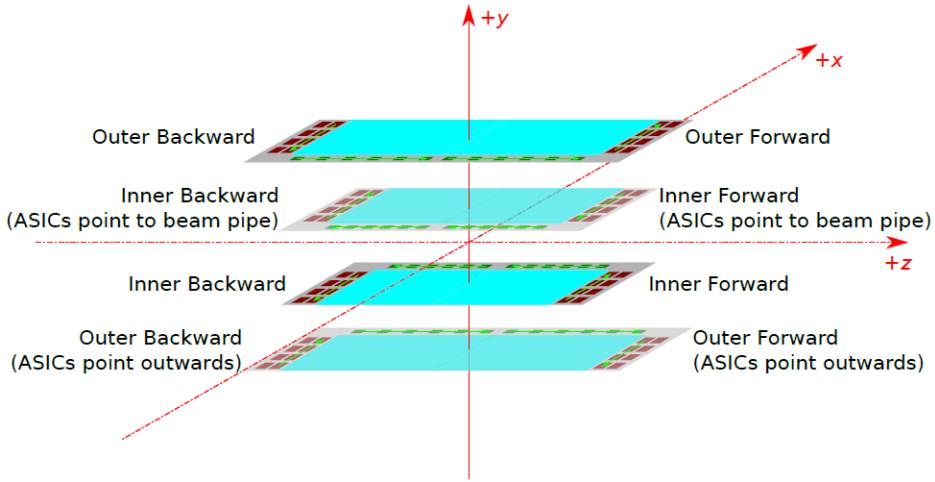
How long will the Gated Mode block an individual layer?

Gated mode **without** read-out:

- SW sequence with “jump” to the correct row after the Gated Mode
- Total time for the Gated Mode: **300ns**

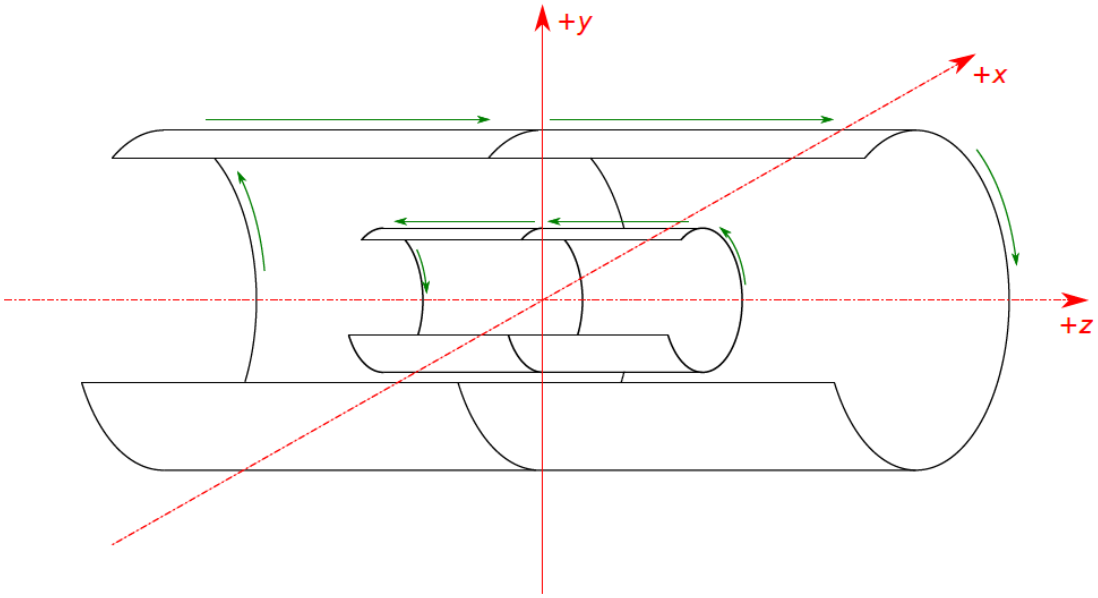


What does this mean to the 2-layer PXD?



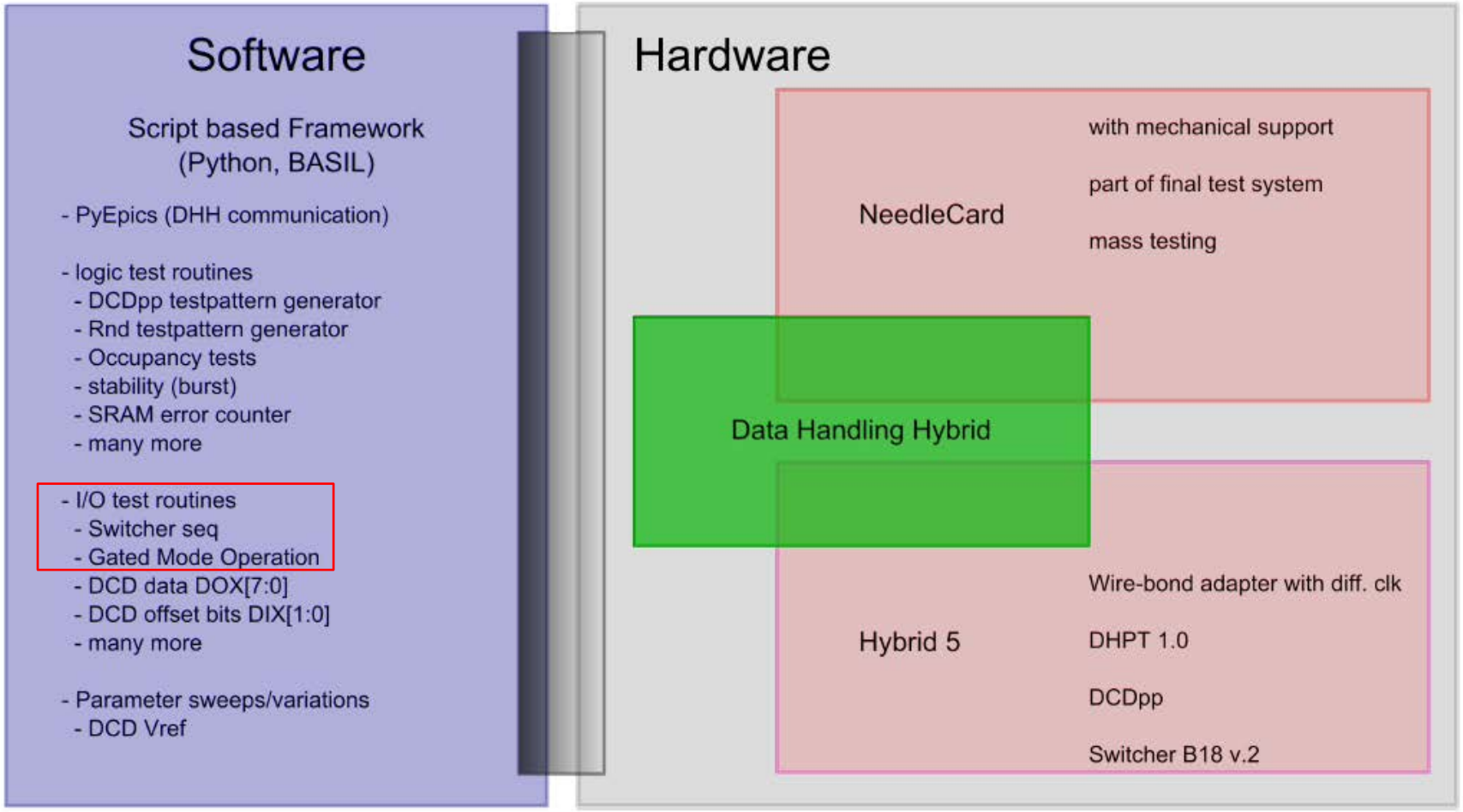
Due to the different read-out direction for the inner and outer layer, the overlap of the blocked, gated region is very small.

Any distortion or loss of data during Gated Mode would affect different areas for the inner and outer layers.

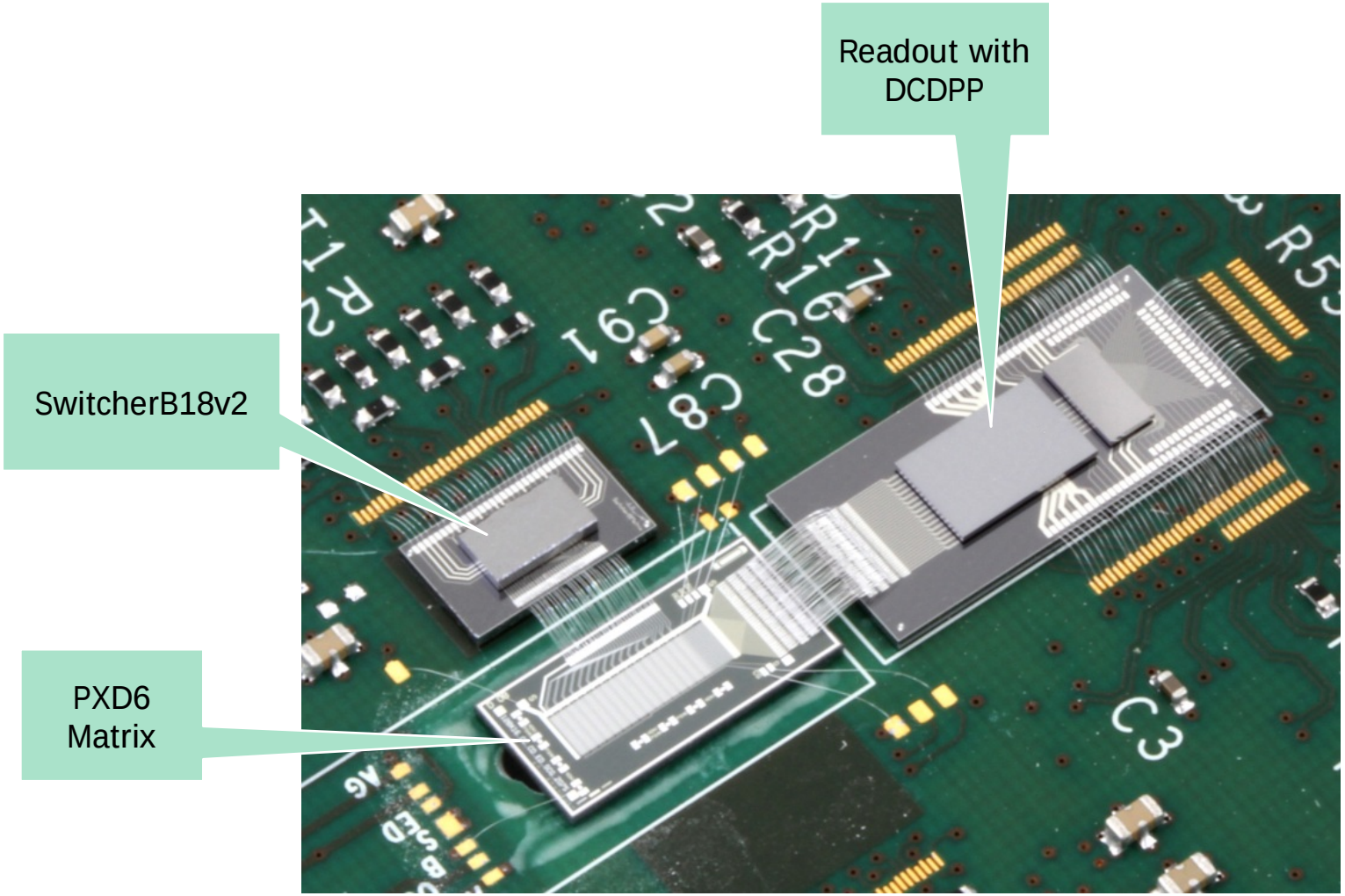


DHPT Functional Verification with Probe Card

DHPT Gated Mode function verified with Probe Card and Hybrid5 setup

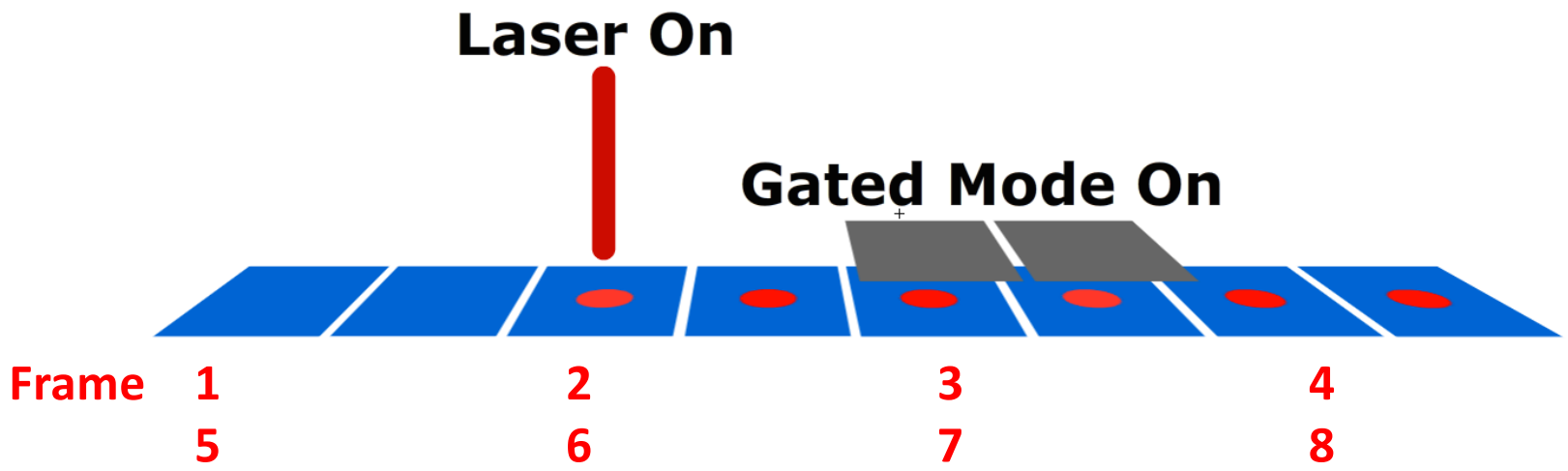


SW, DCDPP and small PXD6 matrix with Hybrid 4

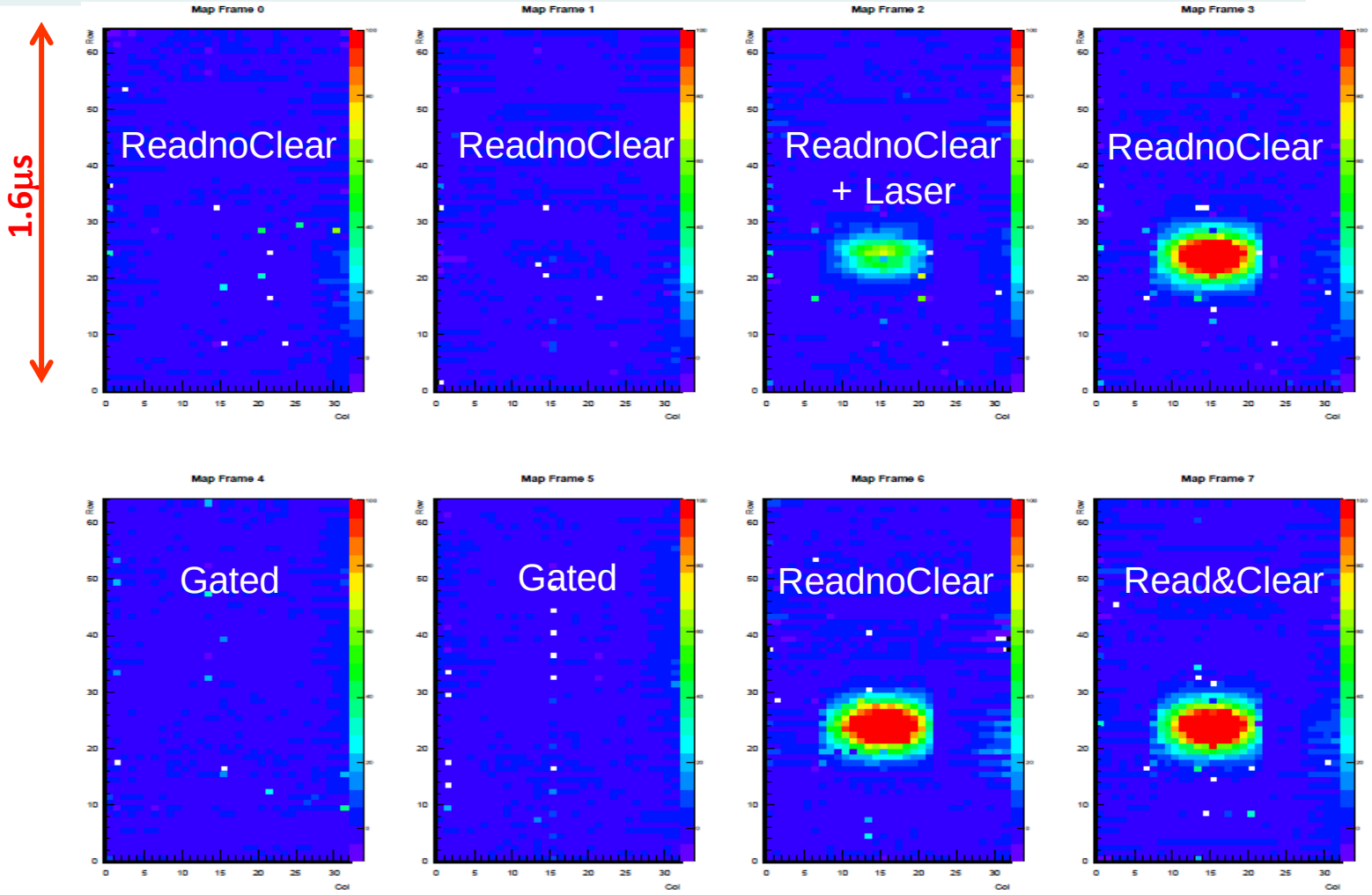


SW, DCDPP and small PXD6 matrix with Hybrid 4

Frame n	Frame 0	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5	Frame 6	Frame 7
Normal sequence	ReadnoClear	ReadnoClear	ReadnoClear + Laser	ReadnoClear	Gated Mode	Gated Mode	ReadnoClear	Read & Clear

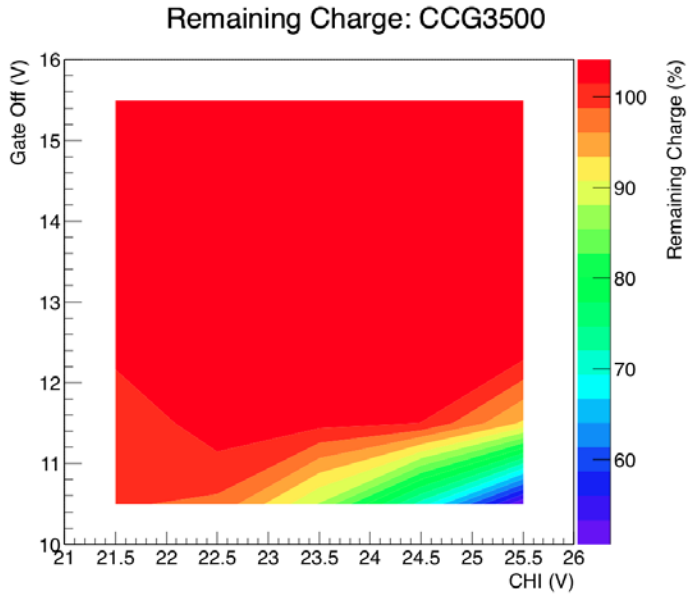


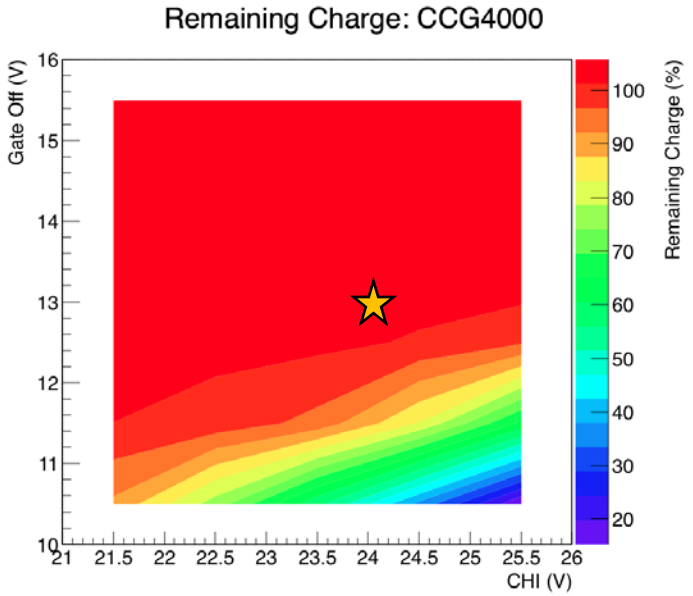
Small Matrix - consecutive Frame Read-out

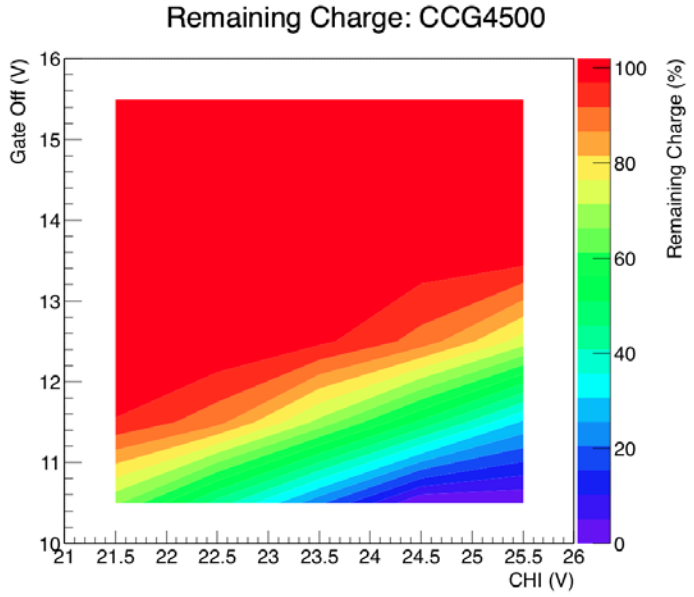


- Laser 1µs, 800mV

Gated Mode with Read-Out



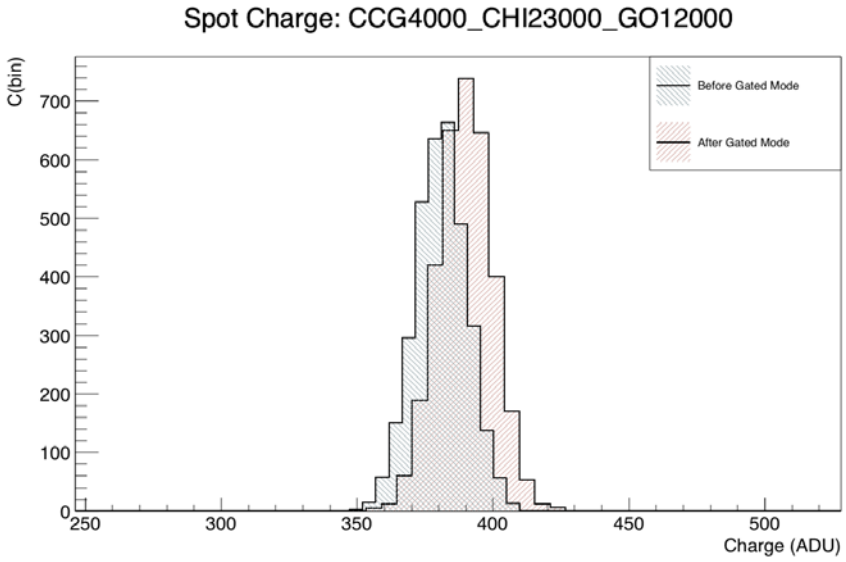


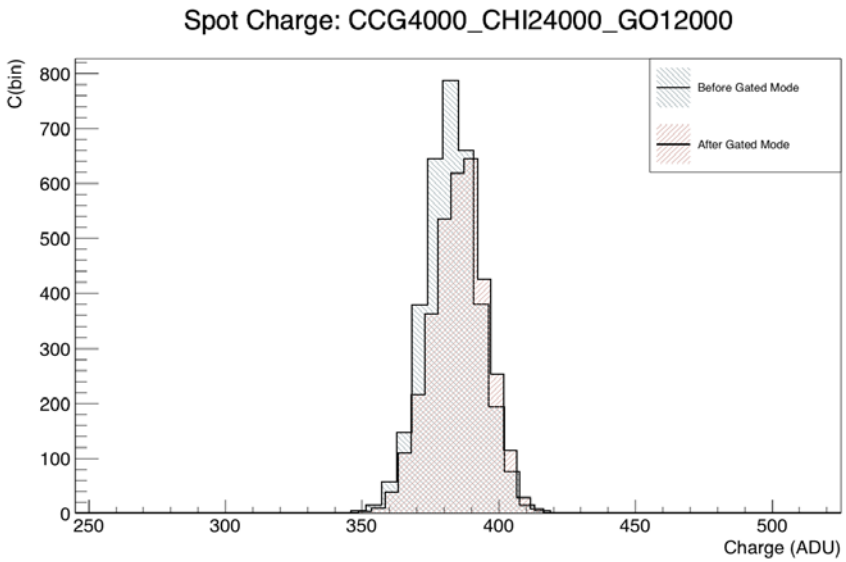


Gated Mode with read-out

- **No charge loss for a large set of voltages**
- Tendency for small increment in charge for higher GateOff voltages respectively lower ClearOn voltages

Gated Mode with Read-out





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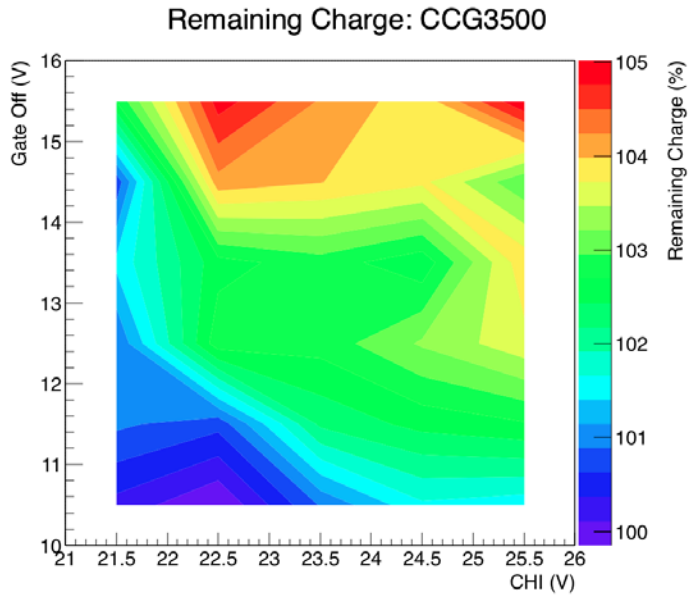
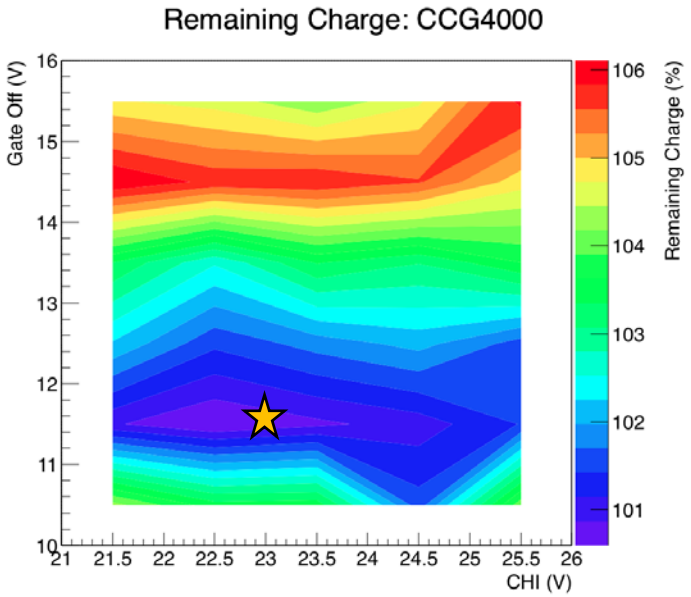
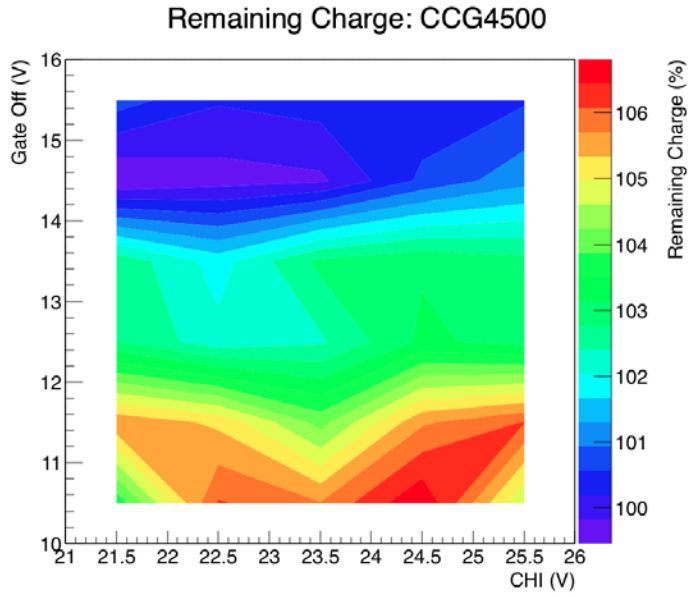


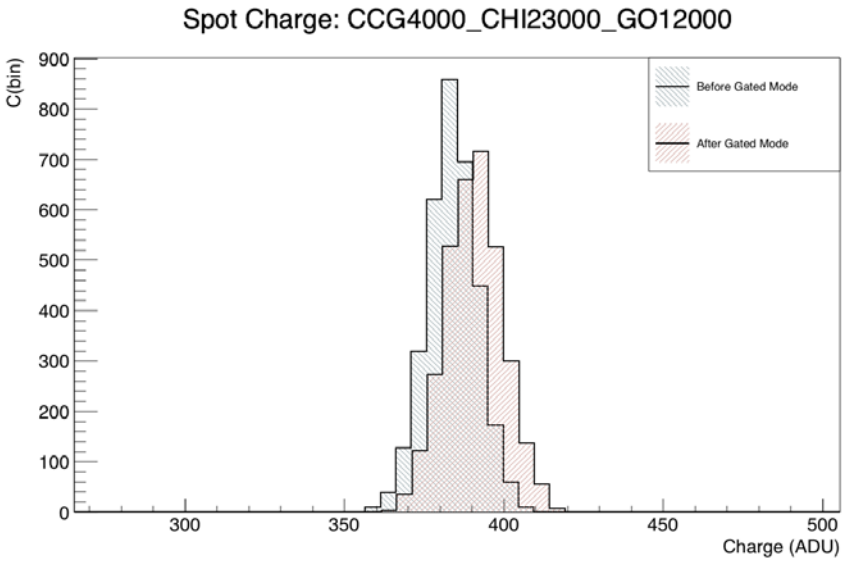


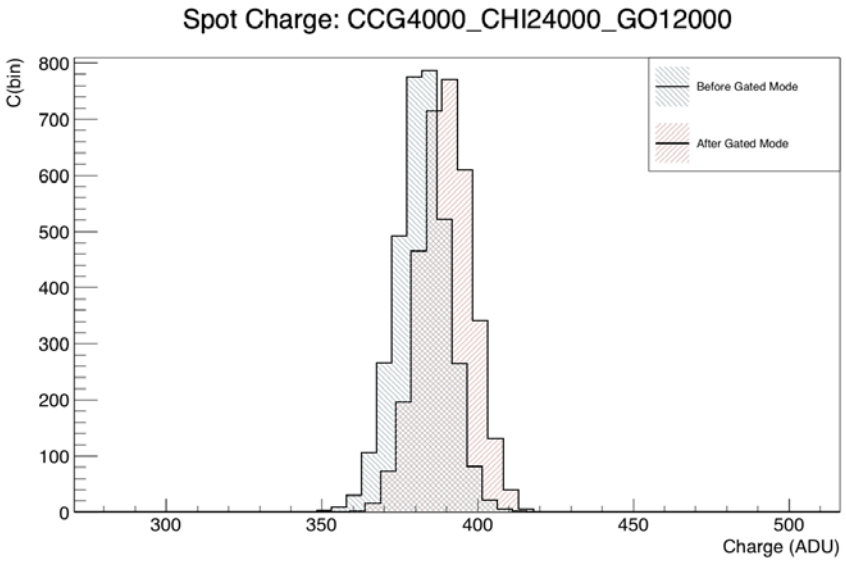


Gated Mode without read-out

- **Stronger effect of ClearGate voltage (CCG)**
- **No charge loss for a large set of voltages**
- Tendency for small increment in charge for higher GateOff voltages respectively lower ClearOn voltages

Gated Mode without Read-Out





Gated Mode without read-out

- **Stronger effect of ClearGate voltage (CCG)**
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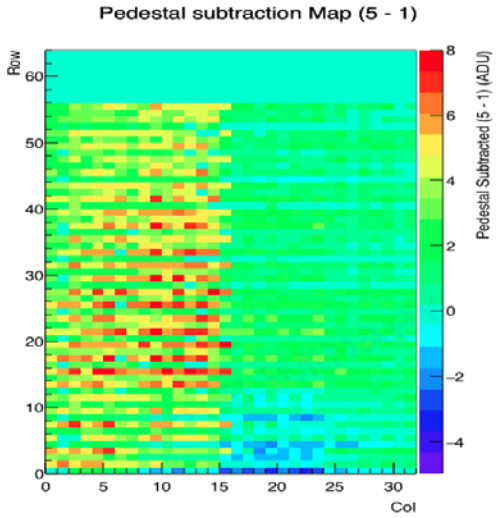
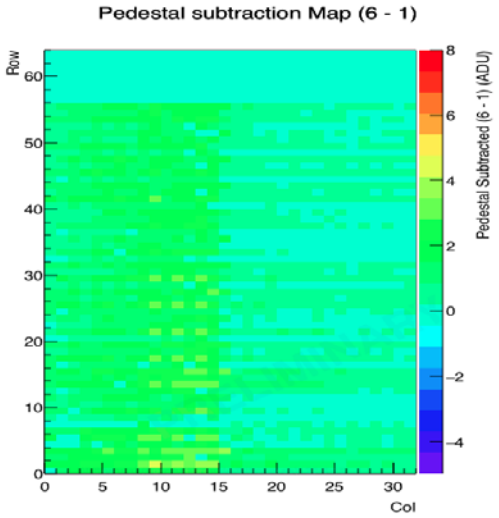
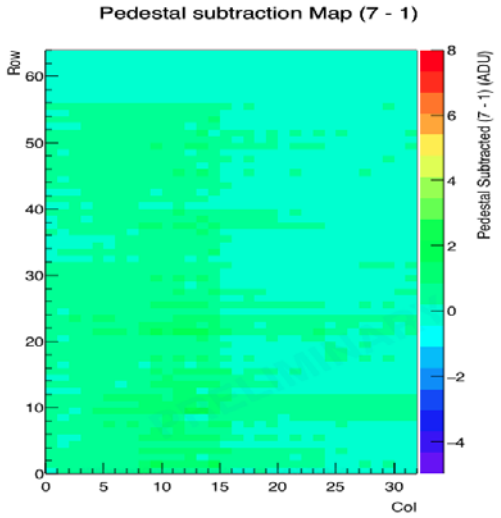
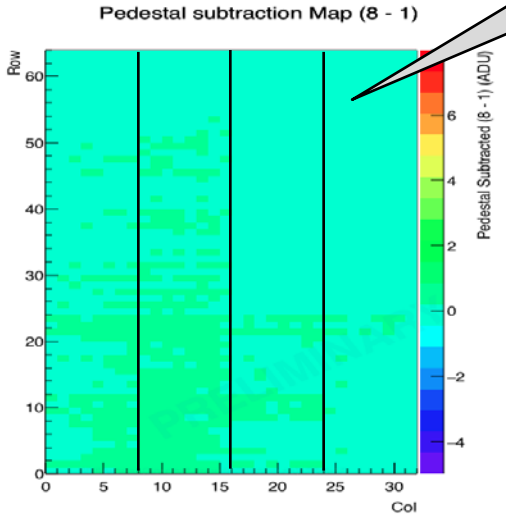
Pedestal Variation: Frame after Gated Mode – Reference Frame





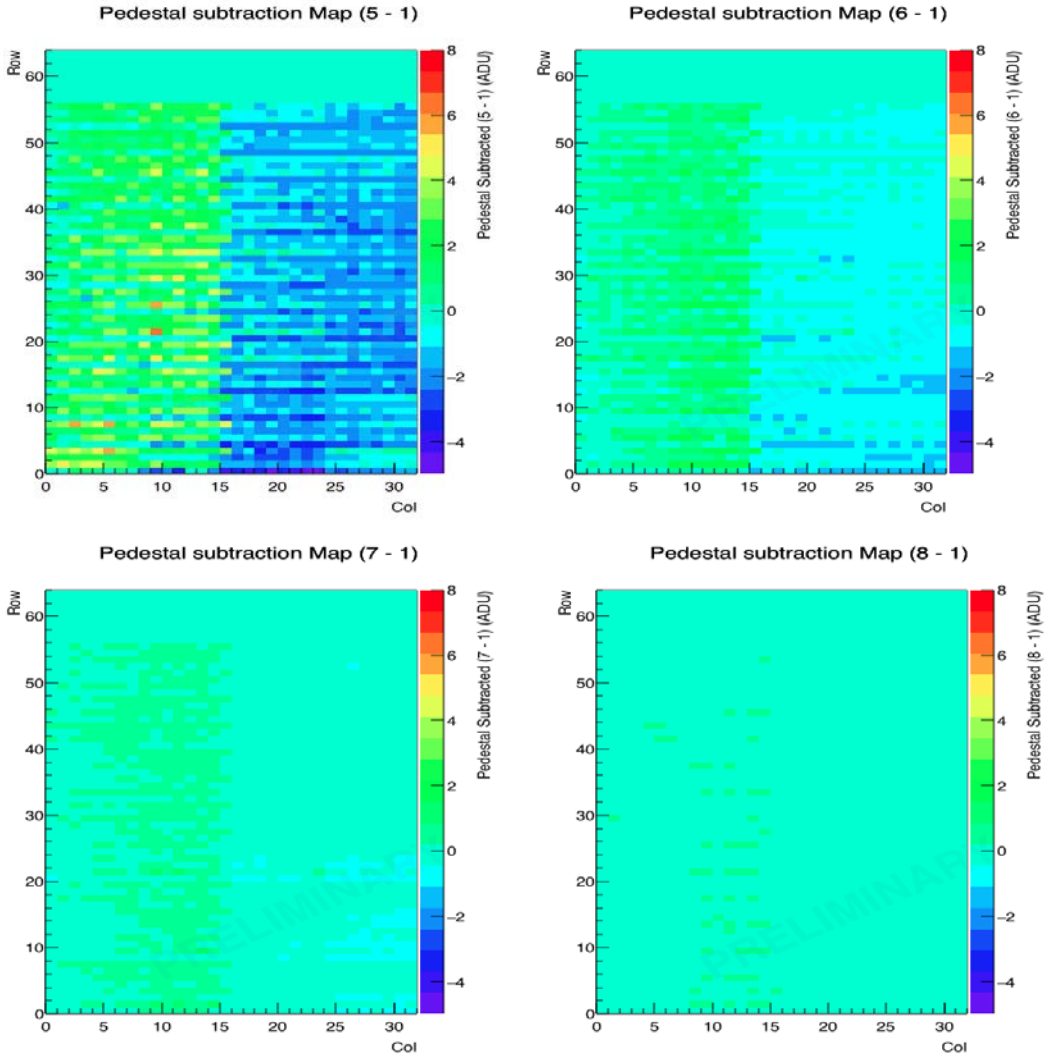




Pedestal variation after common mode correction.

DCD Column Pair
32 channels

Pedestal Variation: Frame after Gated Mode – Reference Frame

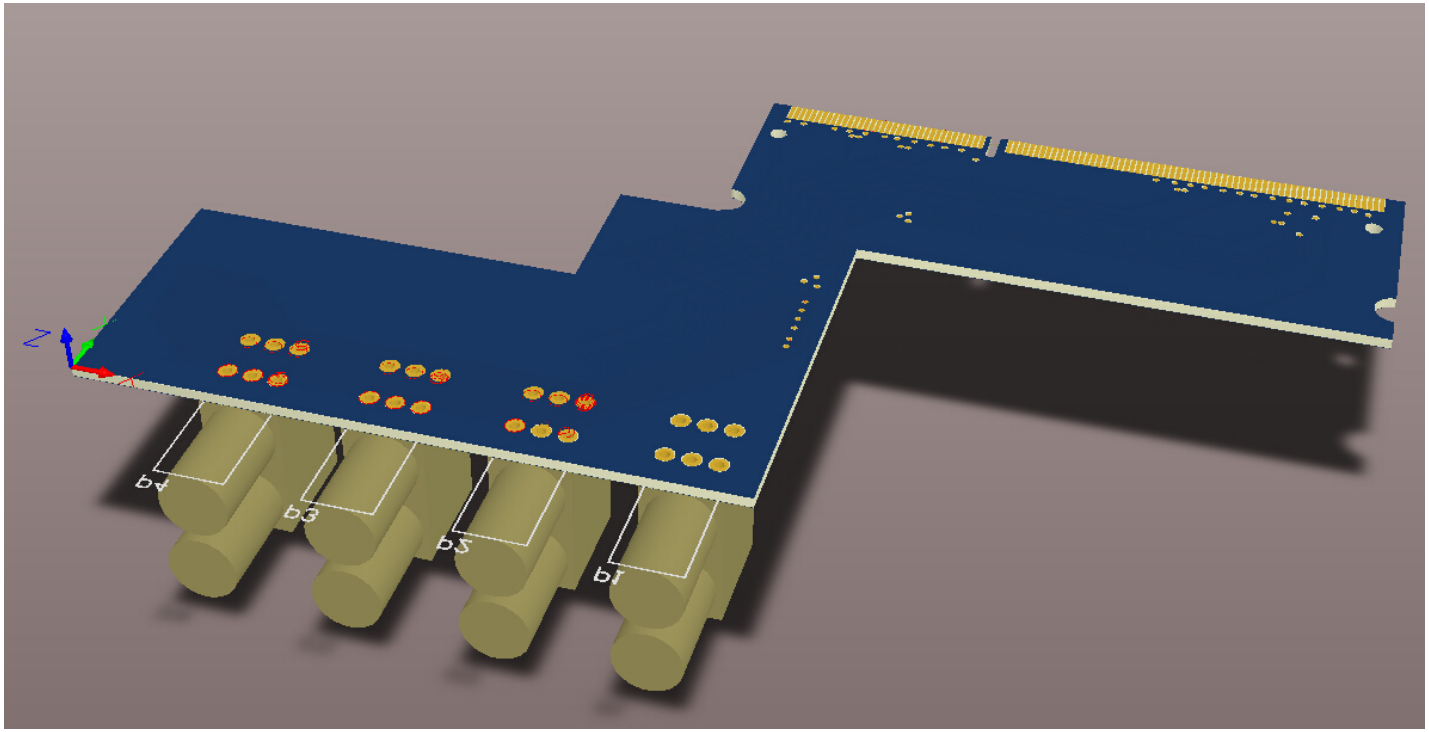


Pedestal variation with common mode filter.

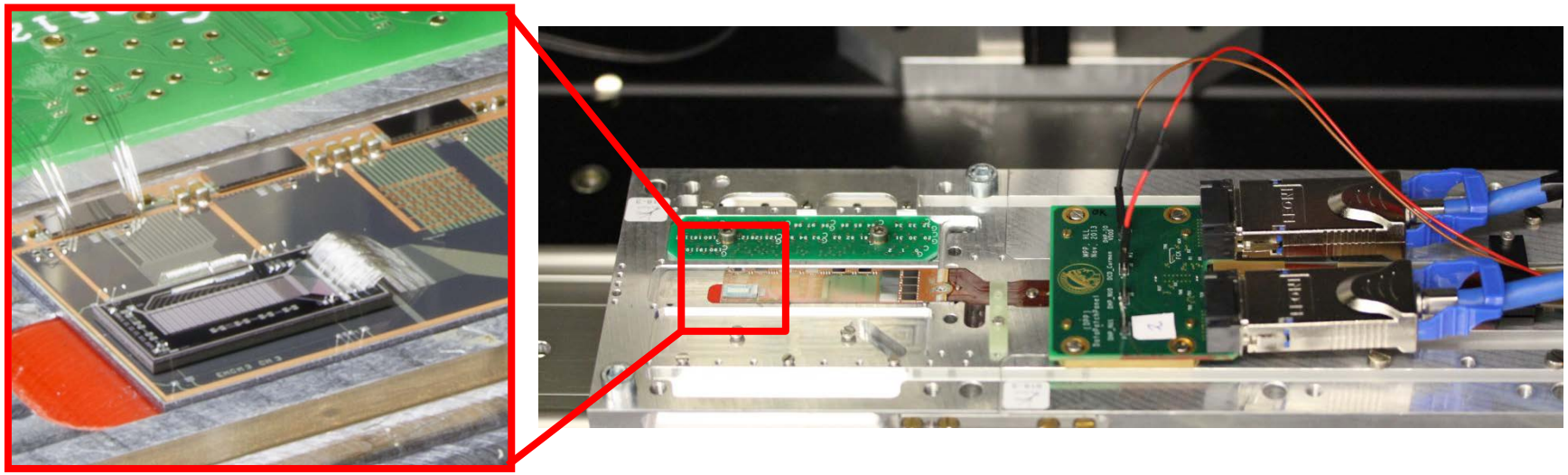
Test system – Gate Mode Testing with DHE

Adapter board in preparation:

- Allows the use of external pulse generator for the Veto signal
- Lead time ~ 2 weeks



EMCM W18-3, small PXD6 matrix



- EMCM W18-3 can be used to test the Gate Mode as soon as the DHE supports it
- Characterization of small DEPFET matrix is ongoing
- SW outputs can be probed on the test board next to the SW

Summary

- **Impact of the Gated Mode: we can save minimum 80 % of the events which would have been discarded due to noisy bunches**
  - Even more since the read-out directions for the two layers are different
- **Assessment on the timing:**
  - Transition time into the Gated Mode and back to normal SW operation takes between 70ns and 700ns, depending on the way we operate the system (with or without read-out)
  - After the Gate Mode there is a time of pedestal variations respectively pedestal shift. It seems to be related to the structure of the DCDPP (column pair with 32 channels) and depends probably on capacitance of the PXD module too
  - The impact of especially a larger Clear capacitance and different Power Delivery Network (Kapton+long cables) will be studied on the EMCM and PXD9-pilot modules
- **Testing**
  - Functional verification of the ASICs (DHPT, SW) done
  - System test in preparation: DHE integration will take approx. 2-3 weeks, then EMCM setup is ready to do Gate Mode measurements
  - But: if there are problems seen in the system test which can be addressed to one ASIC, the submission date may be rescheduled

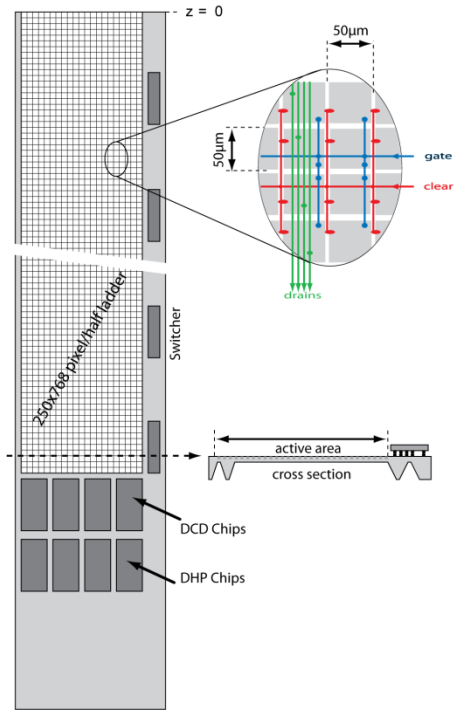
Thank you for your attention!

Gated Mode - System Aspects

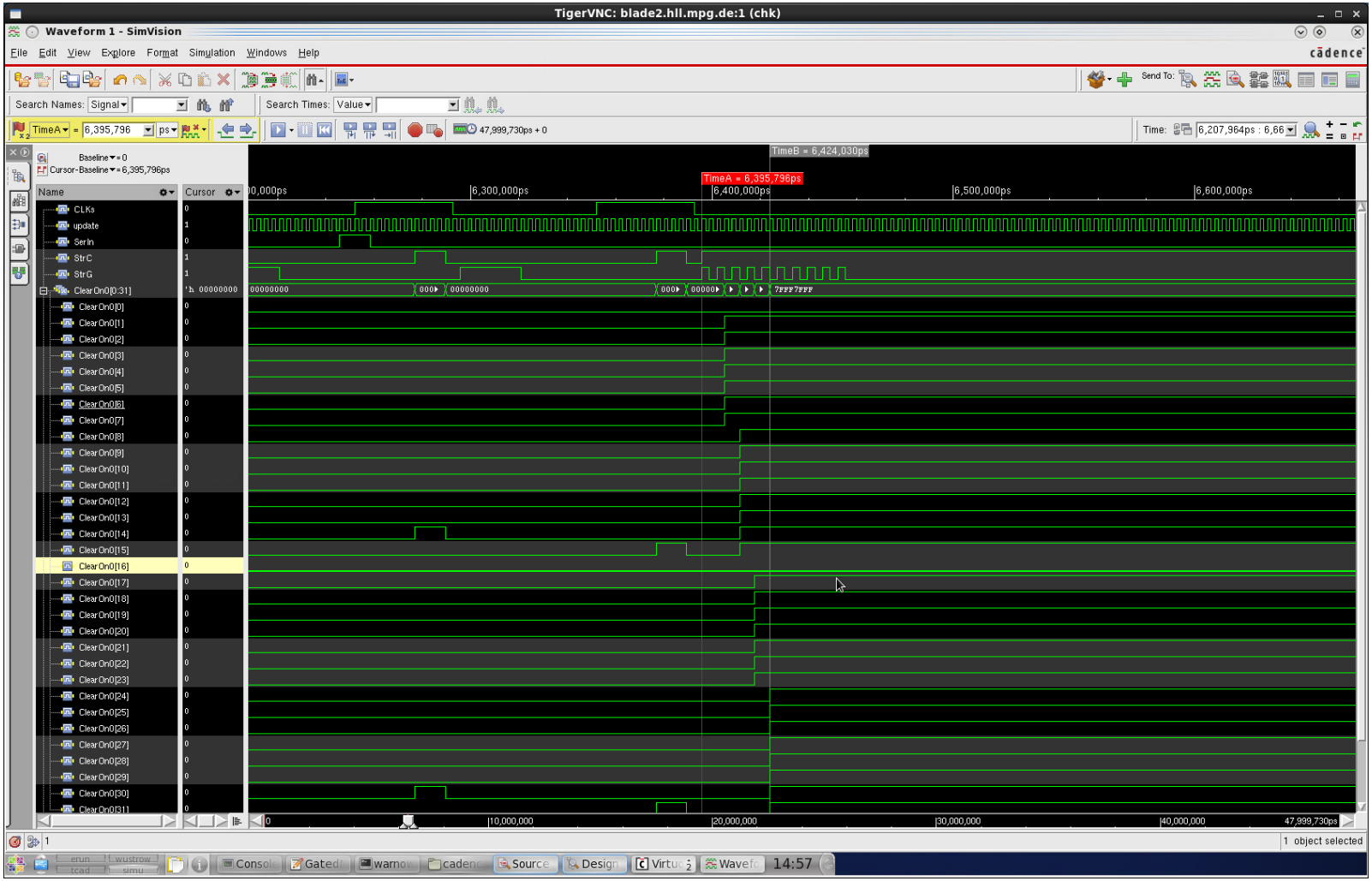
- clear capacitance for the large matrix compared to the PXD6 prototype used on Hybrid 4.1.11
  - Clear capacitance Large matrix: approx. 26nF (small matrix: 0.2nF)
- additional power consumption (ΔVclear:=15V, tcycl=10µs): 0.36W /half ladder
- averaged current into the clear capacitance: 30mA

→ additional coupling capacitors placed: in total 2 x 200nF (20V)

→ Tests with large PXD9 module and close to final ASICs needed to confirm metal routing (e.g. qty. of caps)



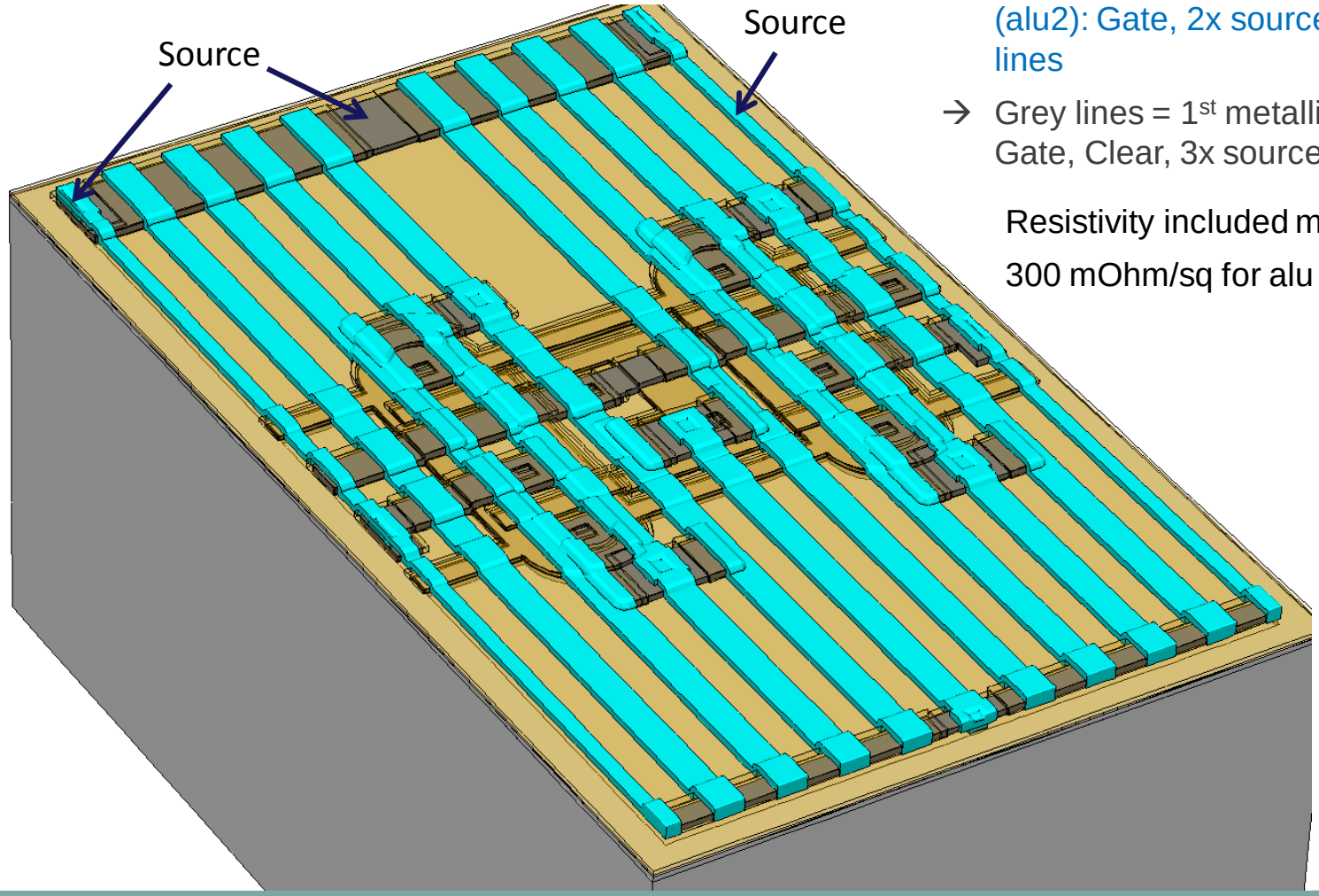
Gate Mode without Read-out – Verilog Simulation



Gated Mode NO read out – 30 ns to switch into gated mode

From RC Extraction to Full Matrix Layout

- 3D model of the PXD9 design to extract the parasitic capacitance

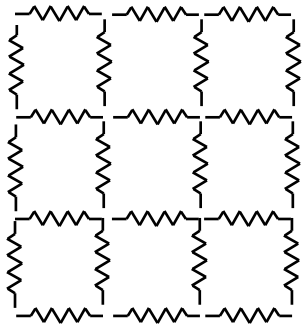


→ Light blue lines = 2nd metallization (alu2): Gate, 2x source, 8 drain lines

→ Grey lines = 1st metallization (alu1): Gate, Clear, 3x source, 4 drains

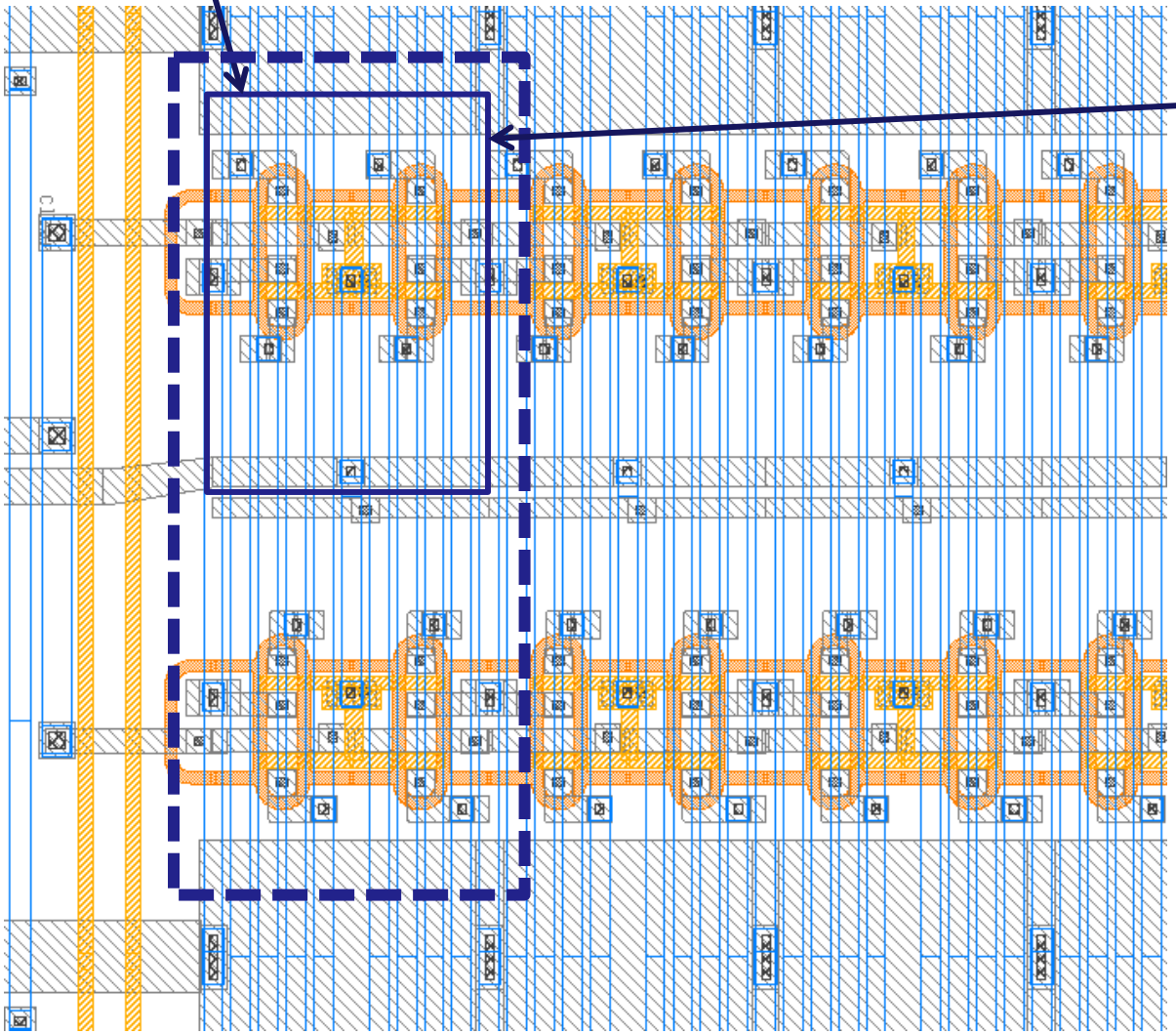
Resistivity included manually:

300 mOhm/sq for alu



From RC Extraction to One Electrical Row

Cell for parasitic extraction

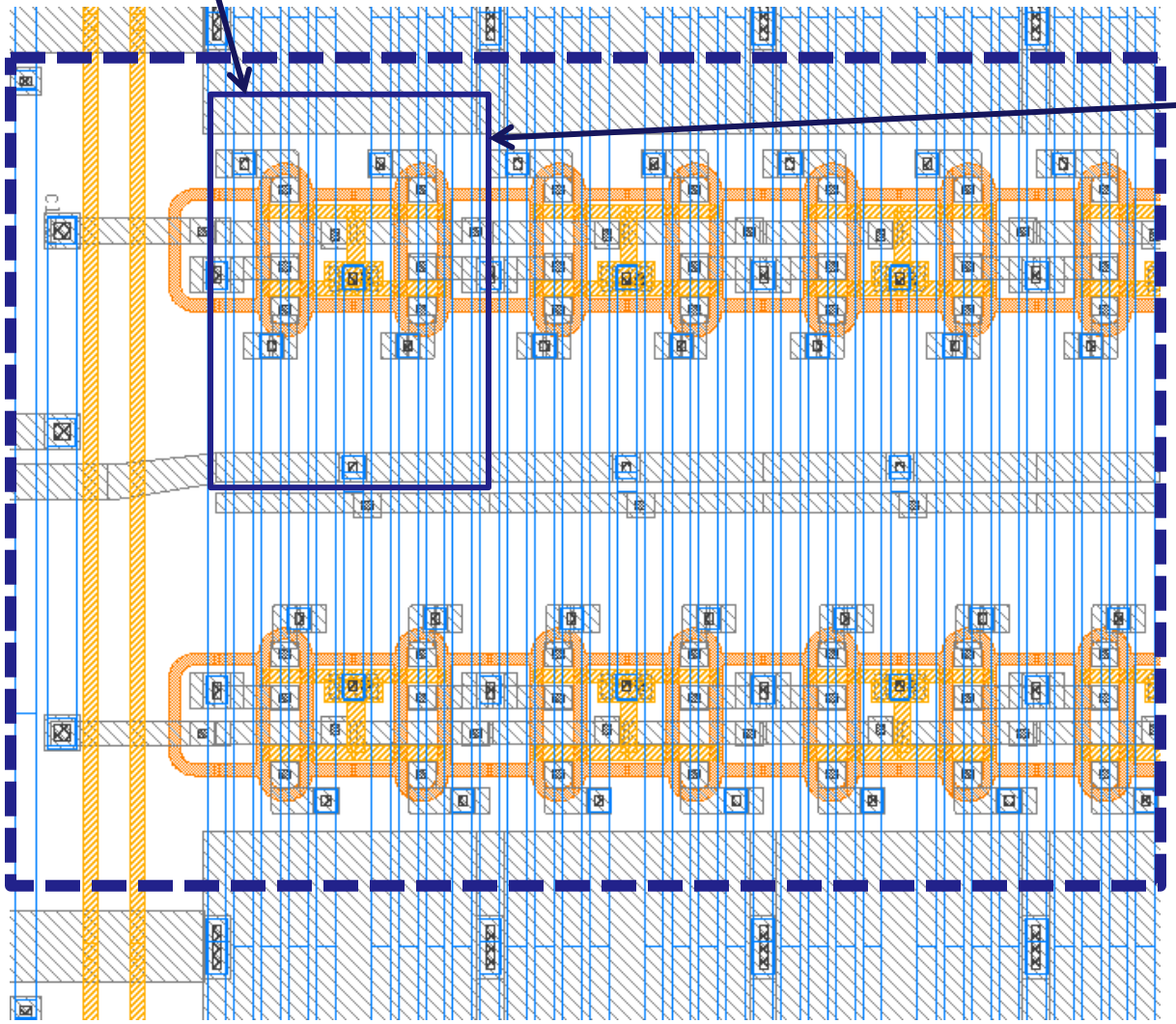


For 4 Pixels
C Clear = 542fF

For 8 Pixels:
C Clear = 1.09pf

Block of one electrical DEPFET row

From RC Extraction to One Electrical Row



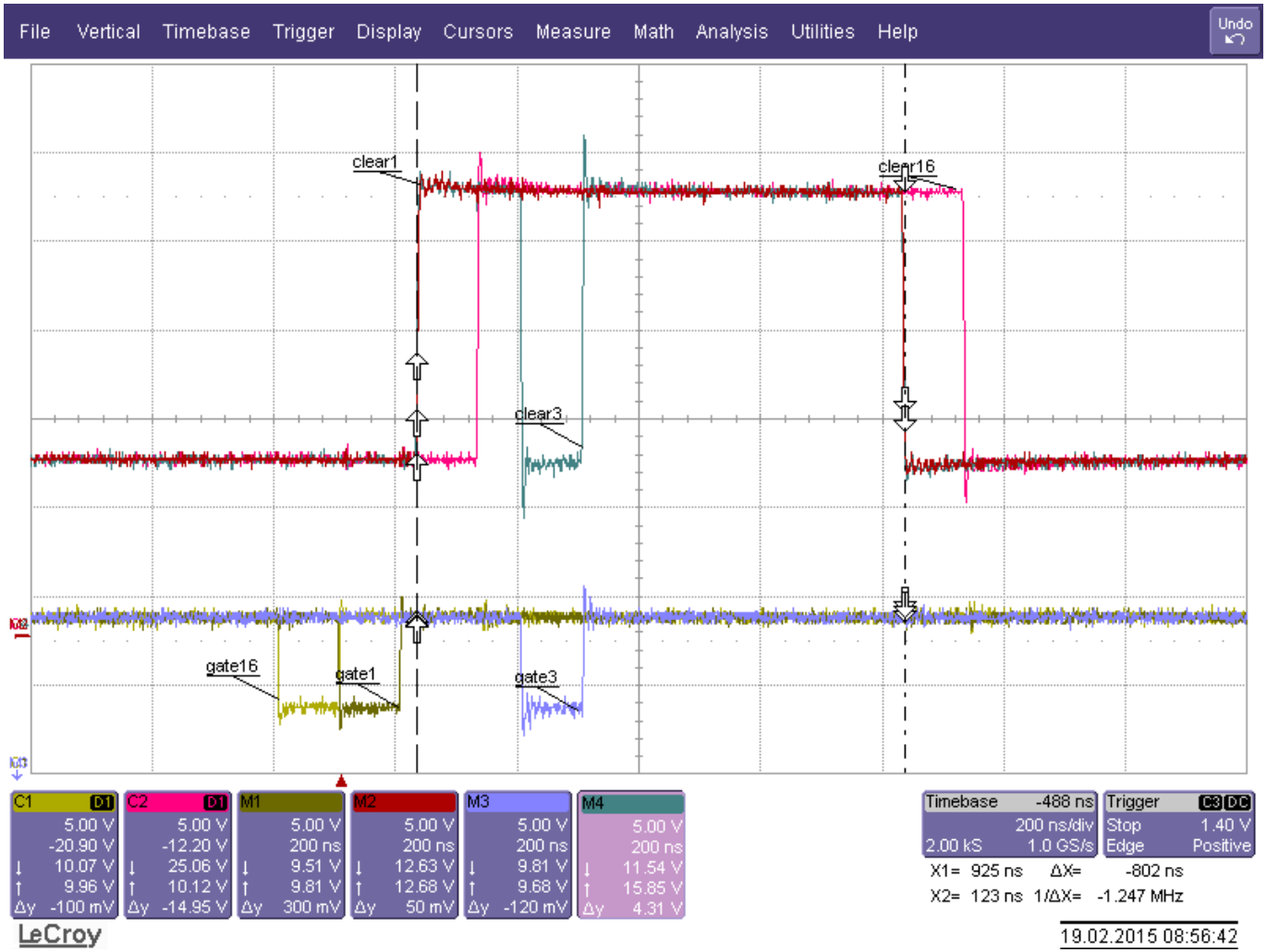
For 4 Pixels
C Clear = 542fF

For 8 Pixels:
C Clear = 1.09pf

For 1 electrical row
C Clear = 1.09pF *125 = 135pF
C Gate = 99pF
C Drain = 29pF

Block of one electrical DEPFET row

Gated mode with read-out: Switcher output



Gated mode without read-out: Switcher output