**General remarks**

For coordination reasons, it would be helpful if the management could present one, agreed-upon schedule.

**Specific recommendations for each ASIC**

**Switcher**

**General comments:**

* Generally in good shape:
  + Concept proven
  + Performance: only concern is speed of Clear signal
* Required changes look modest
* Concern regarding radiation hardness of the HV transistors
* We endorse performing detailed tests of the Gated Mode operation

**Specific charged items:**

1. **The maturity of the chip design**

**Quite mature.**

1. **Completeness and quality of documentation.**

**Comprehensive Specification document lacking. Reference Manual is a good start, needs to be expanded to include performance requirements.**

**Answer:**

**Performance requirements:**

**Size: Should fit to the bump pad pattern – size of the chip may vary**

**Number of channels: 32**

**Radiation tolerance: 20 MRad**

**Power consumption: AC power consumption should dominate**

**Switching speed: clear rise times should be about 10ns – 20ns for 120pF (presently ~20ns)**

**Voltage ranges: Amplitude up to 20V, High level: up to 30V (for clear), Low level: down to -10V (for gate)**

1. **Status of performance tests (stand alone and on system level).**

**Additional Gated Mode tests needed. Further radiation hardness testing likewise needed.**

**Answer:**

**Radiation tests have been done in 2014. Gated mode tests are ongoing.**

1. **Known problems and mitigation/correction plans.**

**Main issue understood and plausible corrective plan proposed. Needs to be implemented.**

1. **Missing measurements and tests.**

**Addressed above.**

1. **Work plan (responsibilities, milestones).**

**Recommend clarifying test program leading to ASIC revision. Designer needs to clarify scope of modification, which will drive the schedule.**

**Answer:**

**Changes needed:**

1. **Output driver will be resized to allow clear pulse of ~20ns width in 120pF capacitance.**
2. **Separated control of the termination resistance for serial input (should be always on) and for the other fast inputs.**
3. **Bump bond pads will be resized.**
4. **Schedule for next submissions.**

**June submission plausible, if consistent with above estimates.**

**Answer:**

**Submission is planned on 24th August**

1. **QA strategy.**

**General test plan looks reasonable. The committee expresses concern regarding the proposed ASIC modifications to support multiplexed testing (additional HV-LV conversion, output multiplexing).**

**Answer: Multiplexer testing will not be implemented**

Recommendations:

* End users should review Reference Manual for completeness
  + Are pin table listings sufficient? – **Answer: to my knowledge yes**
  + Interface control description adequate? – **Answer: to my knowledge yes**
* Recommend creating Hardware Description Language description of Gating functionality

**Answer: Software model of the gating functionality has been created instead.**

* Concern regarding radiation hardness of the HV transistors

**Answer: Radiation tests with x-rays (21 MRad) have been done. Switcher uses MOSFET transistors with thin oxide. Similar transistors in the same technology have been irradiated with neutrons and protons to very high doses (2x 1e15neq/cm2) and work well.**

* We endorse performing detailed tests of the Gated Mode operation

**Answer: Gated mode tests are ongoing, final tests will be done when the large matrices are available.**

* We recommend investigating long-term burn-in/stress testing of HV operation

**Answer: will be done. Comment: The design uses the standard transistors with the standard layout done by the foundry AMS. Such transistors are well characterized for a long term operation.**

**DCD**

**General comments:**

* Basic architecture looks well suited to the requirements
* The committee expresses serious concerns about the details of the ADC implementation
  + Unclear if problems observed are sensitivities to process parameters
  + Further design work needed

**Specific charged items:**

1. **The maturity of the chip design.**

**We forsee significant additional design effort to address concerns regarding the ADC implementation**

**Answer:**

**Mismatch between the transconductors in the memory cell and the comparator, which can cause the long codes cannot be directly measured.**

**In simulation, the random mismatch is not large enough to explain long codes. This is expected, the transistors have been (properly) dimensioned to assure a small enough offset if the random mismatch is the only mismatch source.**

**However, the transistors in different transconductors have a different orientation in layout. The random mismatch formula is derived from measurements on the devices with the same orientation. Therefore it can be expected that the mismatch in reality is larger. (We have observed that matching depends on transistor orientation in various technologies.) As already mentioned, large mismatch can explain the long codes.**

**Layout change is simple; the transistors will be flipped when needed to assure the same orientation. Additionally, three important transistors will be resized.**

**Mismatch between the transconductors in the memory cell and the comparator cannot be measured directly. Instead this we have performed a set of measurements on the transconductor in the first memory cell for every ADC. Notice that in this case we have the equal orientation of the transistors for every measurement.**

**The measurement results agree with the simulation of the random mismatch.**

**Additional issue:**

**We have also observed that the bias current depends on the position of the ADC in the column. This can be addressed to the voltage drop in VDDA line. The PMOS current in the ADCs which are far from the power pads is lower.**

**We have expected this problem. The present DCD version has the separated bias line for lower 8 and the upper 8 ADCs. Such a bias circuit is, however, not working as expected from two reasons:**

1. **The segmentation should be done so that e.g. 4 lower and 12 upper ADCs have a common bias – not 8/8 - the voltage drop is not linear.**
2. **The diode connected transistors used for two bias lines have large mismatch and their drain currents are produced from one bias DAC. The mismatch causes too different bias setting s for the ADC groups. The problem can be solved by adding additional bais DACs.**

**The variation of the PMOS bias currents can lead to systematic threshold offset of the comparators. This in combination with transistor mismatch can lead to long codes.**

**Summary: We will do smaller changes in the layout of the tranconductor – three transistors will be resized and the transistor orientation will be made equal in all cells.**

**Additionally, we will add three more bias DACs and to reduce the effect of voltage drops.**

1. **Completeness and quality of documentation.**

**A comprehensive Specification Document is lacking. Reference Manual is a good start, needs to be expanded to include performance requirements.**

**Answer: Performance requirements have been written.**

1. **Status of performance tests (stand alone and on system level).**

**Strongly recommend further testing to understand variety of pathologies observed. Further ASIC/channel testing statistics are needed.**

**Answer: ADCs have been extensively tested on fresh- and irradiated chips. Additionally DC-characteristics measurements of the transconductors have been done to estimate the mismatch and the voltage drops.**

1. **Known problems and mitigation/correction plans.**

**Matching of observation with simulation is mandatory.**

**Answer: Observations and simulations, to my opinion, match.**

1. **Missing measurements and tests.**

**More an issue of understanding results observed that missing measurements. Encourage further, cross-checked analyses.**

1. **Work plan (responsibilities, milestones).**

**Highly important that before next submission these problems are fully understood, to avoid excessive risk in resubmission.**

**Answer: The problems are to my opinion understood.**

1. **Schedule for next submissions.**

**Given the above concerns, a February submission seems very aggressive. Items above must be resolved prior to submission. Verifying Monte Carlo spreads will likely take time, and sufficient time should be allocated.**

**Answer: Monte Carlo simulations have been done.**

1. **QA strategy.**

**Generally looks OK.**

Recommendations:

* Better understanding of noise performance and instabilities needed

**Answer: We have concentrated or effort to understand the instabilities, they are mostly related to instable data transfer between DCD and DHP. It is caused by larger than expected capacitances of the data lines. Increase of the digital output driver current and decrease of the DHP input capacitance should fix the problem. Measured noise is to my knowledge within required values.**

* Consider an SEU test of the DCD

**Answer: Still to be done, however, to my opinion the DCD, designed in 180nm technology (1.8V power supply, large node capacitances), should be less susceptible to SEU than the DHP designed in 65nm technology (1.2V power supply, smaller node capacitances). Measurements performed on DHP show very low SEU rate.**

* More work is needed prior to a next submission. Submission schedule should be driven by the readiness to address the above issues.
* Careful consideration should be given to assess risk versus rewards of the changes proposed.

**Answer: The changes will be minimal and to my opinion bring lowest possible risk.**

**DHP**

**General comments:**

* Specifications still not concisely presented
* Overall architecture looks very sound
* Cannot put all effort on the ASIC side. System engineering of cabling and interconnects, and an agreed-upon model for output load is needed.
* Complexity makes testing difficult

**Specific charged items:**

1. **The maturity of the chip design.**

**Data flow, PLL, synthesized logic are very mature. Remaining concern is in the verification of the high-speed interfaces.**

1. **Completeness and quality of documentation.**

**Specifications for output loads and timing are needed for signals in Table 1 of the Manual. For such a complex device, a more comprehensive document many be required.**

1. **Status of performance tests (stand alone and on system level).**

**Most IP Block / Task items test results well documented. Remaining issues well presented.**

1. **Known problems and mitigation/correction plans.**

**Proposed further testing seems adequate.**

1. **Missing measurements and tests.**

**Finer step TID testing, SEU testing. Channel masking and Overflow handling tests self-identified.**

1. **Work plan (responsibilities, milestones).**

**Not clear who is doing what to provide further testing and by when. A detailed model of the cabling needed to complete output driver redesign.**

1. **Schedule for next submissions.**

**June submission seems plausible given proposed testing schedule. A rigorous internal review of the proposed changes should be held prior to release for submission.**

1. **QA strategy.**

**Proposed quality control plan seems adequate.**

Recommendations:

* Characterize the electrical properties of the external interconnects and cables.