ASIC Submission Status

DHPT: submitted end of August
(see Carlos M. report Trieste)
100 dies

Important: height of ASICs must be < 400 µm incl. BGrid

Ivan Peric's Email:

Switcher: submitted last week 35 (end of August)
changes according to DCD document (mid August)
100 dies, delivery in December 2015
bumping to be ordered

DCD: Engineering Run decided (faster, wafer level tests)
"conservative" design (see DCD document) ongoing
"optimized" design: increase of transistor size
submission beginning before B2GM