Static measurements of pilot run sensors

PXD Seevogh Meeting
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Outline

- Testing summary
- Yield after phase 1
- Yield after phase 2
- Yield after phase 3
- Conclusions and comments

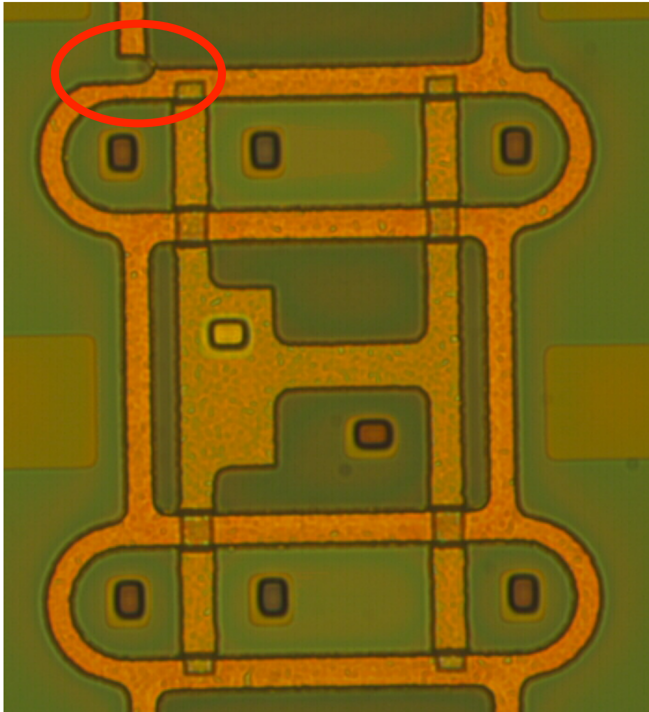
Summary of testing of PXD9 wafers

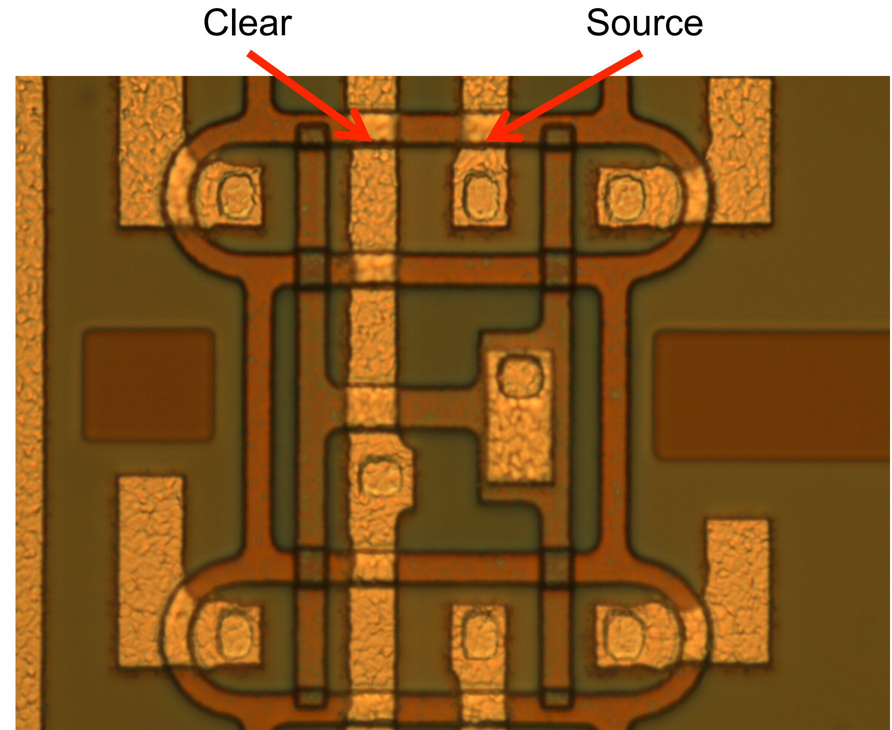
Hardware

Phase	Tests	Hardware
Phase 1: Tests after Al1	• Shorts between metal lines (Source and Clear routing) • Shorts between p+ and n+ implantations • Evaluation of the punch through voltage and characterization of test structures and double DEPFET structures	Probe station with limited HW capabilities
Phase 2: Tests after Al2	• Yield outcome of the half ladders (shorts between adjacent drain lines and discontinuities in drain lines). • Pedestal spread (typically from a set of 1000 pixels) • Threshold voltage (typically from a set of 1000 pixels)	Probe station equipped with Keithley 4200 SCS and switch system
Phase 3: Tests after Cu	• Final quality assurance after tests on the periphery of the half ladder. Possible to detect inter and intra level shorts and discontinuities in the routing lines.	High speed and position accuracy atg prober

Shorts in Al1, Al2 or Cu, found in these phases can be repaired.

Phase 1 tests summary



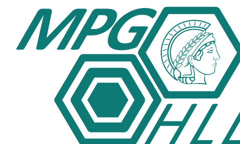


Phase 1a allows the detection of shorts (not easily distinguishable)

- between n+ and p+ implantations, caused by discontinuities in the poly-Si
- between two adjacent Al1 lines (Clear and Source)

Phase 1b allows for the detection of shorts between Clear Gate (poly1) and All Gate (poly2).
It is not possible to state the precise number of shorts detected, unless equal to one. Therefore, in some cases the yield is given as an interval.

Yield (%) after phase 1



	Phase 1a results			Phase 1b results		
	W30	W35	W36	W30	W35	W36
IF	100	100	100	< 98.9	< 98.9	98.4 – 99.4
OF1	100	100	100	**100**	< 98.9	98.9 – 99.4
OF2	100	100	100	99.4	98.9 – 99.4	99.4
OB1	100	100	**0**	< 98.9	**100**	99.4
OB2	100	**0**	100	99.4	98.9 – 99.4	98.9 – 99.4
IB	100	**0**	100	< 98.9	**100**	99.4

Yield calculation criteria:

- Phase 1a: A yield of 100% is assigned to healthy half ladders. In case the module does not pass the test, it is assigned a 0 yield.
- Phase 1b: The yield is calculated according to the formula $Y_{1b} = (1 – N_F/192)*100$, with N_F the number of shorts detected.

Phase 2 tests summary

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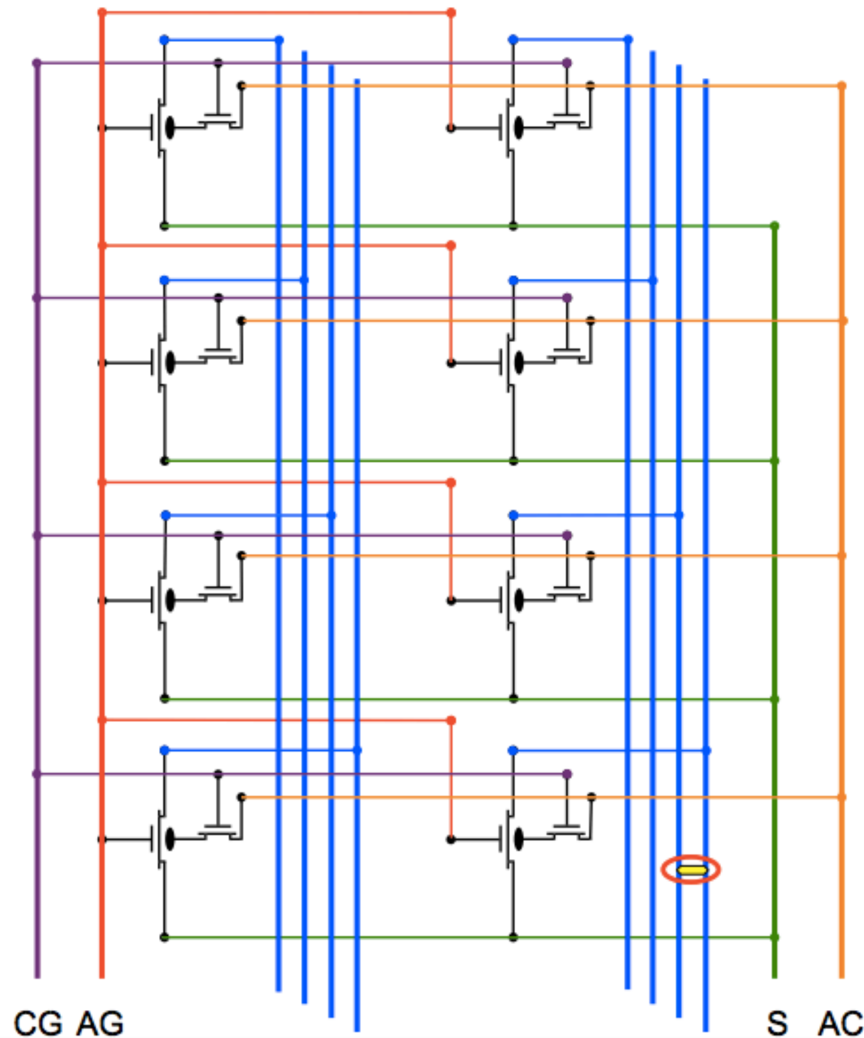
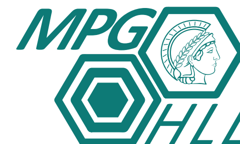


In this phase it is possible to determine in each half ladder the exact number of shorts among multiple drain lines using the equation $I_{shorts} = N_{shorts} * I_{1drain}$, while for discontinuities it is true $I_{disc} = 0$.

It must be noted that

- shorts can be repaired by rework on the full module or on a selected area
- The presence of a discontinuity does not imply a whole faulty line. In fact, in case the discontinuity is at the end of the half ladder, just the very last pixels located after the open will result disconnected.

Yield (%) after phase 2



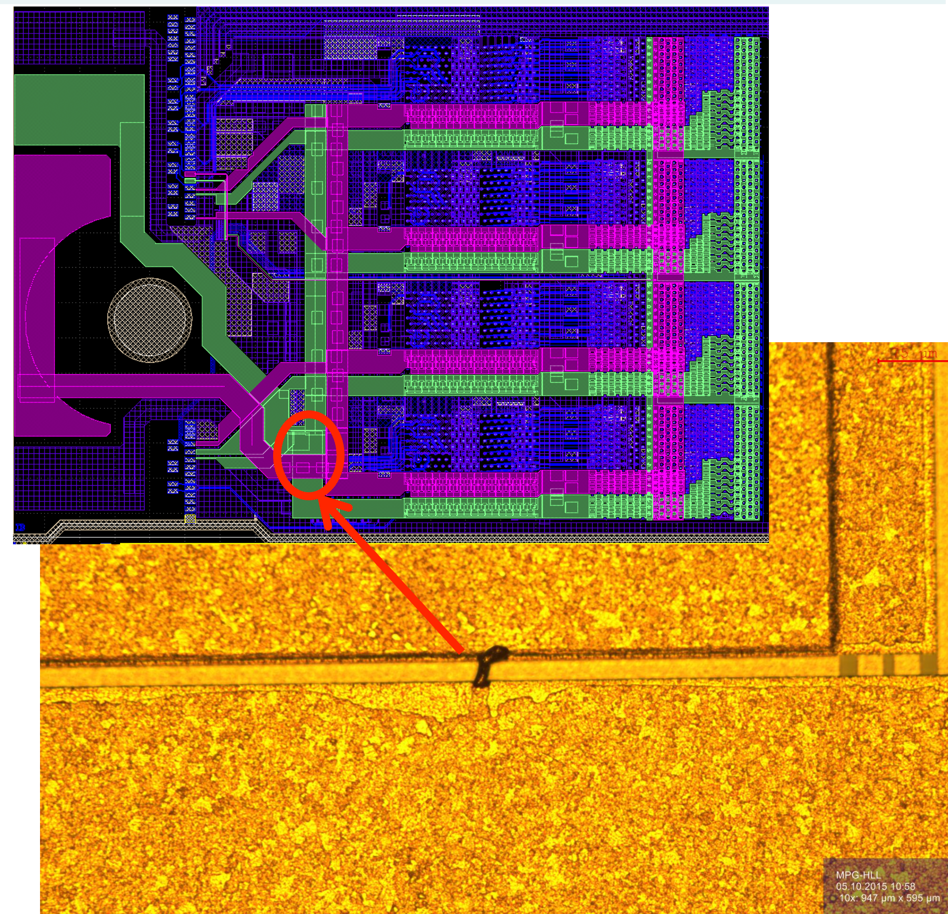
	Yield in %			After rework (expected)		
	W30	W35	W36	W30	W35	W36
IF	75	100	100	75	100	100
OF1	100	100	100	100	100	100
OF2	100	100	100	100	100	100
OB1	99.8	99.4	0	99.8	99.4	0
OB2	99.6	0	99.8	100	0	100
IB	100	0	100	100	0	100

- Matrices that resulted with a 0 yield after phase 1 were not considered for tests at phase 2.
- The yield is calculated using the formula: $Y_2 = (D - D_S)/10$, with D = 1000 and D_S the number of faulty drain lines.
- The half ladders OB2/W30 and OB2/36 were repaired and the expected yield (in pink) is reported in the table. (It was not possible to re-test the aforementioned modules, due to the fact that the rework was performed together with the etching of the half-ladder fan-out)

Yield (%) after phase 3

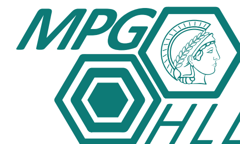
- In phase 3, inter and intra level shorts as well as discontinuities in the nets are detected.
- All the nets that are not in the matrix area, i.e. not connected to the pixels, are tested.

	W30	W35	W36
IF	0	100	100
OF1	100	100	100
OF2	100	100	100
OB1	100	100	100
OB2	100	100	100
IB	100	100	tbc



- During this phase only one type of fault, precisely a lethal fault, was detected and localized and identified.
- Module IB/W36 was found defective, due to a lethal short between two power lines. The short was identified and is scheduled to be repaired in the next days.

Final yield outcome and grading



Yield in %

	W30	W35	W36
IF	0	< 98.9	98.4 – 99.4
OF1	100	< 98.9	98.9 – 99.4
OF2	99.4	98.9 – 99.4	99.4
OB1	< 97.6	99.4	**0**
OB2	99.4	**0**	98.9 – 99.4
IB	< 98.9	**0**	99.4 (tbc)
Tot	**83.3**	**66.6**	**83.3** (tbc)

Wafer grading

W30	W35	W36
4	2	2
0	2	2
2	2	2
2	2	**4**
2	**4**	2
2	**4**	2 (tbc)

- The final yield is calculated taking into account the yield outcome of each phase, according to the formula: $Y_{final} = Y_{1a}*Y_{1b}*Y_2*Y_3$.
- The total yield is calculated per each wafer *taking into account the number of operative modules available per wafer*. It is not included any quality info whatsoever.
- **Grading legend: 0** = no faults; **1** = pixel level faults; **2** = row/column level faults; **3** = high impact faults; **4** = lethal faults; **5** = to be clarified.

Conclusions and comments

- After phase 1a it was found that 3 out of 18 half-ladders are affected by shorts between n+ and p+ implantations. In phase 1b it was found that only 3 out of 18 modules have no shorts between poly1 and poly2.
- After phase 2 it was found that 10/18 modules have no shorts/opens in the drain lines. One module (IF/W30) was reduced to a 75% usability by human mistake. Other 4 modules were found with a small amount of defects in the drain lines (< 0.6%). It was possible to repair two of these latter (OB2/W30 and OB2/W36).
- After phase 3, 1/18 module was found faulty, with no possibility of repair (IF/W30 – as a consequence of the fault in phase 2). Another module (IB/W36) was found faulty, the defect localized and identified. The module is currently under repair (with good chances of successful repair).
- An attempt of final grading is given. Though info/suggestions from tracking experts are very welcome for the finalization of quality assurance criteria.

Thank you for your attention!