JTAG Boudary Scan of the Belle II Pixel Vertex Detector

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33rd IMPRS Workshop
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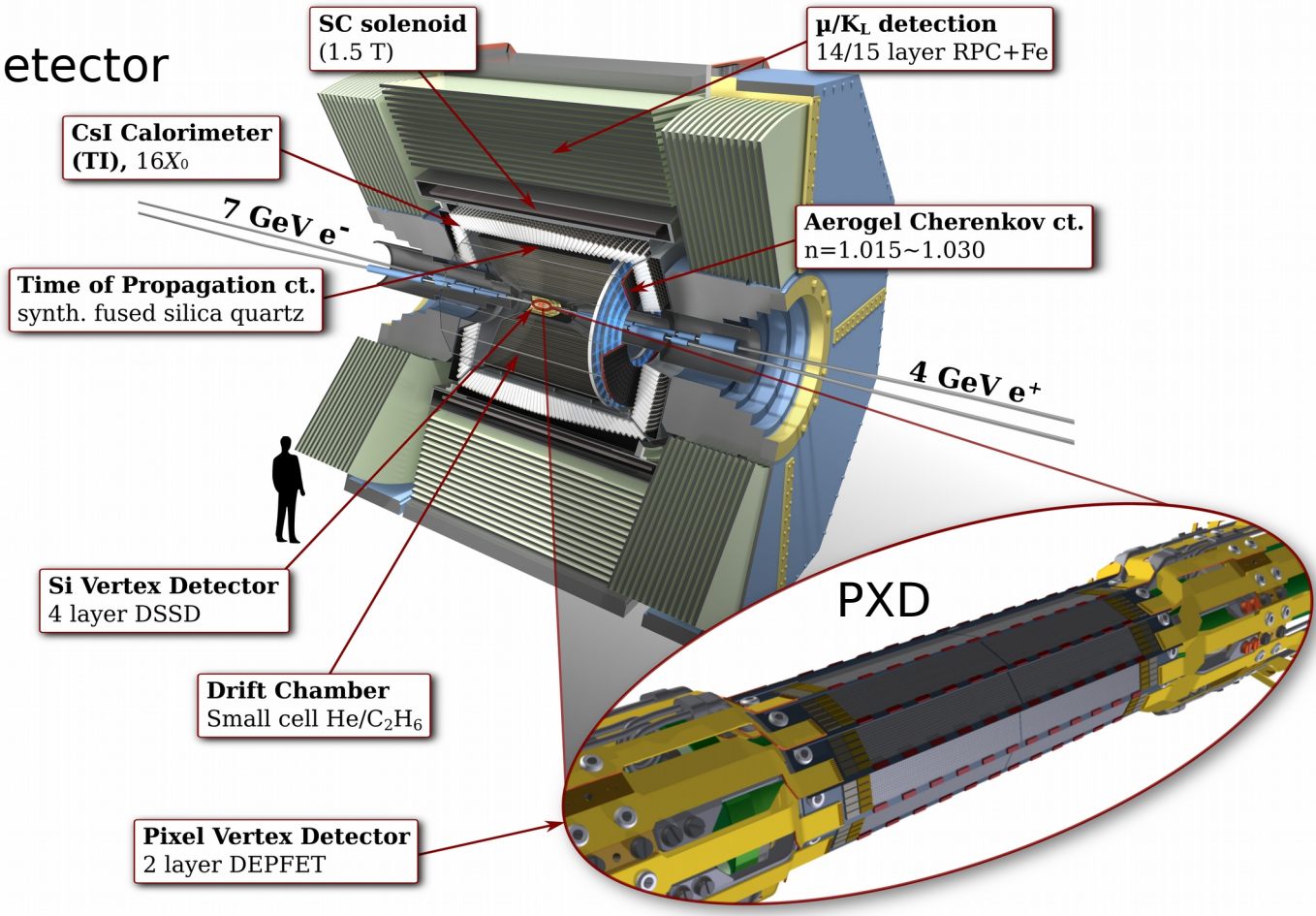
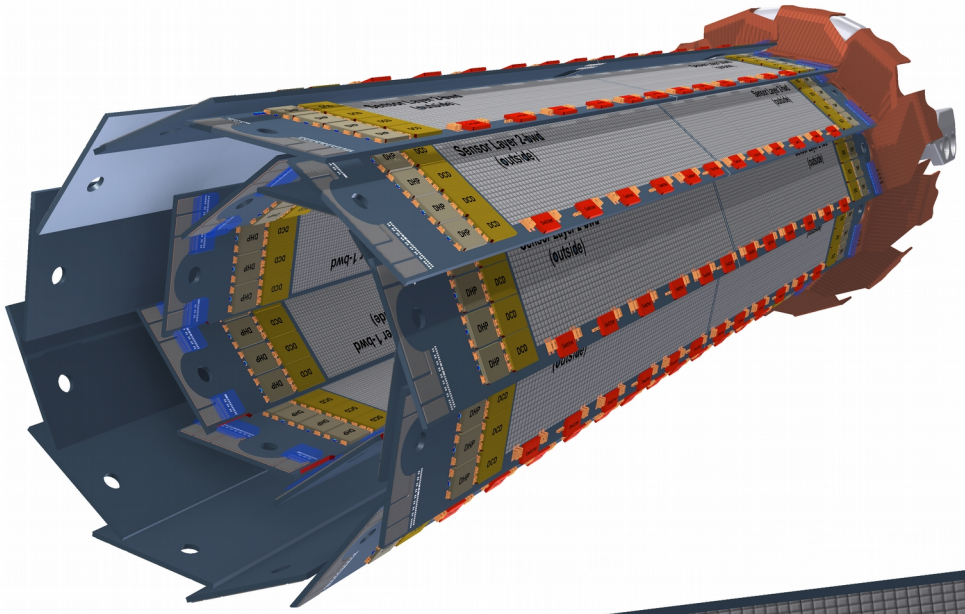
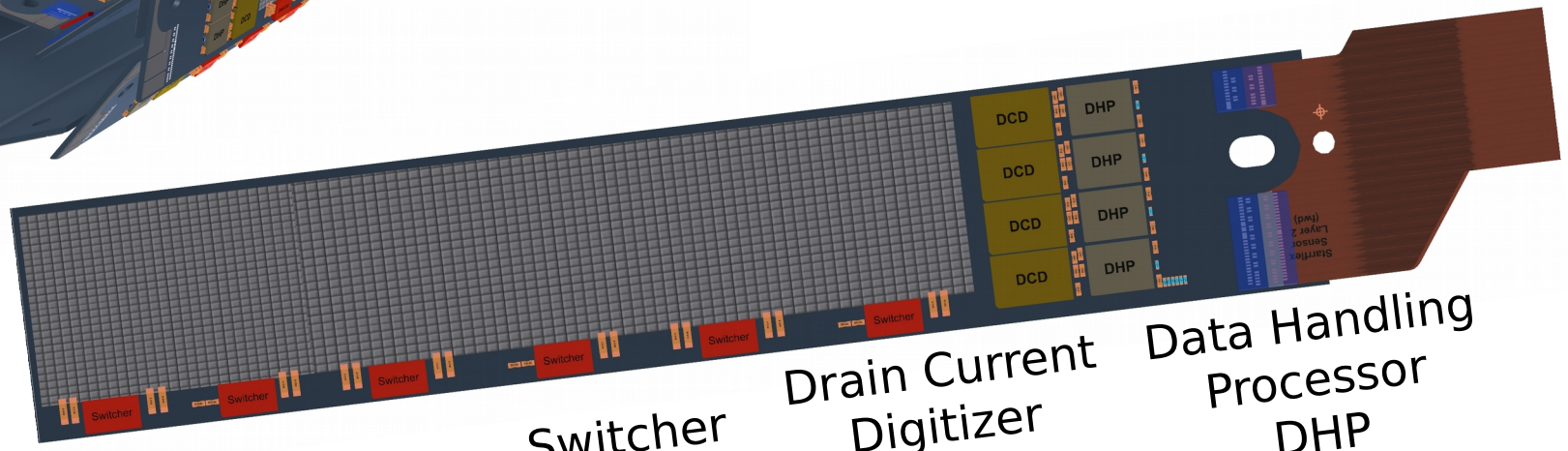
- multilayer particle detector
- at SuperKEKB electron-positron collider
- in Tsukuba, Japan
- Target luminosity: $8 \times 10^{35}\ cm^{-2}s^{-1}$



PXD



- two layers: 14 mm and 22 mm radii
- 20 ladders (40 modules)
  → 8 million pixels
- 20 µs readout time
- 560 ASICs for steering and readout



Switcher
Drain Current Digitizer
DCD
Data Handling Processor
DHP

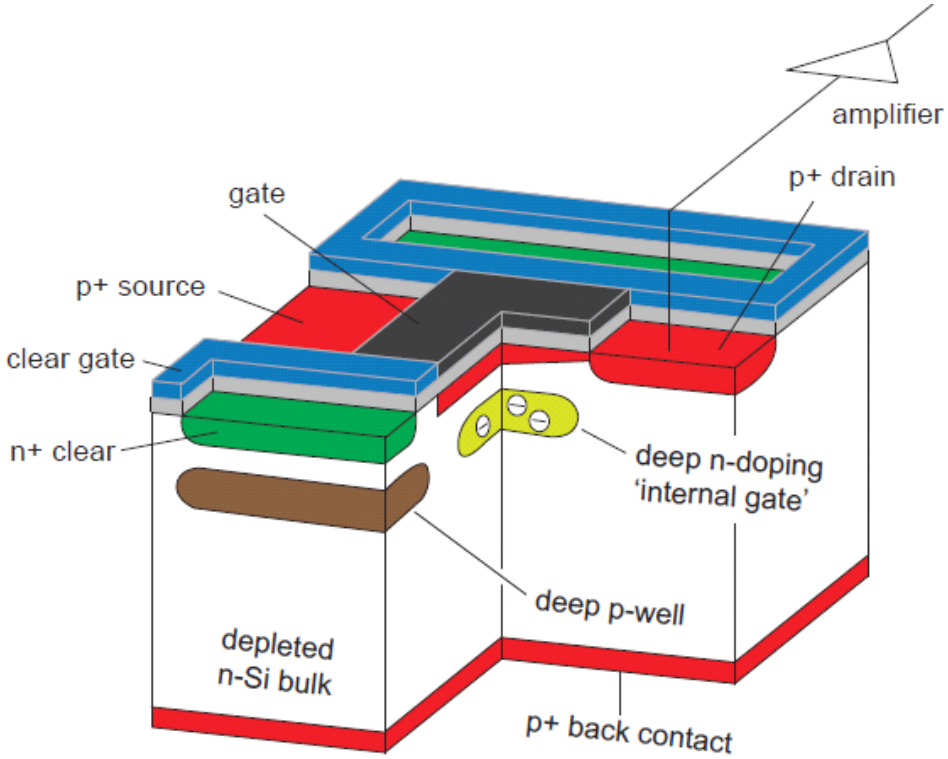
DEPFET

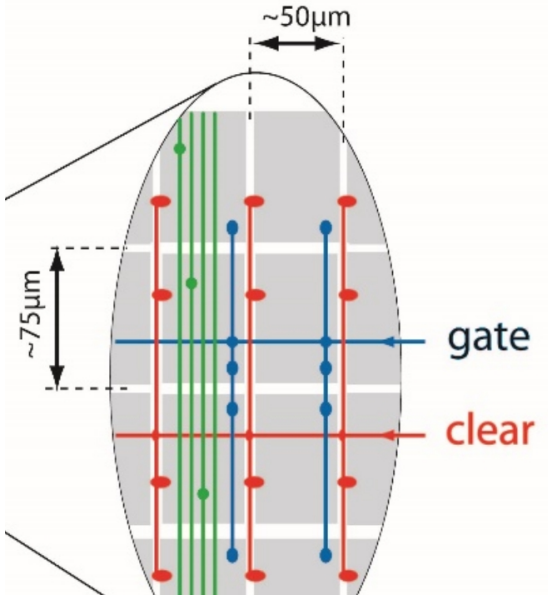
DEPleted p-channel Field Effect Transistor

charge in internal gate influences drain current

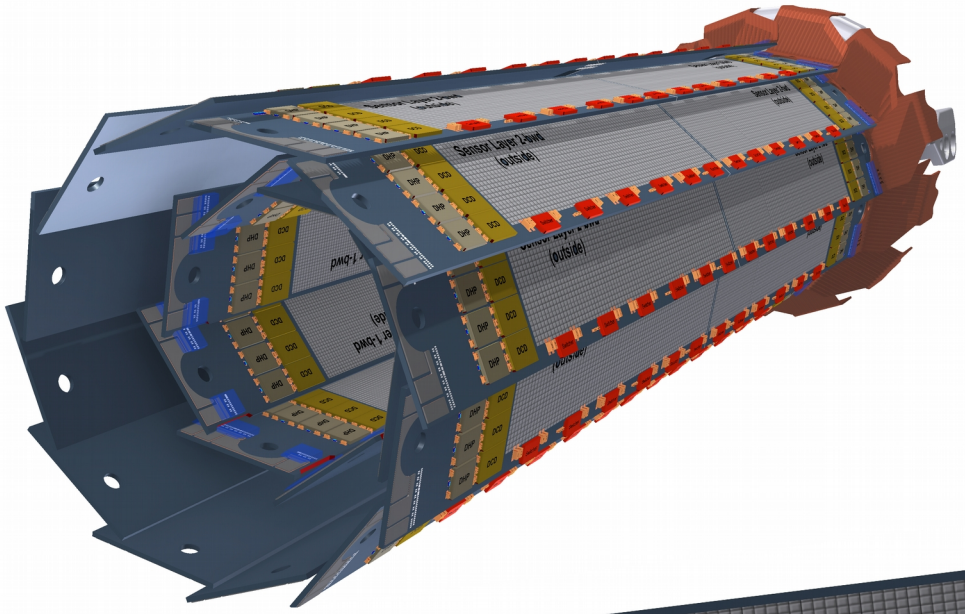
non-destructive readout

clear voltage to reset the detector





PXD



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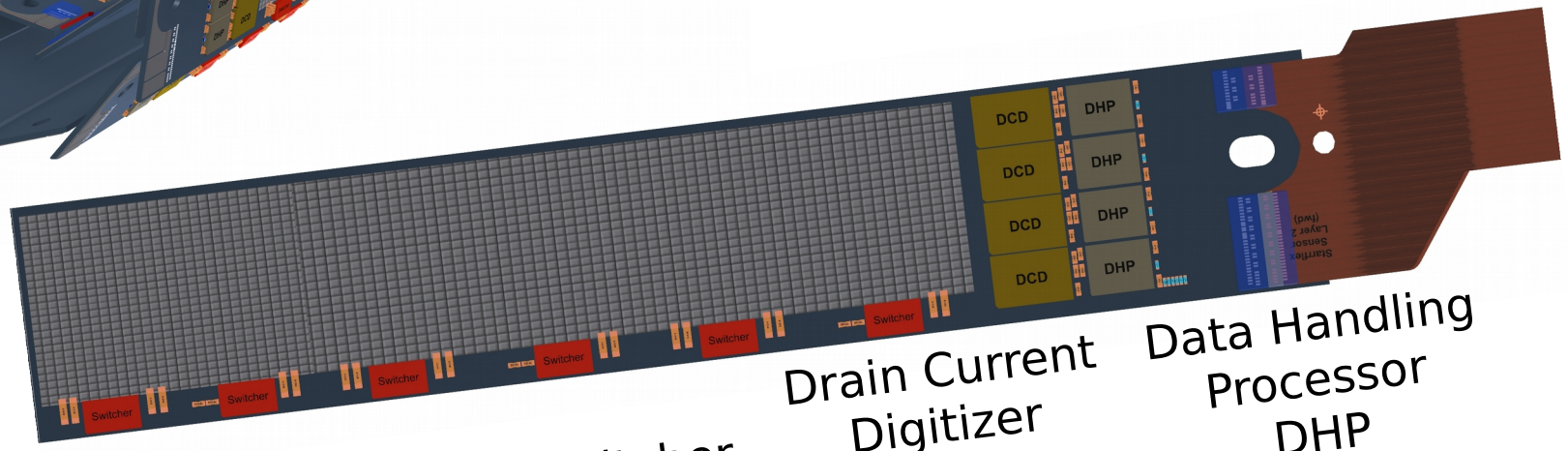


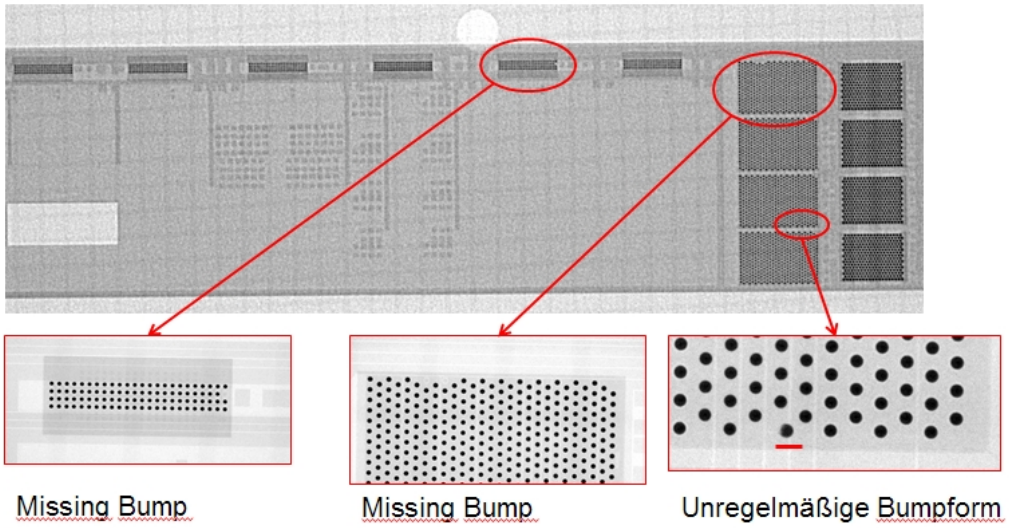
Switcher
Leitl

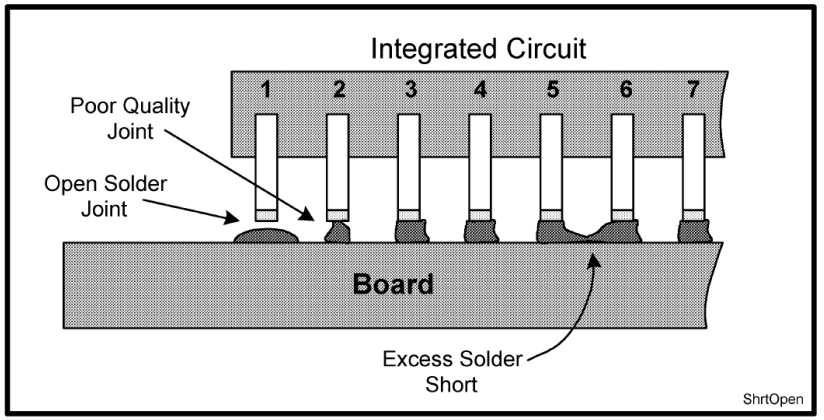
Drain Current
Digitizer
DCD

Data Handling
Processor
DHP

PXD bump bonds

X-Ray W17-4



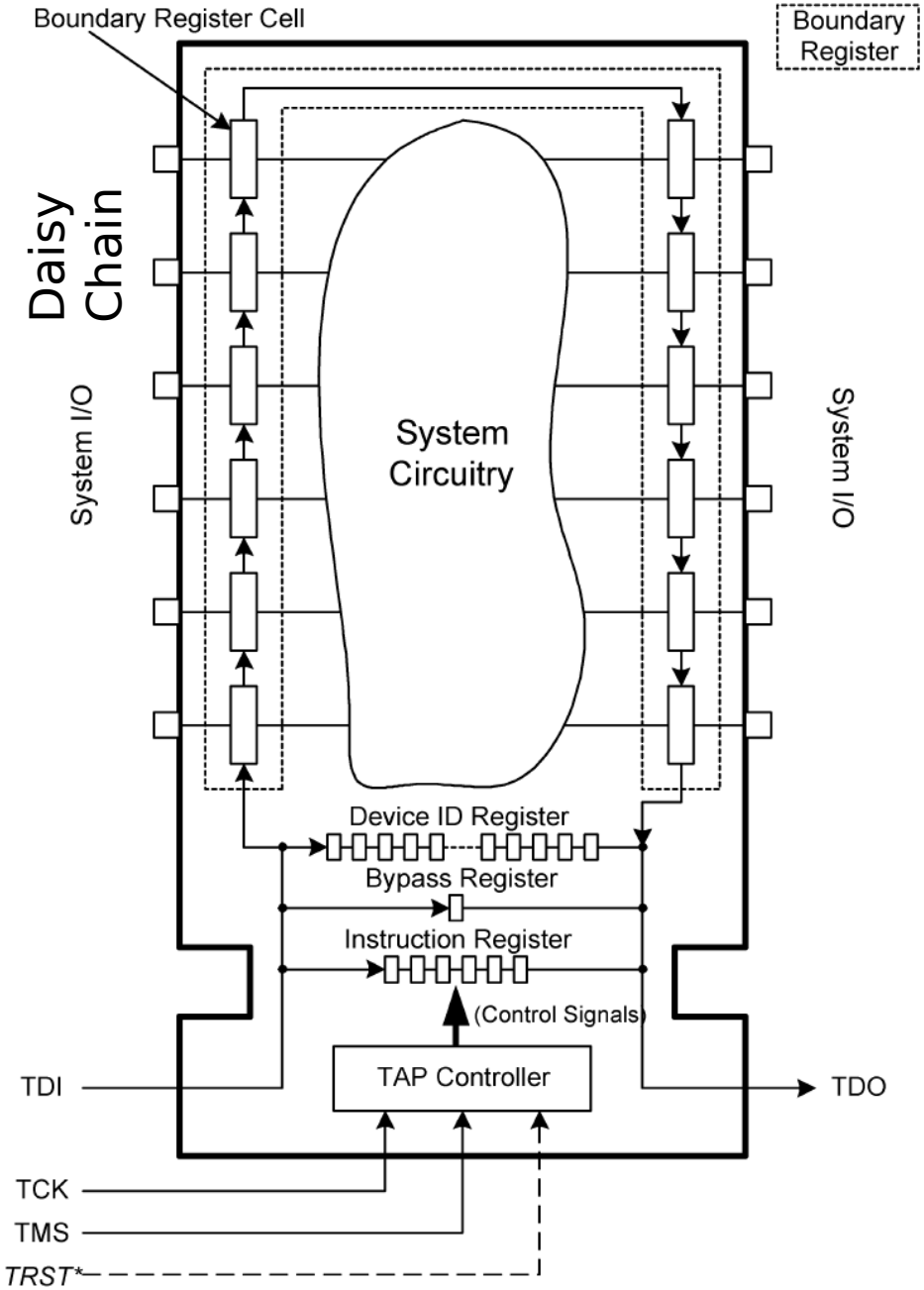


Fraunhofer IZM

e.g. DCD chip bump pitch:
200µm in y and 180µm in x

not accessible for a probe station with needles

JTAG



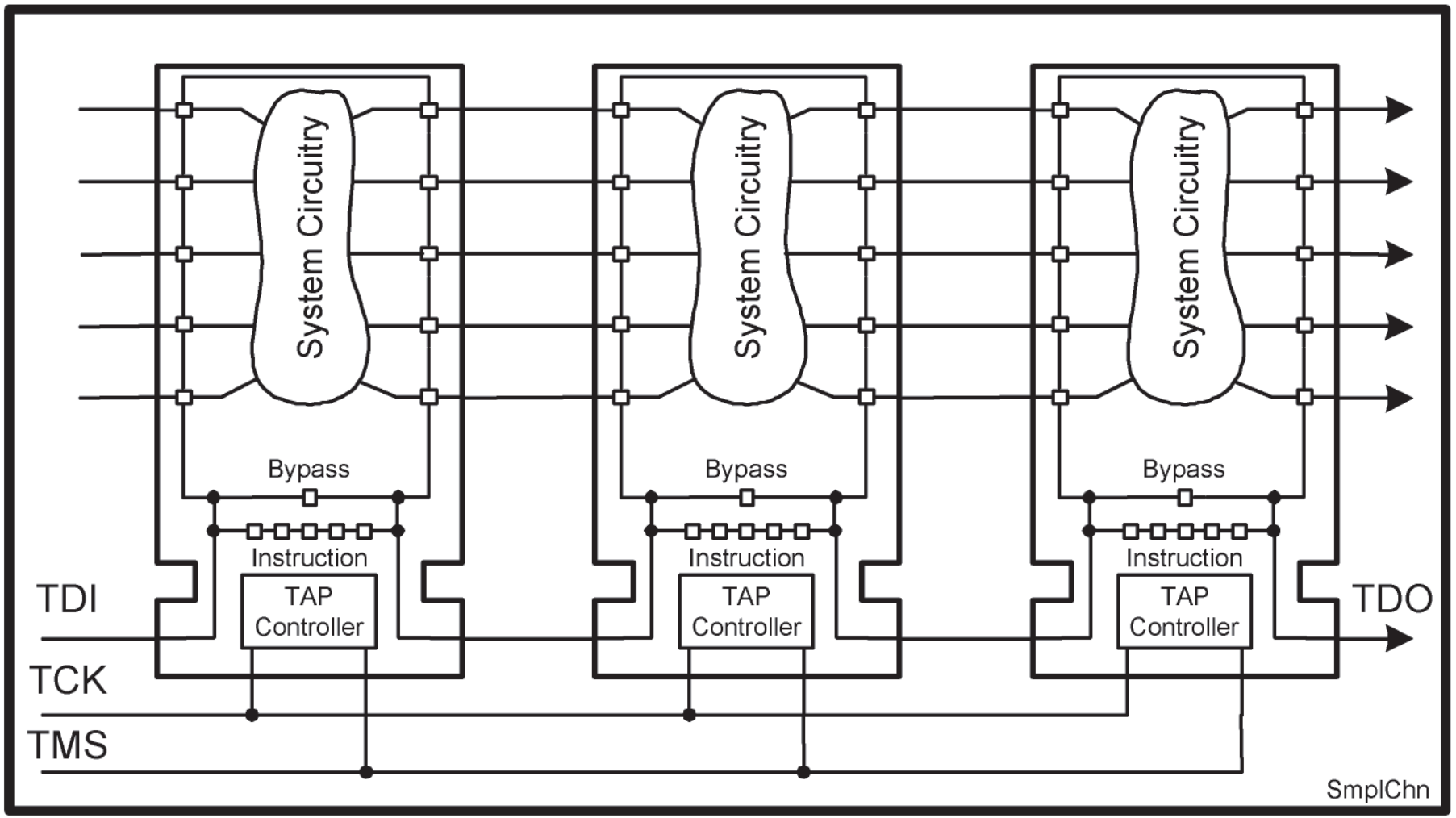
IEEE Std. 1149.1
Joint Test Action Group (JTAG)

additional boundary-scan cells (BSC) at the I/Os of an IC

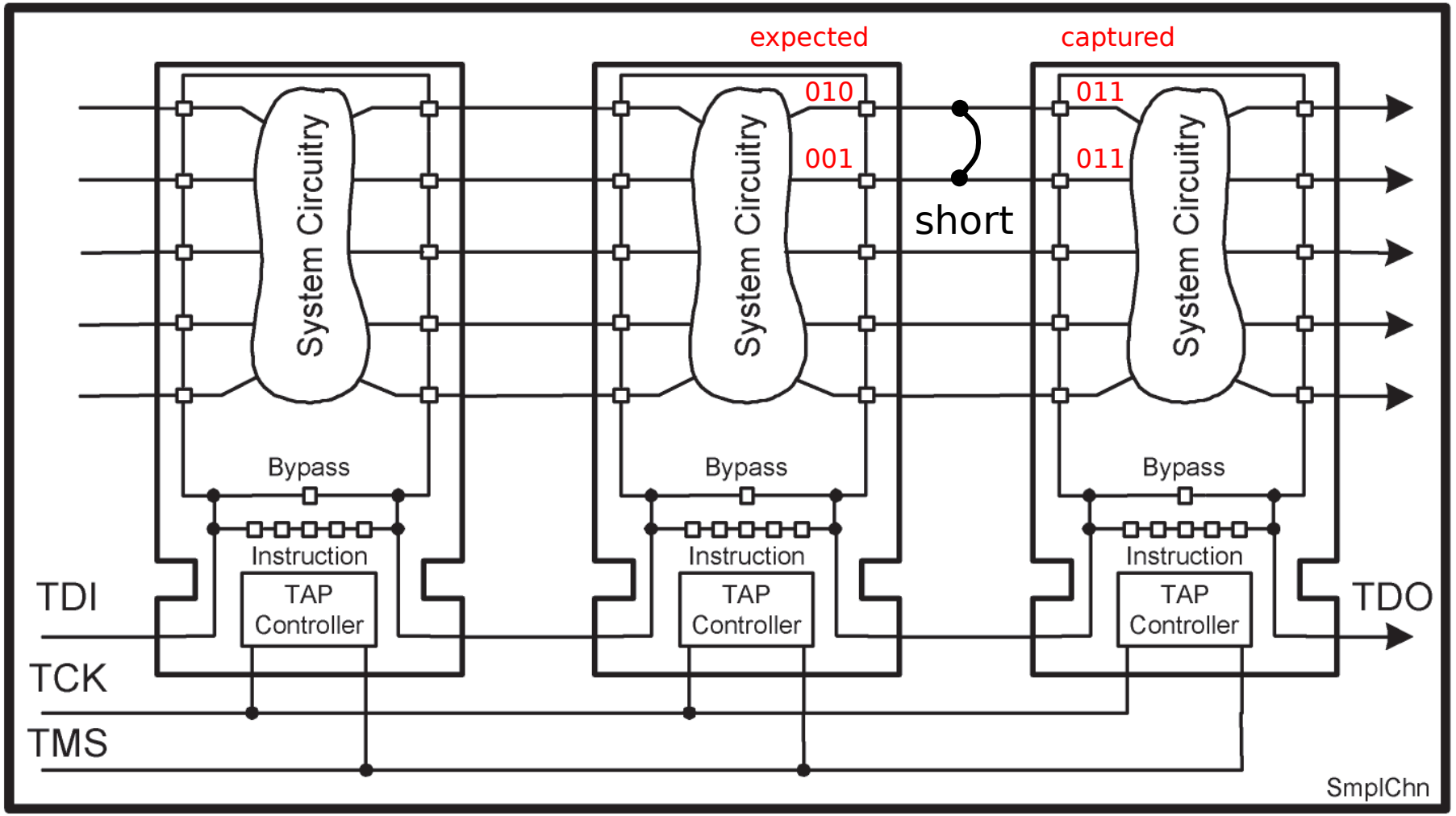
four additional I/O ports
Test Access Port (TAP)

TCK	test clock
TMS	test mode select
TDI	test data input
TDO	test data output
(TRST	test reset)

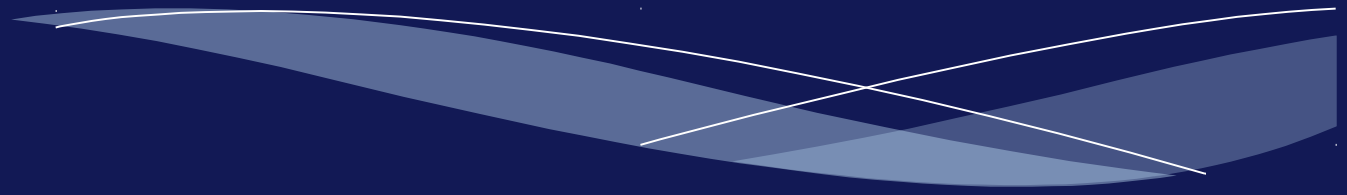
Chain of Boundary Scan ICs



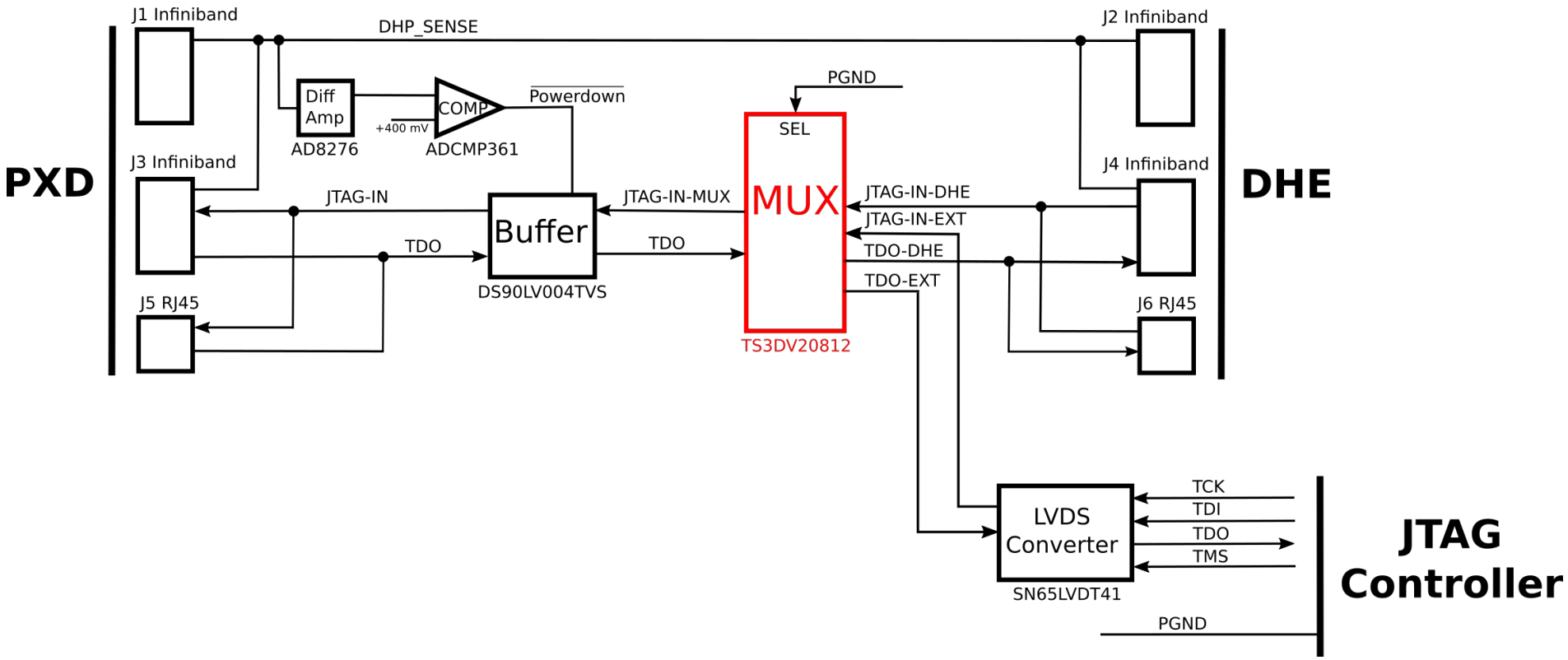
Chain of Boundary Scan ICs



HARDWARE



JTAG Breakout Board



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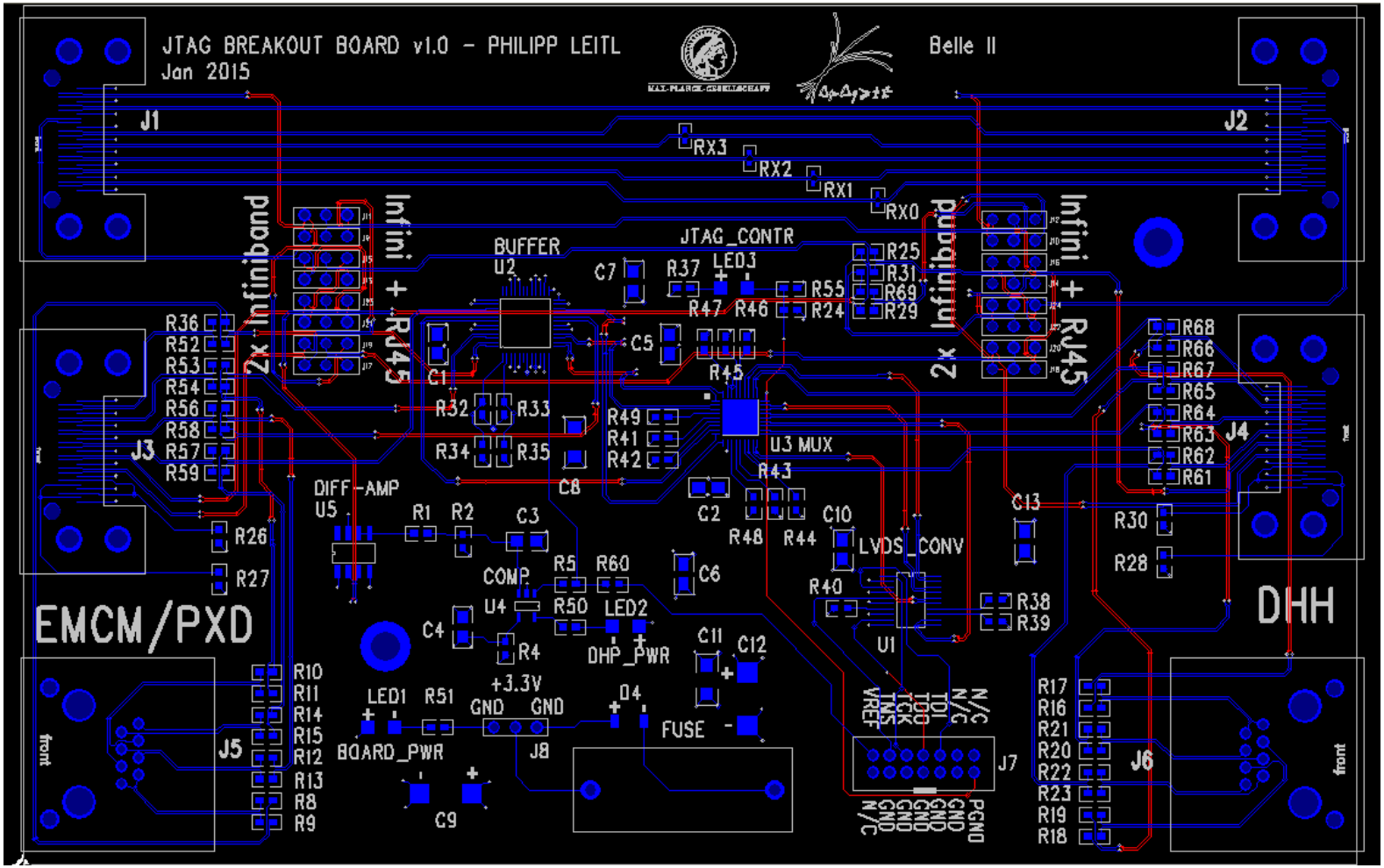

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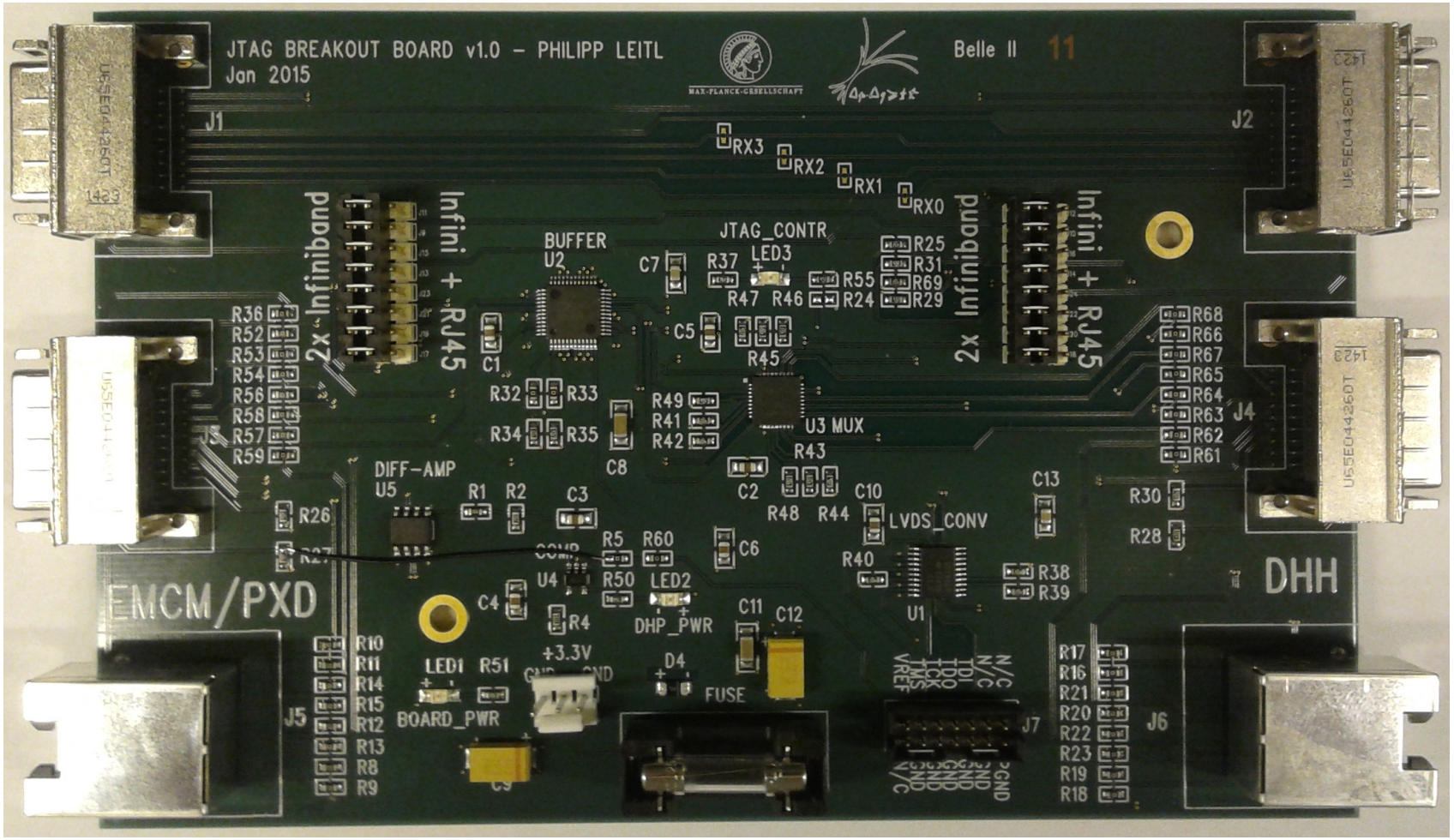
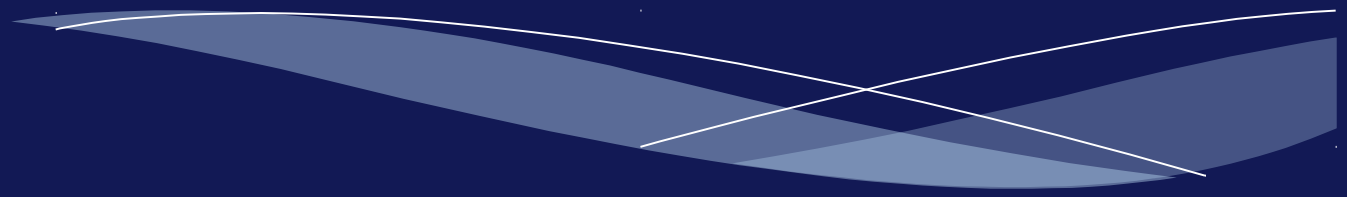


SOFTWARE



Boundary Scan Software

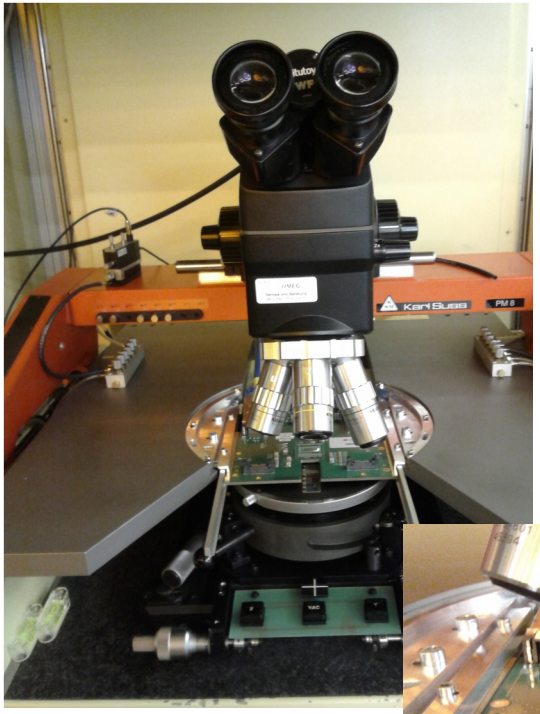
- New commercial system needed → offers from different vendors
  - demo-version in the meantime
  - different approaches to the issue
  - different JTAG controller → adapter needed
  - decision for XJTAG

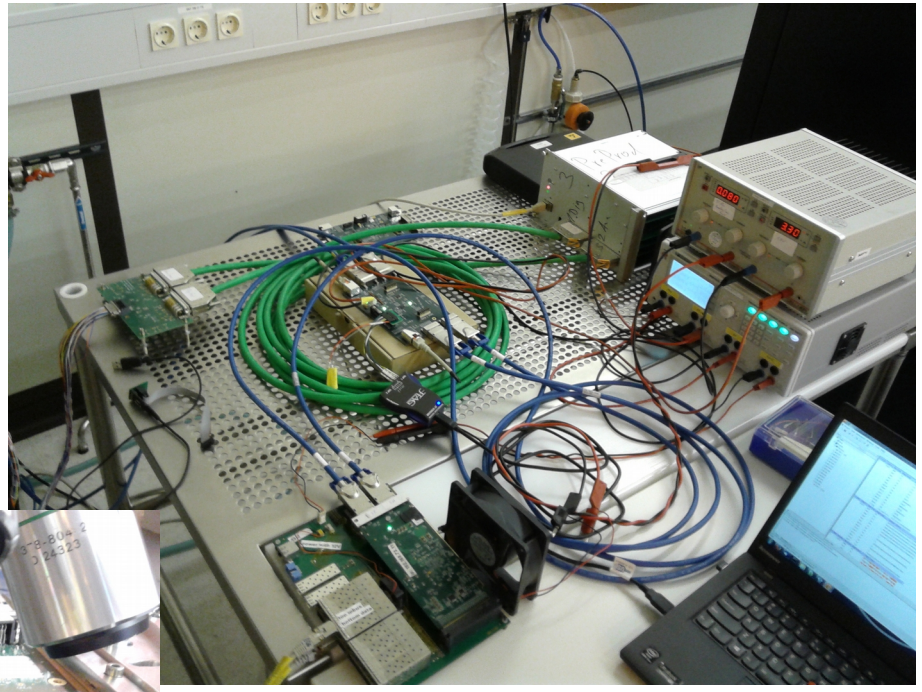
- Boundary Scan Description Language (BSDL) files
  - DHP02 and DHPT10: software generated
  - SwitcherB18 v1 and v2: manually written
  - DCD-Bv2 and Bv4-pipeline: manually written

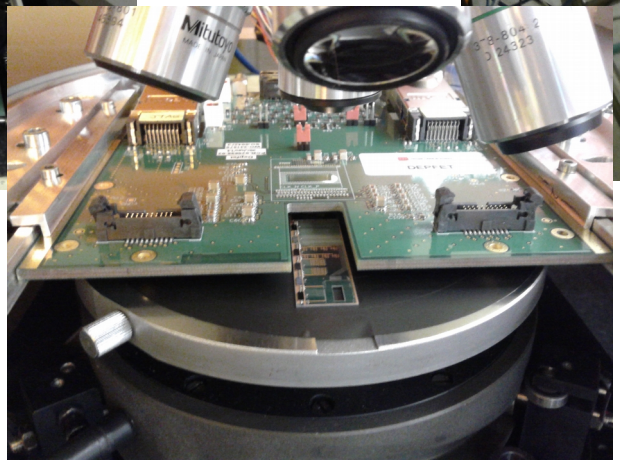
} several versions

- Netlist
  - problematic EDIF format (“flavours”)
  - import settings for EDIF (XJTAG support)
  - manually edited

Boundary Scan Tests



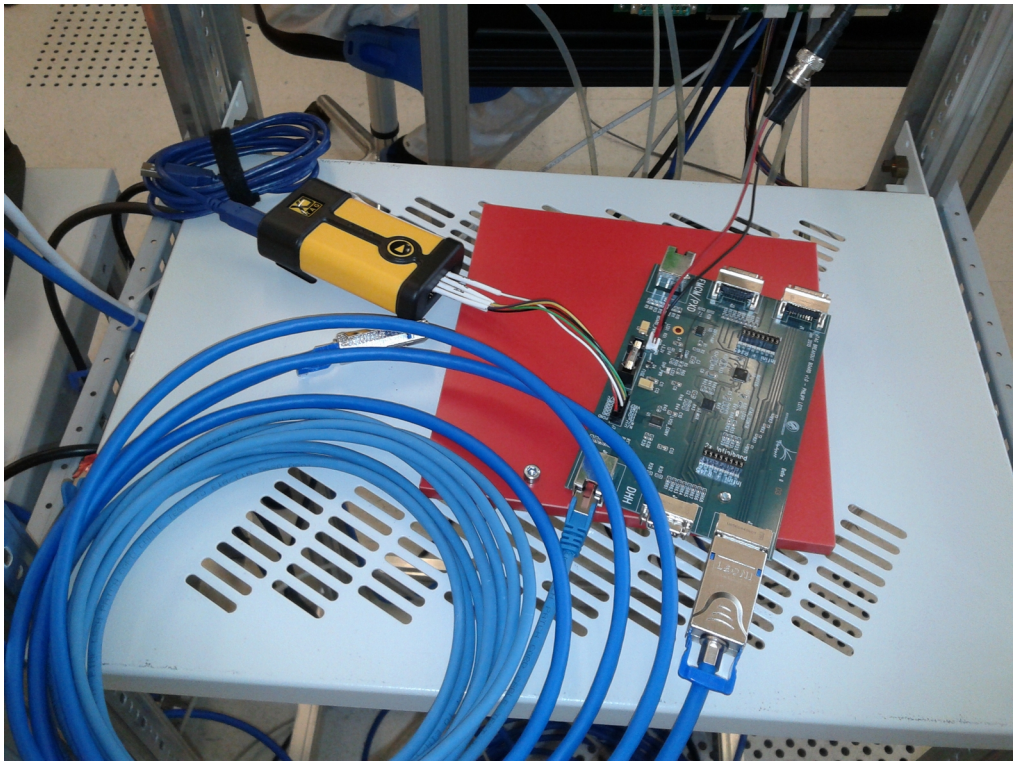




ProbeCard

Boundary Scan Tests

EMCM P6-1	✓
EMCM P6-2	✓
EMCM W17-4	✗
EMCM W18-3	✗
EMCM W18-4	✓
EMCM W31-3	✓
EMCM W31-4	✓
PXD9 W30-OB1	✓



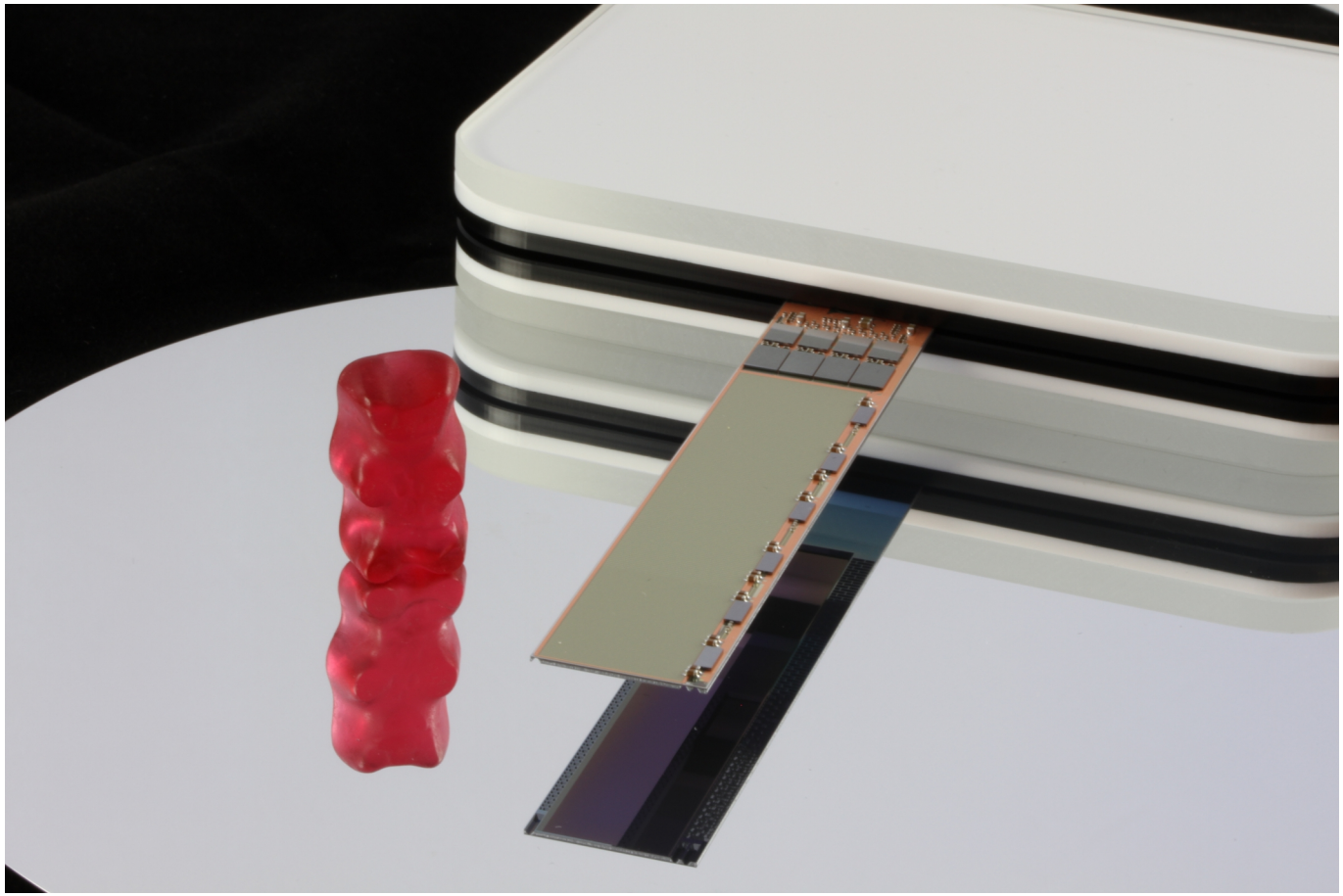
~23% test coverage of all ASIC pins

(30.720 of 132.800 bump bonds for the hole PXD directly accessible)

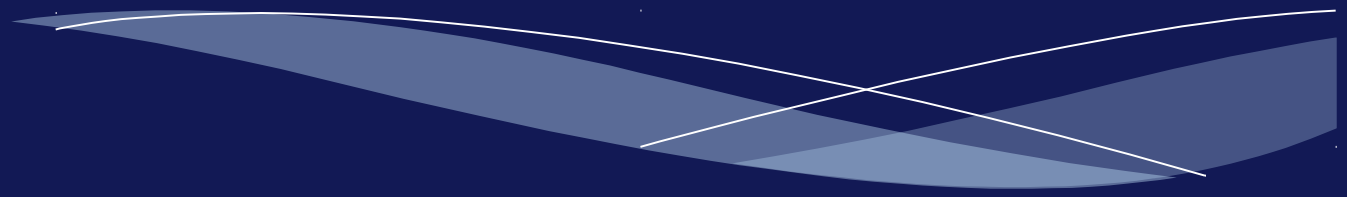
Summary

- Boundary Scan Test can now be used for the PXD series production (start end of 2015)
- Design of JTAG Breakout Board (JBB)
  (11 boards assembled and successfully tested)
- System of hardware (incl. probe station) and software (incl. BSDL files and netlist) working
- Development of a standardized procedure for testing the new PXD9 modules (XJTAG project)

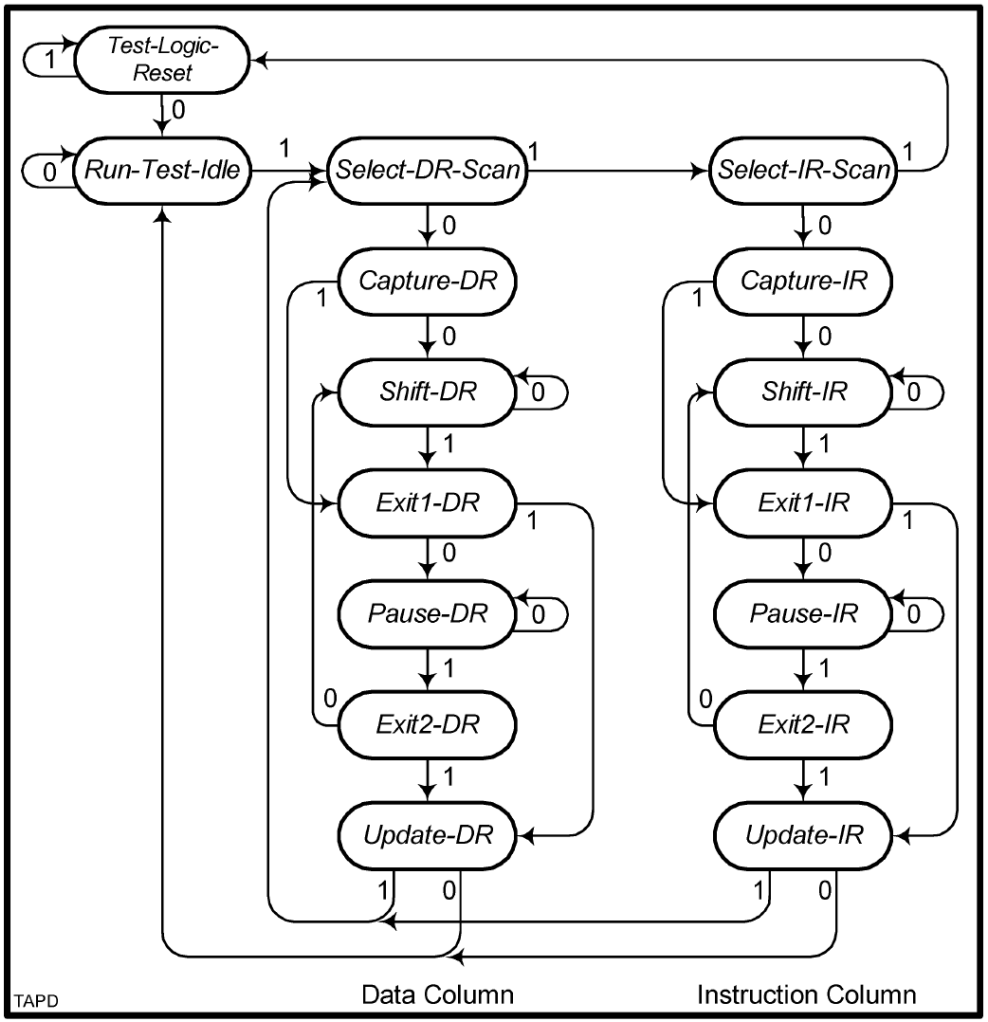
Thank you for your attention!



Backup



TAP controller

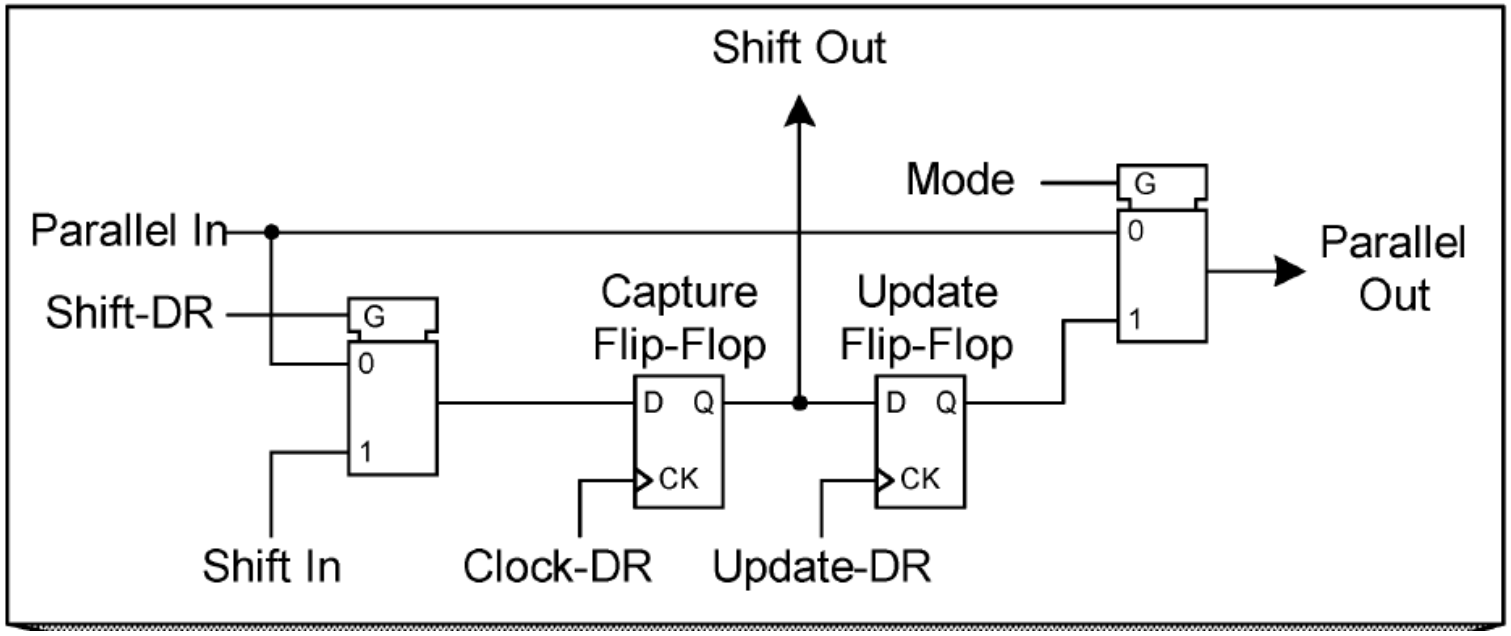


state transition diagram of the TAP controller (Test Access Port)

16 state machine

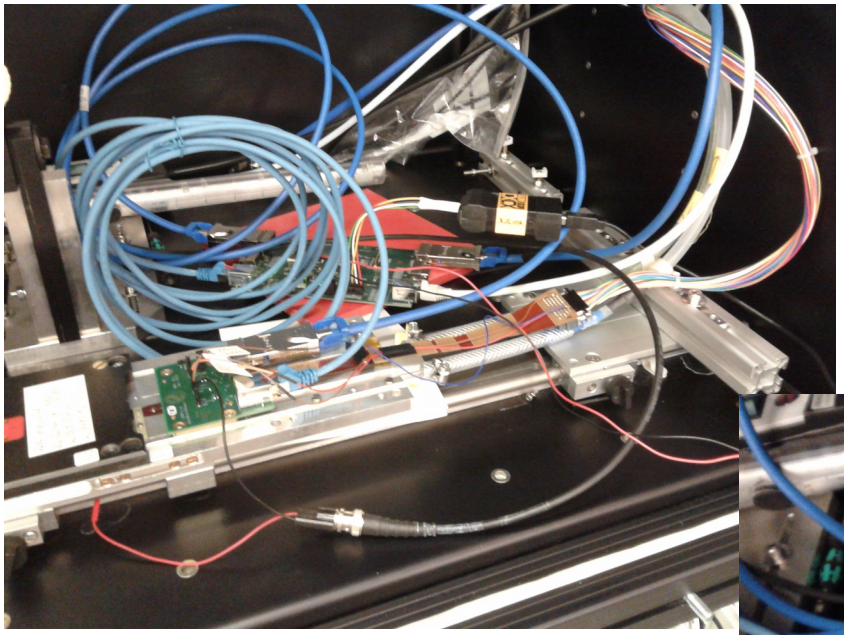
controlled by TCK and TMS

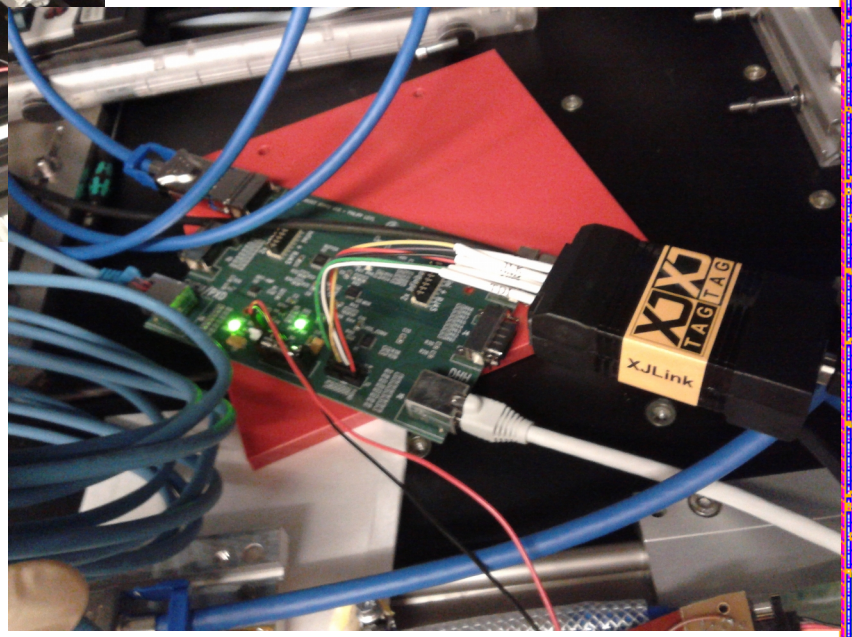
Boundary Register Cell

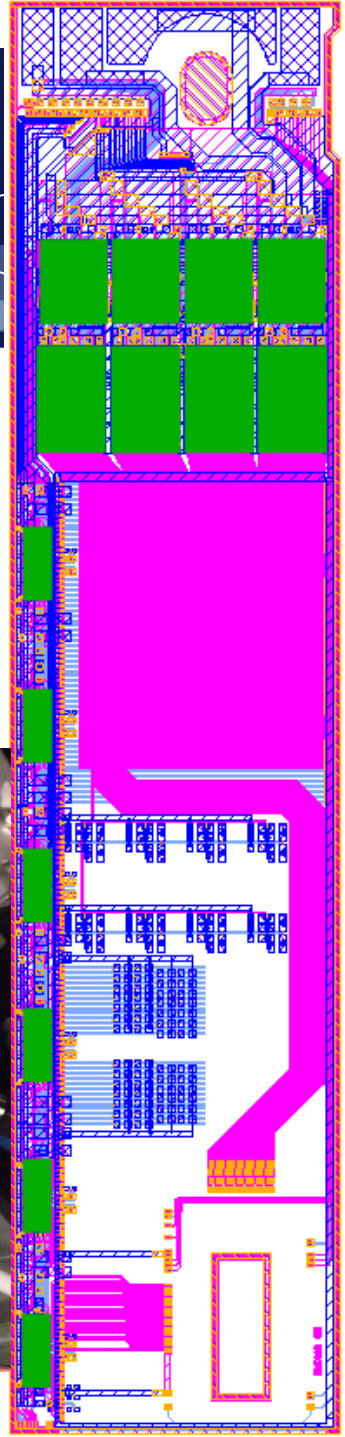


two multiplexer
two flip-flops

EMCM W18-3







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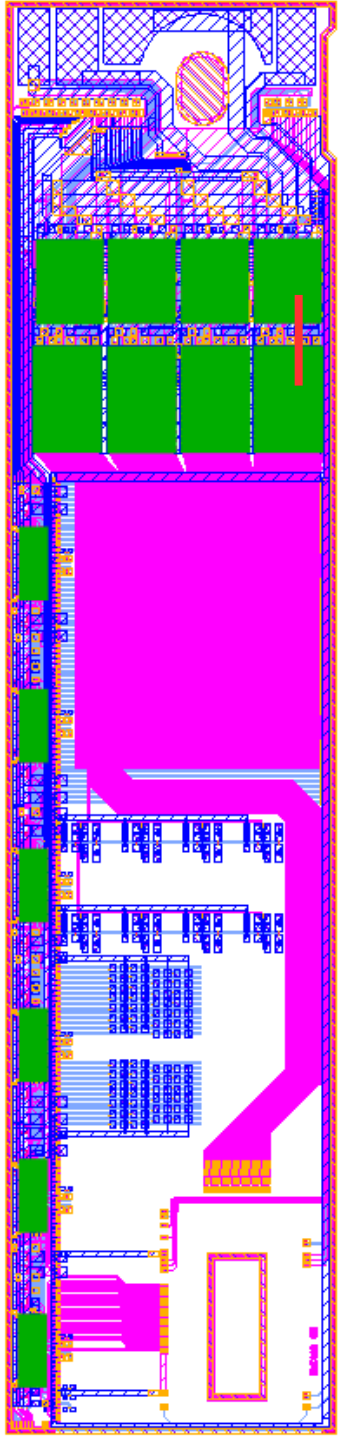


Infrastructure Test (goepel) – CheckChain (XJTAG): **OK**

Interconnection Test - goepel:

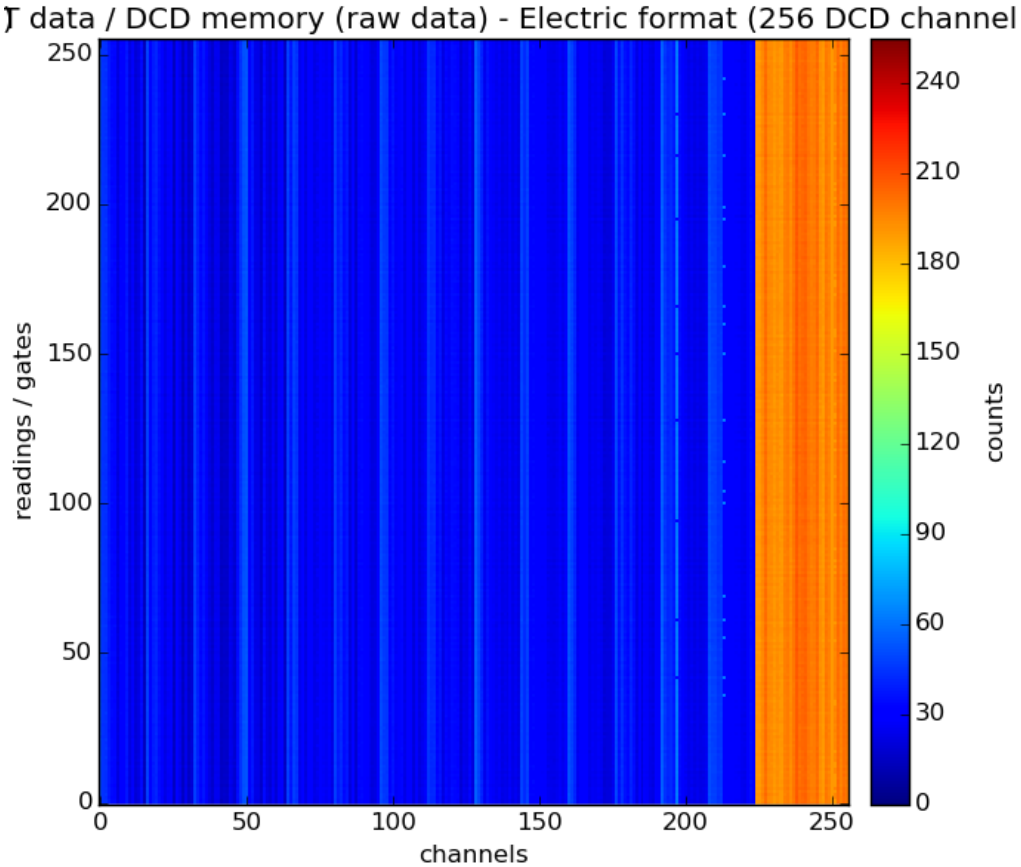
6/15/2015 2:19:33 PM UUT: EMCM-P6-1 Start Test: Interconnection
==========
DCD0:DI7_0(#P14)EL MH

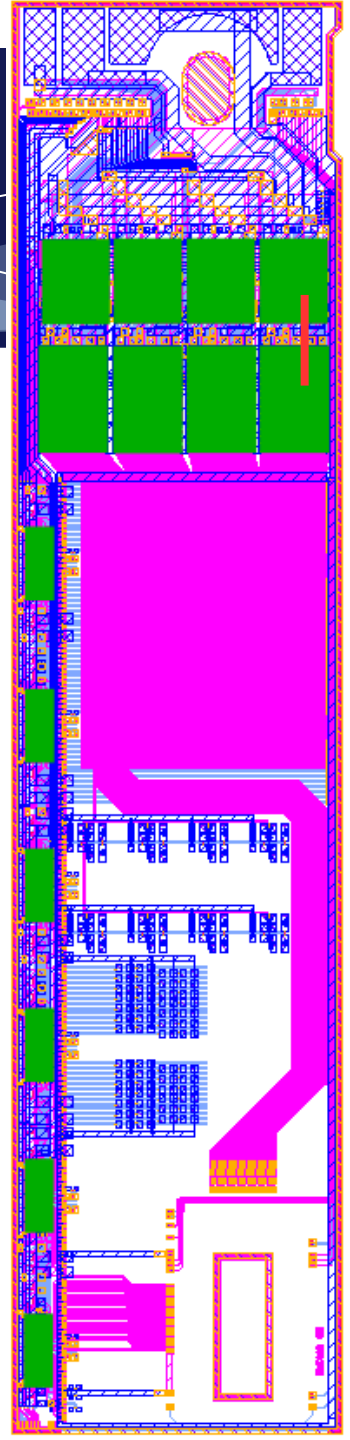
- 1- Line NET0191_1 defective:
-73- 1. pin <: Out DHP0:DO7_0(#93) {BScan} DHP10_FOOTPRINT NET0191_1
-73- 2. pin >: In DCD0:DI7_0(#P14) {BScan} DCD_FOOTPRINT NET0191_1
- 9- Stuck at High of the line

-24- Test step table of the line NET0191_1:
-25- Expected H L H L H H H H H H L L H L L L L L L H
-29- Measured <Stuck at high>
-30- Output pin DHP0:DO7_0(#93) H L H L H H H H H H L L H L L L L L L H
-31- Input pin DCD0:DI7_0(#P14) H>H H>H H H H H H H H>H>H H>H>H>H>H>H>H H
==========
2:19:33 PM F A I L Elapsed Time 00:00:00.232
==========

EMCM W18-3

DCD1 shows 32 out of 256 channels stuck at the upper half of the dynamic range of the ADC (MSB stuck)





EMCM W18-3

Interconnection Test - XJTAG:

#3670

Error on net net0191<1>: Stuck at 1.

- Net Detail

  Net net0191<1> contains:

  - dcd0.B2(DI7_0)
  - dhp0.H30(DO7_0)

- Error Detail

Test Summary: 1 error
CONNTEST failed

>>>> FAILED <<<<

NAME	RESULT	SUMMARY	TIME
JTAG CON	Failed		1,544
TOTAL TIME			1,544