ASICs at B2GM/BPAC

:- missing codes not an issue anymore
:- Emphasis on system performance
:- critical: inter-chip communication

DEPFET

DCDB4.1

Recent measurements show that the current DCDB4 is well advanced

Still, minor changes, in particular to increase the operation robustness, will be implemented

:- improve robustness of data transmission by increasing the output driver strength

:- missing code mitigation
:- add antenna diodes where missing to minimize transistor mismatch in comparator
:- add dummy structures in first comparator for the same reason

:- optimize gain and dynamic range settings in the light of the recently measured PXD9 DEPFET characteristics

:- change the sampling polarity for the pixel and global JTAG registers to rising edge and the data output to falling edge to be in line with the industry standard

DCDB4.1 design done, submission next week, Engineering Run, shared
:- estimated time of arrival ~mid Jan 2016

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DHPT1.1

- Serializer: timing bug
  Mistake during extraction and simula
  Workaround for DHPT1.0: VDD = 1.6
  Fixed for the DHPT1.1, with all corne
- CML driver enhancement (off-module data TX)
  Works fine but still output amplitude
- Delay elements issue: duty cycle distortion
  Overlooked during DHPT1.0 sign off
  Fixed by custom delay elements mac
- Data receiver robustness:
  reduce input pad capacitance
  symmetric delay line elements
  remove hysteresis

DHPT1.1 submitted 24.8.2015, MPW
:- estimated time of arrival cw47, mid Nov.

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DEPFET

Switcher-B18 v2.1

:- decrease the rise time of the C
to widen the sampling

:- exclude the serial input from th
(the scheme disconne
the LVDS input pads)

:- change the size of the current I
low-stress connection
required due to the ch

Switcher-B18v2.1 submitted 24.8.2015, MPW
:- estimated time of arrival ~mid December
:- need two (four because of X-Mas) more weeks for bumping

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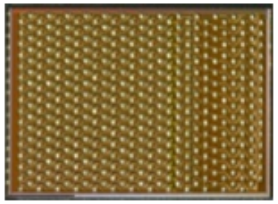
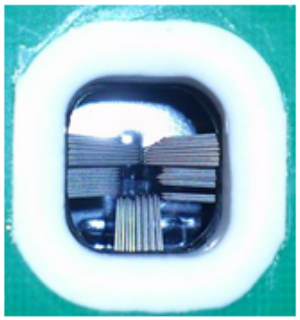
After the chips are back from foundries





Testing!!!

DHPT1.1: at Bonn University

:- straight forward – using existing test setups at Bonn University (probe card, hybrid5)

DCDB4.1 and Switcher-B18 v2.1: at KIT Karlsruhe

:- probe card setups at Uni Heidelberg will be moved to KIT Karlsruhe, incl. new probe cards
:- generous help from KIT IPE (Marc Weber): Probe stations, engineering support, technician
:- setup will be qualified with existing DCDB4 to be ready when new chips arrive
:- existing hybrid setups (hybrid5) can be used

:- Switcher-B18 v2.1 testing less difficult, possible help for testing at Uni Heidelberg

BPAC first response

PXD

The committee applauds the successful production of the first functioning pixel sensor ladder with electronics by the PXD group. This is a substantial step for the success of the project. On the other hand, the committee noted with concern that two of the three necessary ASICs did not perform as expected and revised designs have been submitted for production. Even if the corrected version of ASICs perform as expected, the new PXD production schedule looks very tight with little contingency for the planned date of the VXD installation. The PXD group should be prepared well in advance so that ASIC chip functionalities can be immediately verified upon delivery.

:- not unexpected: see previous slide ...

:- schedule indeed very tight, need tested ASICs in March 2016!!!

testing

SWBs: as soon as they are back (when??)

:- bumping at PacTech
:- probe station testing in Mannheim (tbc!!!)
:- testing on Hybrid level (rise times..), who??? Where??

DHPT: Mid November

:- propose that Bonn focuses on Hybrid5 and probe station tests
:- start with DCDB4 as soon as new DHPTs available
:- H5 should be available, HLL can help with bump adapter testing and Flip-Chip
:- discussion after BPAC with Christian Koffmane:
    :- as soon as tests on H5 okay, assemble two(?) more pilot modules with new SWB, DHPTs
    :- with DCDB4s, can be used in the DESY test???

DCDB4.1: when available??

:- start probe card test setup at KIT now (started already??)
:- tests on Hybrid5 level, one setup to be at KIT
:- not certain that DCDB4.1 will be available in time for DESY test
:- **prepare for backup: DCDB4 for DESY test**
:- at Mannheim: 98 DCDB4s (350µm thick), 480 DCDB4s (700µm thick)