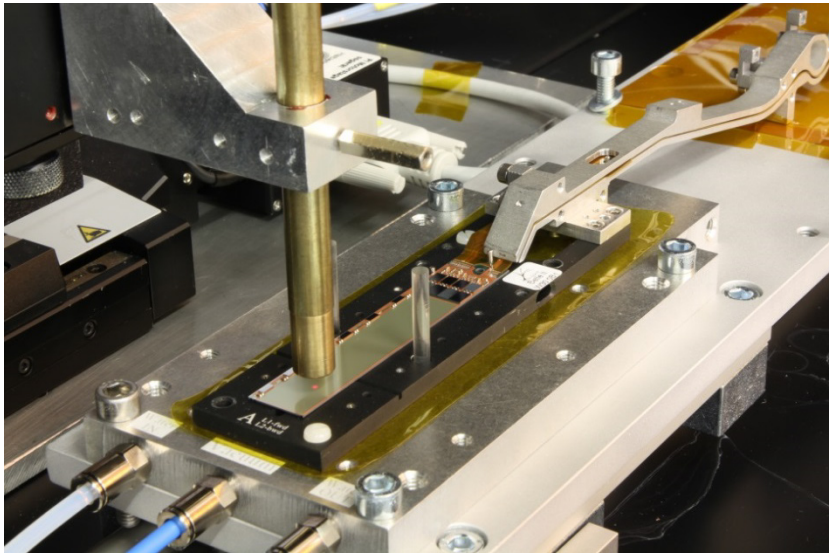
PXD9 Pilot Module

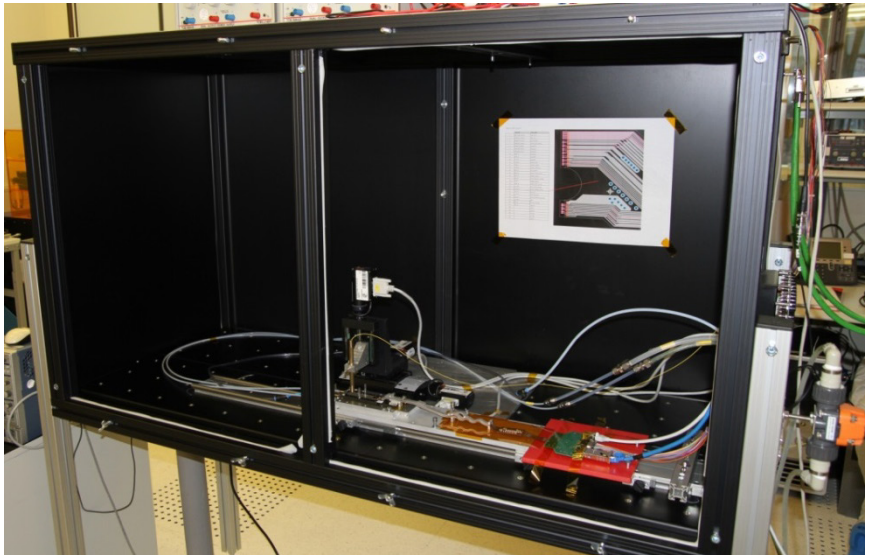
Status Verification of the Metal Routing

PXD SeeVogh – November 10, 2015

Felix Müller, Christian Koffmane for the Testing Crew

PXD9 Pilot Module – Verification of the Metal Routing





Module operated @ 250MHz (128ns per row)

- power-up ASICs – sanity check voltages + currents ✓
- configure ASICs via JTAG ✓
- boundary Scan: PASS (no faults in the digital I/Os) ✓
- DHPT serial link – parameters of the pre-emphasis ✓
- DCD <-> DHPT communication – timing adjustment ✓
- **sampling point scan**
- optimize DCD analogue performance (IPSource/2, IFBPBias, RefIn)

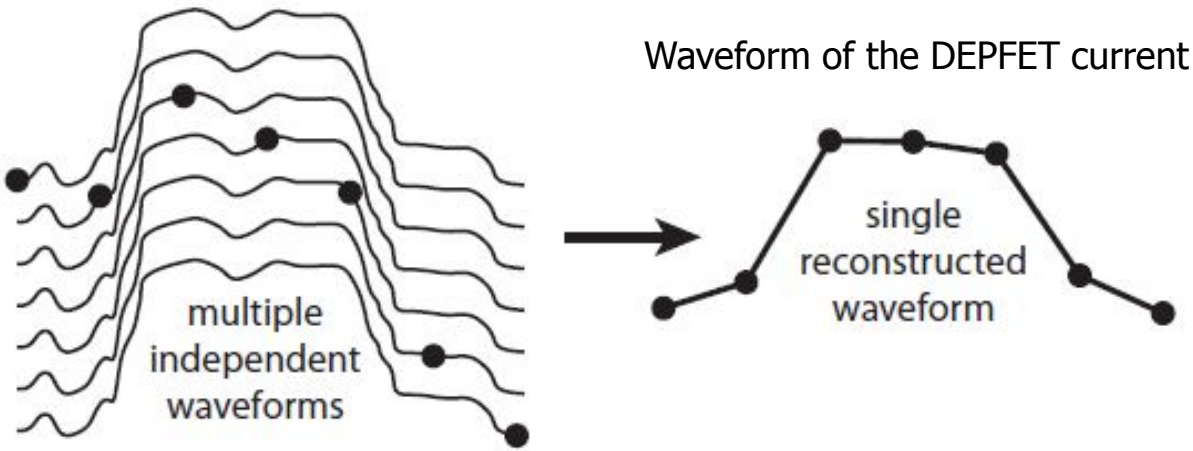
- 2 outer backward modules are assembled with kapton
- 1 outer forward module is prepared for the assembly on Hybrid7

Sampling Point Scan

Time resolved measurements with DHPT and DCD

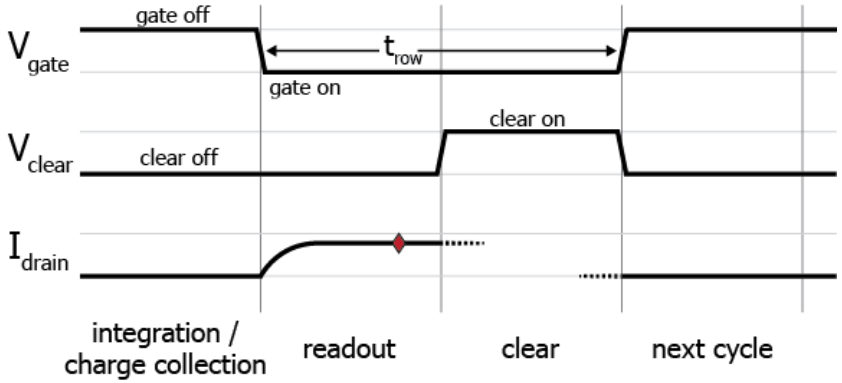
Applying a technique called sequential sampling a continuous time waveform of the DEPFET current can be measured

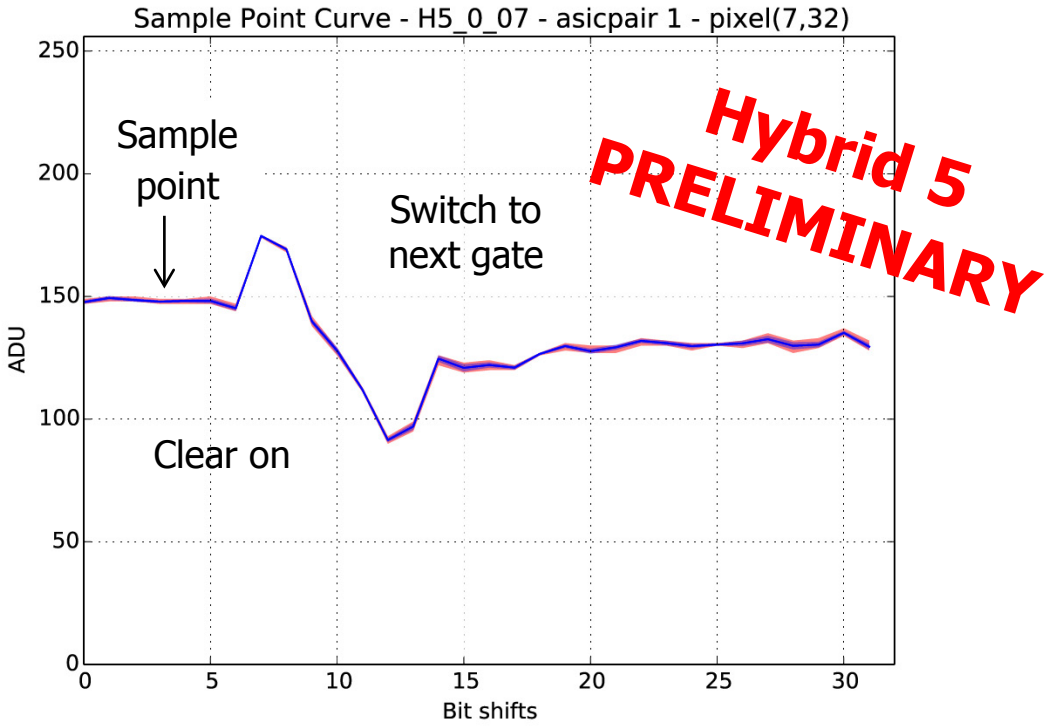
- From a periodic and stable input a single sample is taken
- The sample point is shifted by deltaT
- The single samples are assembled to form a combined waveform
- Averaging can be used to suppress electronic noise



Sampling Point Scan

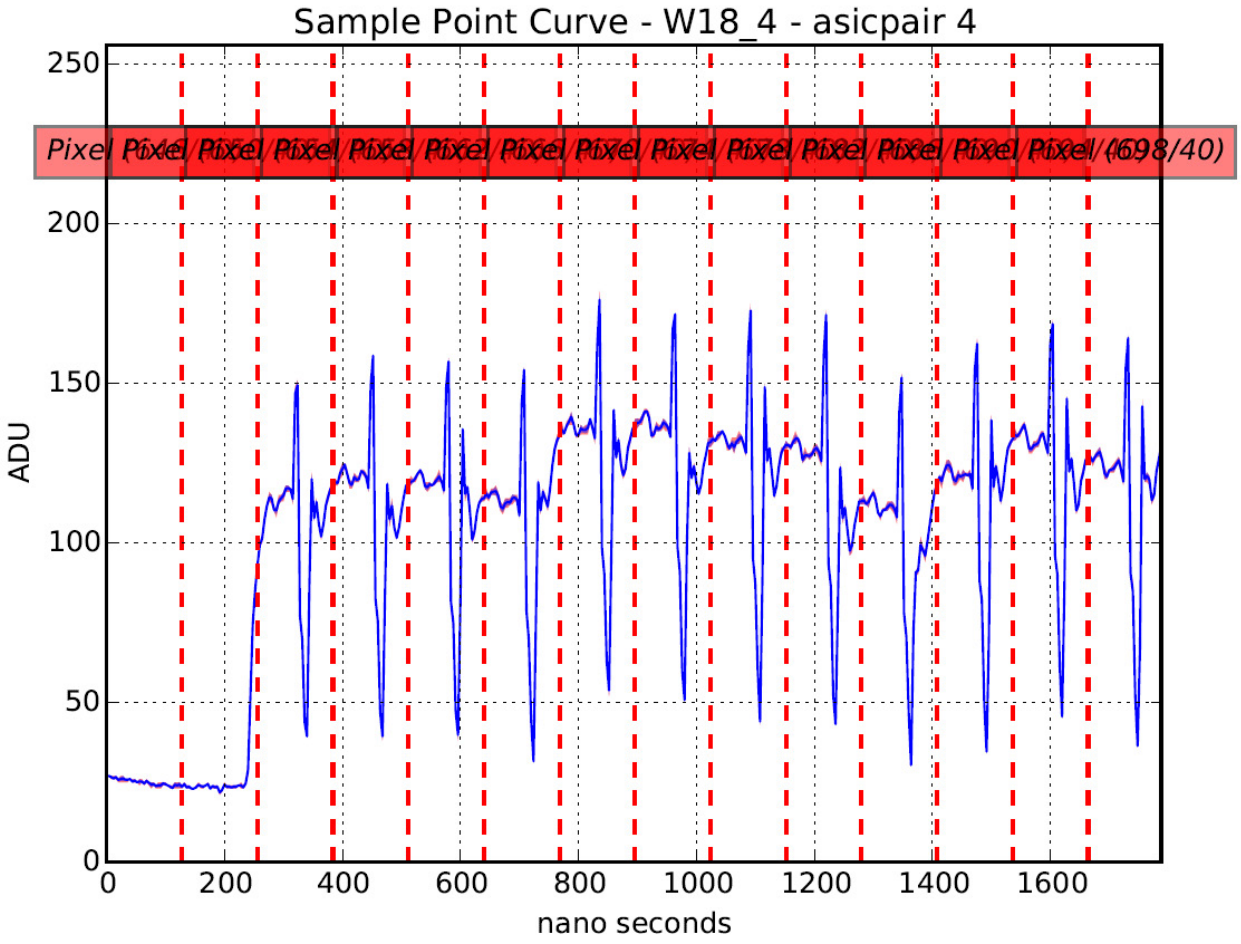
- Sampling the DEPFET current at the correct point of time is extremely important
- The scan is currently implemented with DHPT as controller for the timing
- Step size coarse = 4ns
- Step size fine = ~250ps

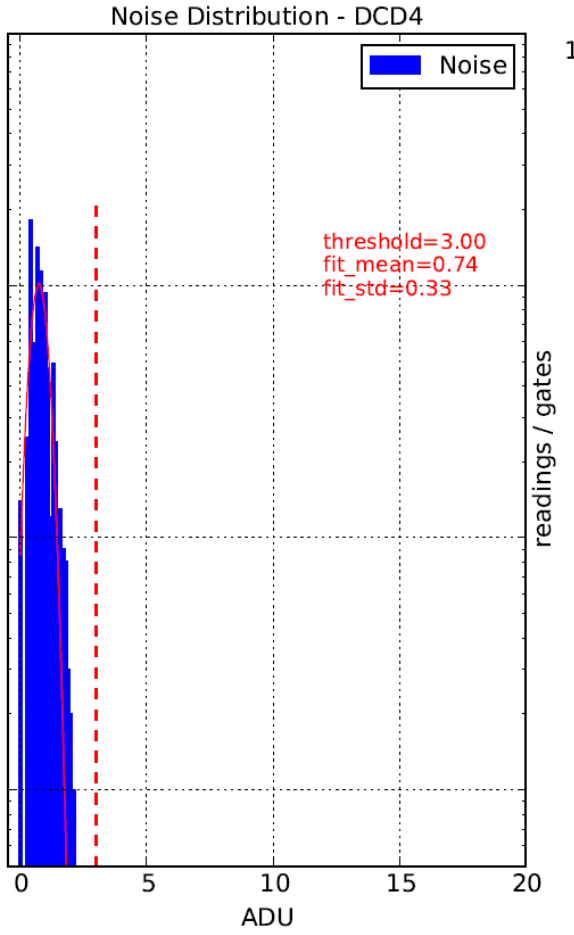




- Sampling point curve using Hybrid5 DHPT/DCDB4 + small PXD9 matrix @ 250MHz
- 1 bit shift = 4ns

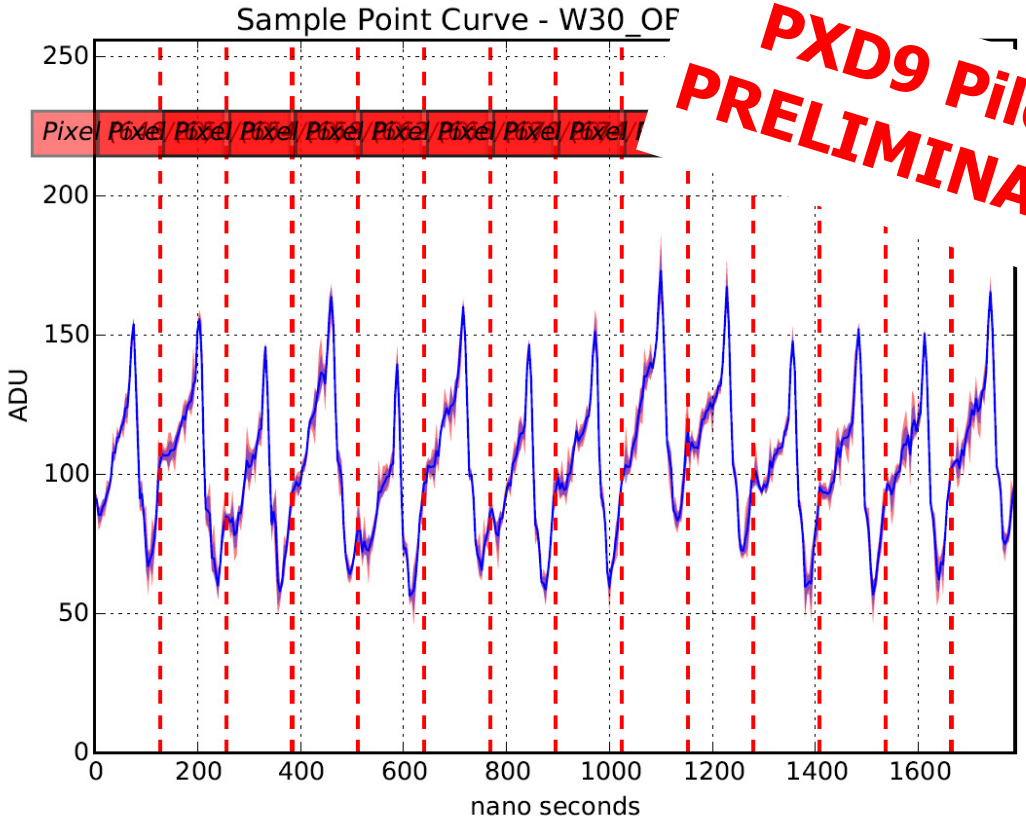
EMCM W18-4: Sample Point Scan and Noise (small PXD9)





Sampling Point Scan

- Same sequence as for EMCM applied
- No plateau for stable current sampling @ 128ns per row
- Timing of a subset of the rows changed to 384ns (32 out of 192)
- Work in progress: scan of the switcher Strobe-Clear signal with respect to Switcher-Clock and Strobe-Gate



PXD9 Pilot
PRELIMINARY

128ns per row

- We need more time to understand the sampling point scans
- Measurements @ full speed are delayed
- Still we would like to keep the date for a expert F2F meeting @ HLL in cw. 48

PXD9 Pilot Verification Plan

<table>
<tr><td></td><td>26.-30. Oct</td><td>2.-6. Nov</td><td>9.13. Nov</td><td>16.-20. Nov</td><td>23.-27. Nov</td><td>30. Nov - 4.Dec.</td><td>Dec. 7th</td></tr>
<tr><td>CW</td><td>44</td><td>45</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td></tr>
<tr><td>HLL (pxdtest2)</td><td colspan="3">sampling point scan</td><td>increase to nominal freq.</td><td>gated mode</td><td></td><td rowspan="10">Go for PXD9 metallization or agreement on the necessary changes</td></tr>
<tr><td></td><td colspan="3">pedestal/noise all DCDs</td><td>DHPT serial link - IBERT/oscilloscope</td><td>pedestal compression</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>DCD <-> DHPT (delay)</td><td>Cd109 spectrum</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>sampling point scan</td><td>Laser spot</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>pedestal/noise all DCD</td><td rowspan="6">F2F Meeting @ HLL</td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td>zero suppressed data</td><td></td></tr>
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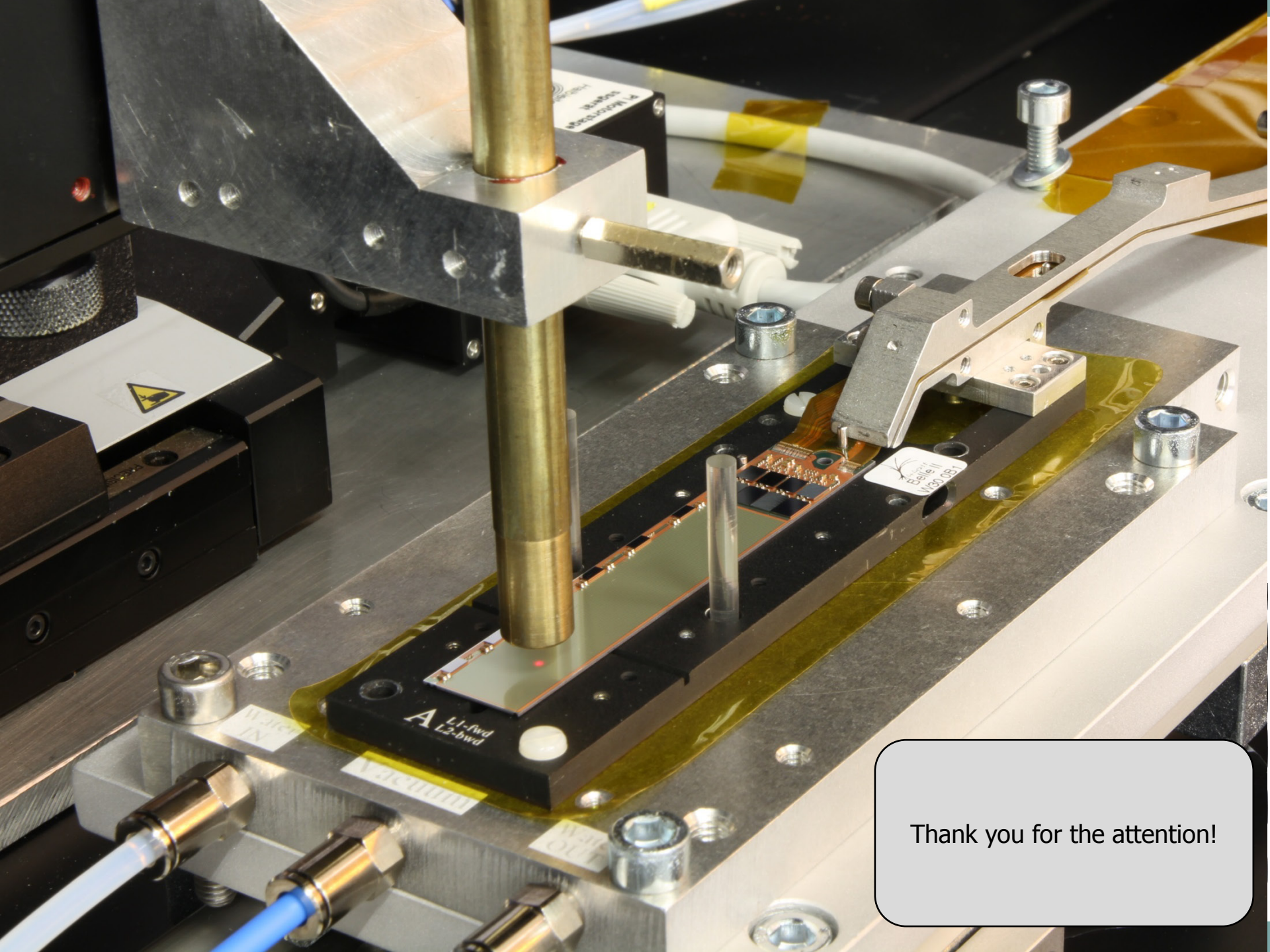
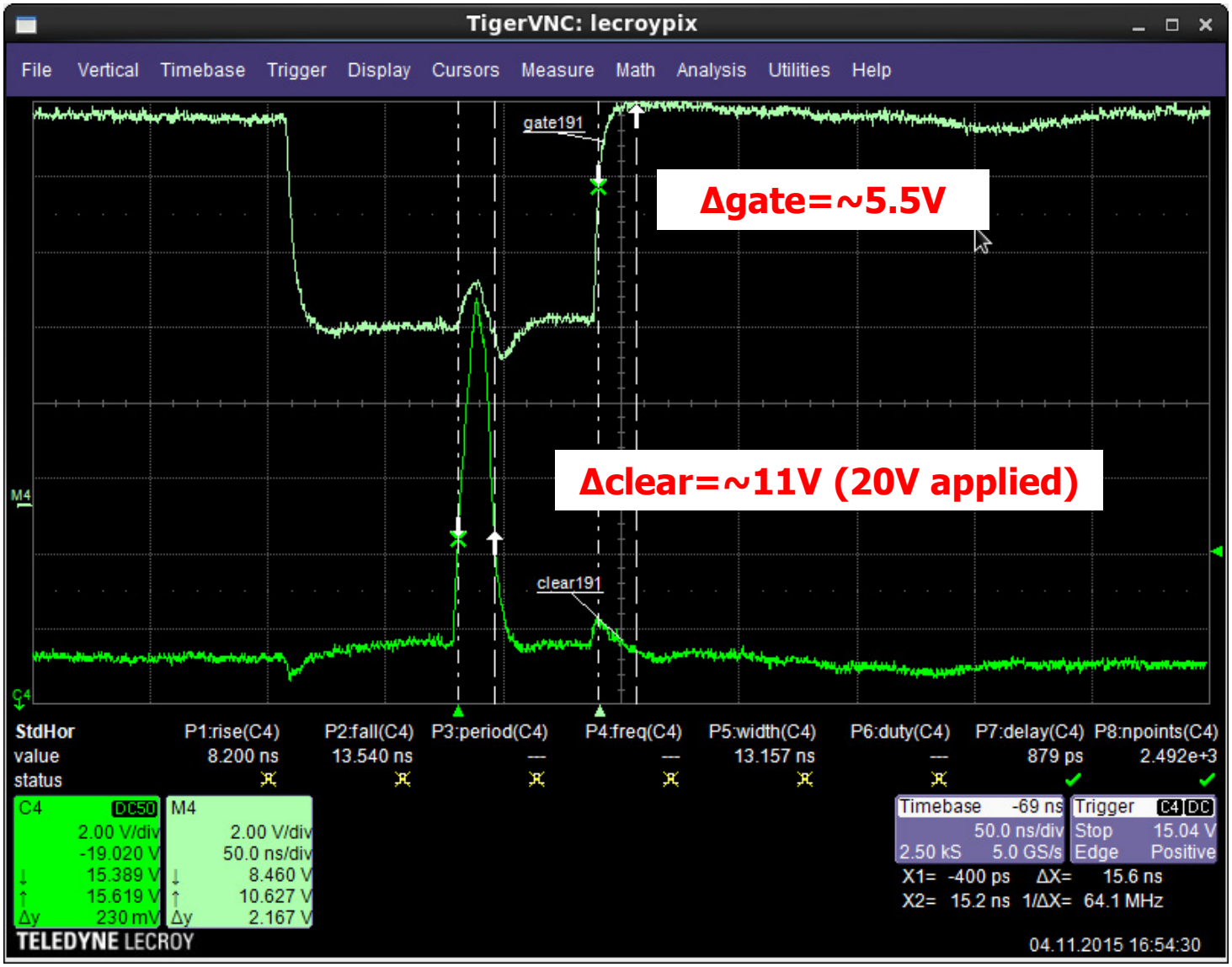
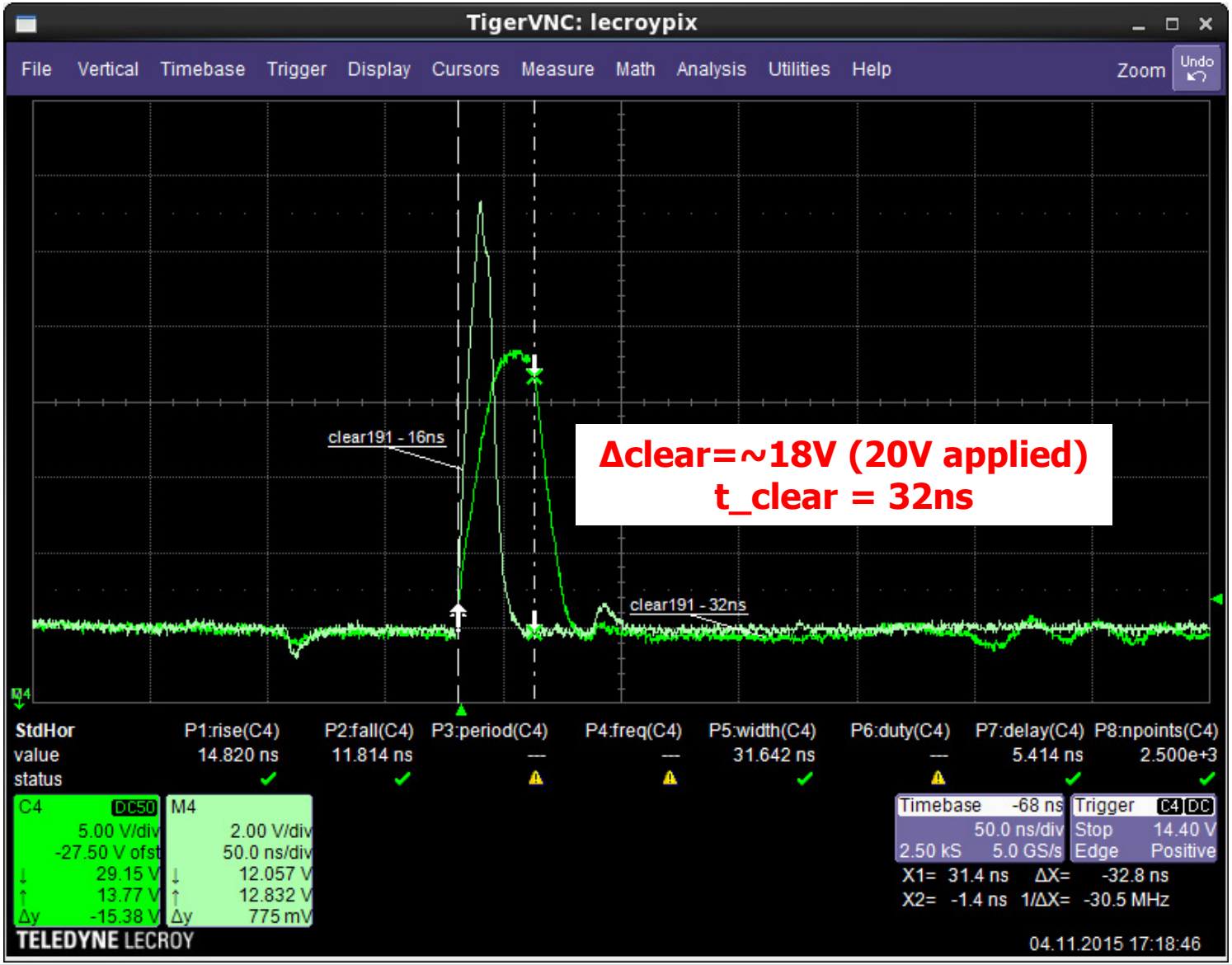
<tr><td>HLL (pxdtest4)</td><td></td><td></td><td>Preparation Gated Mode Test EMCM</td><td></td><td>Hybrid 7 Testing to verify OF/IB balcony and EOS layout</td><td></td></tr>
</table>



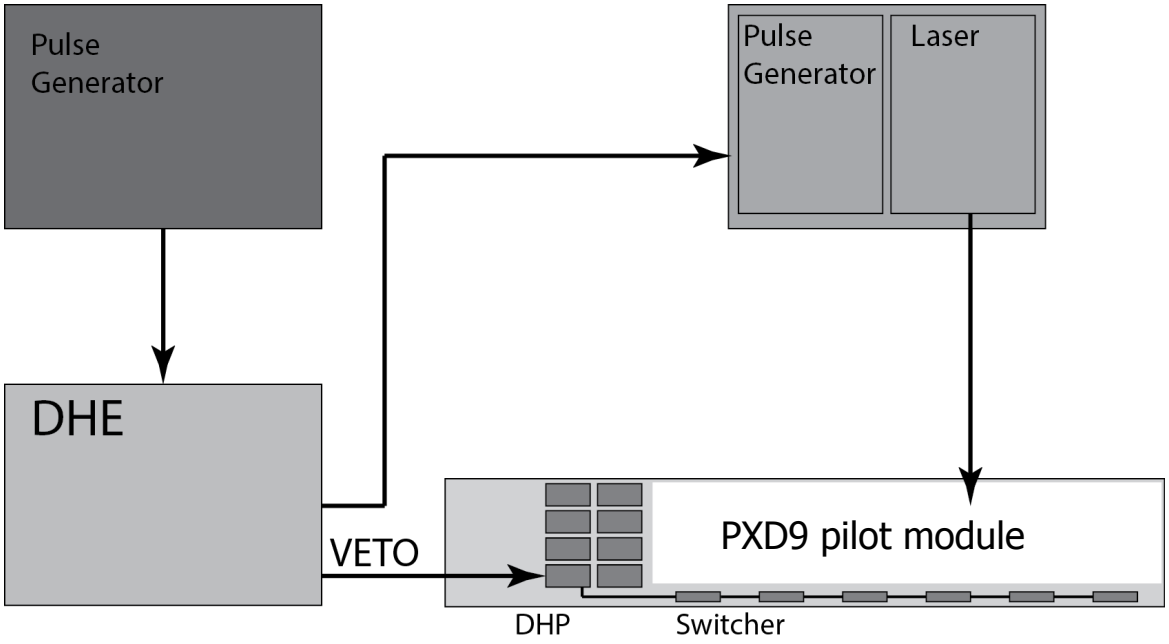
Thank you for the attention!


TigerVNC: lecroypix
File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
gate191
Δgate=~5.5V
Δclear=~11V (20V applied)
clear191
M4
C4
StdHor P1:rise(C4) P2:fall(C4) P3:period(C4) P4:freq(C4) P5:width(C4) P6:duty(C4) P7:delay(C4) P8:npoints(C4)
value 8.200 ns 13.540 ns --- --- 13.157 ns --- 879 ps 2.492e+3
status
C4 DC50 2.00 V/div -19.020 V 15.389 V 15.619 V Δy 230 mV
M4 2.00 V/div 50.0 ns/div 8.460 V 10.627 V Δy 2.167 V
Timebase -69 ns 50.0 ns/div 2.50 kS 5.0 GS/s
Trigger C4 DC Stop 15.04 V Edge Positive
X1= -400 ps ΔX= 15.6 ns
X2= 15.2 ns 1/ΔX= 64.1 MHz
TELEDYNE LECROY
04.11.2015 16:54:30


TigerVNC: lecroypix
File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help
Zoom
Undo
clear191 - 16ns
clear191 - 32ns
Δclear=~18V (20V applied)
t_clear = 32ns
StdHor
value
status
P1:rise(C4) 14.820 ns
P2:fall(C4) 11.814 ns
P3:period(C4) ---
P4:freq(C4) ---
P5:width(C4) 31.642 ns
P6:duty(C4) ---
P7:delay(C4) 5.414 ns
P8:npoints(C4) 2.500e+3
C4 DC50
5.00 V/div
-27.50 V ofst
29.15 V
13.77 V
Δy -15.38 V
M4
2.00 V/div
50.0 ns/div
12.057 V
12.832 V
Δy 775 mV
Timebase -68 ns
50.0 ns/div
2.50 kS 5.0 GS/s
Trigger C4 DC
Stop 14.40 V
Edge Positive
X1= 31.4 ns ΔX= -32.8 ns
X2= -1.4 ns 1/ΔX= -30.5 MHz
TELEDYNE LECROY
04.11.2015 17:18:46

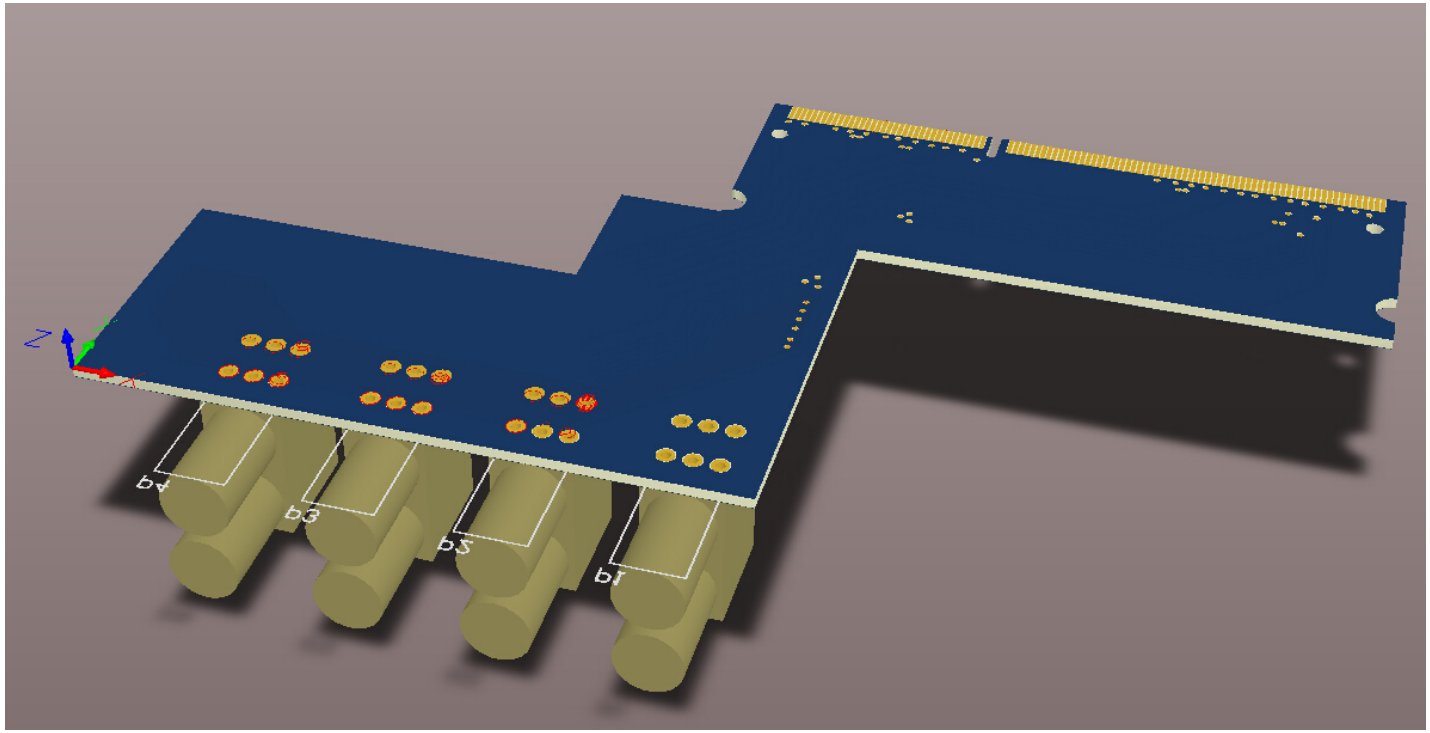
Gated Mode Verification

- DHE receives VETO trigger from external pulse generator and forwards it to the DHPT
- the DHPT jumps from the current sequencer memory address to a dedicated address where the Gated Mode sequence is defined
- via the control lines (StrG, StrC, CLK) the Switcher is programmed into Gated Mode – the timing can be chosen in steps of ~3.3ns
- separated in 4 groups of Switcher output channels all the Clear lines are switched to the ClearOn potential, the Gate line keep the GateOff potential
- the DHE generates a trigger for a laser to verify that the gating works



Gated Mode Verification

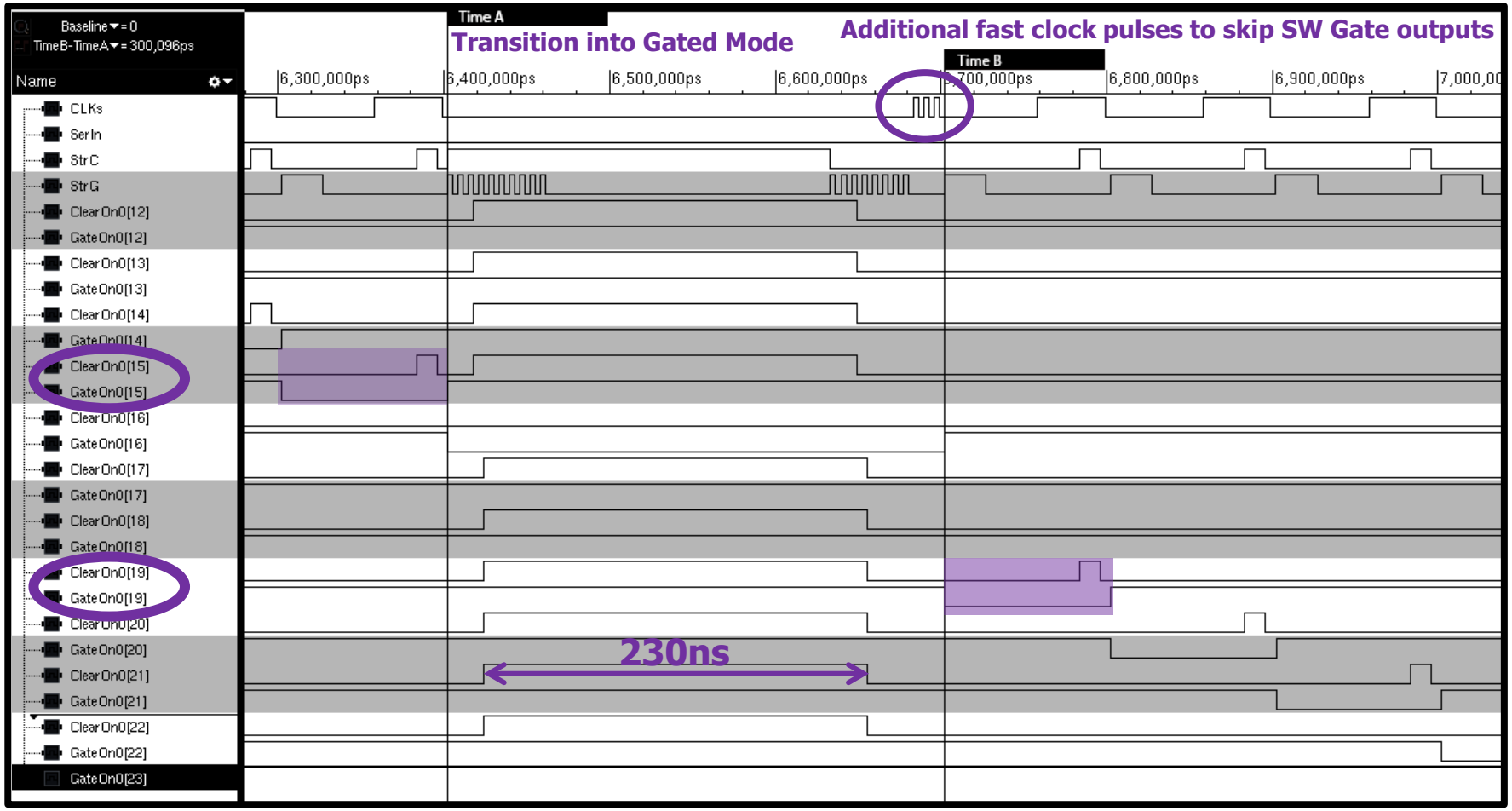
- DHE adapter board for external VETO trigger is available and tested
- dedicated firmware for the Gated Mode test in the lab also available and tested @ TUM
- system test with EMCM and small PXD9 matrix planned for next week @ HLL



Unfortunately I missed to take a photo …

Gated Mode Verification

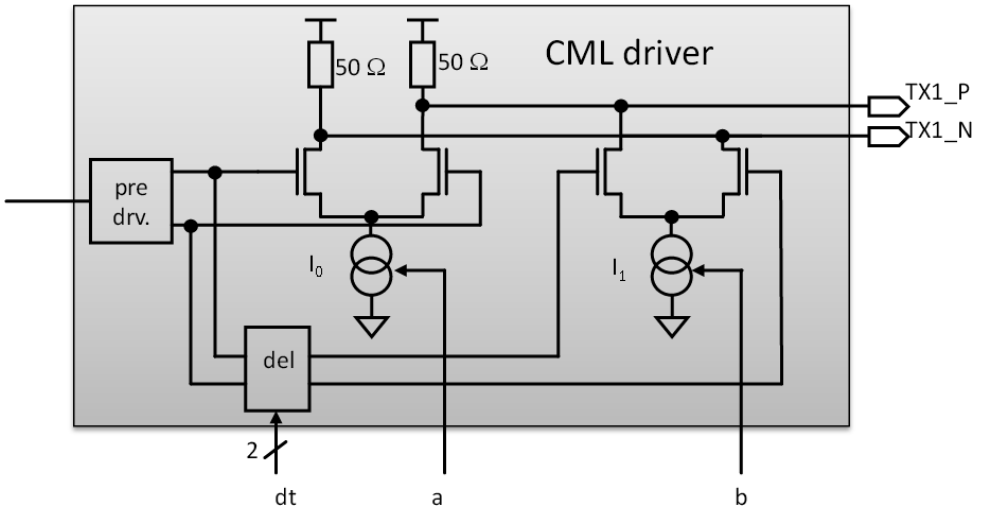
- Verilog simulation to make sure that the Switcher sequence is correct
- Switcher behavior was verified on hybrid4 test board

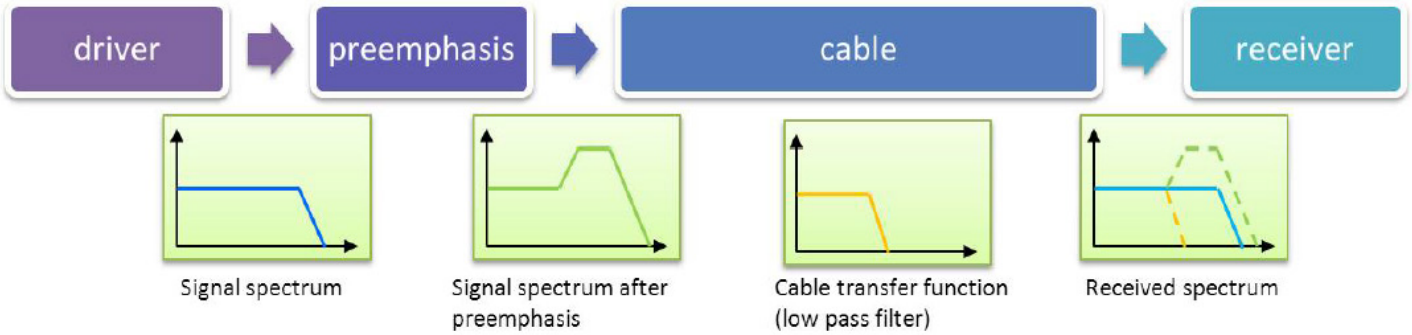


DHPT serial link – parameters of the pre-emphasis

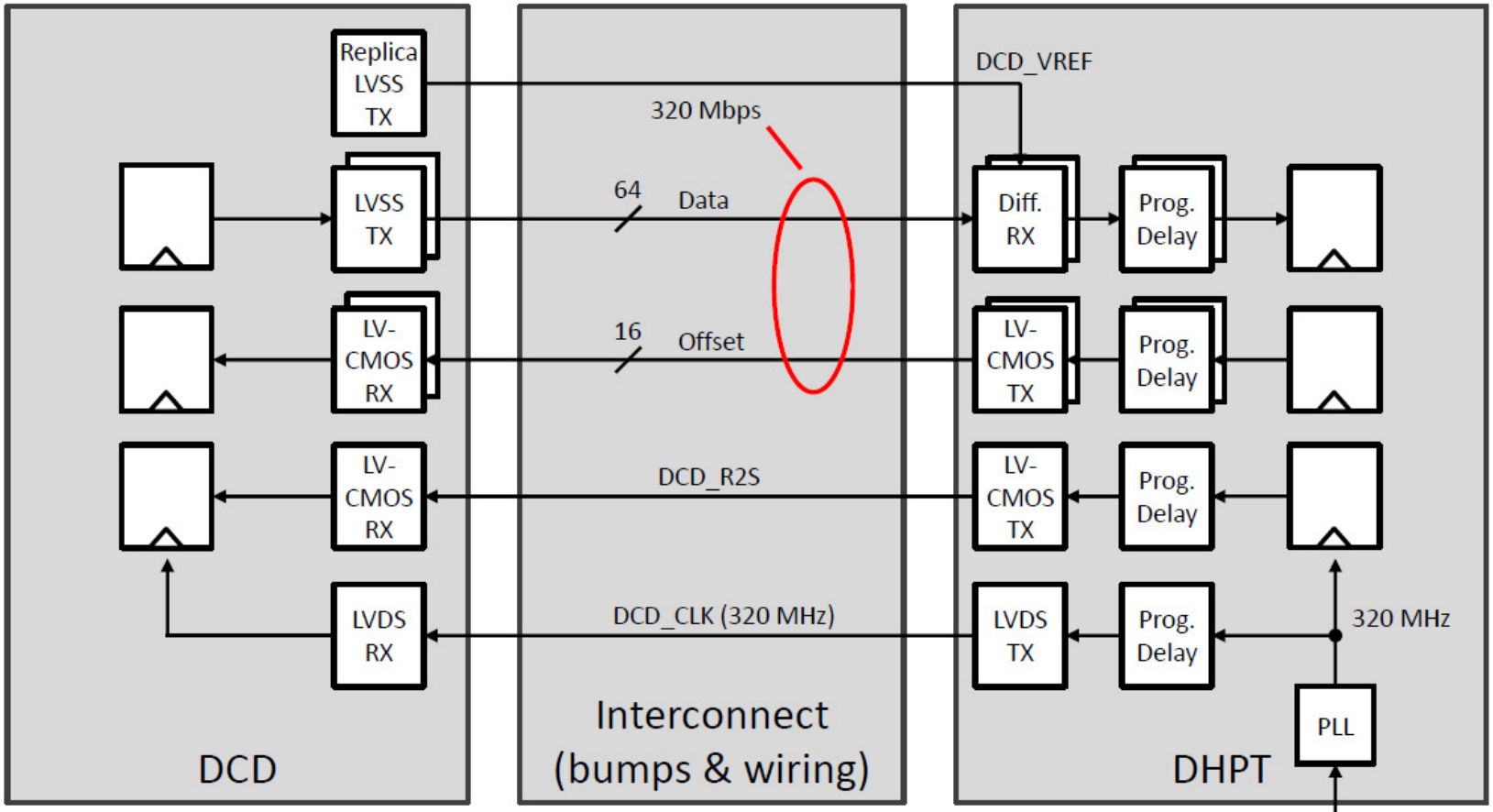
with this scan the parameters for the pre-emphasis are determined

	Register Name	Register Length
a	IDAC CML TX BIAS	256
b	IDAC CML TX BIASD	256
c (dt)	pll cml dly sel	4





DCD <-> DHPT communication – timing adjustment



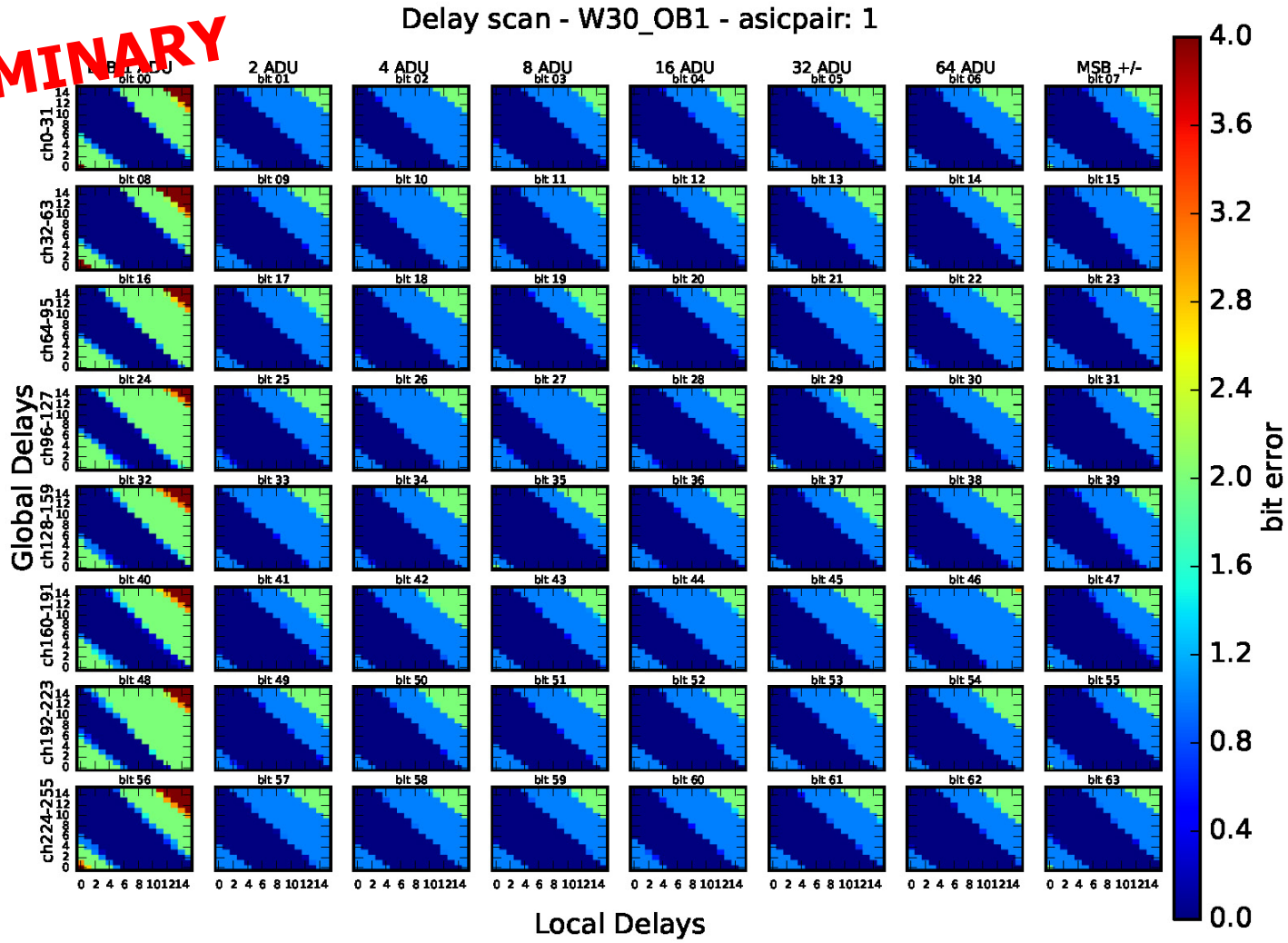
8 links with 8 data + 2 offsets bits each

ADC sample rate = 10MHz

32 ADCs per link → 320 Mbps

scan the parameters of the delay elements to do the phase adjustment at the DHPT receivers

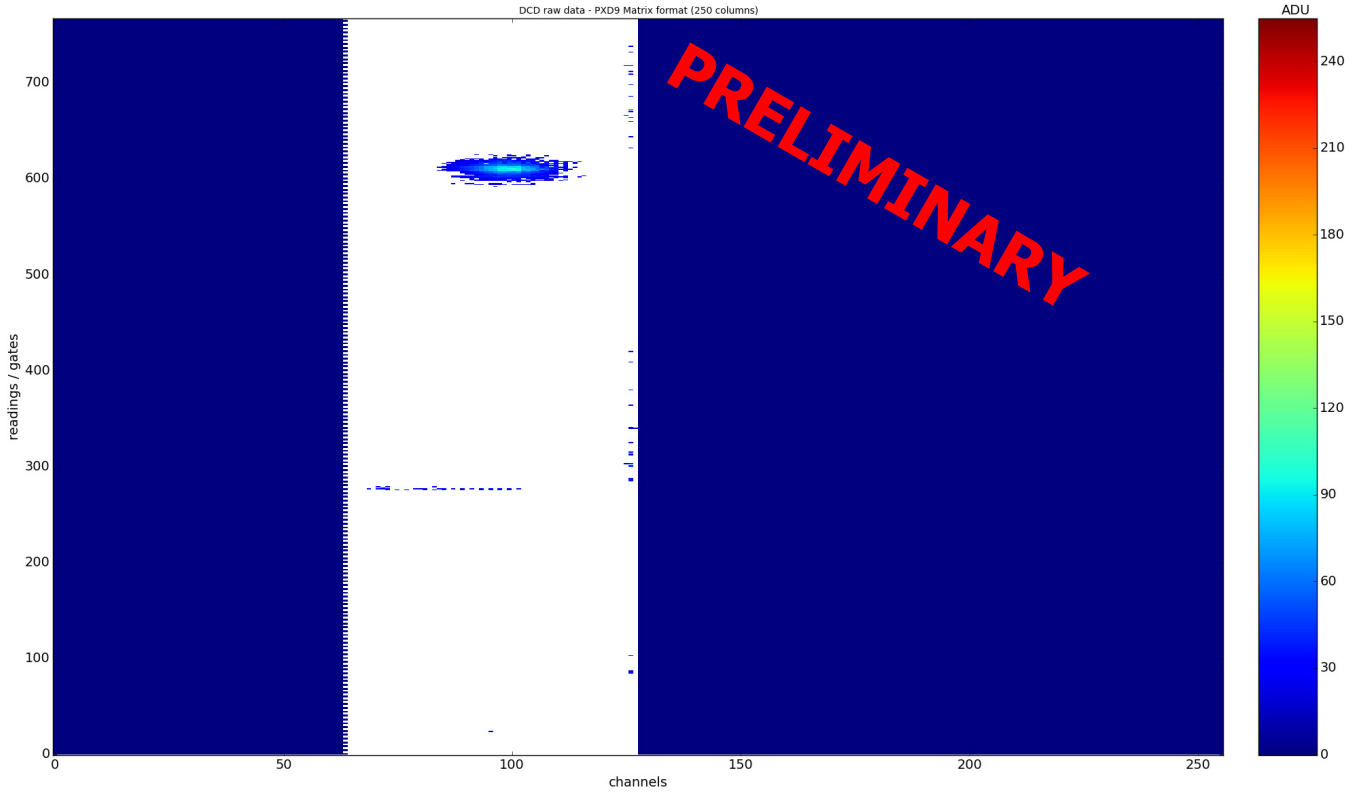
DCD <-> DHPT communication – timing adjustment



PXD9 – delay element scan @ 250Mpbs

Measure DEPFET response (Source, Laser spot, homogeneously illuminated)

PXD9 W30-OB1



- Laser Spot in the area between SW5 and SW6
- Zero Suppressed read-out of DHPT2 only

PXD9 Pilot Verification Plan @ BPAC

To verify the routing of the 3 metal layers of the PXD9 module the following measurements have to be done:

	26.-30. Oct	2.-6. Nov	9.13. Nov	16.-20. Nov	23.-27. Nov	30. Nov - 4.Dec.	Dec. 7th
CW	44	45	46	47	48	49	50
HLL (pxdtest2)	sampling point scan	increase to nominal freq.	zero suppressed data	gated mode	DEPFET Lab F2F Meeting @ HLL		**Go for PXD9 metallization or agreement on the necessary changes**
	pedestal/noise all DCDs	DHPT serial link IBERT	pedestal compression				
		DHPT serial link oscilloscope	Cd109 spectrum				
		DCD <-> DHPT (delay)	Laser spot				
		sampling point scan					
		pedestal/noise all DCDs					
HLL (pxdtest4)			Hybrid 7 Testing to verify OF/IB balcony and EOS layout				