SI LAB
Silizium Labor Bonn

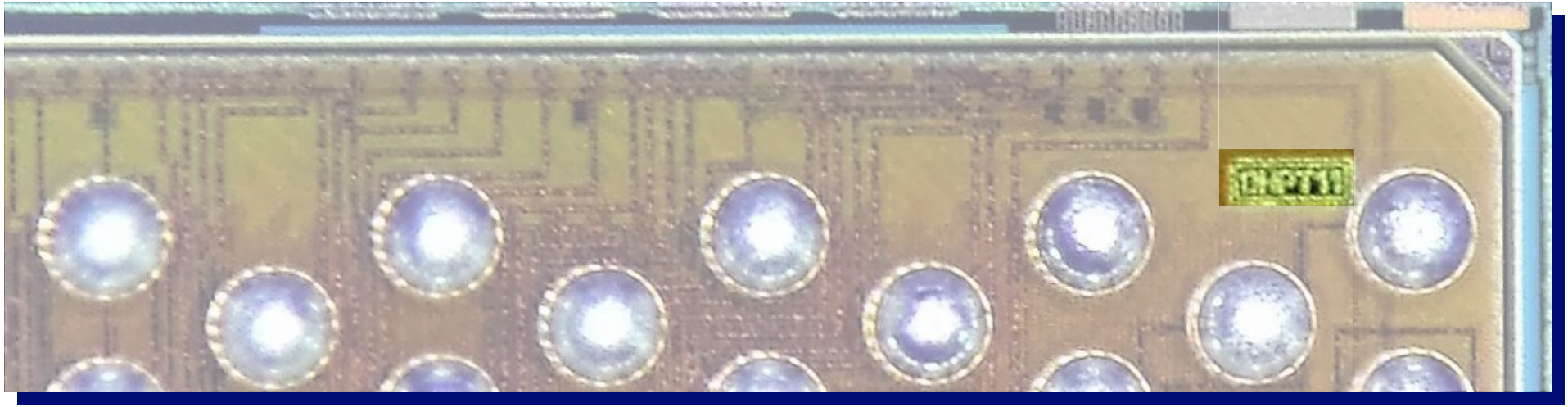
universitätbonn

DHPT1.0 Comparision

9th VXD Belle II Workshop
13-15 Jan. 2016, Valencia Spain

Leonard Germic
Carlos Marinas, Hans Krüger, Norbert Wermes
University of Bonn
ボン大学

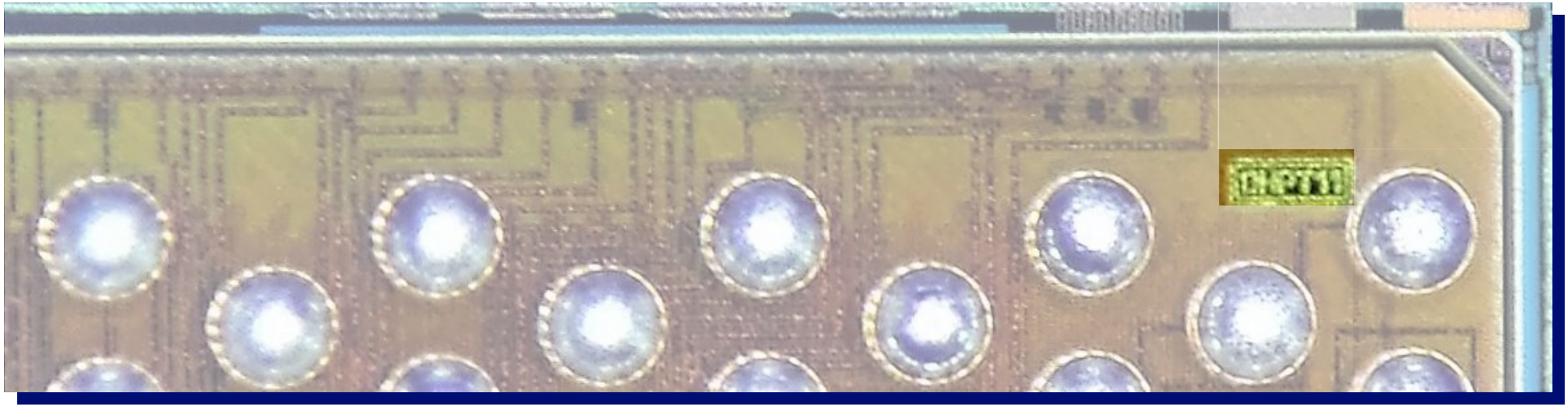
Changes from DHPT1.0 to DHPT1.1



Results

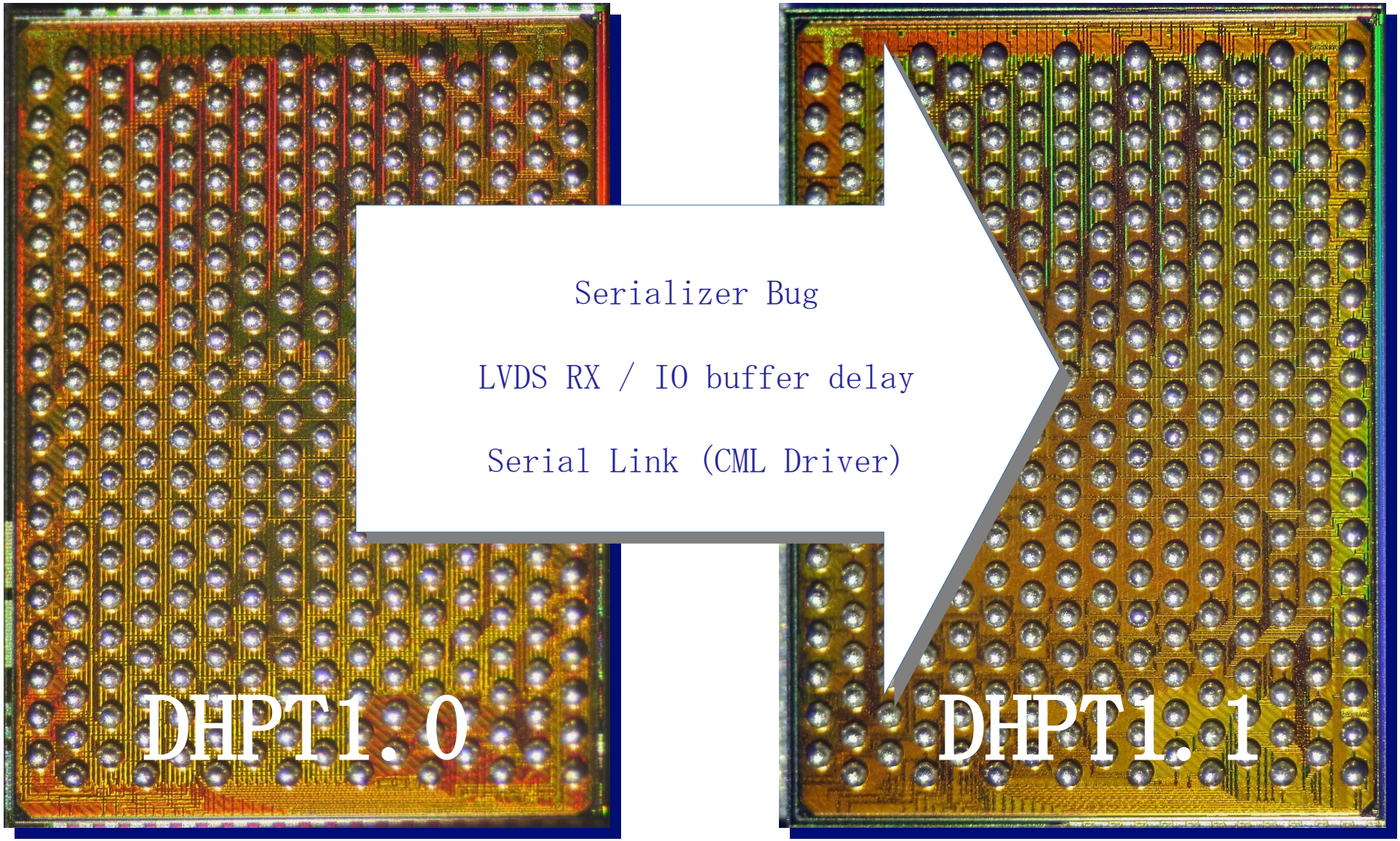
universitätbonn

Changes from DHPT1.0 to DHPT1.1



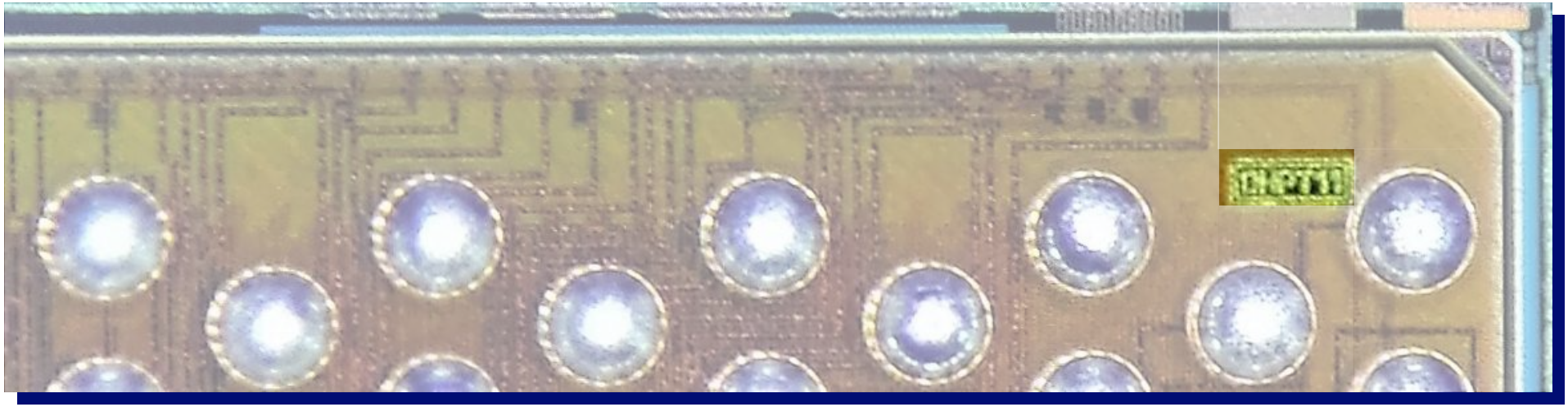
Results

universitätbonn



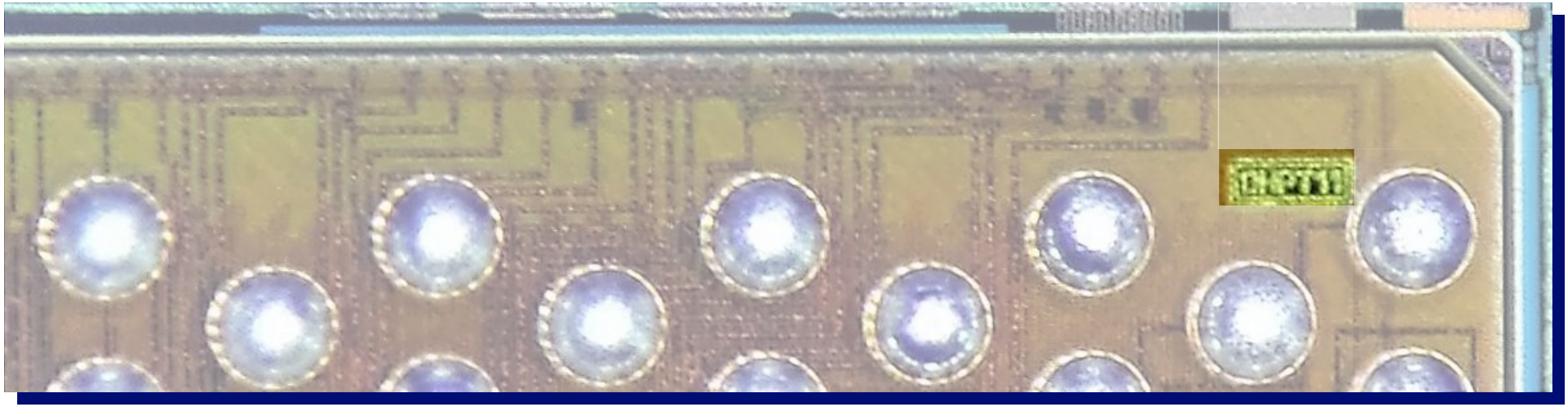
universitätbonn

Changes from DHPT1.0 to DHPT1.1



Results

Changes from DHPT1.0 to DHPT1.1



Results Serializer Bug

Serializer Bug

universitätbonn

- Mistake made during extracting and simulating the layout with all process corners

- Serializer works, but VCC and/or GCK have to be adjusted:
  - GCK= 80 MHz → VCC = 1.6V (works but should not be applied for a long time)
  - GCK= 60 MHz → VCC = 1.4V (ok)

- Manufacturer test data ➔ wafer batch has „slow NMOS“ (too high threshold)

PARAMETER BY LOT:		SPEC LO	SPEC HI	MIN	MAX	MEAN	STD DEV
VTl_N4	(N/.3/.06/1)	0.300	0.490	0.368	0.490	0.423	0.029
Isof_N4	(N/.3/.06/1)	-1.400E-07	0.000	-8.958E-10	-3.833E-11	-2.339E-10	2.063E-10
Isat_N4	(N/.3/.06/1)	0.491	0.735	0.547	0.673	0.593	0.031

Digital checks for DHPT 1.1:

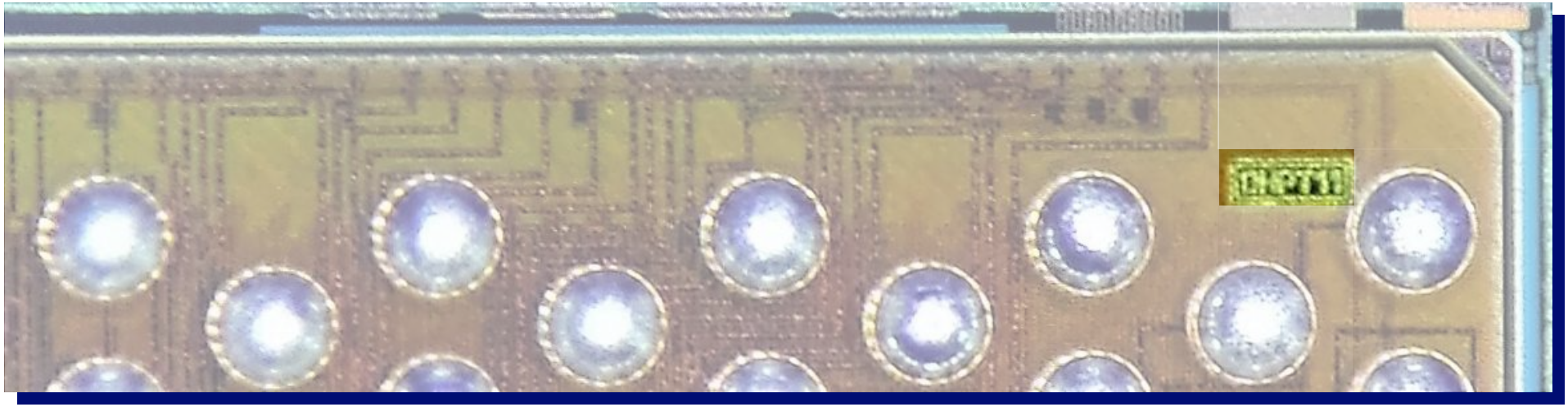
Jtag communication DHE & DHPT

Memory tests

All digital tests passed

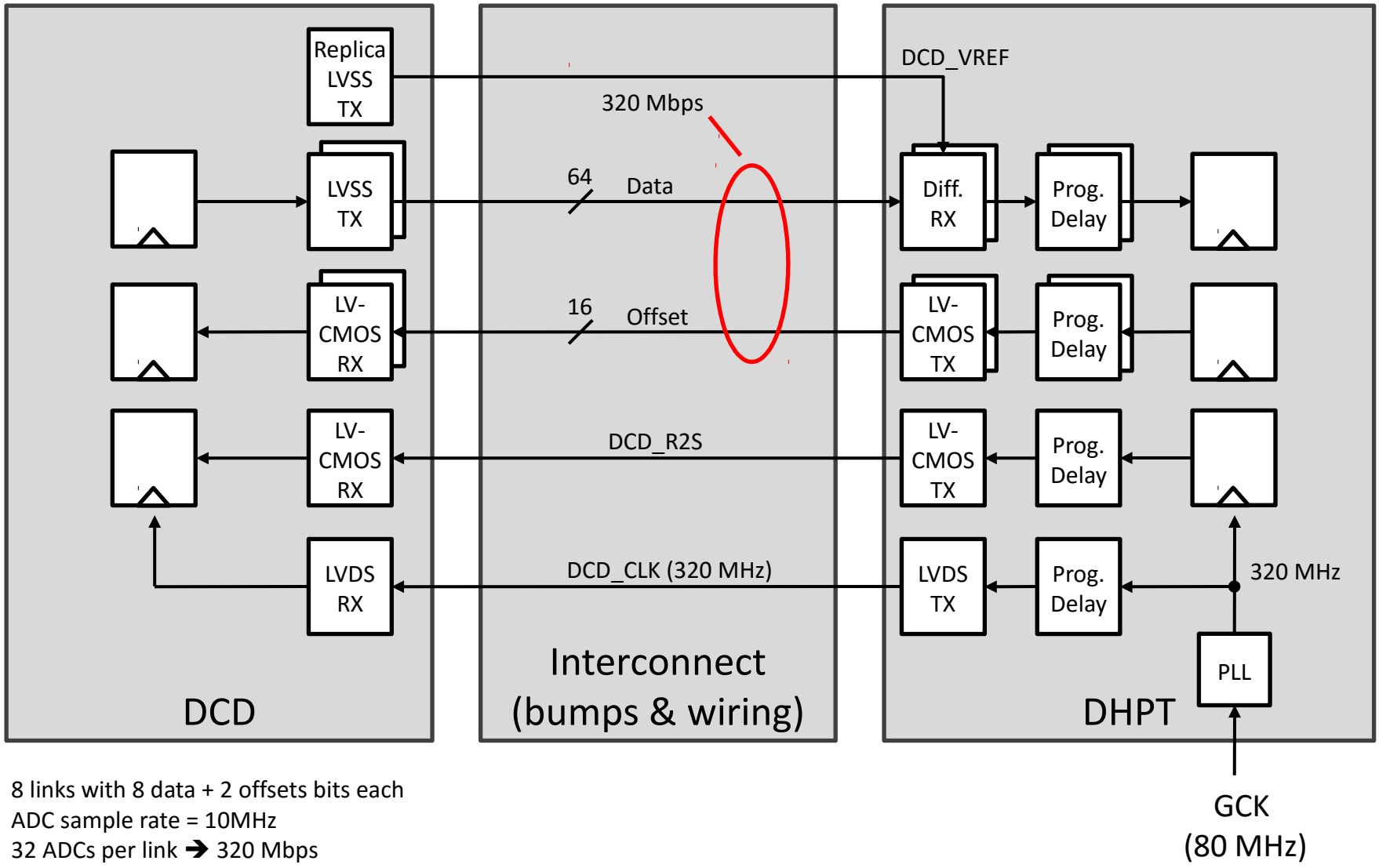
Link established
(down to VDD 1.25V !unsensed!)

Changes from DHPT1.0 to DHPT1.1



Results LVDS RX / IO buffer delay

DCD – DHPT Interface Block Diagram

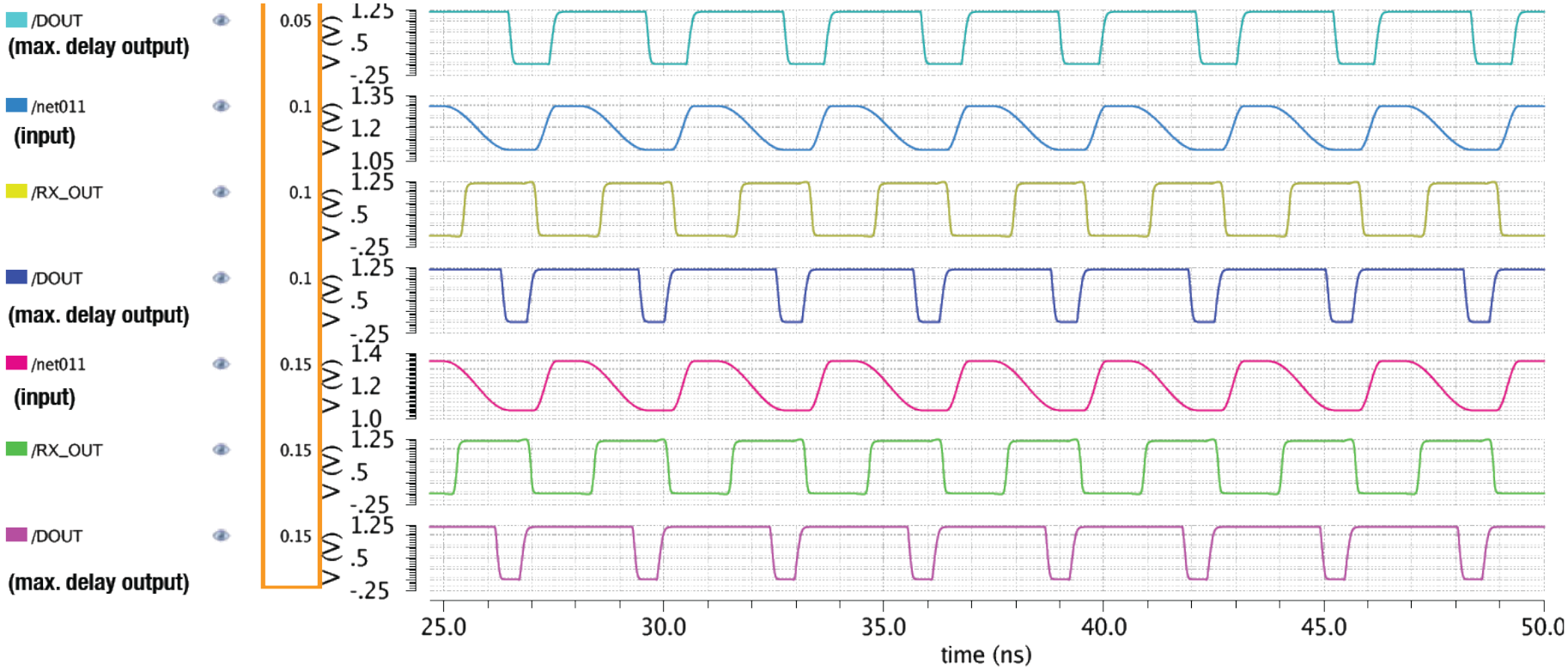


8 links with 8 data + 2 offsets bits each
ADC sample rate = 10MHz
32 ADCs per link ➔ 320 Mbps

Duty cycle distortion

universitätbonn

- Duty cycle distortion was overlooked during DHPT 1.0 sign-off



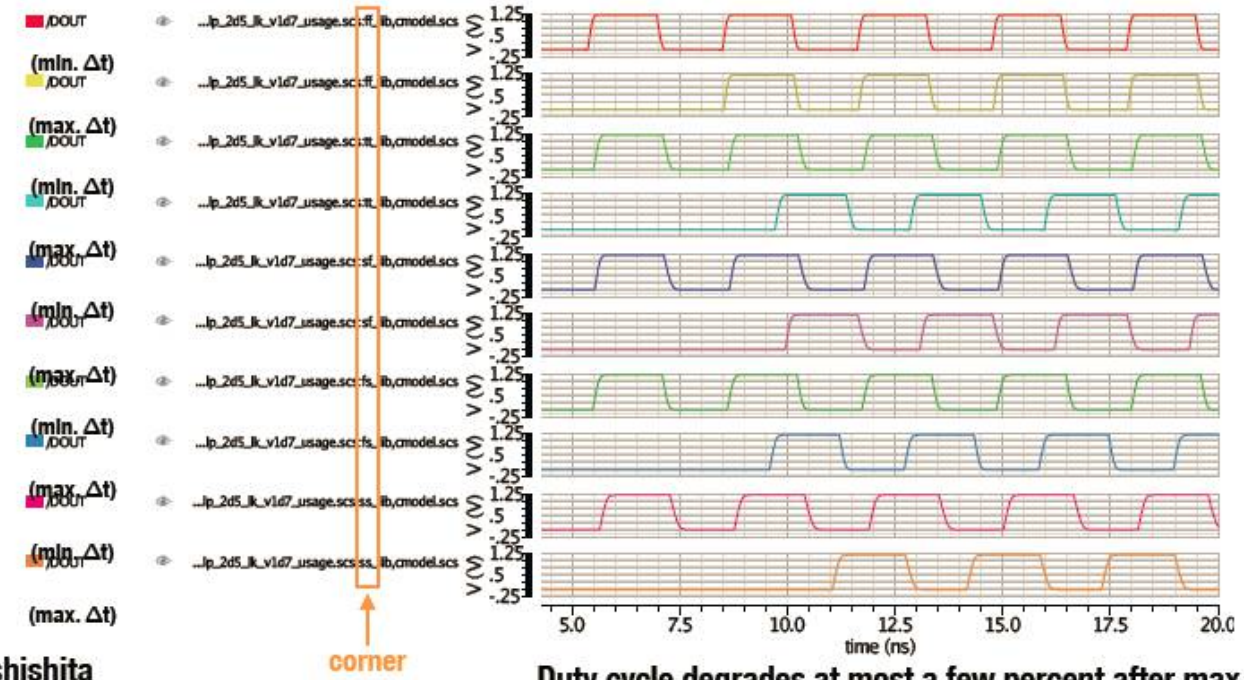
Delay Element Modification

- Custom delay elements made out of identical inverters

All corners covers 3.125 ns (←320 MHz).

Max. delay time with extracted model

	Δt	duty cycle (min. Δt)	duty cycle (max. Δt)
tt	4.20 ns	52.0%	53.3%
ff	3.15 ns	51.4%	52.2%
fs	4.10 ns	51.6%	51.8%
sf	4.43 ns	52.2%	54.9%
ss	5.42 ns	52.8%	54.9%



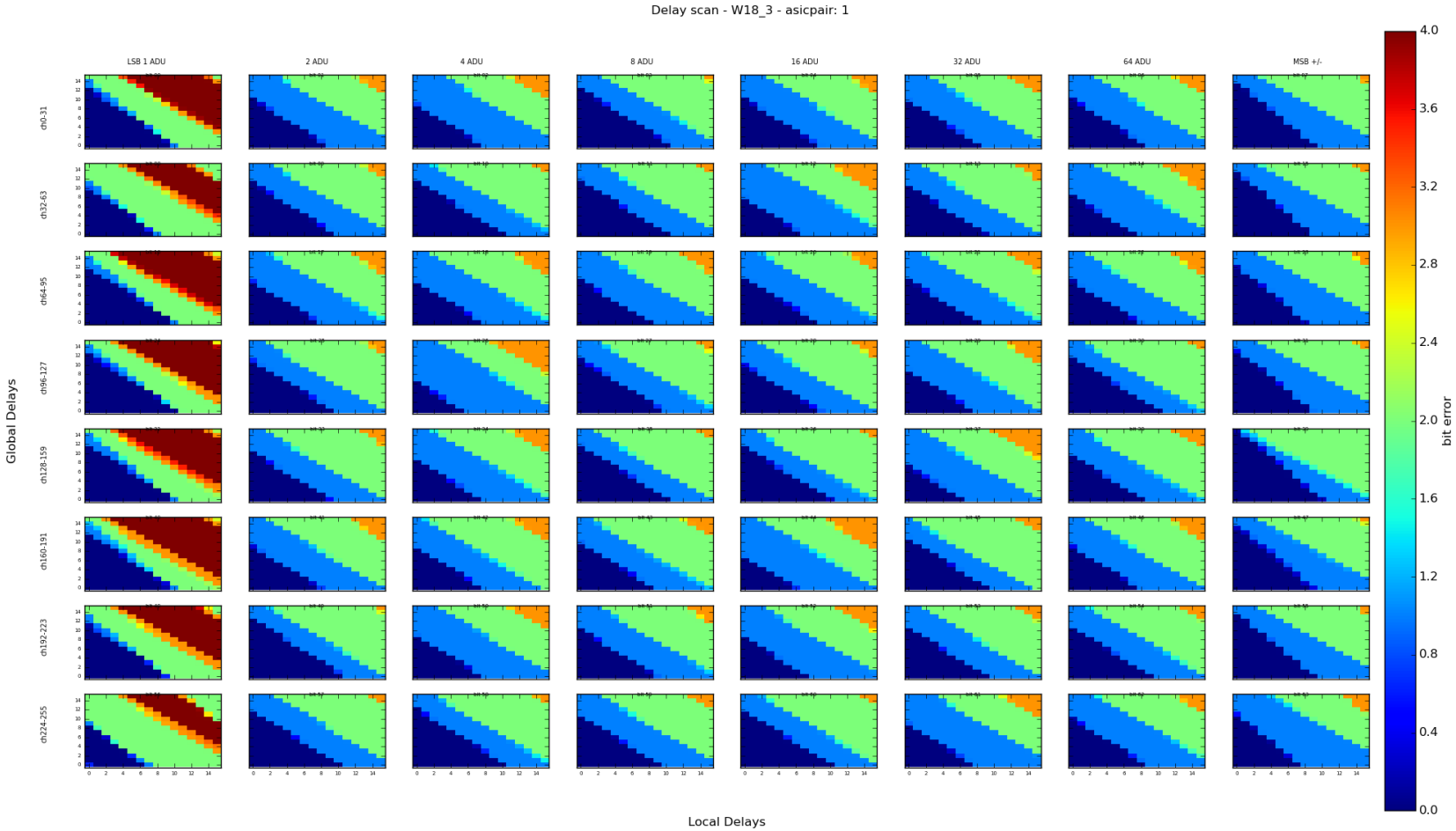
07.04.2015, T.Kishishita

Duty cycle degrades at most a few percent after max. delay.

universitätbonn

DHPT 1.0: Duty cycle distortion of signal present

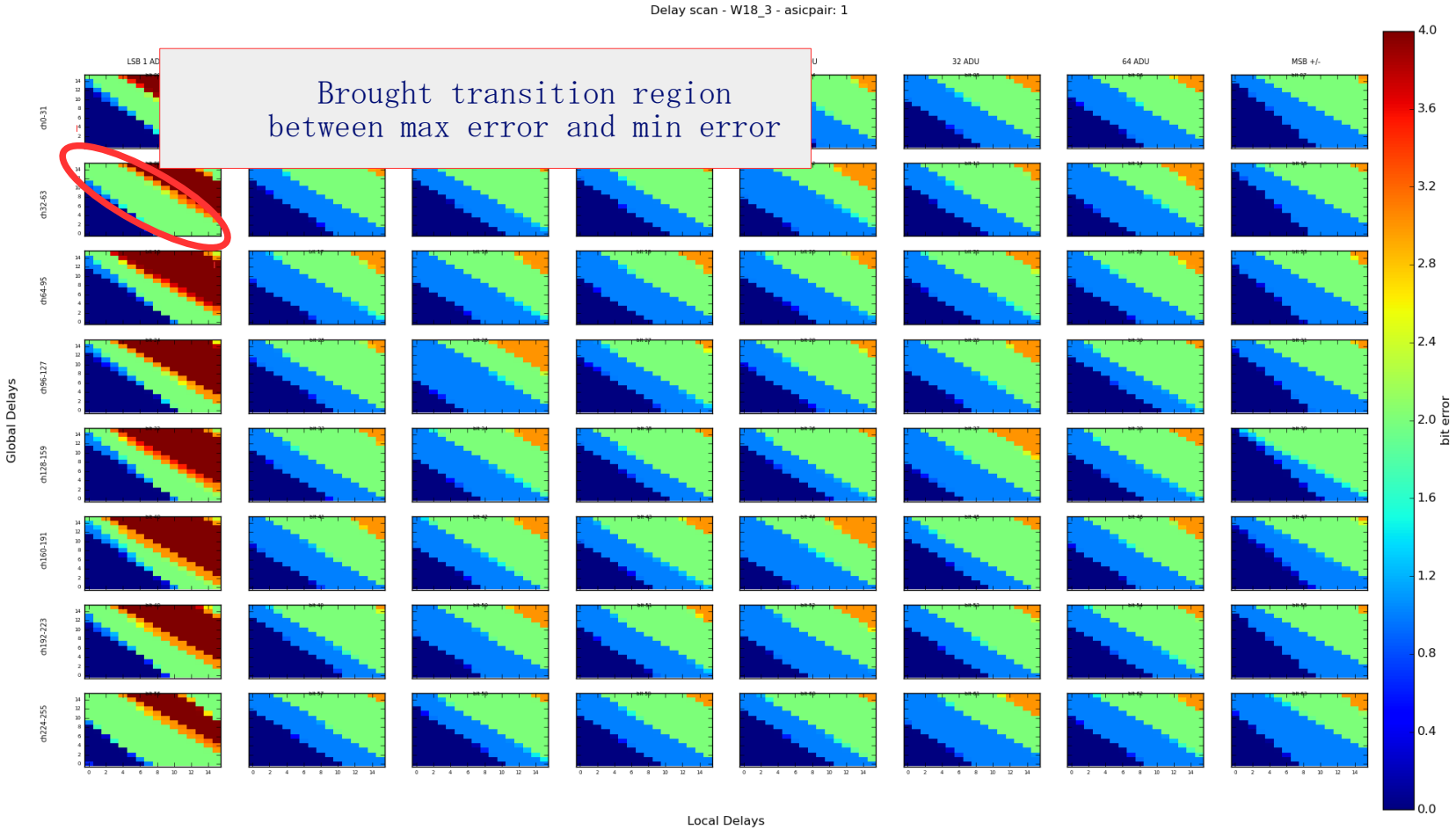
- Each inverter pairs introduces a duty cycle distortion



universitätbonn

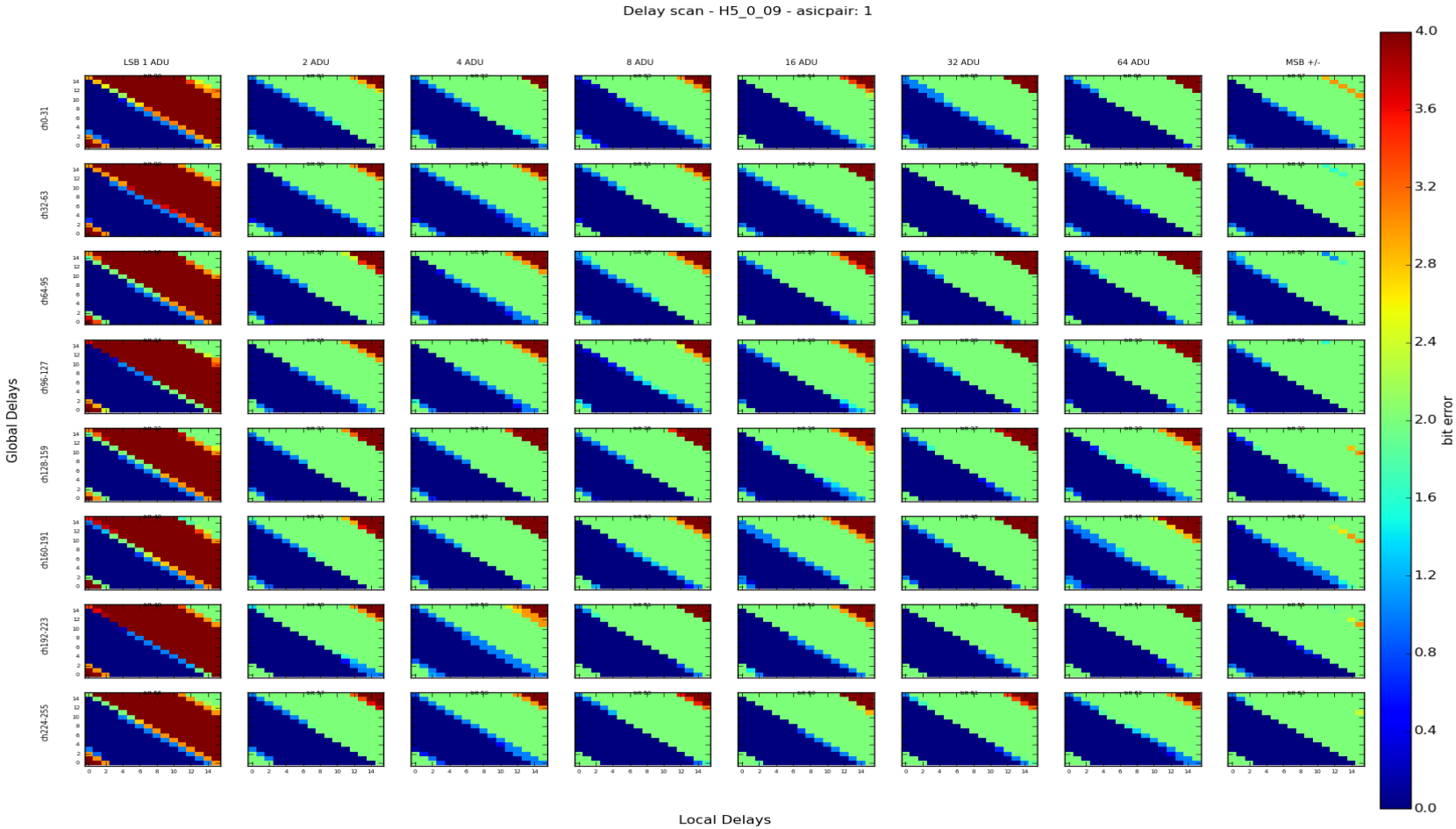
DHPT 1.0: Duty cycle distortion of signal present

- Each inverter pairs introduces a duty cycle distortion



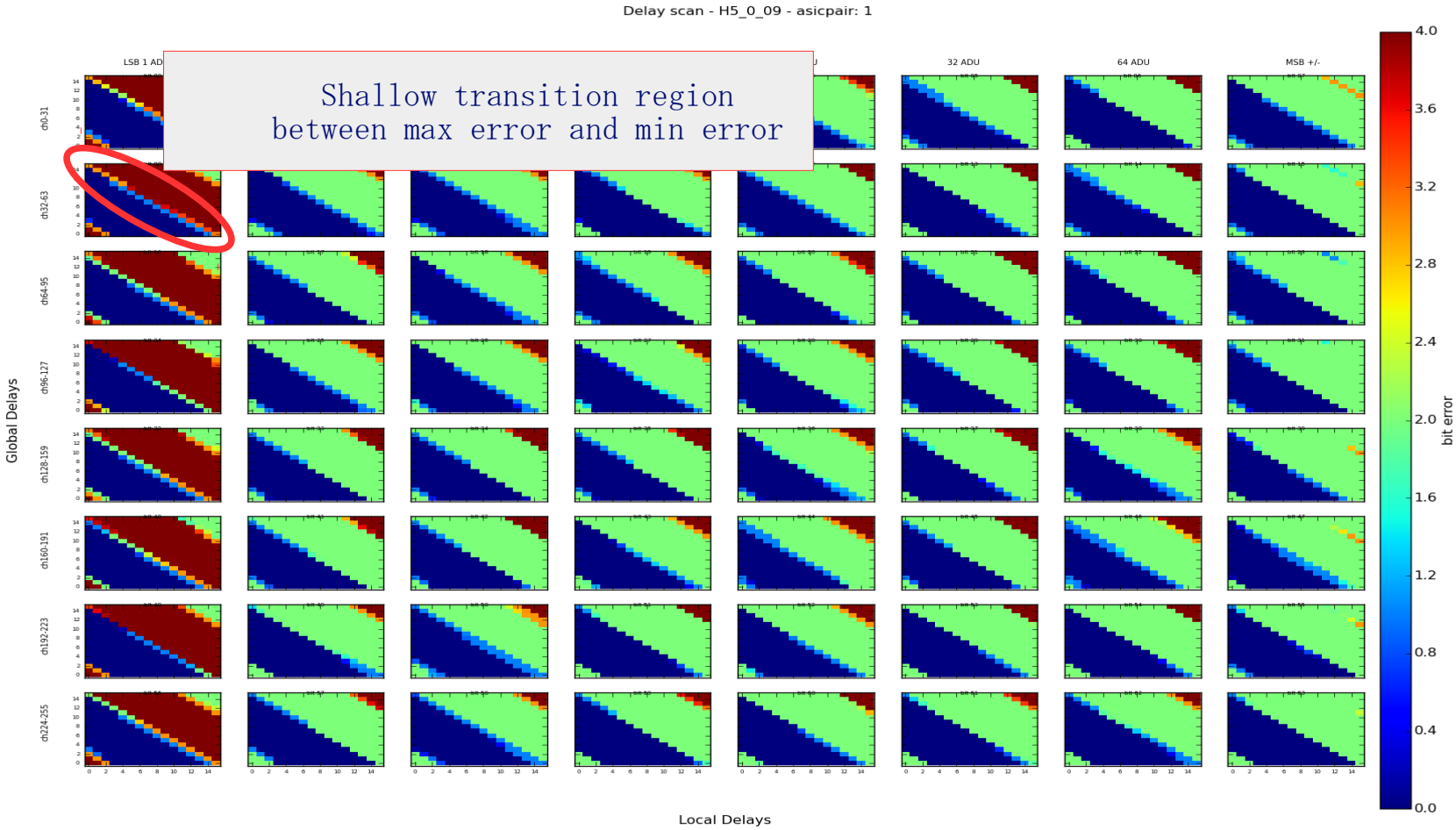
universitätbonn

DHPT 1.1: No duty cycle distortion of signal present

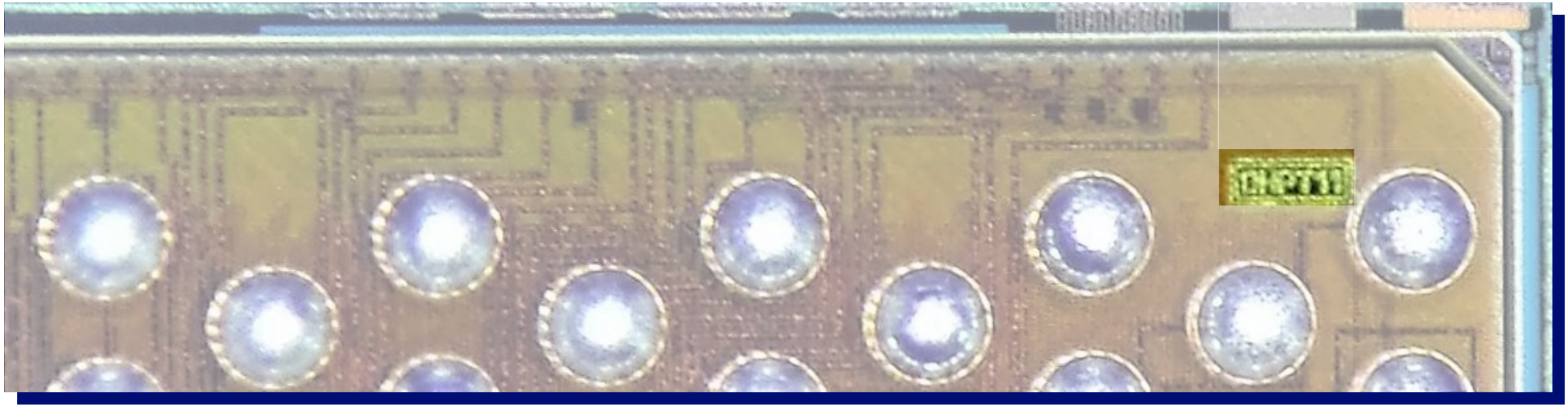


universitätbonn

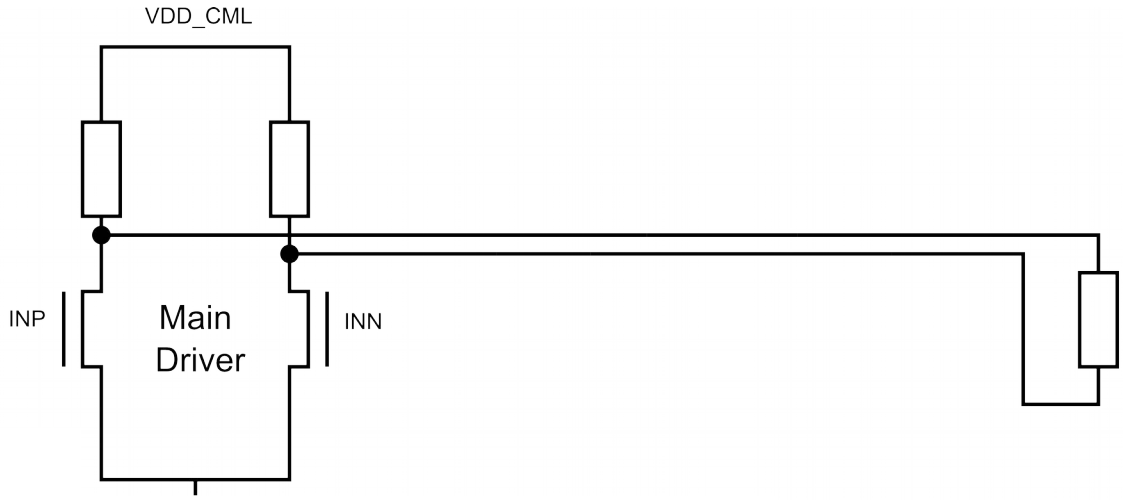
DHPT 1.1: No duty cycle distortion of signal present

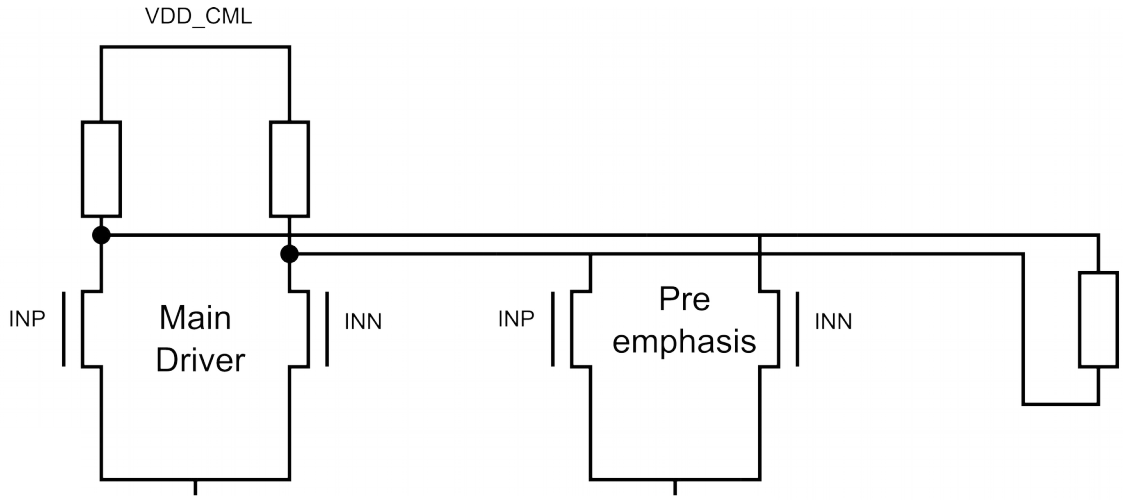


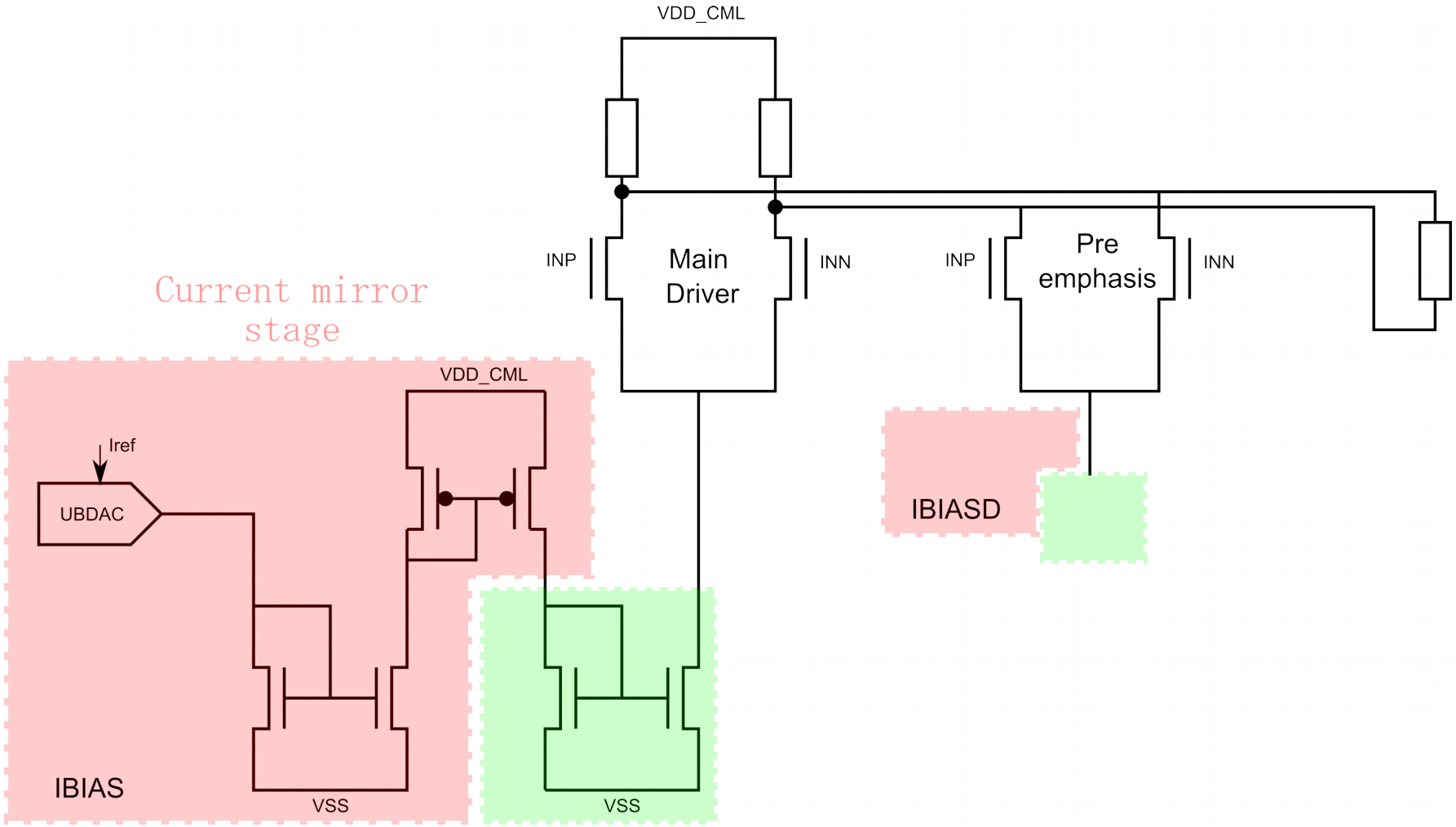
Changes from DHPT1.0 to DHPT1.1



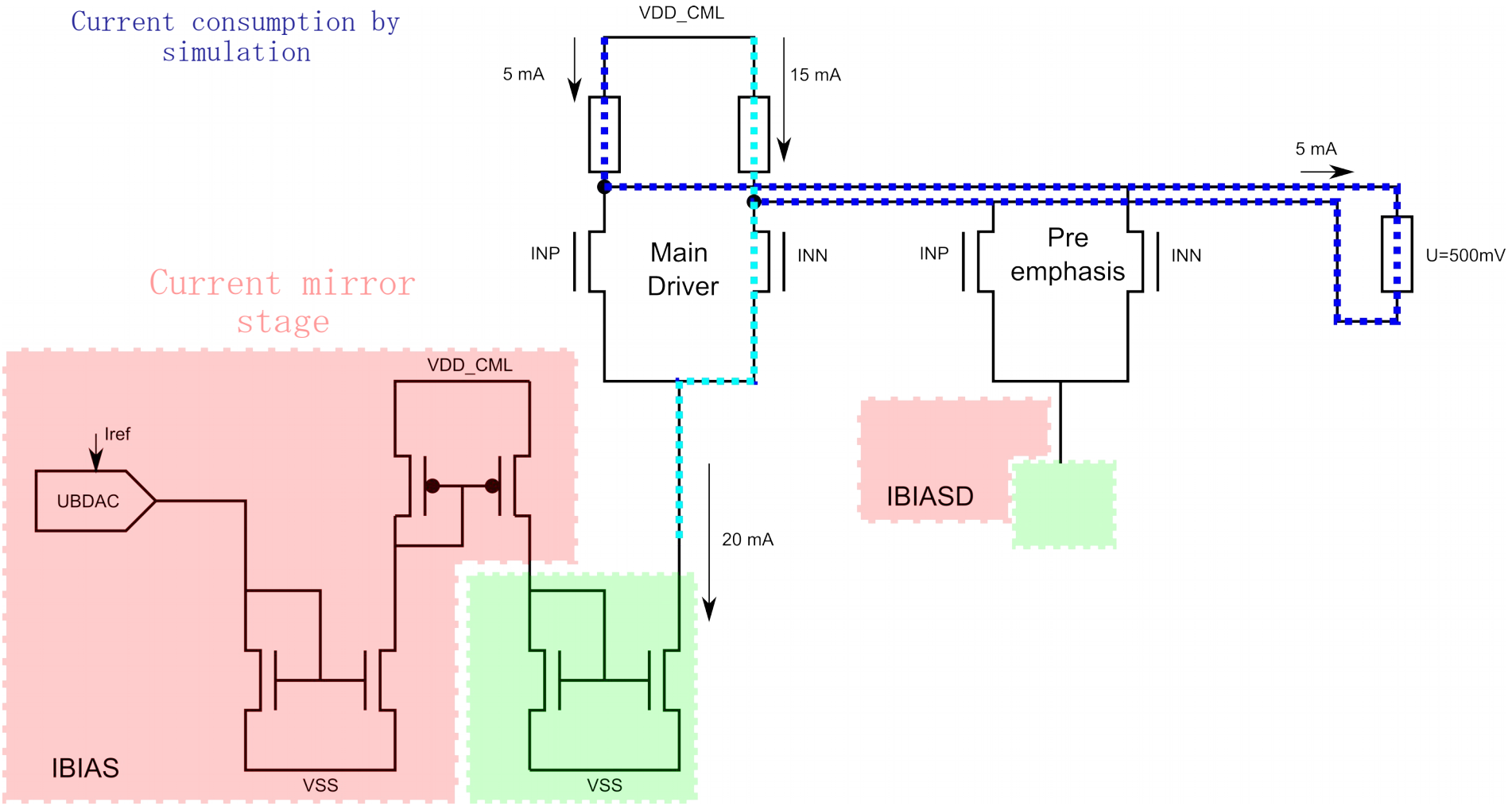
Results Serial Link (CML Driver)

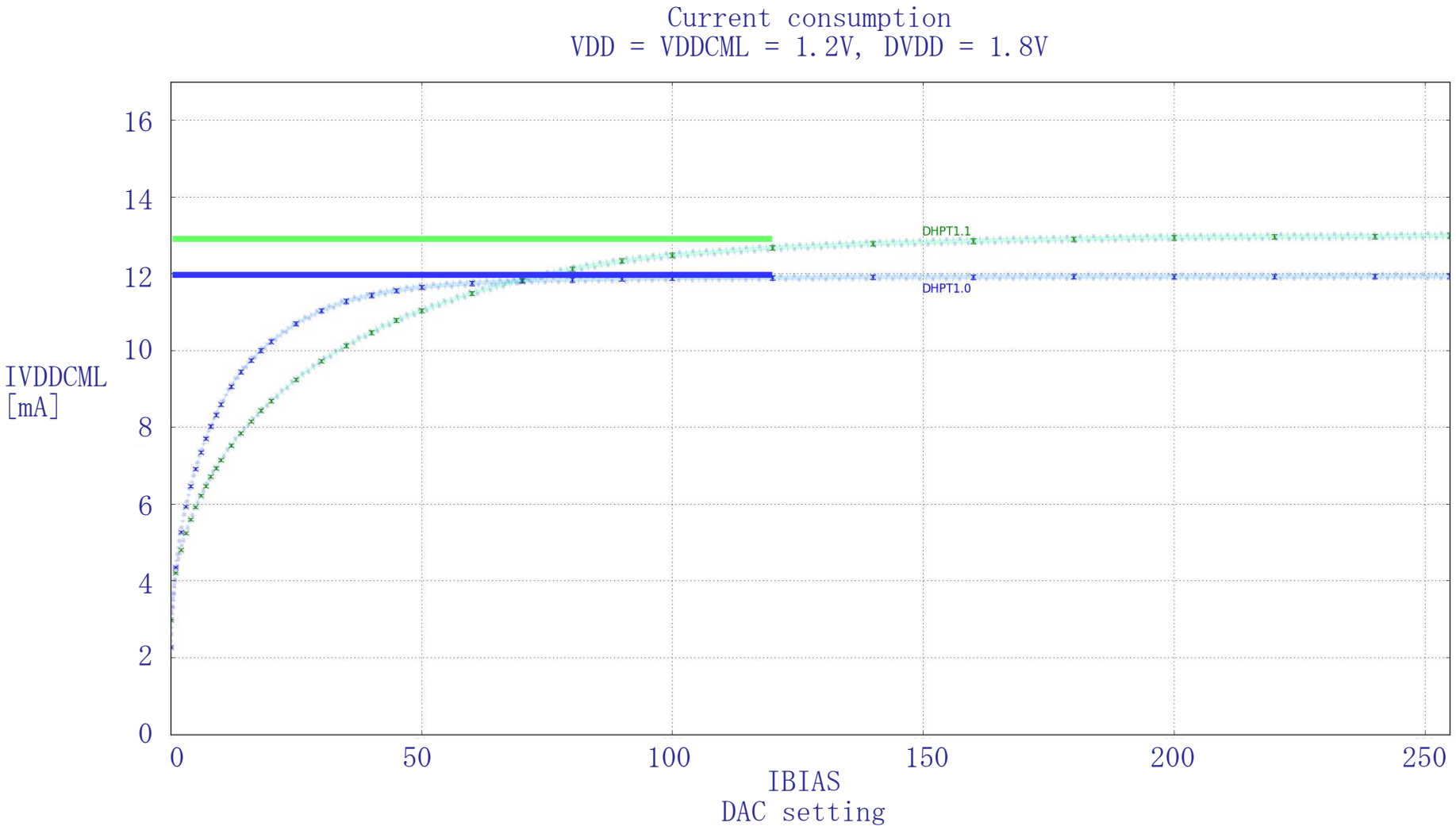

VDD_CML
INP
Main
Driver
INN

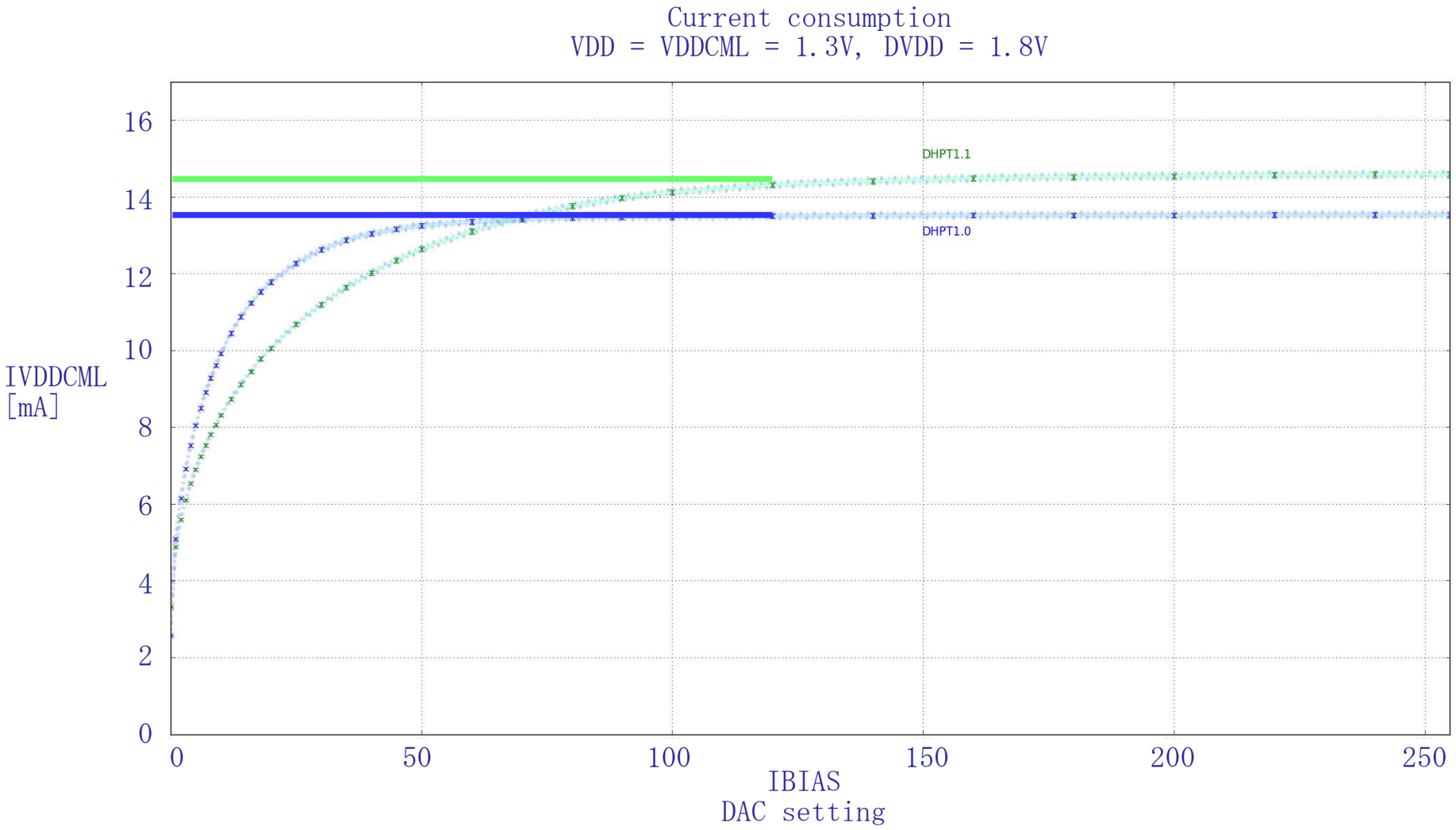

VDD_CML
INP
Main
Driver
INN
INP
Pre
emphasis
INN


VDD_CML
INP
Main
Driver
INN
INP
Pre
emphasis
INN
Current mirror
stage
VDD_CML
Iref
UBDAC
IBIASD
IBIAS
VSS
VSS

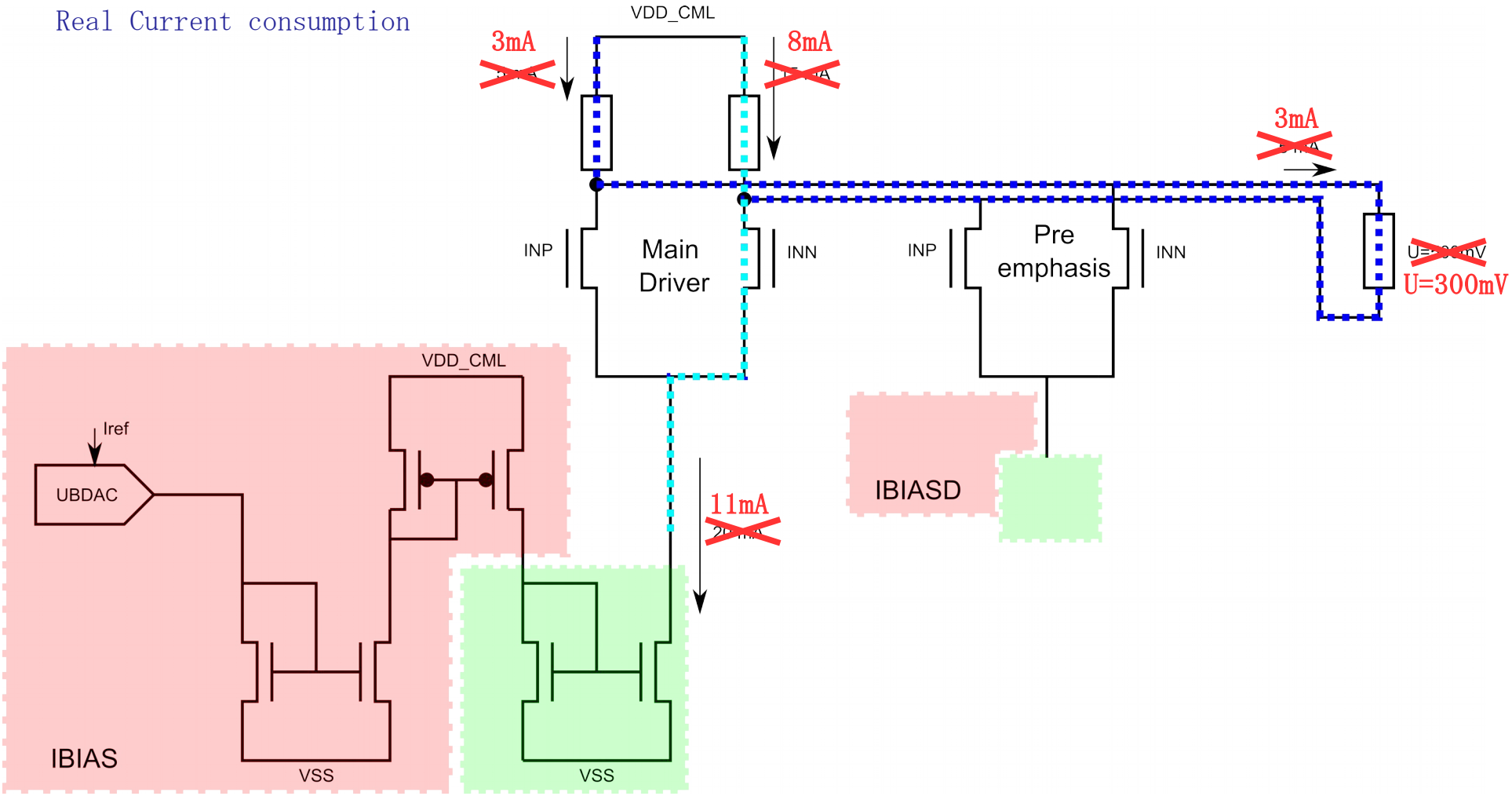
Current consumption by simulation




Current consumption
VDD = VDDCML = 1.2V, DVDD = 1.8V
IVDDCML [mA]
16
14
12
10
8
6
4
2
0
0
50
100
150
200
250
IBIAS DAC setting
DHPT1.1
DHPT1.0

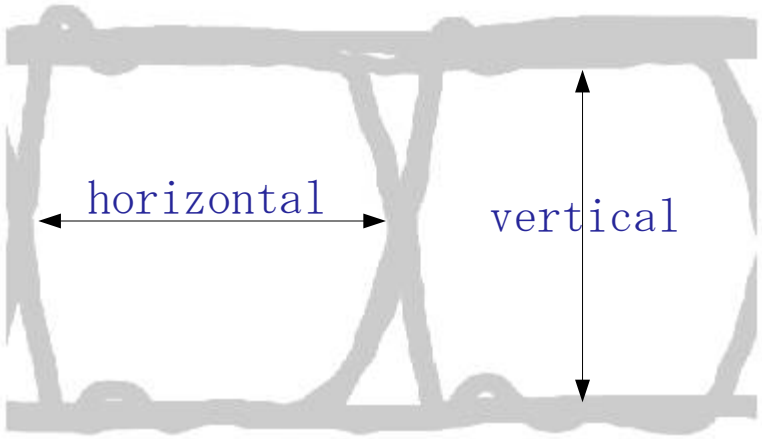

Current consumption
VDD = VDDCML = 1.3V, DVDD = 1.8V
IVDDCML [mA]
16
14
12
10
8
6
4
2
0
0
50
100
150
200
250
IBIAS DAC setting
DHPT1.1
DHPT1.0

Real Current consumption



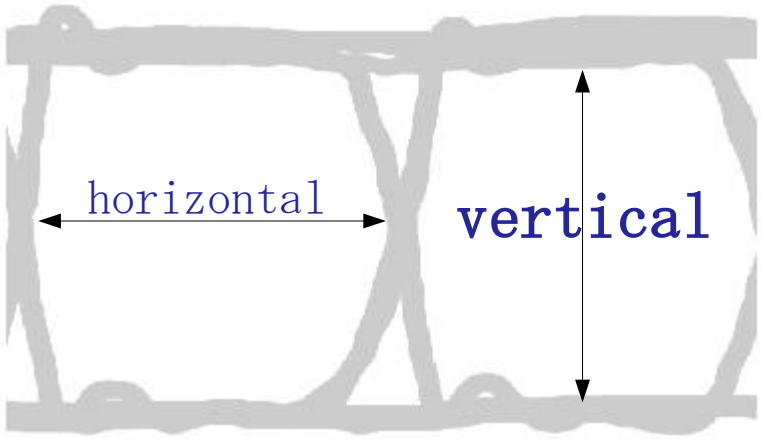
CML driver

Eye diagram measurements



CML driver

Eye diagram measurements



DHE specification

From Virtex-6 User Guide

Table 4-26: **RX Margin Analysis Ports**

Port	Dir	Clock Domain	Description
RXDATA[31:0]	Out	RXUSRCLK2	The user needs to detect data errors on RXDATA in order to monitor the bit error rate of the link.
DFEEYEDACMON[4:0]	Out	RXUSRCLK2	Average vertical eye height (voltage domain) used by the DFE as an optimization criterion. 11111: Indicates approximately 200 mV_{PPD} of internal eye opening.

5bit value (0-31) for the vertical opening

From Virtex-6 FPGA Data Sheet: DC and Switching Characteristics

Table 17: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125	–	2000	mV
		External AC coupled > 4.25 Gb/s	175	–	2000	mV

Min 125mV vertical opening

universitätbonn

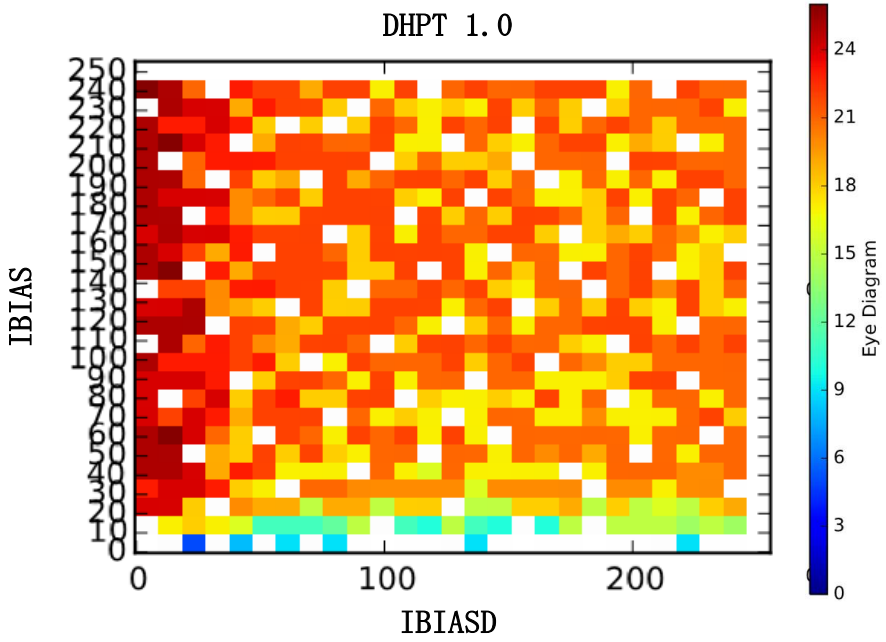
CML driver

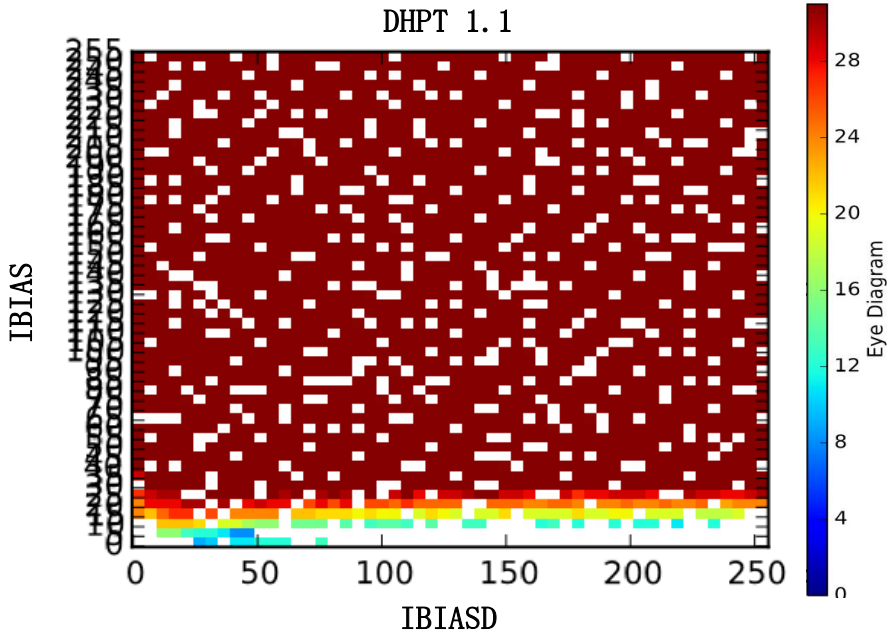
Scan over parameter space

IBIAS, *IBIASD* and *pll_cml_dly*

no receiver equalizing

Examples for pll_cml_dly = 0 and GCK = 62.50 MHz





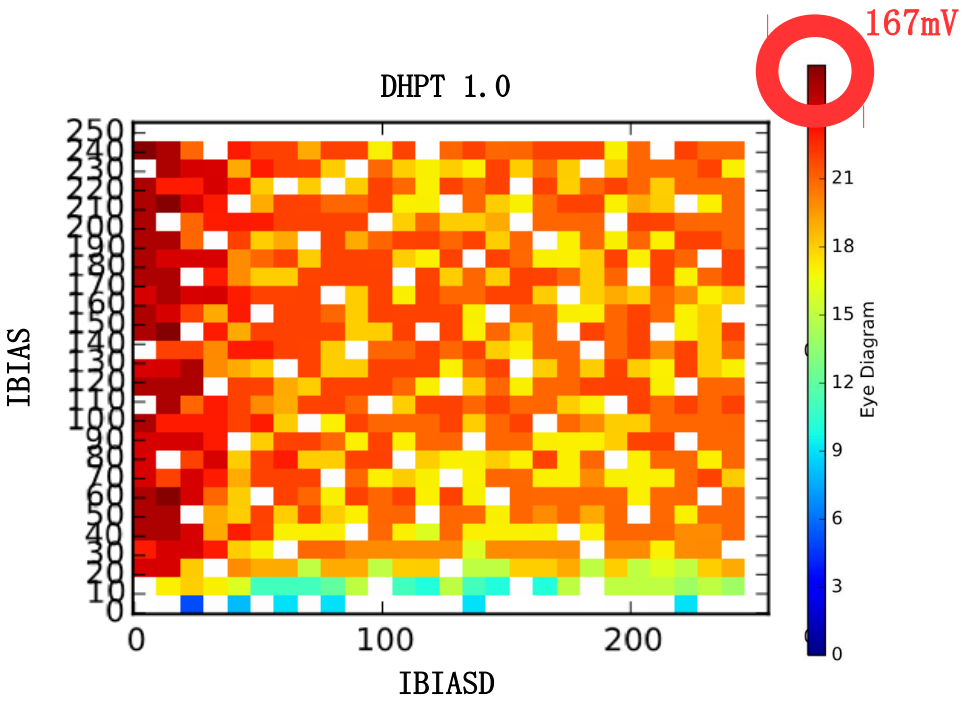
CML driver

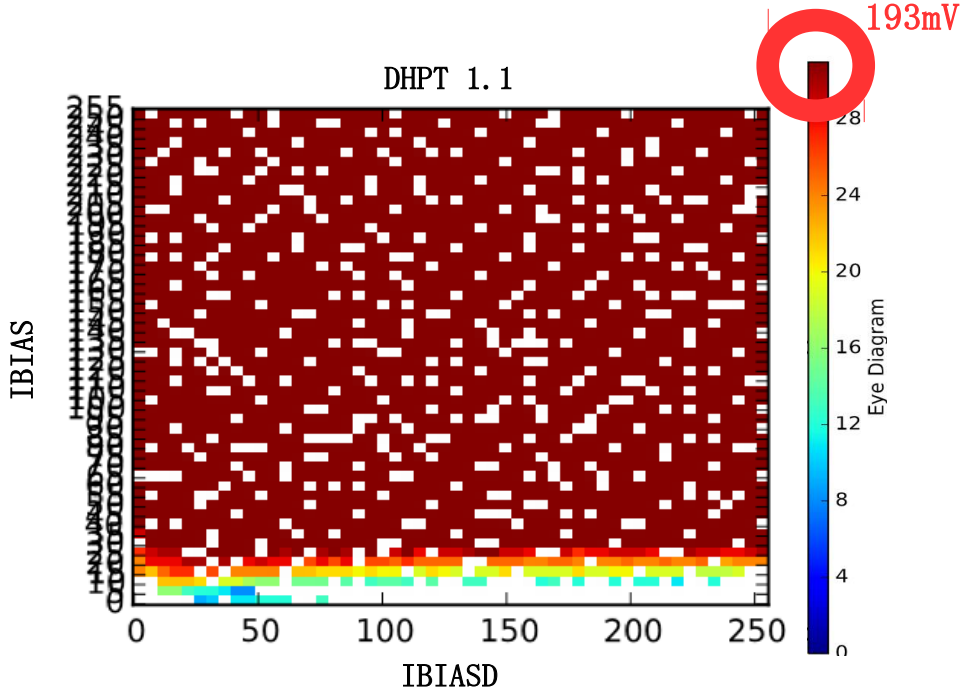
Scan over parameter space

IBIAS, *IBIASD* and *pll_cml_dly*

no receiver equalizing

Examples for pll_cml_dly = 0 and GCK = 62.50 MHz





universitätbonn

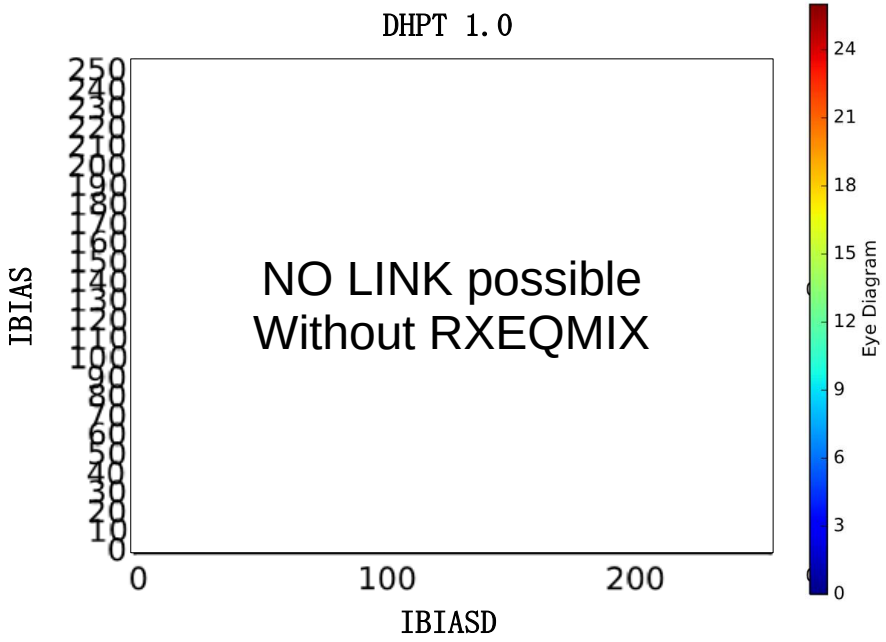
CML driver

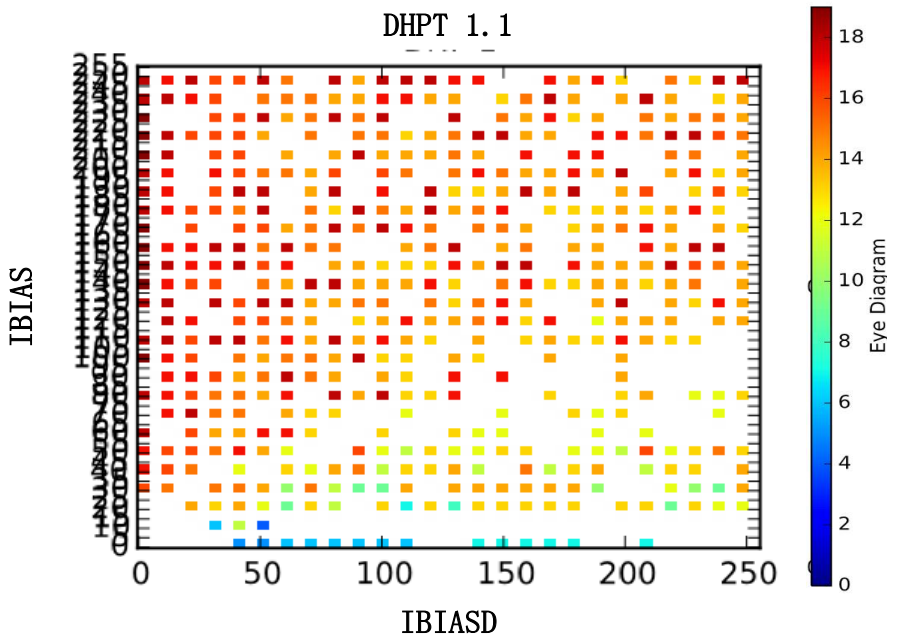
Scan over parameter space

IBIAS, *IBIASD* and *pll_cml_dly*

no receiver equalizing

Examples for pll_cml_dly = 0 and GCK = 76.23 MHz





universitätbonn

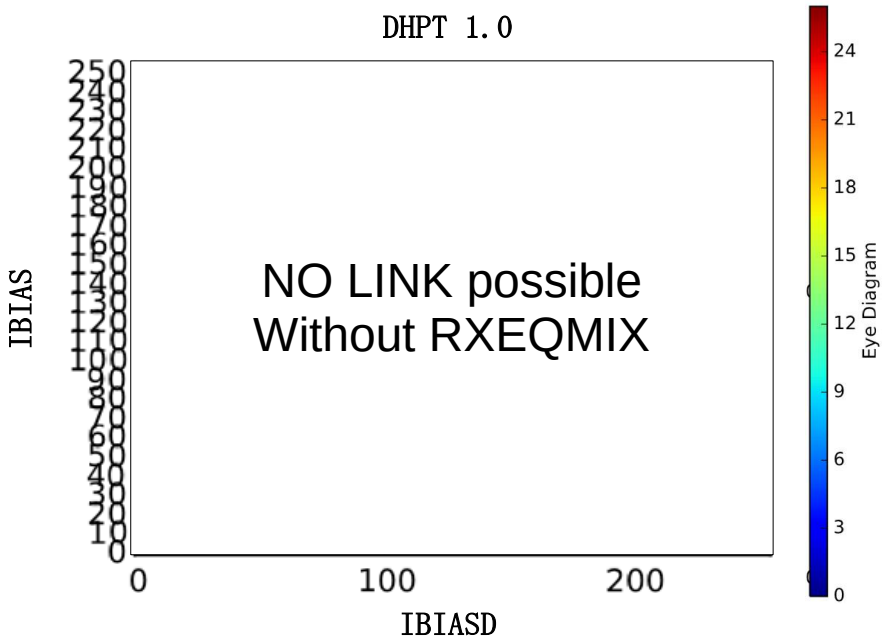
CML driver

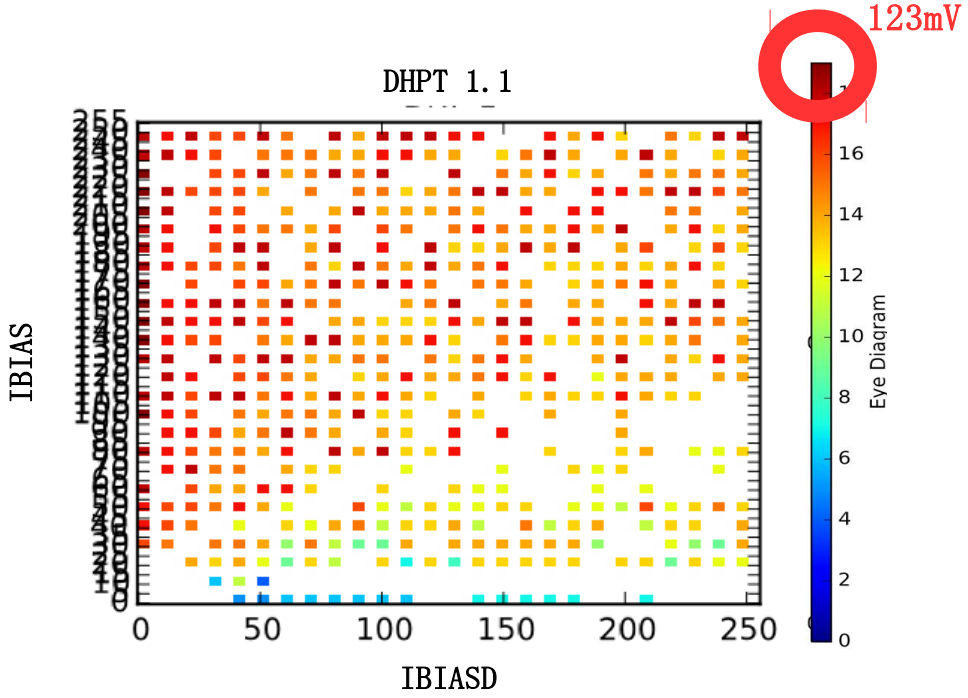
Scan over parameter space

IBIAS, *IBIASD* and *pll_cml_dly*

no receiver equalizing

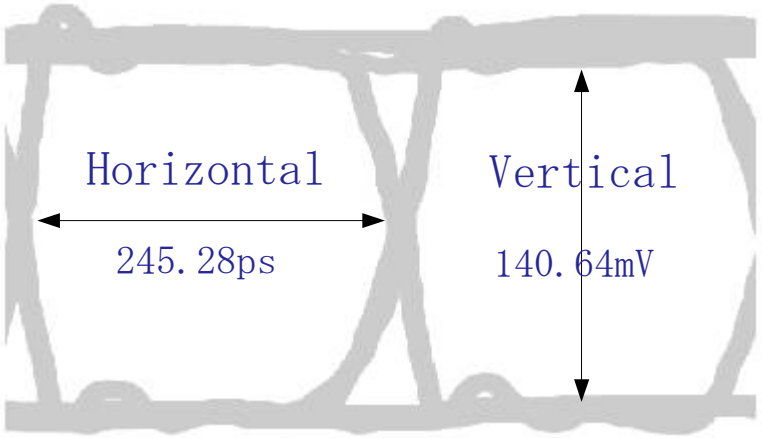
Examples for pll_cml_dly = 0 and GCK = 76.23 MHz

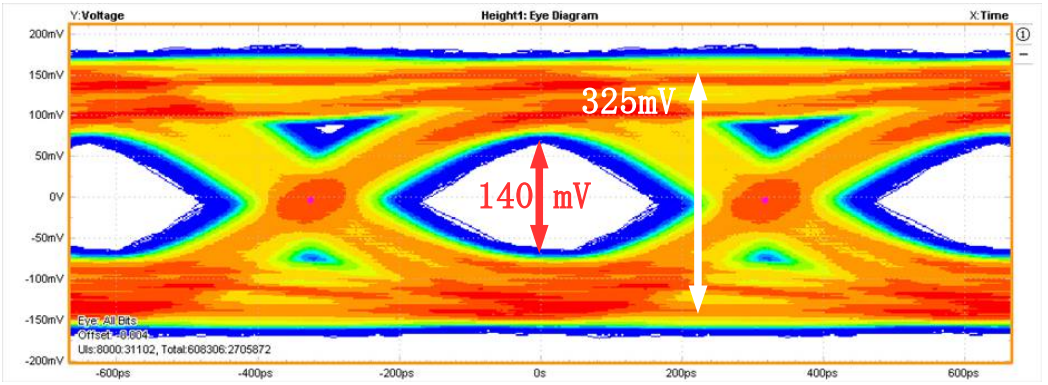




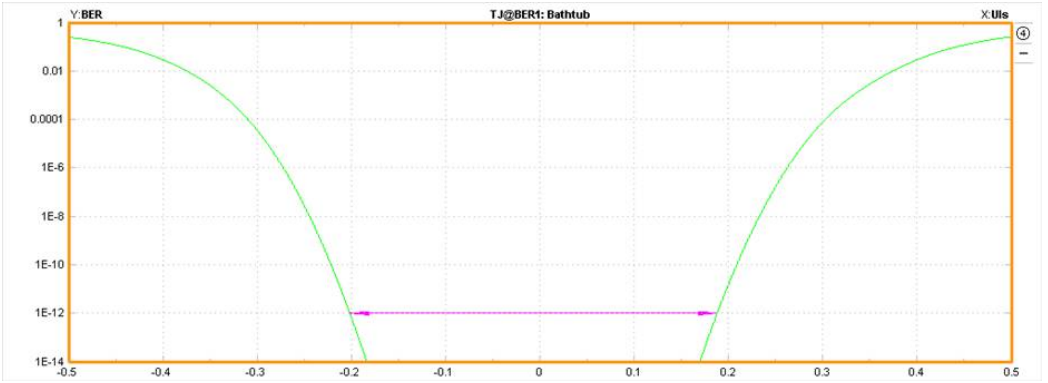
CML driver
Best eye diagram
With adjusted PLL settings
(jitter improvement)
for **15m** TWP cable

Virtex5/6 specs: min 125mV
for < 4.95Gbps

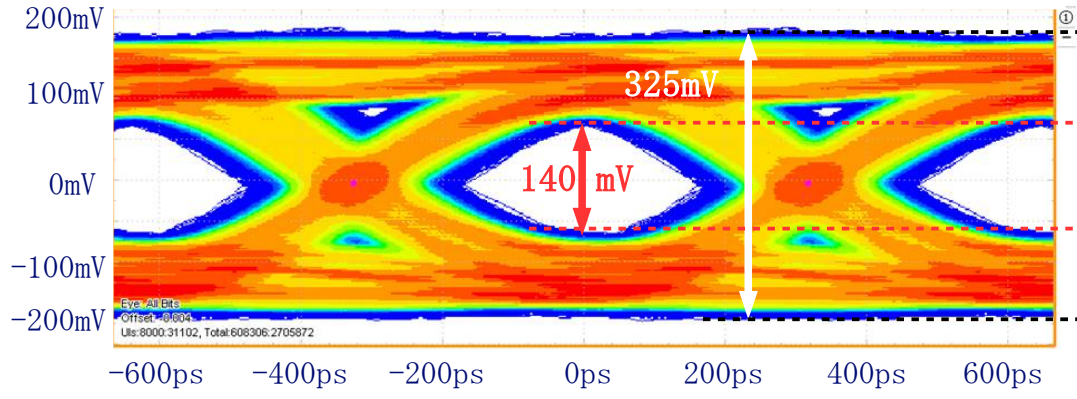




IBIAS =255 IBIASD =20 pll_cml_dly_sel =1
PLL_ICP =255(10) PLL_VCO =255(96) IREF =15(8)

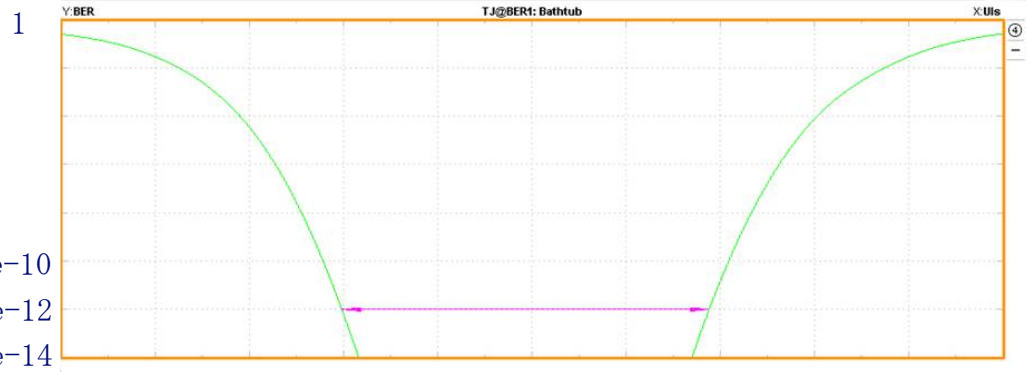


VDD=VDD_CML=1.2V

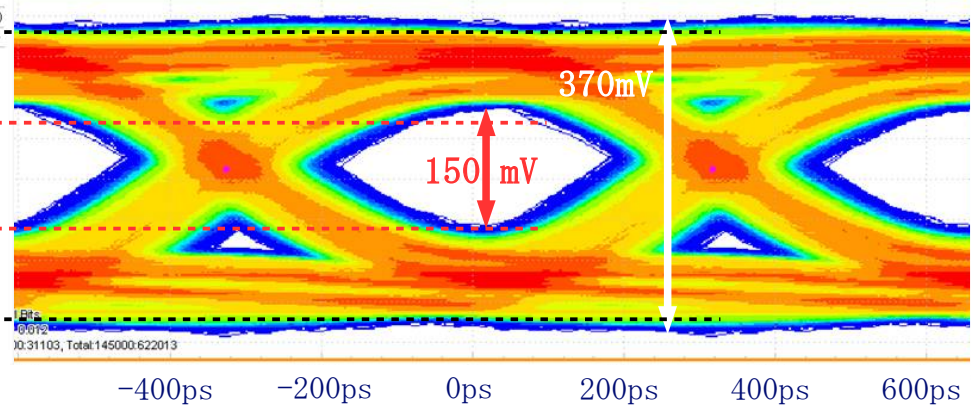


IBIAS =255 IBIAS =20 pll_cml_dly_sel =1

PLL_ICP =255(10) PLL_VCO =255(96) IREF =15(8)

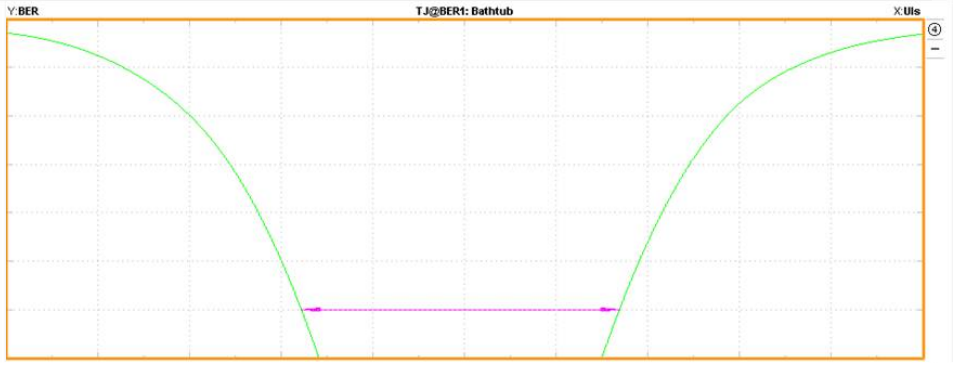


VDD=VDD_CML=1.3V



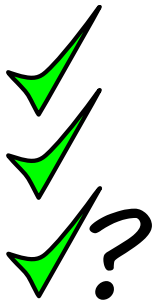
IBIAS =255 IBIAS =20 pll_cml_dly_sel =1

PLL_ICP =255(10) PLL_VCO =255(96) IREF =15(8)



Improvement of the design achieved:

a) Resolvment of the Serializer Bug
b) IO Buffer delay do not suffer from duty cycle distortion
c) Slight improvement of the CML driver



The diviation of the CML driver performance with respect to simulation vs real measurement needs to be investigated in more detail

Tests and Measurements prove that the DHPT 1.1 is in a very good shape for the final experiment.

DHPT 1.1

universitätbonn

Production

- Tape-out: September 9, 2015
- Delivery (100 bumped samples): November 14, 2015

Changes from DHPT 1.0 to DHPT 1.1

- DCD – DHPT Interface
  - Improved data receiver pads (no hysteresis, reduced input capacitance)
  - New delay elements (improved duty cycle balance)
- Serial Data Link
  - New Serializer (fix of the timing bug)
  - Improvement of the CML driver (reduction of parasitic resistances)

➔ Digital part did not change (data processing, configuration etc.)

DHPT Chips for Module Production

universitätbonn

- Decision for DHPT 1.1 as the production candidate by February (?)
- Then: Order of 9 additional wafers (1000 chips in total)
- Two new needle cards for probe station testing currently being produced (HTT)

➔ Estimated testing throughput: ~50 chips per week

If a further DHPT re-design should be unavoidable (for example: Gated-mode operation not yet tested) a DHPT 1.2 with changes in the digital part will be designed and submitted.

- One month re-design (digital synthesis)
- Two months production

➔ ~3 months delay in the delivery of chips for PXD production

universitätbonn

SI LAB
Silizium Labor Bonn

Thank you

germic@physik.uni-bonn.de

universitätbonn

SI LAB
Silizium Labor Bonn

Backup

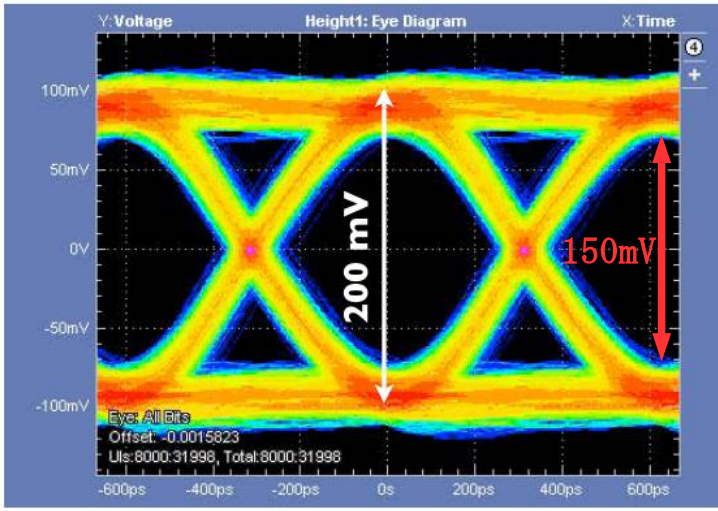
germic@physik.uni-bonn.de

universitätbonn

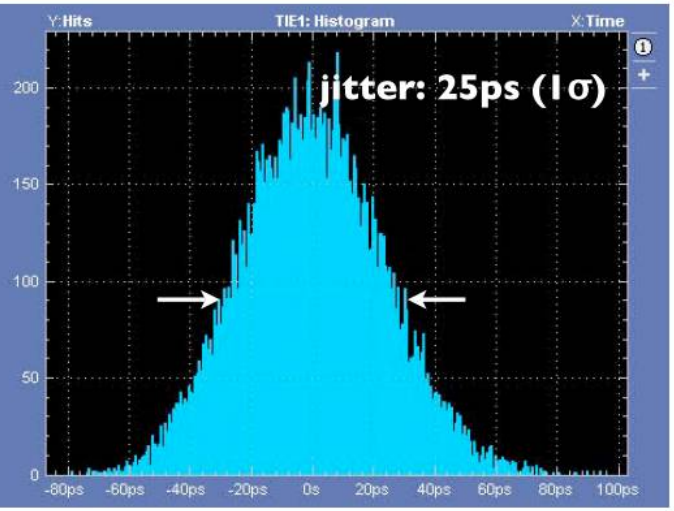
Signal Integrity Analysis

universitätbonn

- 1.6 Gbps, 8bit LFSR sequence **38 cm flex** (I.V.) **+ 10m** Infiniband cable (LEONI, AWG 26)
- Max. pre-emphasis settings



10m + 0.38m Kapton



15m TWP
DHPT1.1 (fullscale)

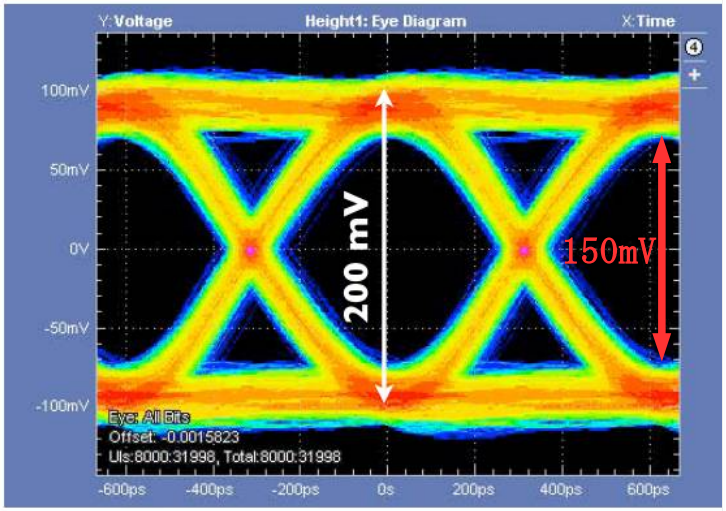
-18/20-

universitätbonn

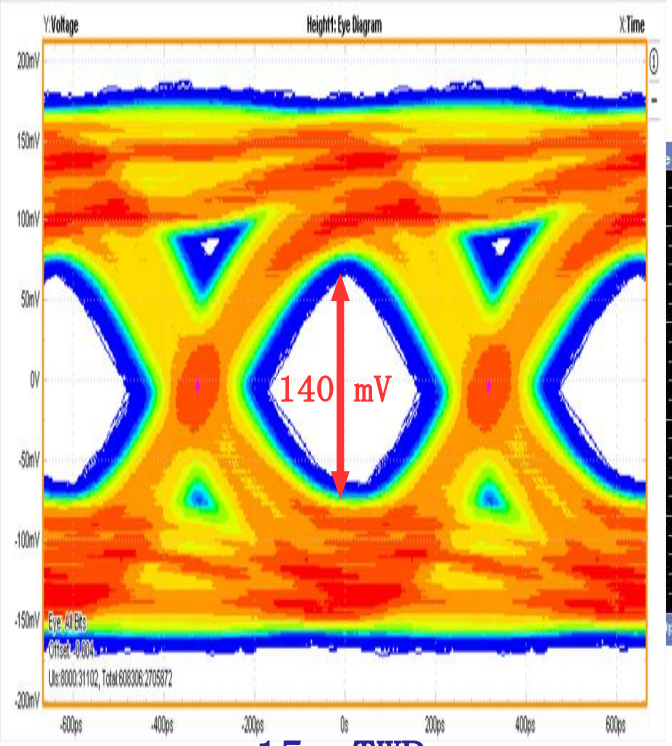
Signal Integrity Analysis

universitätbonn

- 1.6 Gbps, 8bit LFSR sequence **38 cm flex** (I.V.) **+ 10m** Infiniband cable (LEONI, AWG 26)
- Max. pre-emphasis settings



10m TWP + 0.38m Kapton
DHPT0.1 (test)



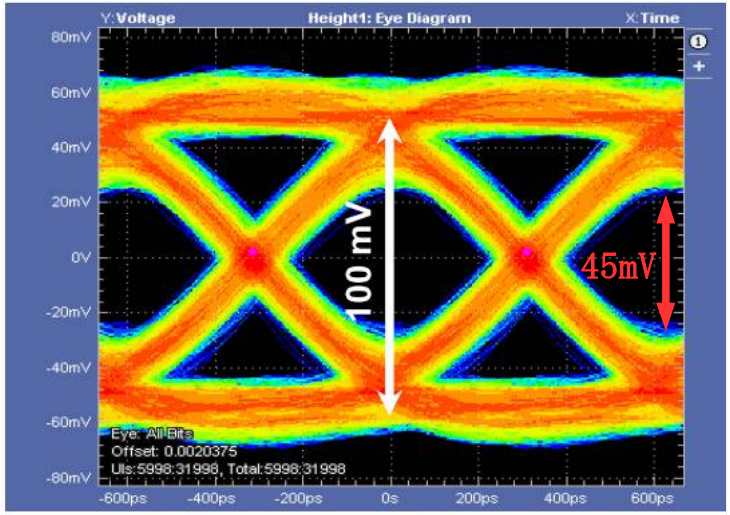
15m TWP
DHPT1.1 (fullscale)

universitätbonn

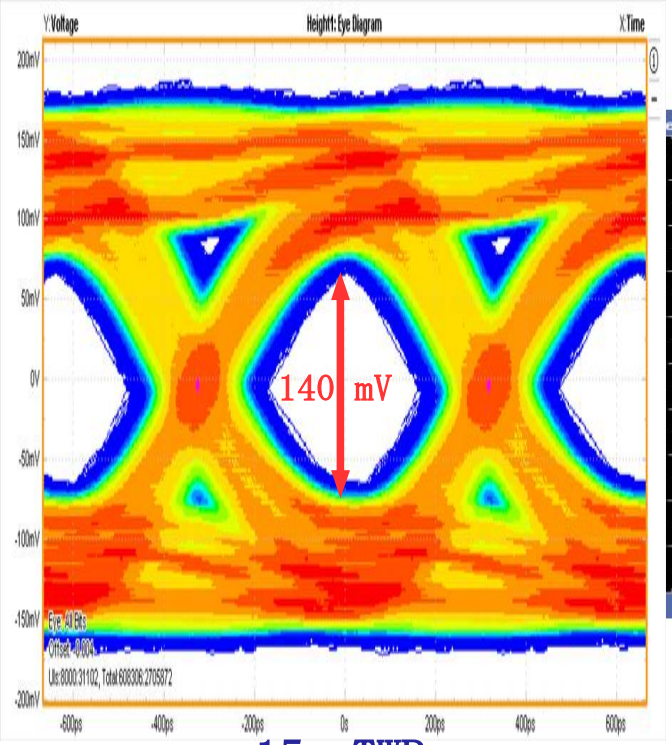
Signal Integrity Analysis

universitätbonn

1.6 Gbps, 8bit LFSR sequence **38 cm flex** (I.V.) **+ 20m** Infiniband cable (LEONI, AWG 26)
Max. pre-emphasis settings

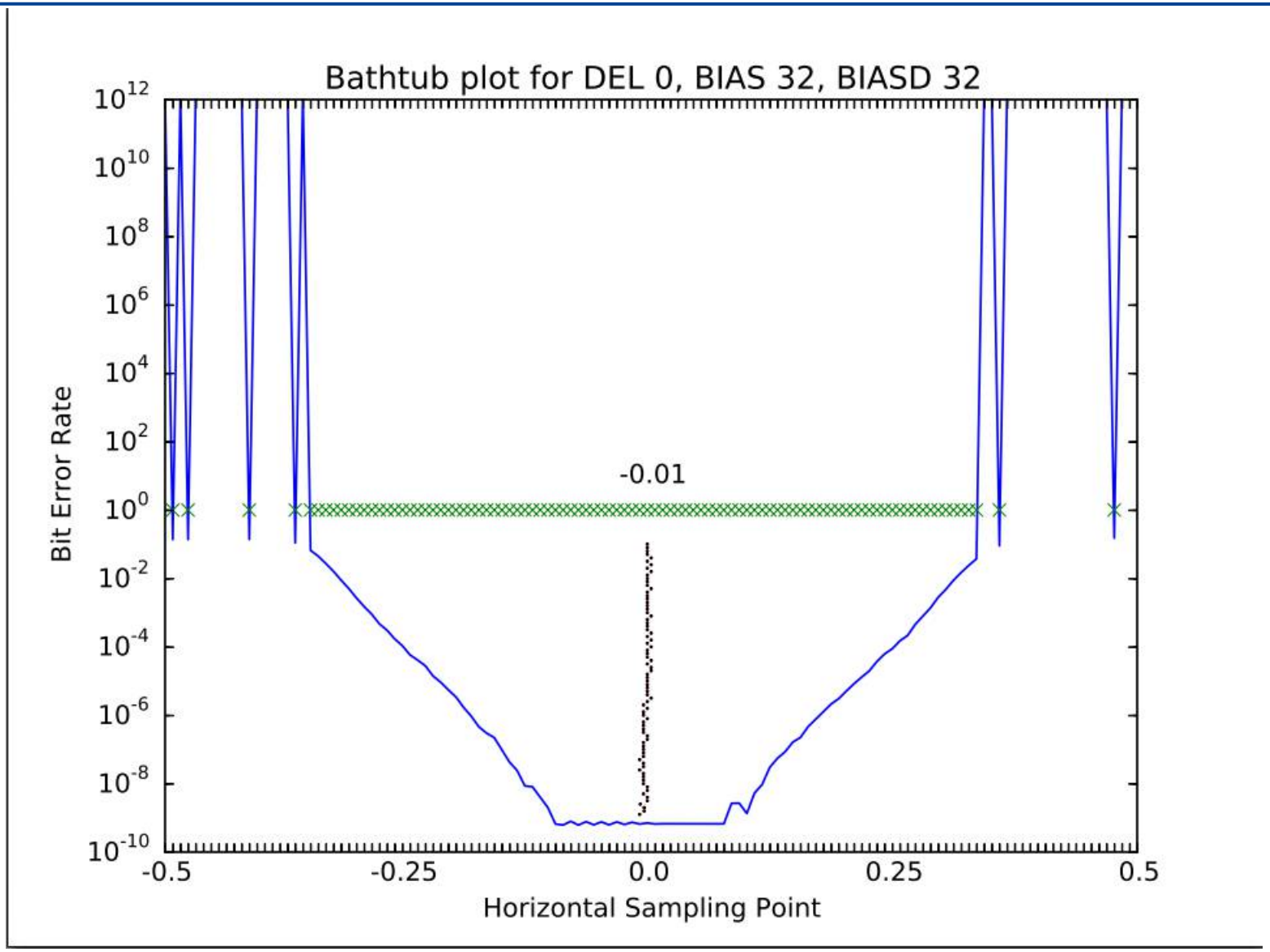


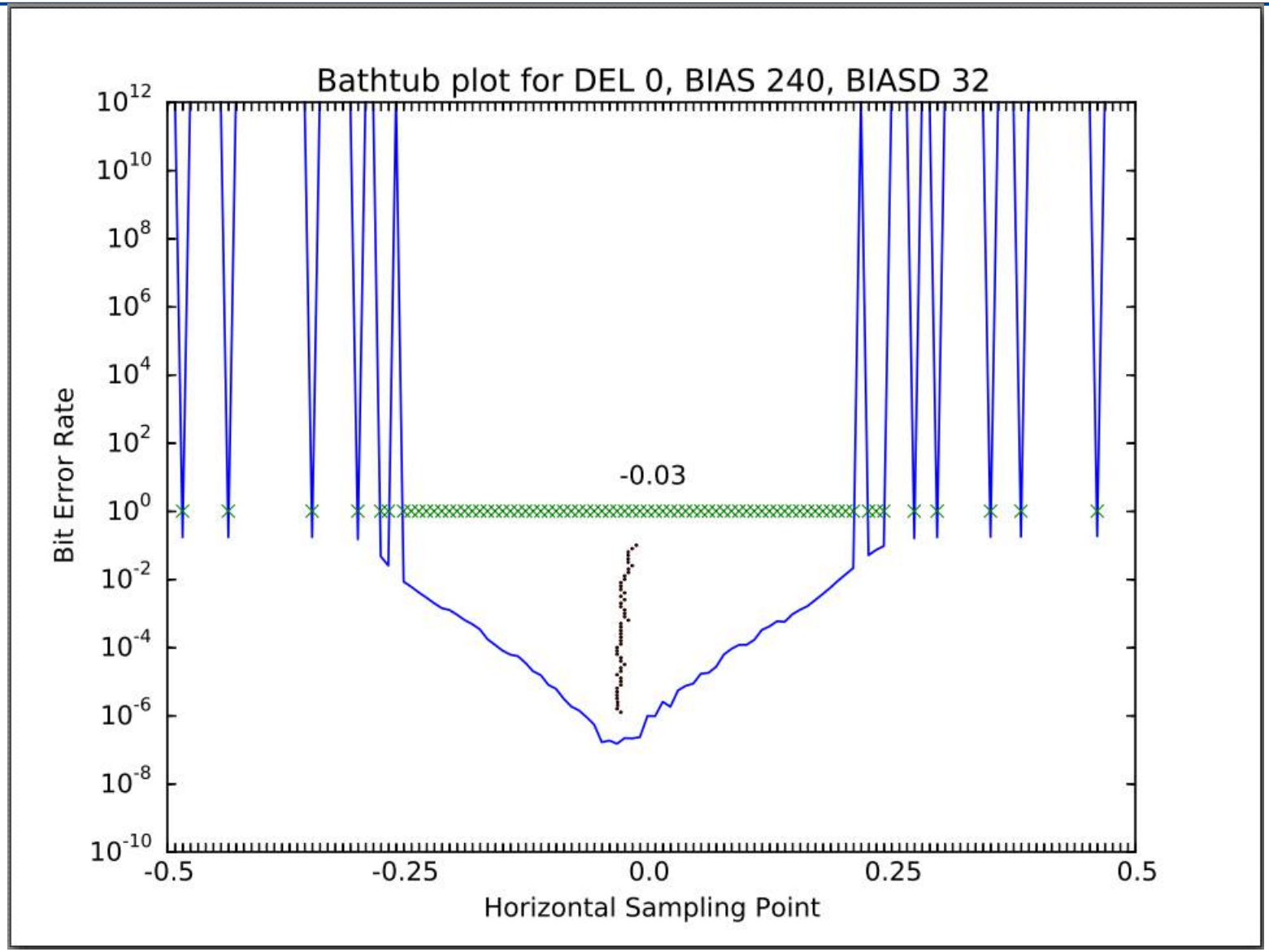
20m TWP + 0.38m Kapton
DHPT0.1 (test)



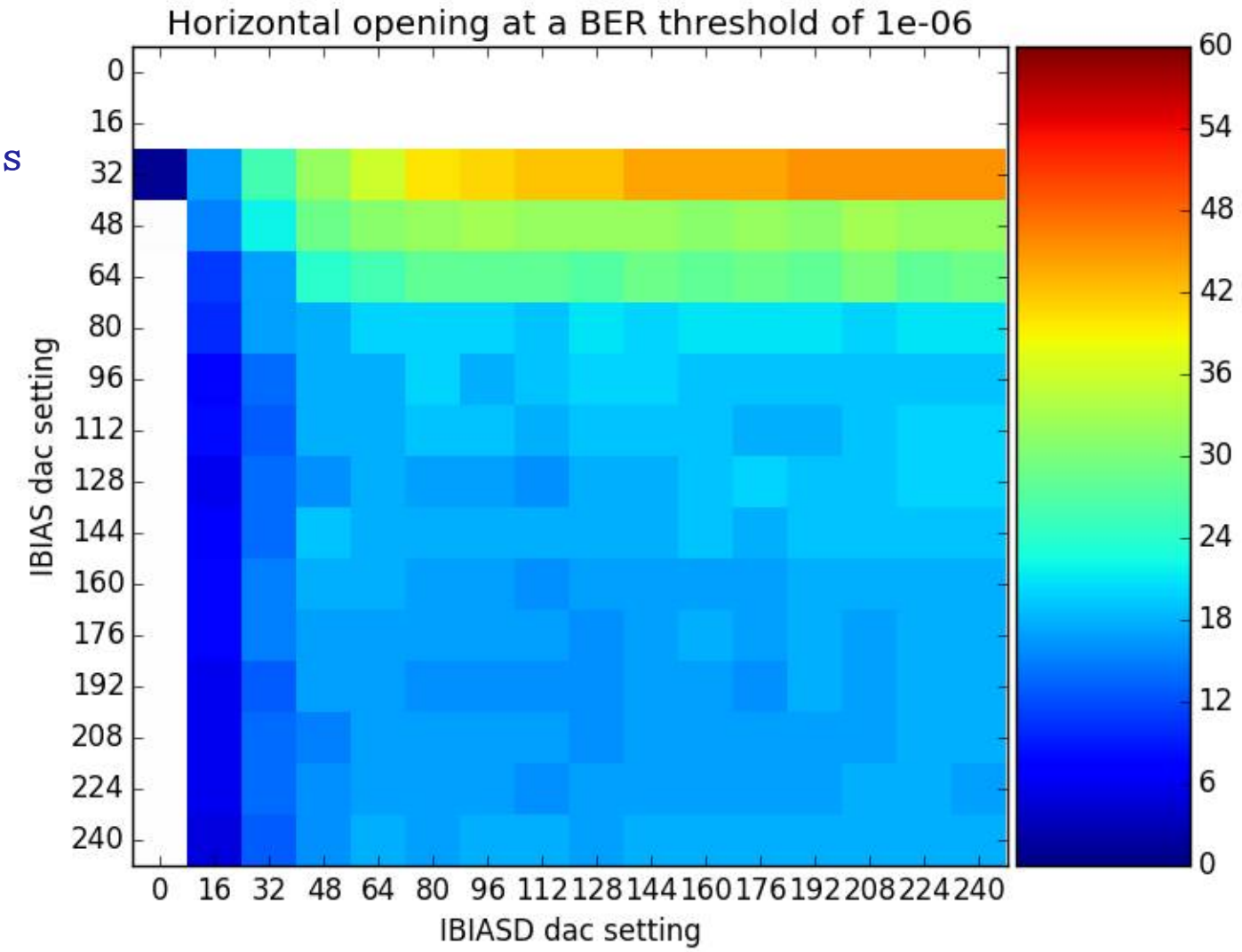
15m TWP
DHPT1.1 (fullscale)

-19/20-


Bathtub plot for DEL 0, BIAS 32, BIASD 32
Bit Error Rate
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
-0.01
-0.5
-0.25
0.0
0.25
0.5
Horizontal Sampling Point

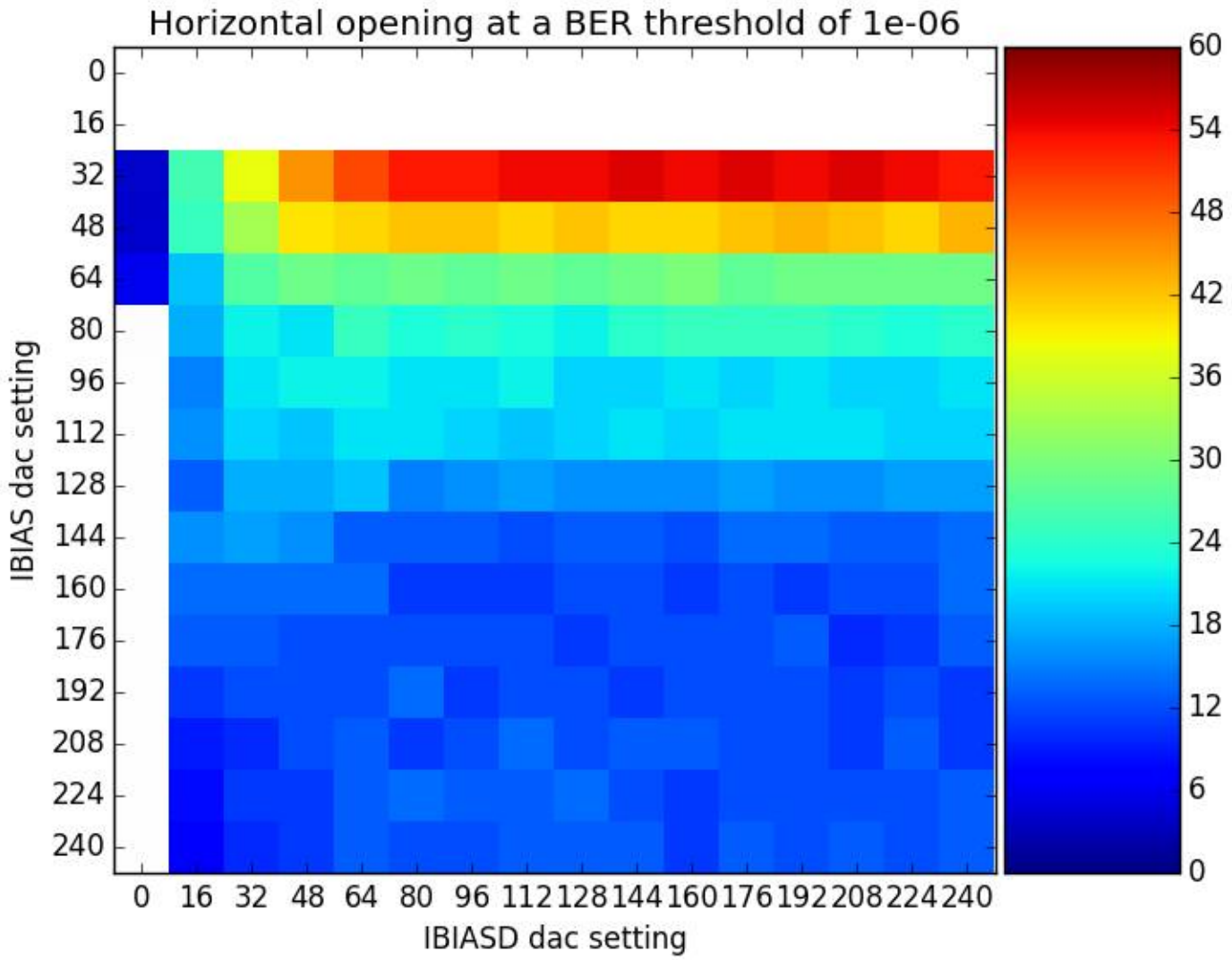

Bathtub plot for DEL 0, BIAS 240, BIASD 32
Bit Error Rate
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
10^{0}
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
-0.03
-0.5
-0.25
0.0
0.25
0.5
Horizontal Sampling Point

DLY3
Small
preemphasis
width



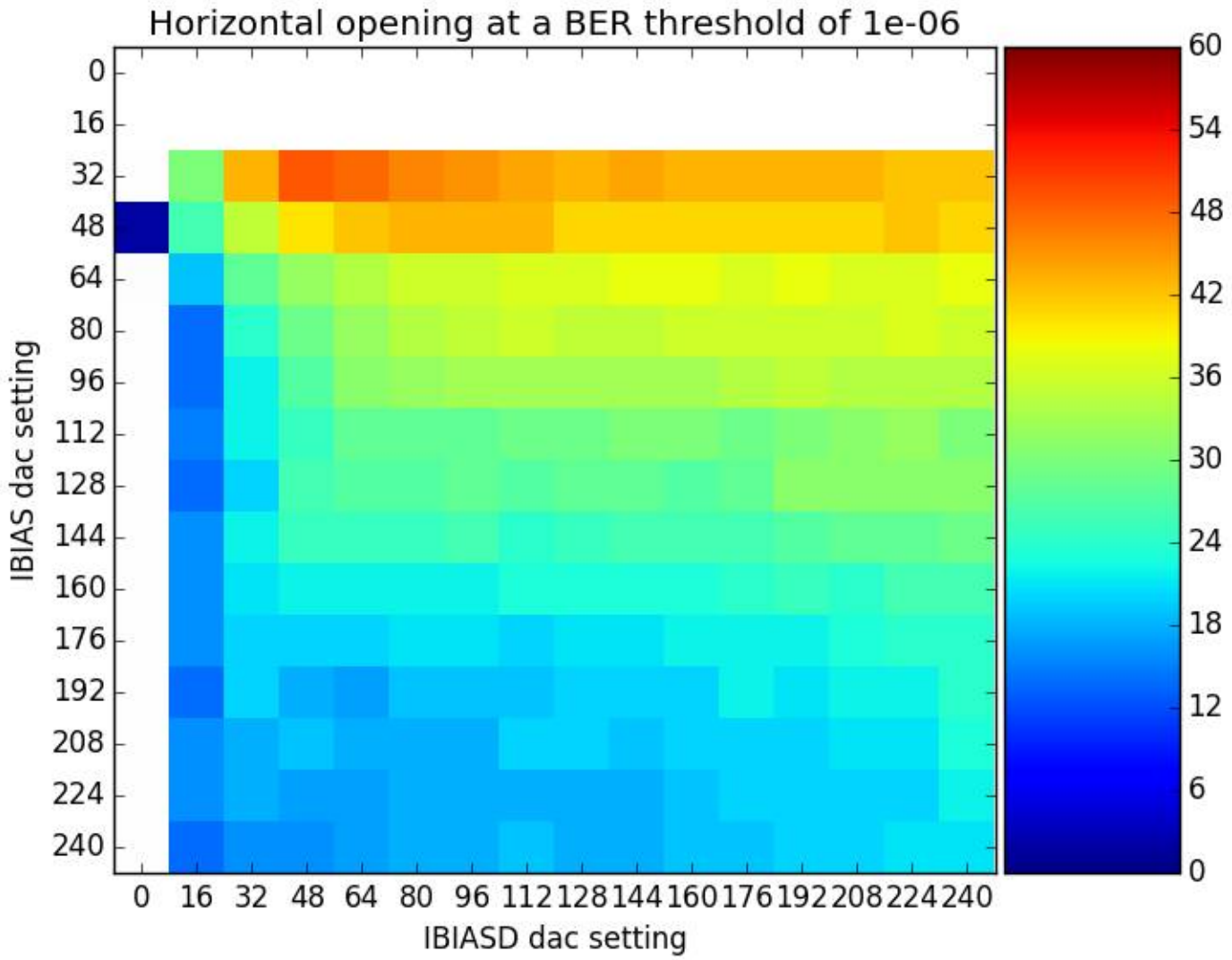
universitätbonn

DLY2

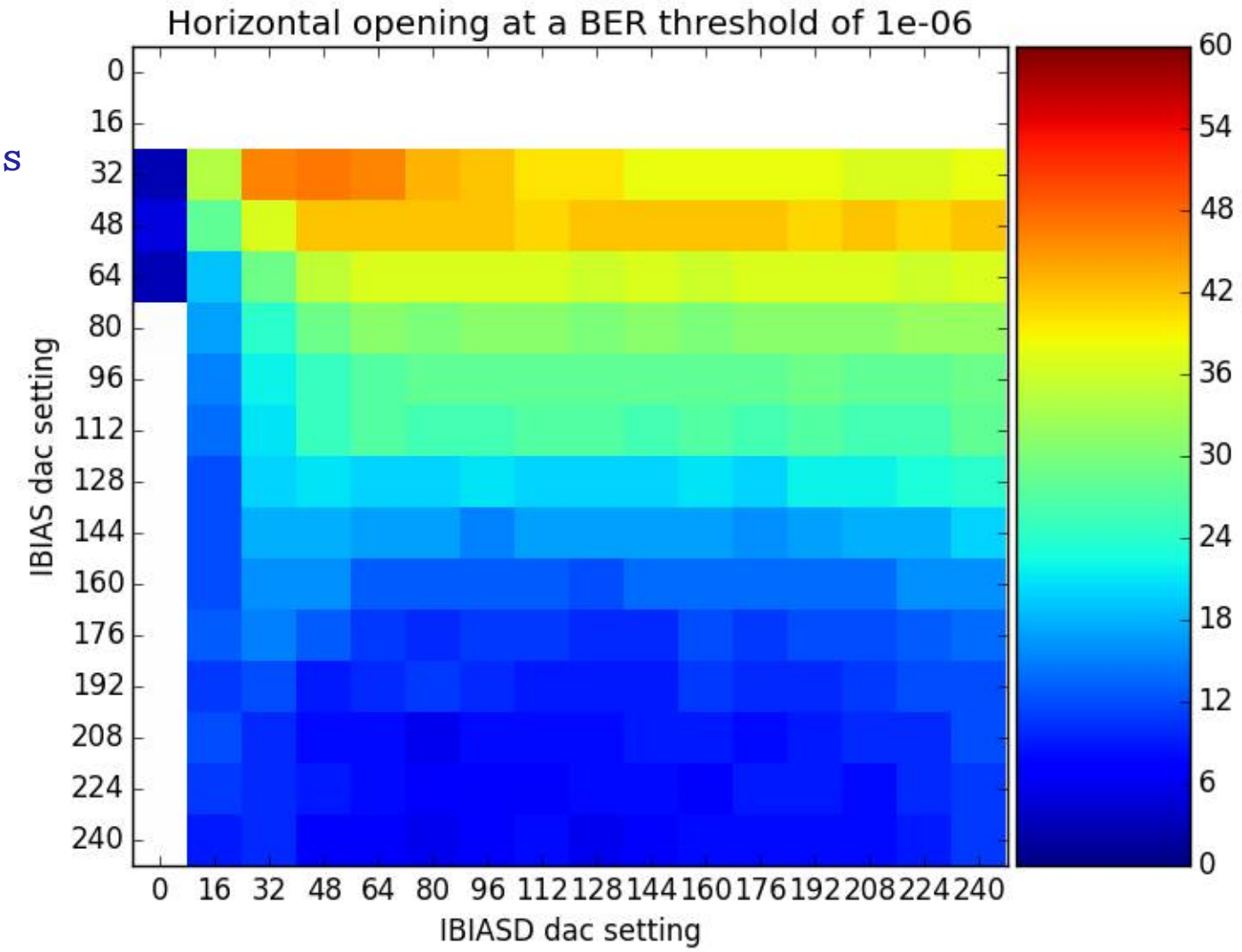


universitätbonn

DLY1



DLY0
Large
preemphasis
width



universitätbonn

Changes from DHPT 1.0 to DHPT 1.1

VXD Workshop, Valencia

Jan 13-15, 2016

DHPT 1.1

universitätbonn

Production

- Tape-out: September 9, 2015
- Delivery (100 bumped samples): November 14, 2015

Changes from DHPT 1.0 to DHPT 1.1

- DCD – DHPT Interface
  - Improved data receiver pads (no hysteresis, reduced input capacitance)
  - New delay elements (improved duty cycle balance)
- Serial Data Link
  - New Serializer (fix of the timing bug)
  - Improvement of the CML driver (reduction of parasitic resistances)

➔ Digital part did not change (data processing, configuration etc.)

DHPT Chips for Module Production

universitätbonn

- Decision for DHPT 1.1 as the production candidate by February (?)
- Then: Order of 9 additional wafers (1000 chips in total)
- Two new needle cards for probe station testing currently being produced (HTT)

➔ Estimated testing throughput: ~50 chips per week

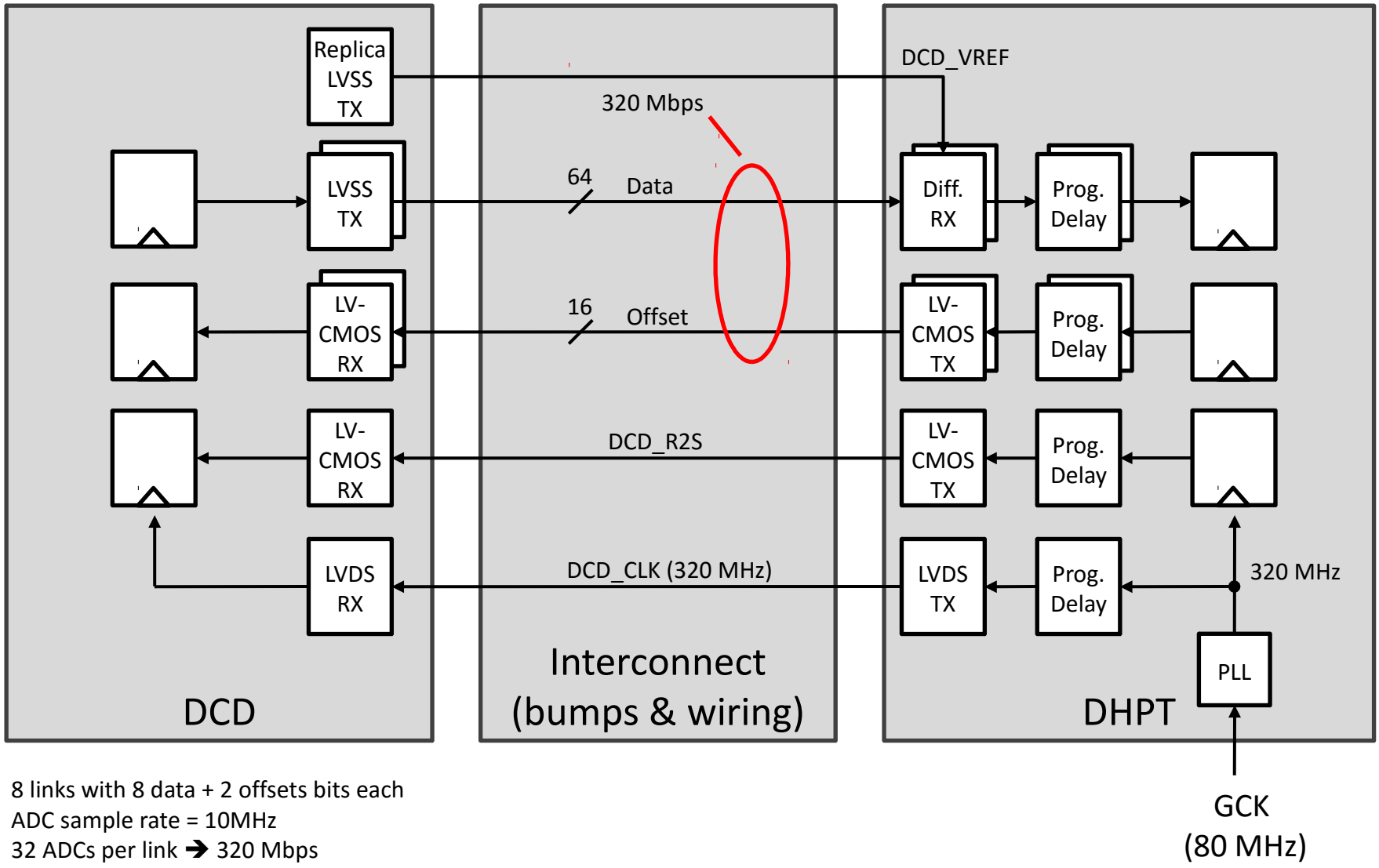
If a further DHPT re-design should be unavoidable (for example: Gated-mode operation not yet tested) a DHPT 1.2 with changes in the digital part will be designed and submitted.

- One month re-design (digital synthesis)
- Two months production

➔ ~3 months delay in the delivery of chips for PXD production

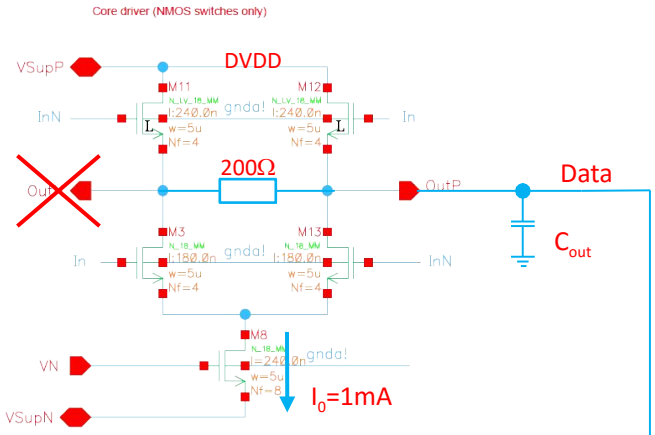
DCD- DHPT INTERFACE

DCD – DHPT Interface Block Diagram

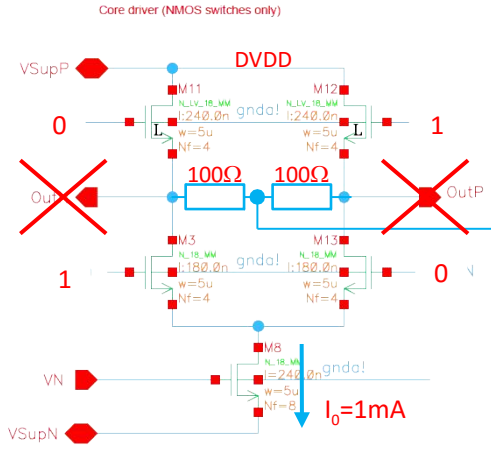


8 links with 8 data + 2 offsets bits each
ADC sample rate = 10MHz
32 ADCs per link ➔ 320 Mbps

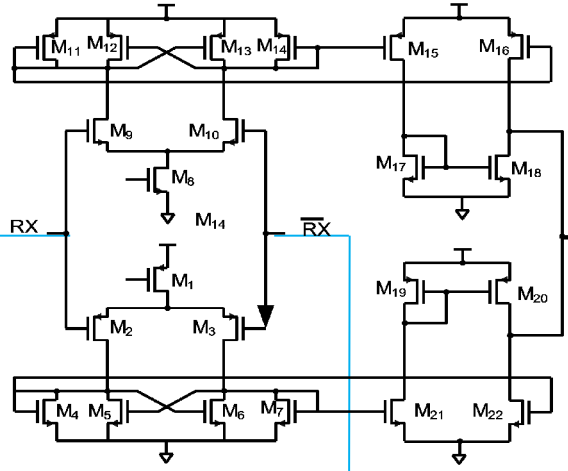
DCD – DHPT Data Transmission Schematic Details



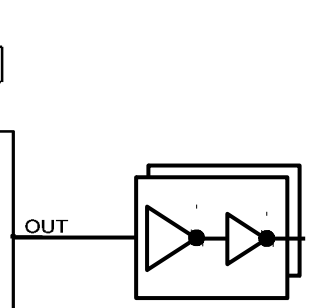
DCD output driver



DCD output reference voltage generation



DHPT receiver



to DHPT core

Prog. delay
Tapped delay line,

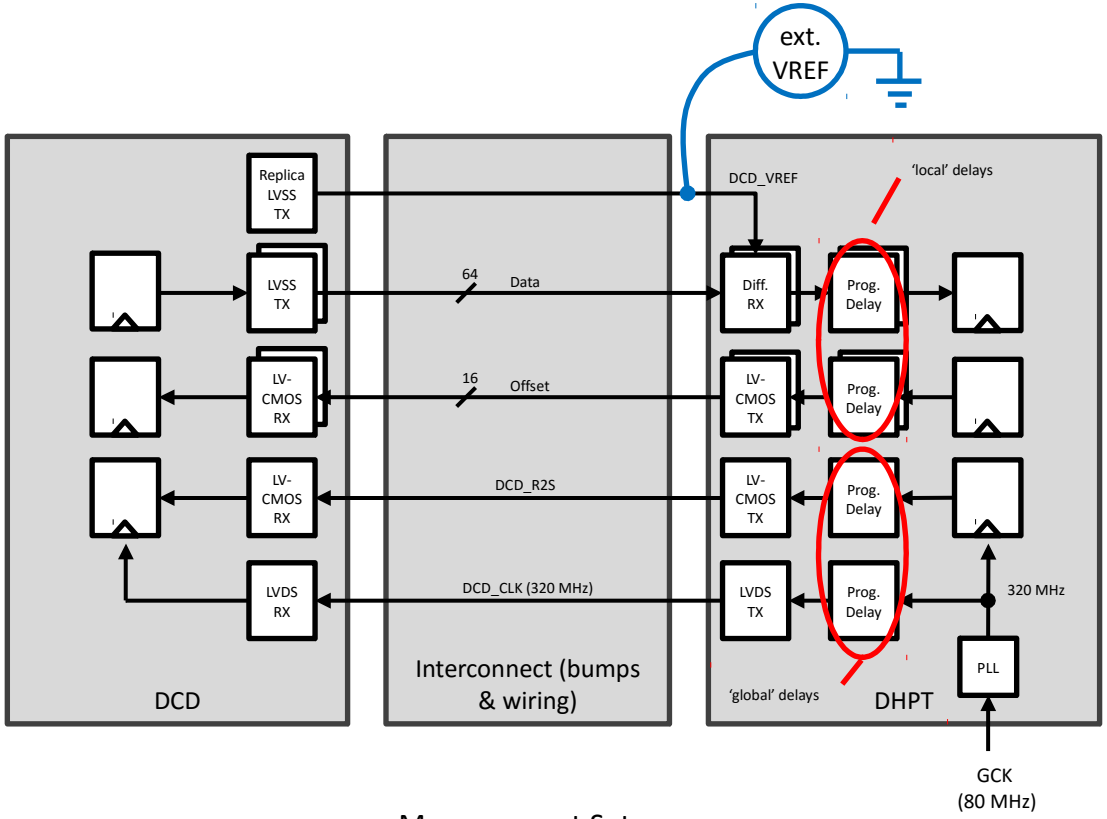
Data Link Synchronization

- DCD can produce a simple test pattern for synchronization of the data links

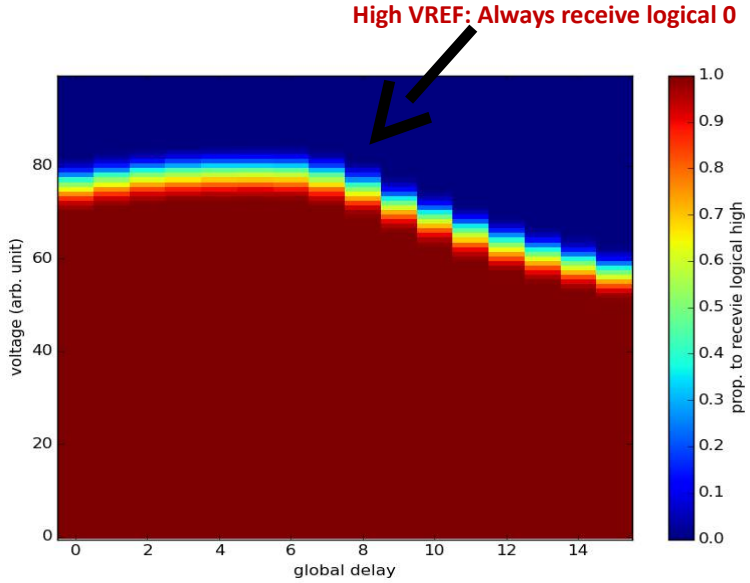
Bitline	Time (clock period) ≙ADC channel																														
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
1	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
2	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
3	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
4	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
5	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
6	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
7	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Data Line Waveform Analysis

- Combined reference voltage- and delay scan (no direct access to data lines)

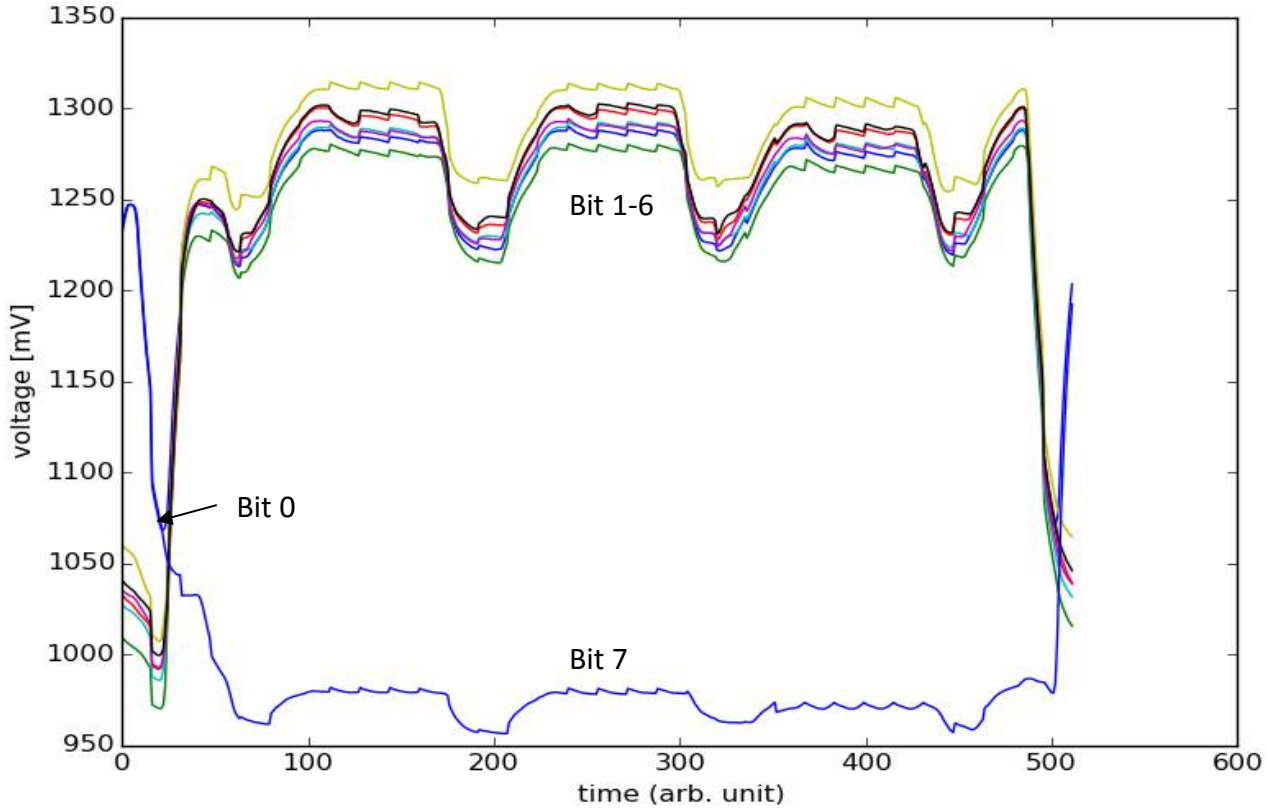


Measurement Setup



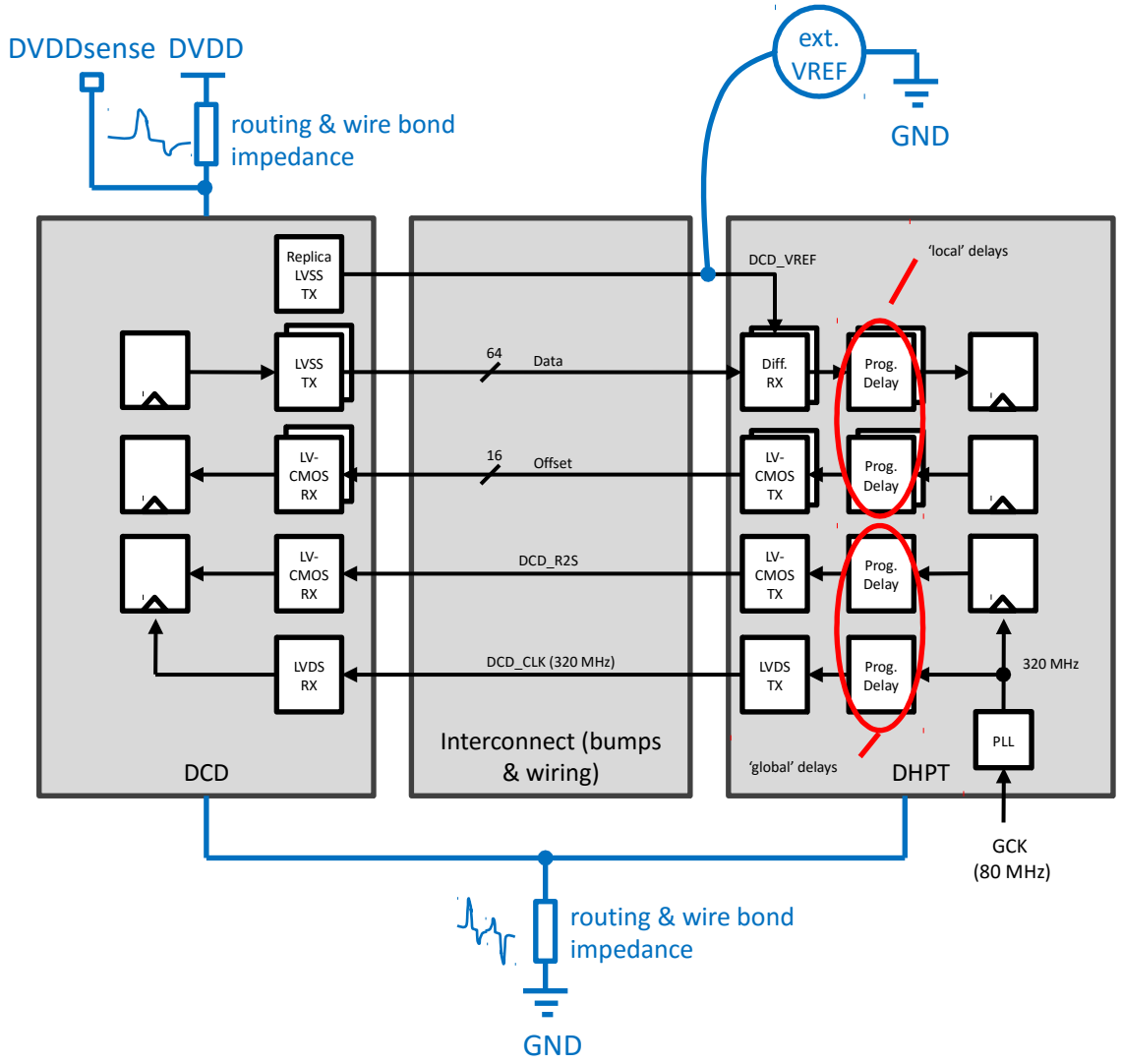
Typical scan result

All Bit lines of one Link

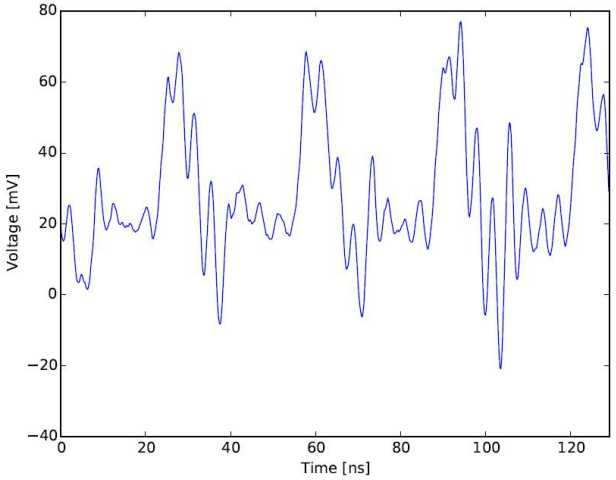


Bit line																																
	0	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	1-6	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
	7	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

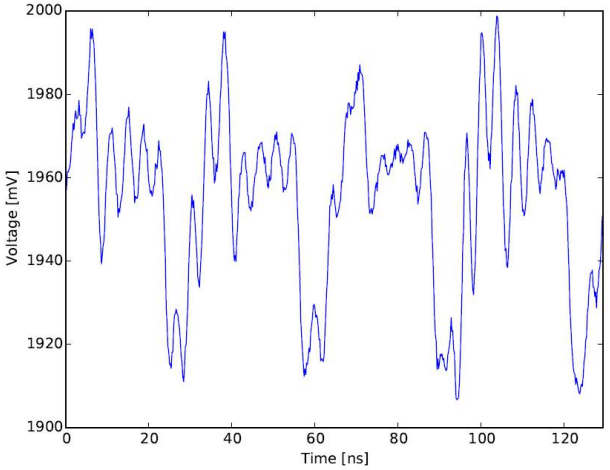
DCD_VREF external Control & Measurement



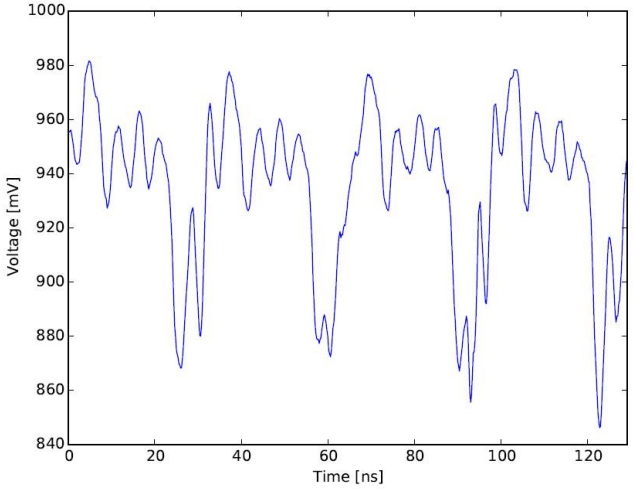
Measurement Artefacts



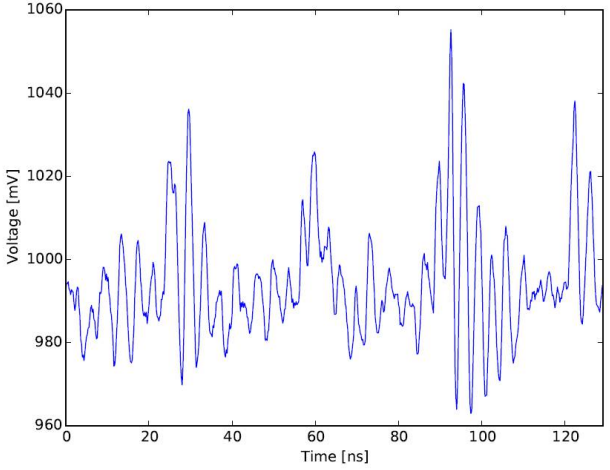
DVDD – DVDDsense



DVDDsense – GND



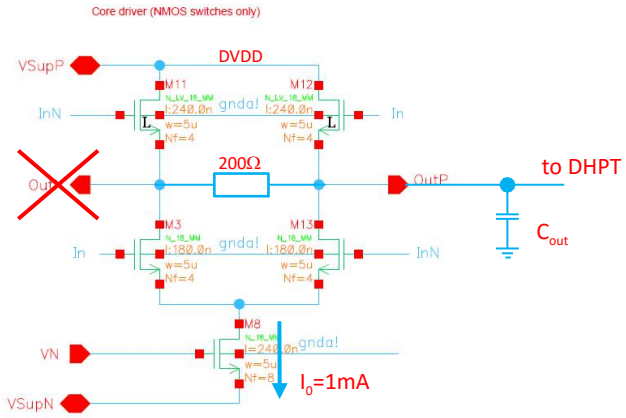
DVDDsense – DCD_VREF

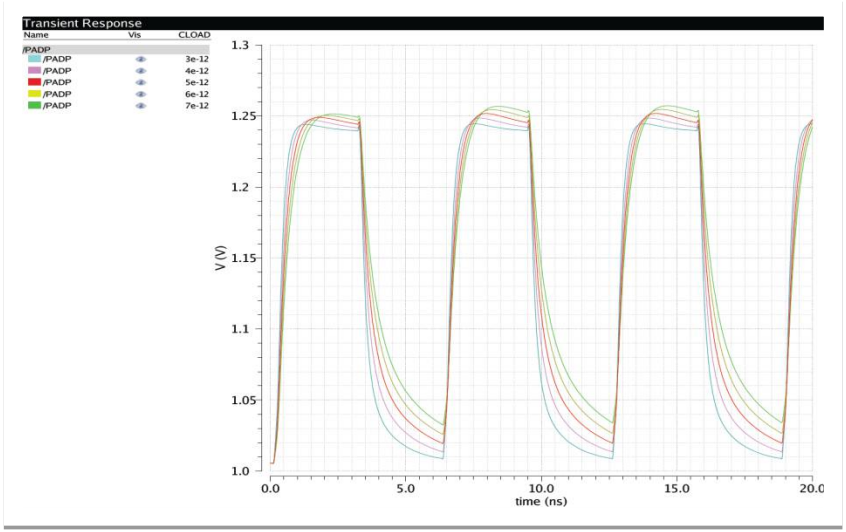


DCD_VREF – GND

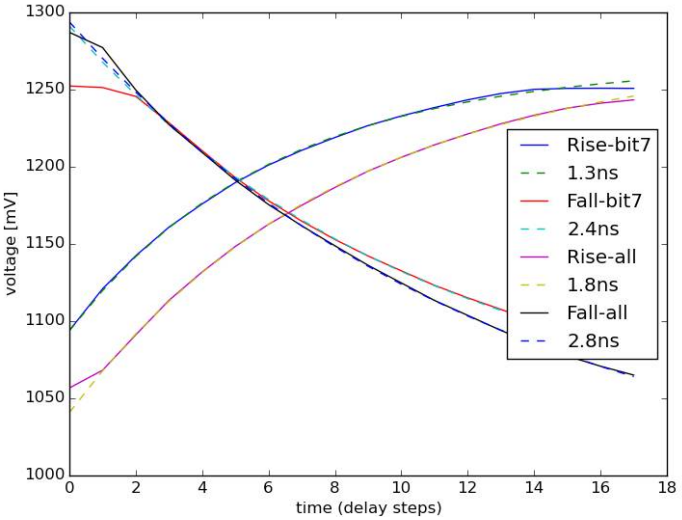
DCD output driver

- Schematic level simulation
  - capacitive load (C_{out}=3..7pF)





- Rise-/fall time extraction from Vref/deltaT scans



Interface Issues

universitätbonn

- Synchronization of data line critical
  - Little contingency for delay settings
  - Sensitive against TID
- Distortion of the duty cycle
  - Delay elements on DHPT
  - Hysteresis of the DHPT differential receiver (plus asymmetric rise and fall times of the DCD driver)
- Slow signals
  - Underestimated parasitic capacitance of wiring and pads
  - DCD driver output levels not adjustable and drive strength asymmetric

Design Changes

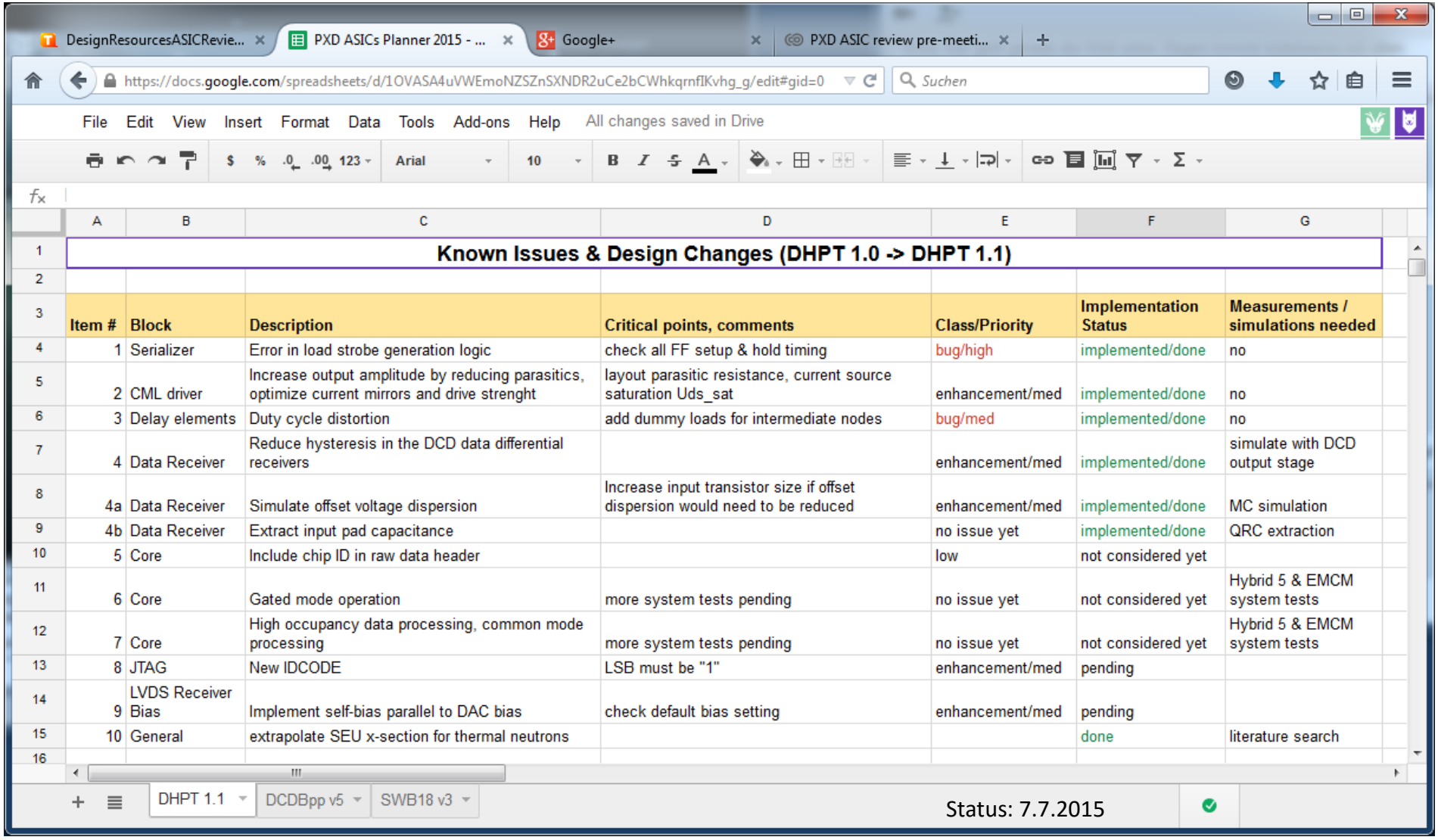
universitätbonn

- Fix duty cycle distortion
  - Symmetric delay elements on DHPT inputs
  - DHPT differential receiver → remove hysteresis

  } See next chapters

- Make signal faster
  - Reduce parasitic capacitance of the DHPT input pads ($C_{PAD} \simeq 3$ pF dominated by ESD protection) → analysis/simulation started, pad layout change in progress
  - DCD output driver → Increase drive strength, make programmable (see Ivan's talk)
  - Changes of routing on PXD module ? (estimated $C_{line} \simeq 1$pF) TBD

Known Issues & Design Changes (DHPT 1.0 -> DHPT 1.1)



Known Issues & Design Changes (DHPT 1.0 -> DHPT 1.1)

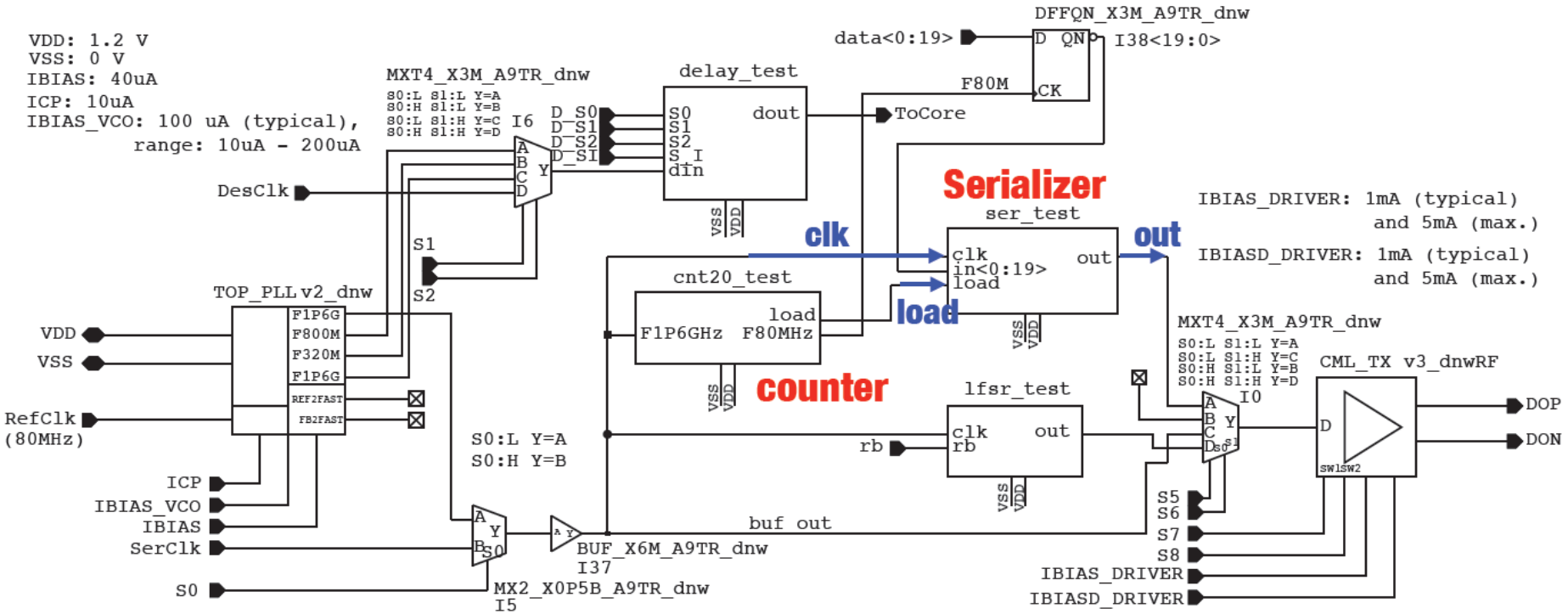
Item #	Block	Description	Critical points, comments	Class/Priority	Implementation Status	Measurements / simulations needed
1	Serializer	Error in load strobe generation logic	check all FF setup & hold timing	bug/high	implemented/done	no
2	CML driver	Increase output amplitude by reducing parasitics, optimize current mirrors and drive strenght	layout parasitic resistance, current source saturation Uds_sat	enhancement/med	implemented/done	no
3	Delay elements	Duty cycle distortion	add dummy loads for intermediate nodes	bug/med	implemented/done	no
4	Data Receiver	Reduce hysteresis in the DCD data differential receivers		enhancement/med	implemented/done	simulate with DCD output stage
4a	Data Receiver	Simulate offset voltage dispersion	Increase input transistor size if offset dispersion would need to be reduced	enhancement/med	implemented/done	MC simulation
4b	Data Receiver	Extract input pad capacitance		no issue yet	implemented/done	QRC extraction
5	Core	Include chip ID in raw data header		low	not considered yet	
6	Core	Gated mode operation	more system tests pending	no issue yet	not considered yet	Hybrid 5 & EMCM system tests
7	Core	High occupancy data processing, common mode processing	more system tests pending	no issue yet	not considered yet	Hybrid 5 & EMCM system tests
8	JTAG	New IDCODE	LSB must be "1"	enhancement/med	pending	
9	LVDS Receiver Bias	Implement self-bias parallel to DAC bias	check default bias setting	enhancement/med	pending	
10	General	extrapolate SEU x-section for thermal neutrons			done	literature search

Status: 7.7.2015

DHPT 1.0

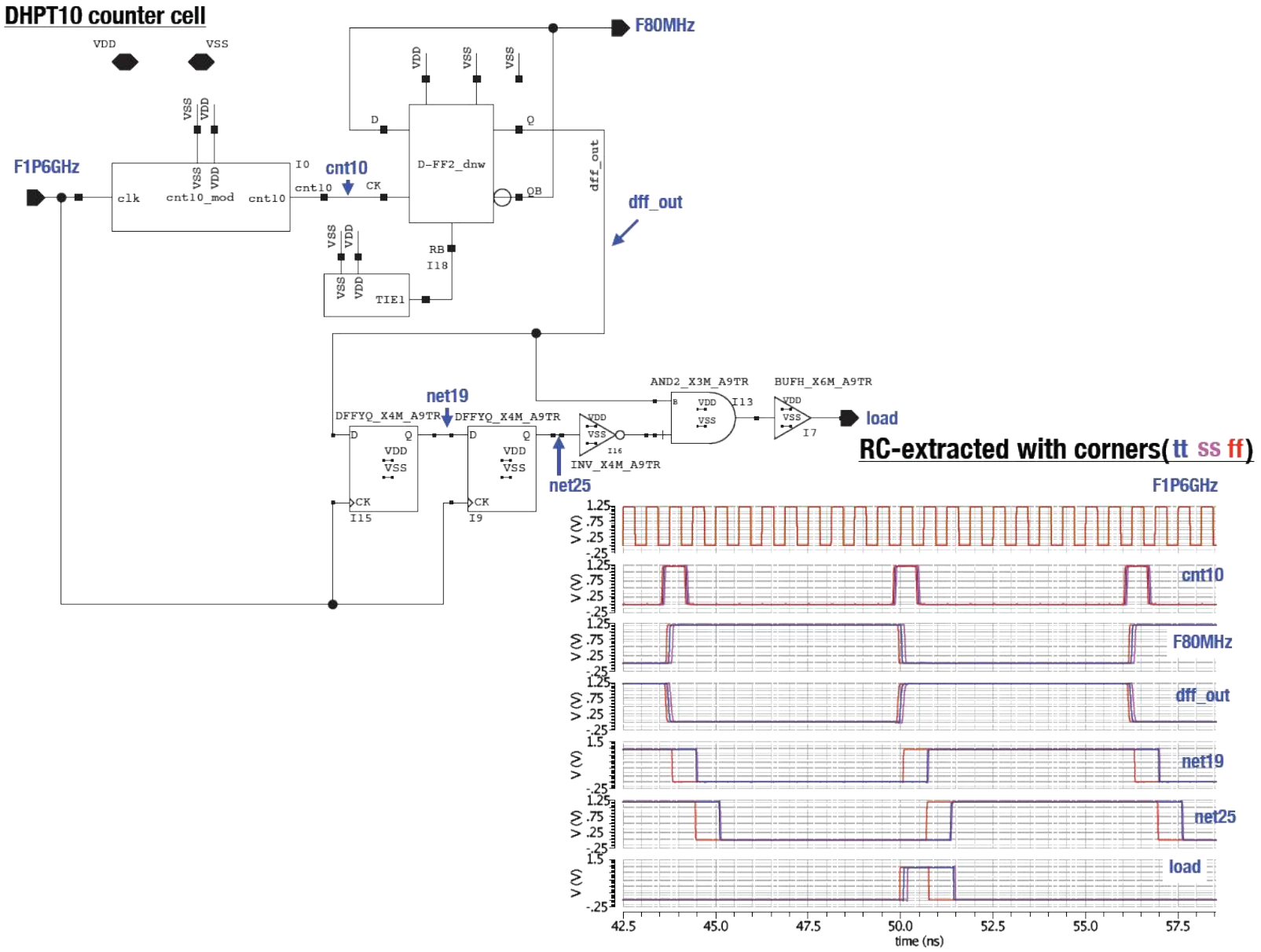
SERIALIZER

PLL + SER Block Diagram



Load Strobe Generation (Counter)

universitätbonn



Serializer Bug

universitätbonn

- Mistake made during extracting and simulating the layout with all process corners

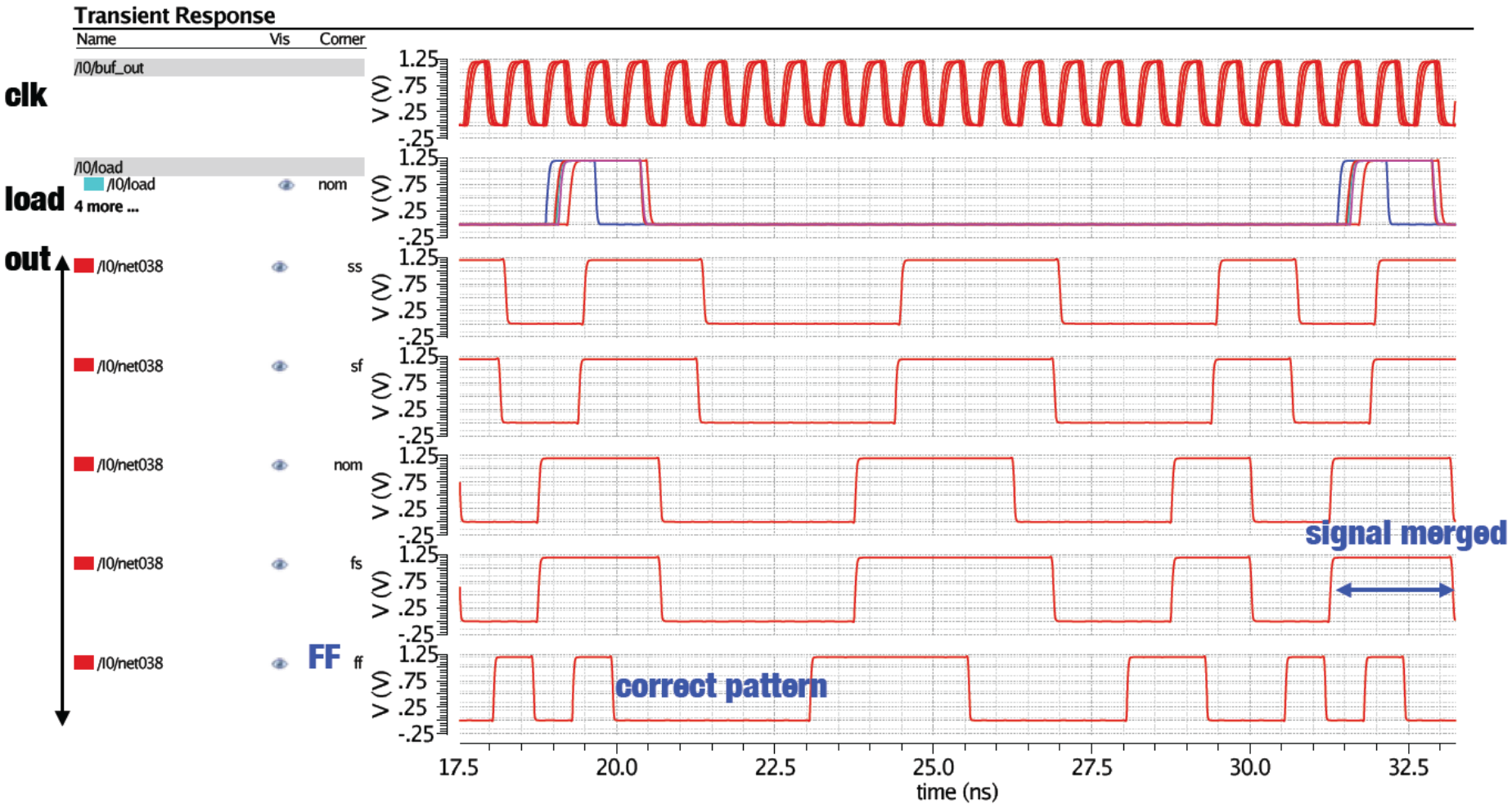
- Serializer works, but VCC and/or GCK have to be adjusted:
  - GCK= 80 MHz → VCC = 1.6V (works but should not be applied for a long time)
  - GCK= 60 MHz → VCC = 1.4V (ok)

- Manufacturer test data ➔ wafer batch has „slow NMOS“ (too high threshold)

PARAMETER BY LOT:		SPEC LO	SPEC HI	MIN	MAX	MEAN	STD DEV
VTl_N4	(N/.3/.06/1)	0.300	0.490	0.368	0.490	0.423	0.029
Isof_N4	(N/.3/.06/1)	-1.400E-07	0.000	-8.958E-10	-3.833E-11	-2.339E-10	2.063E-10
Isat_N4	(N/.3/.06/1)	0.491	0.735	0.547	0.673	0.593	0.031

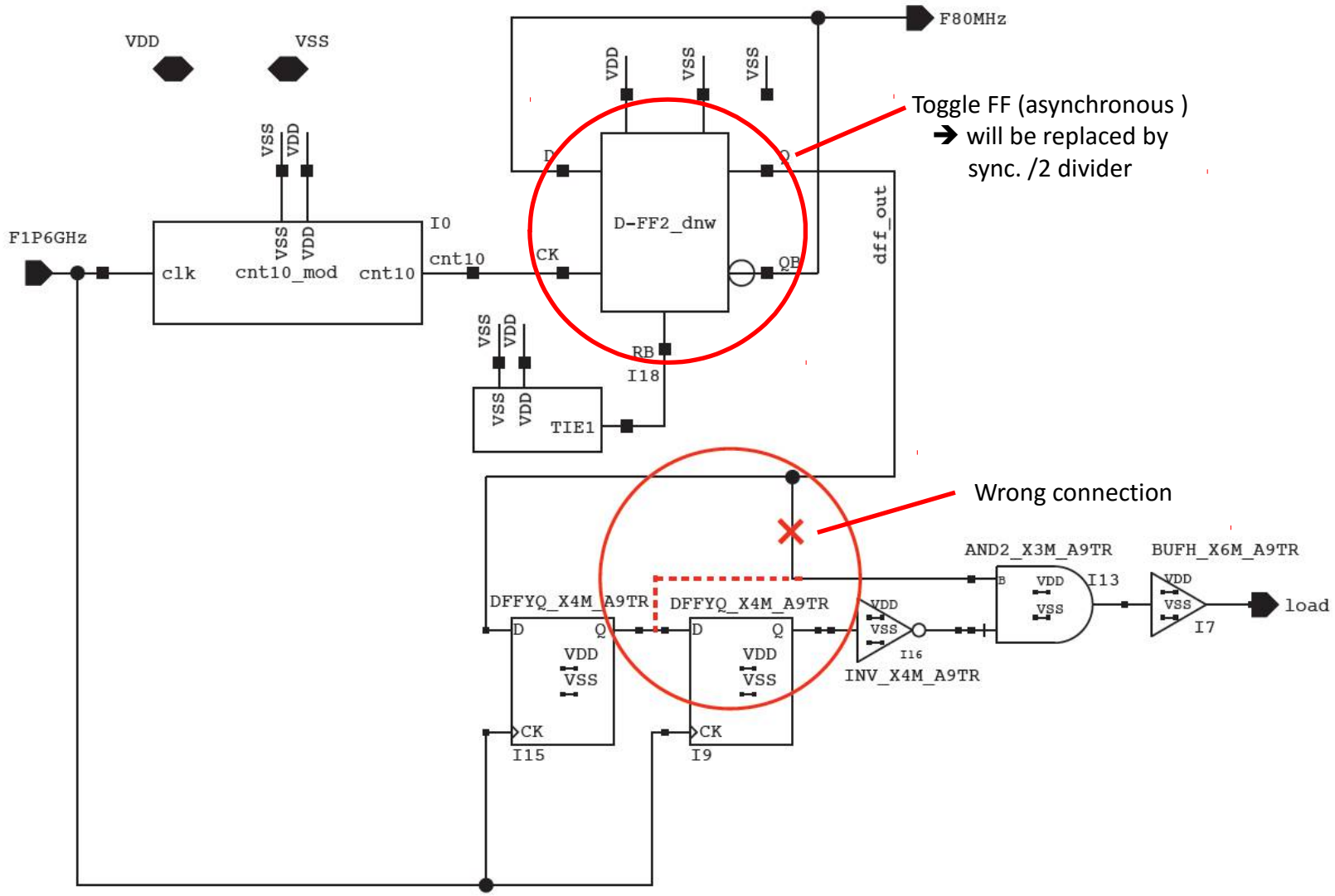
DHPT 1.0 Serializer Simulation

universitätbonn



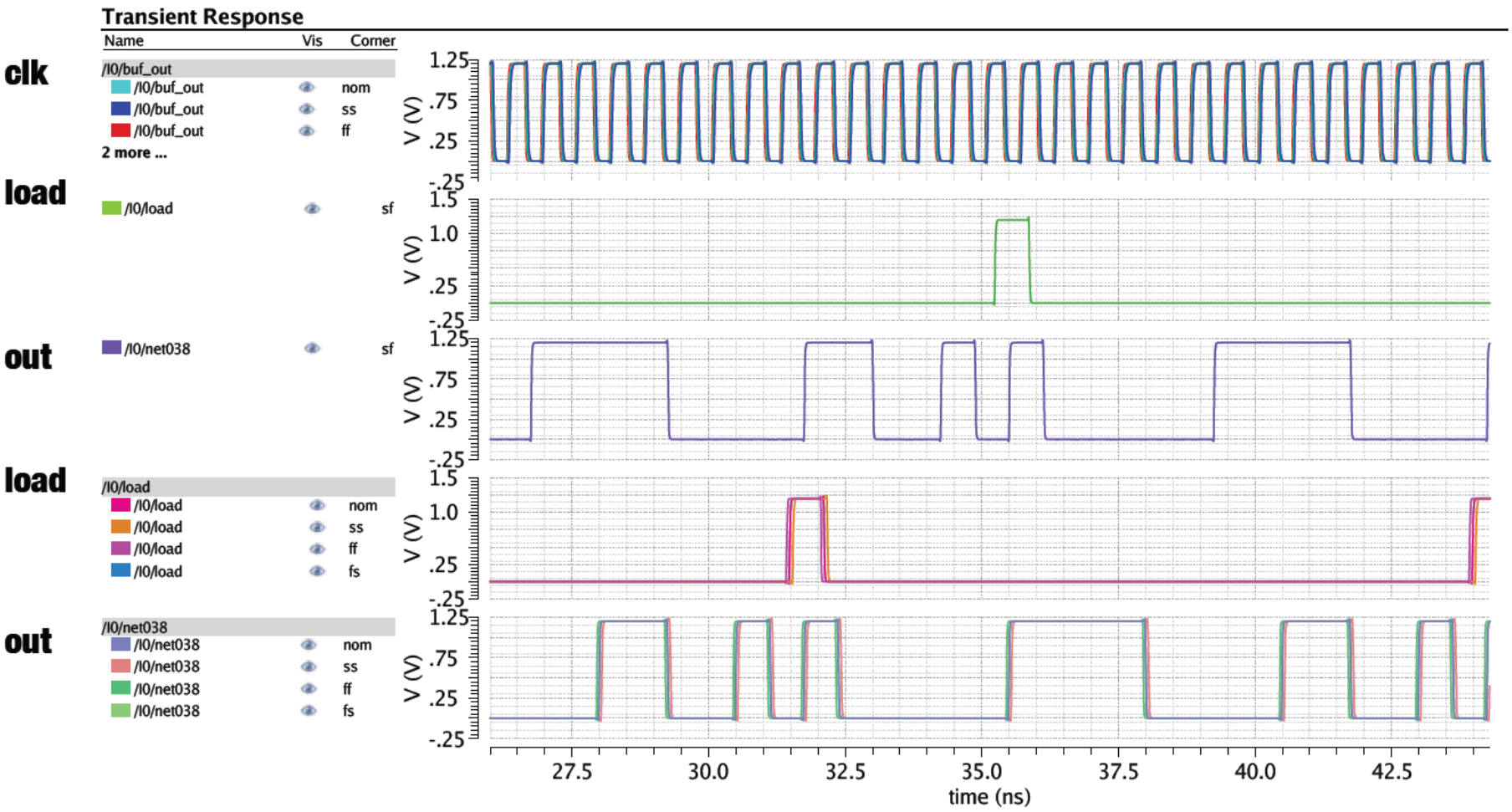
Timing of "load" is not provided correctly, except fast-fast corner.

Design Fix in the Counter Circuit



Serializer Simulation with Modification (DHPT 1.1)

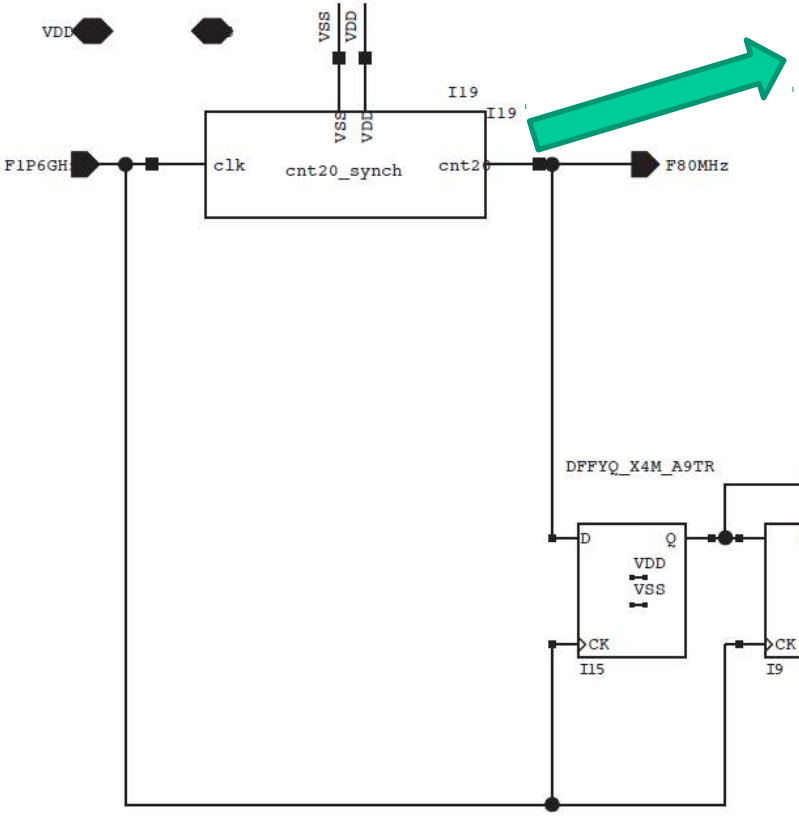
universitätbonn

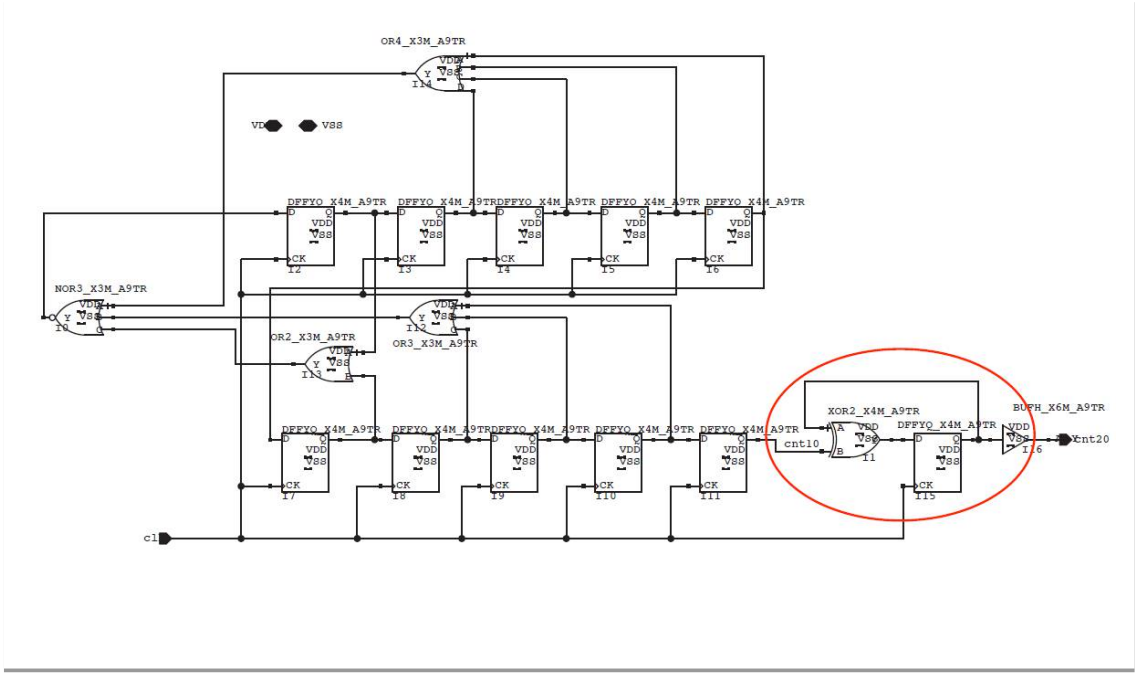


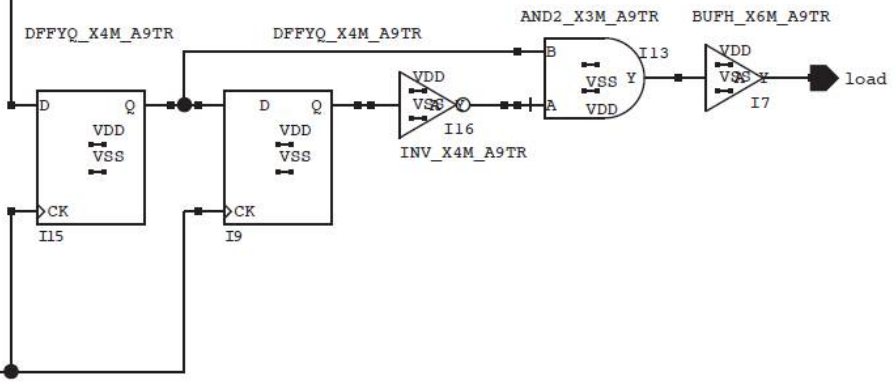
Correct pattern can be obtained with all corners.

New Serializer Load Strobe Generator

- Synchronous design

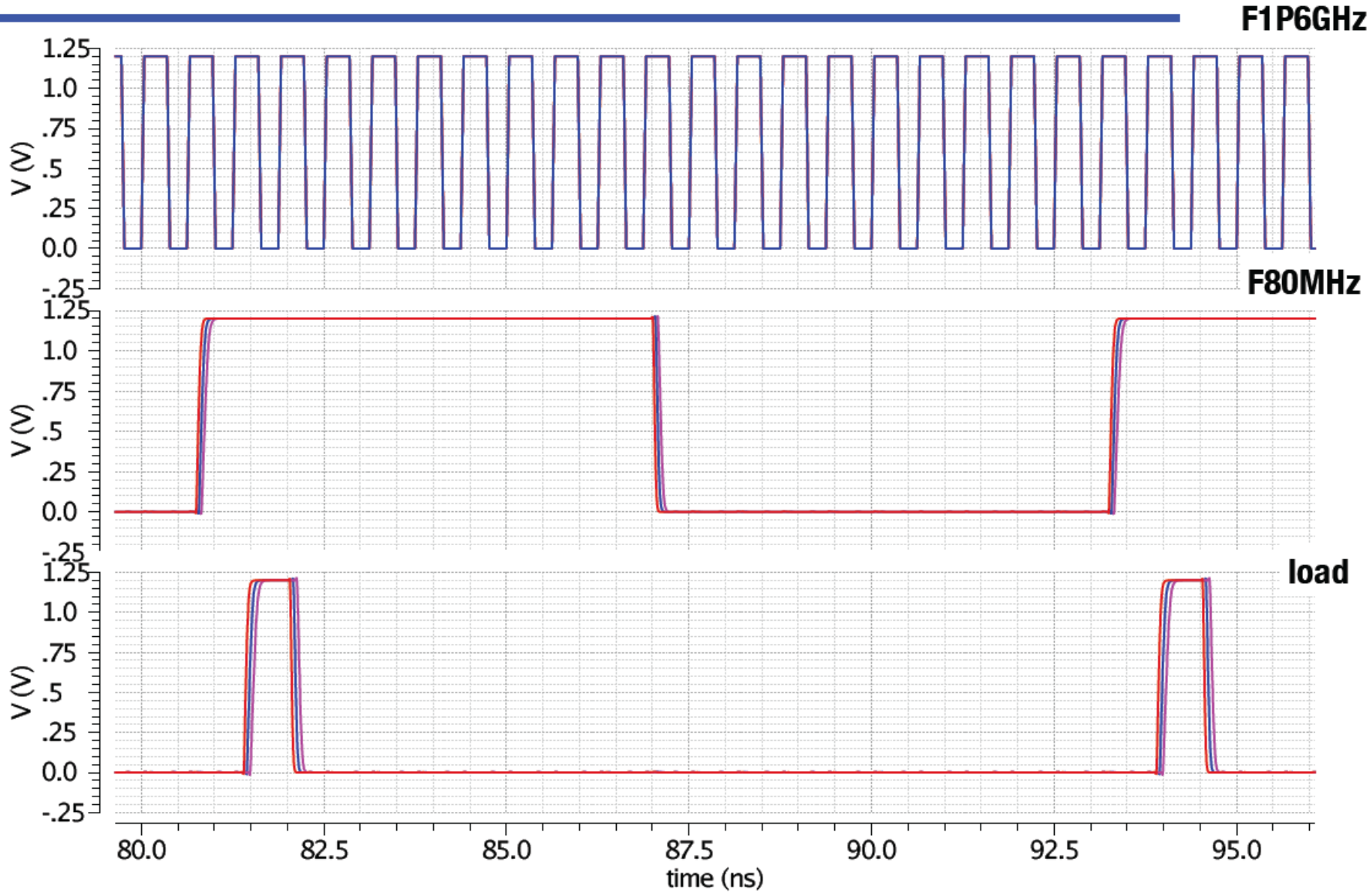






RC-extracted simulation with corners(tt ss ff)

universitätbonn



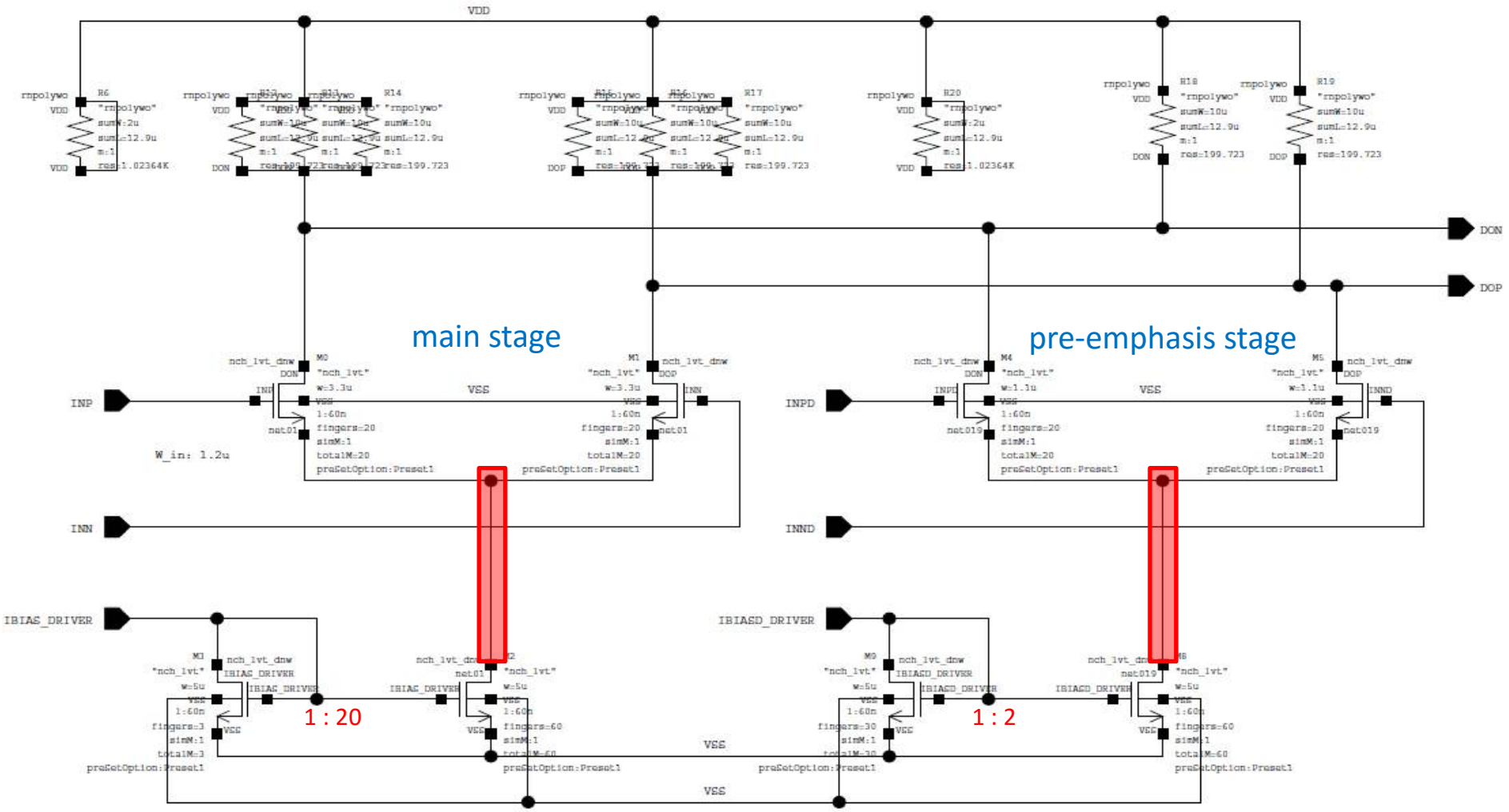
DHPT 1.0

CML DRIVER

DHPT 1.0

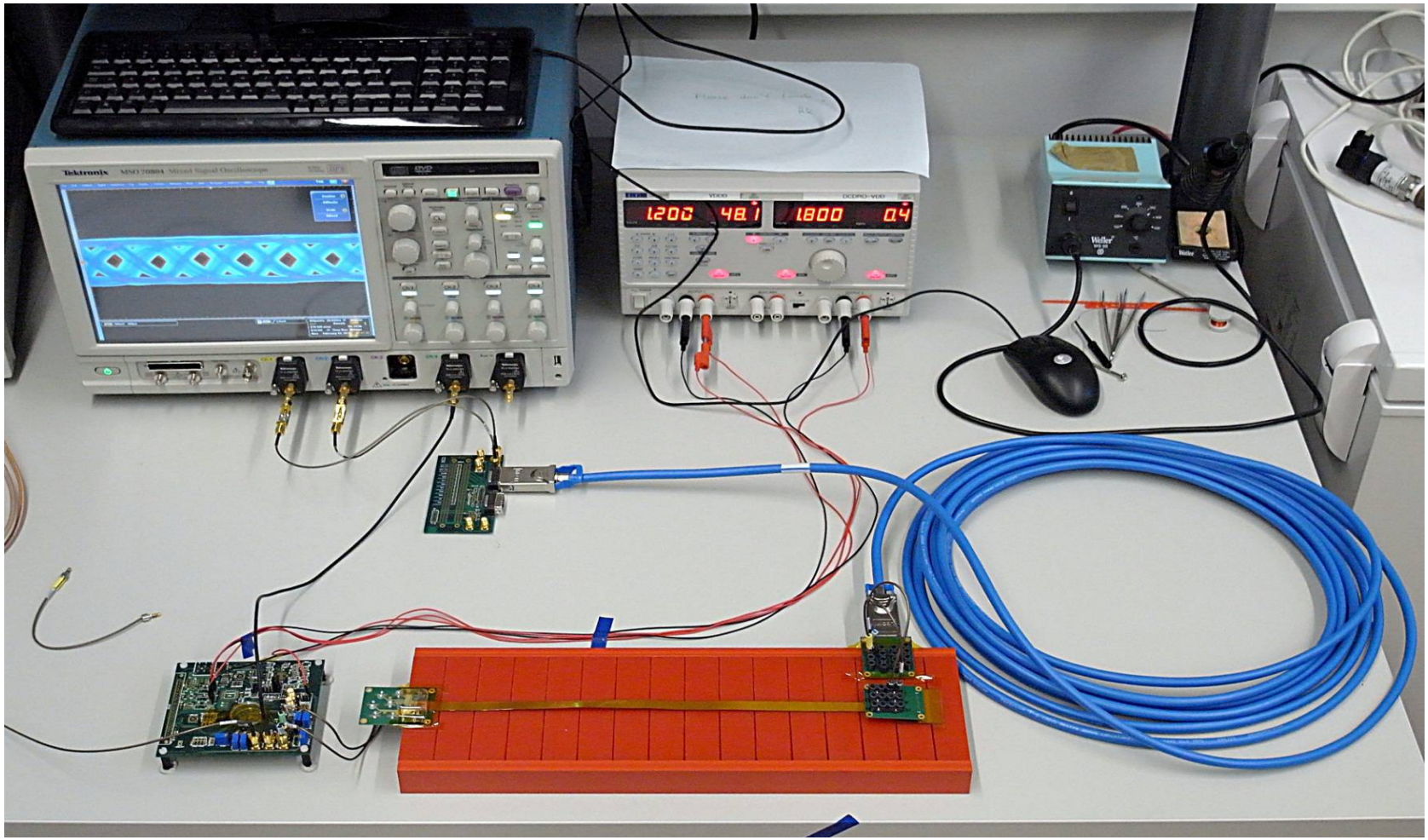
CML DRIVER

Driver Schematic



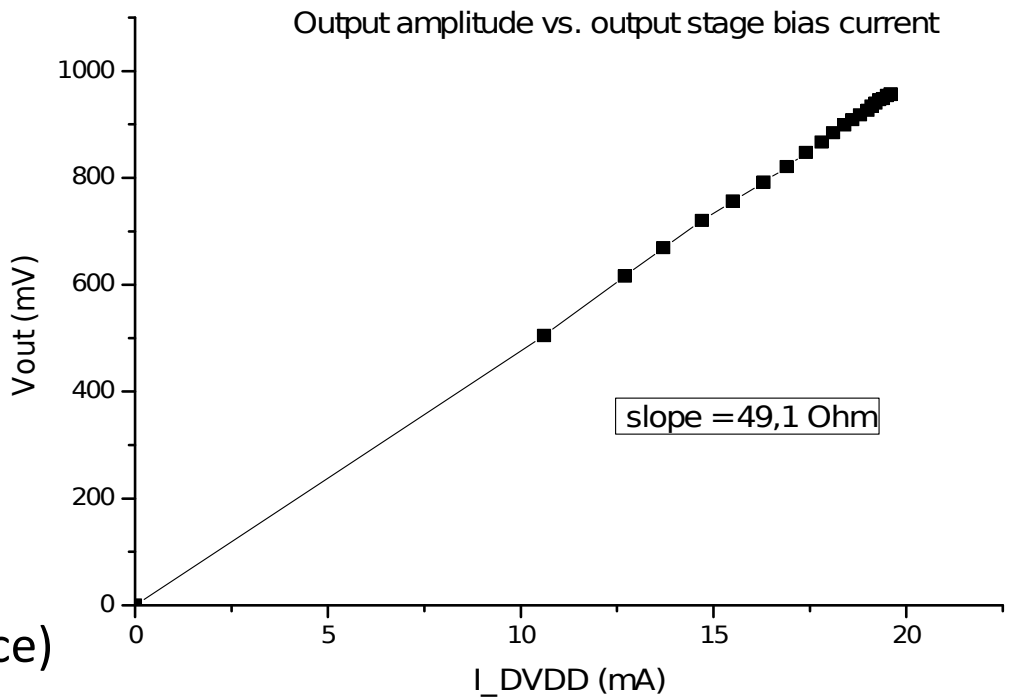
DHPT 0.1 – Test setup

universitätbonn



Differential Output Amplitude

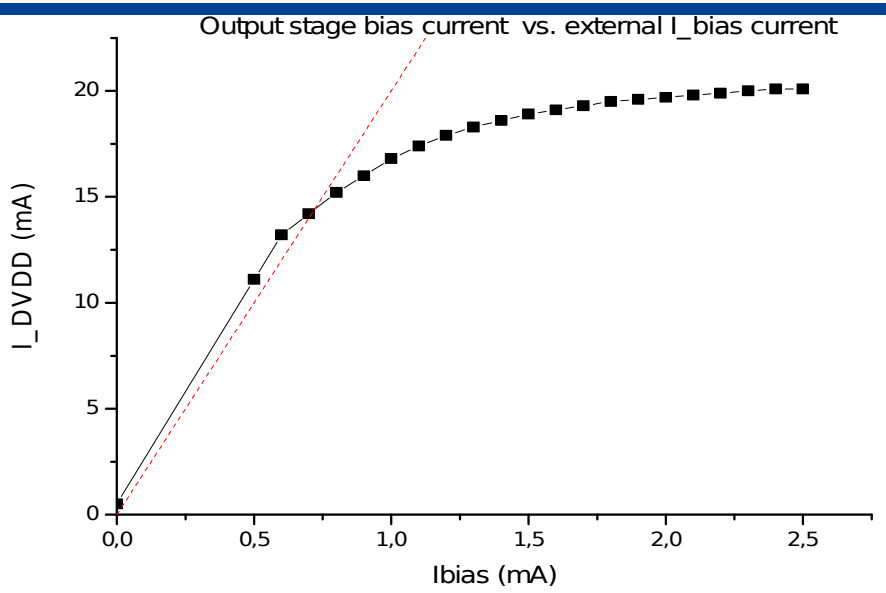
- Linear function of bias current (IBIAS_DRIVER)
- IBIAS_DRIVER ≈ I_DVDD
- Preemphasis off (IBIASD_Driver = 0)
- Effective output resistance: 49.1 Ohm
- DC output resistance: 55 Ohm
- ➔ ~3.5 Ohm Series resistance (chip wiring, bond wire, PCB trace)



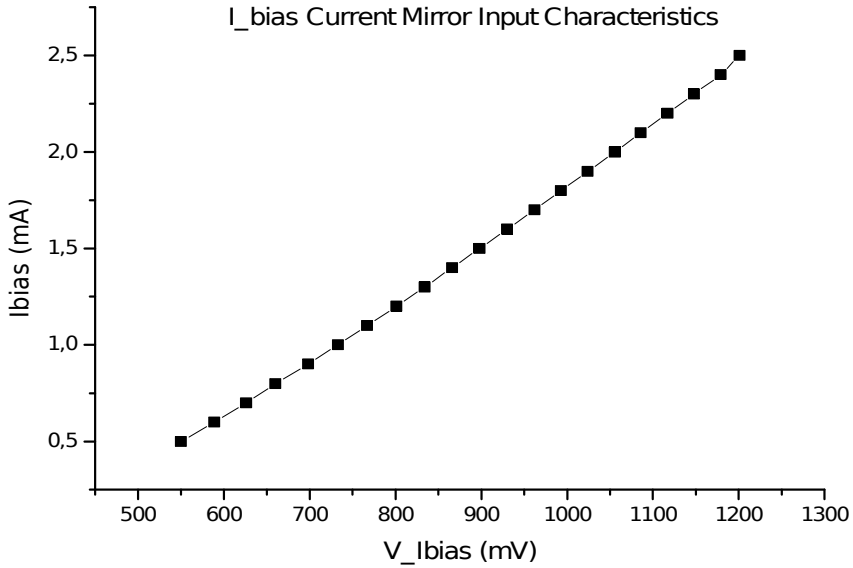
➔ Output resistance Ok

Main Output Current Mirror

- IBIAS_DRIVER current mirror
- Design value
  IBIAS_DRIVER/Ibias = 20
- Non-linear for Ibias > 0.7mA
  ➔ M2 not saturated?
- Drive current limited to 20 mA
  → $Vout_{max}$ = 957 mV

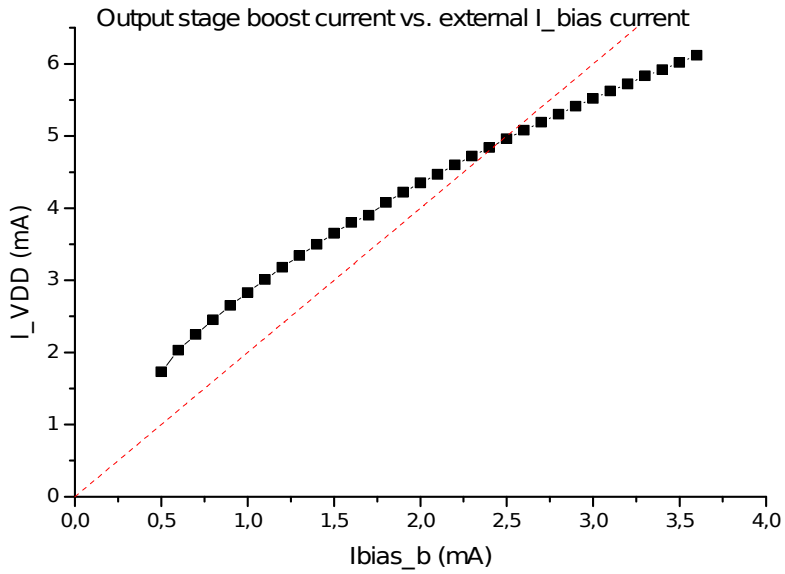


➔ Limited by current sink (M2) or switches M0/M1 (too high on resistance or parasitic wiring resistance)

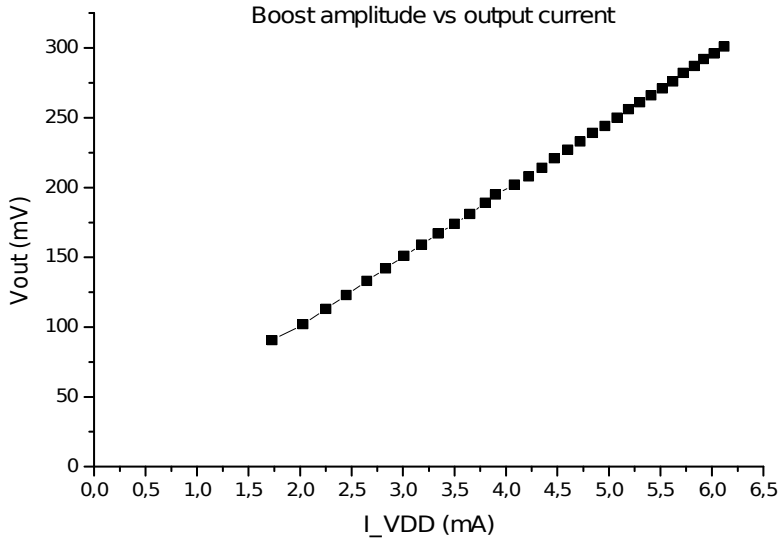


Boost Output Current Mirror

- IBIASD_DRIVER current mirror
- Design value
  IBIASD_DRIVER/Ibiasd = 2
- Fair linearity
- Drive current limited to 6.12 mA
  → $Vboost_{max}$ ~300mV



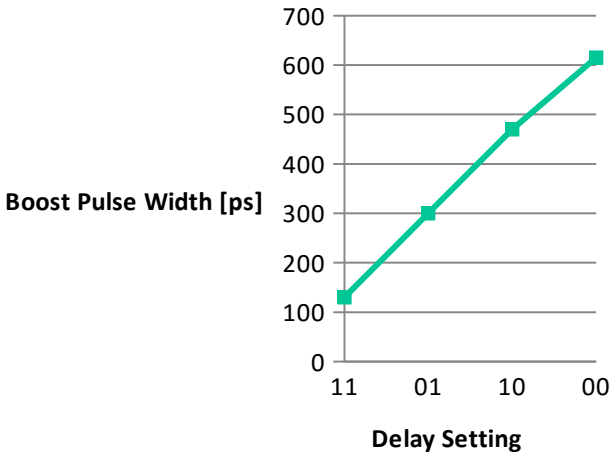
➔ Enhancement:
Make boost current sink M8 stronger

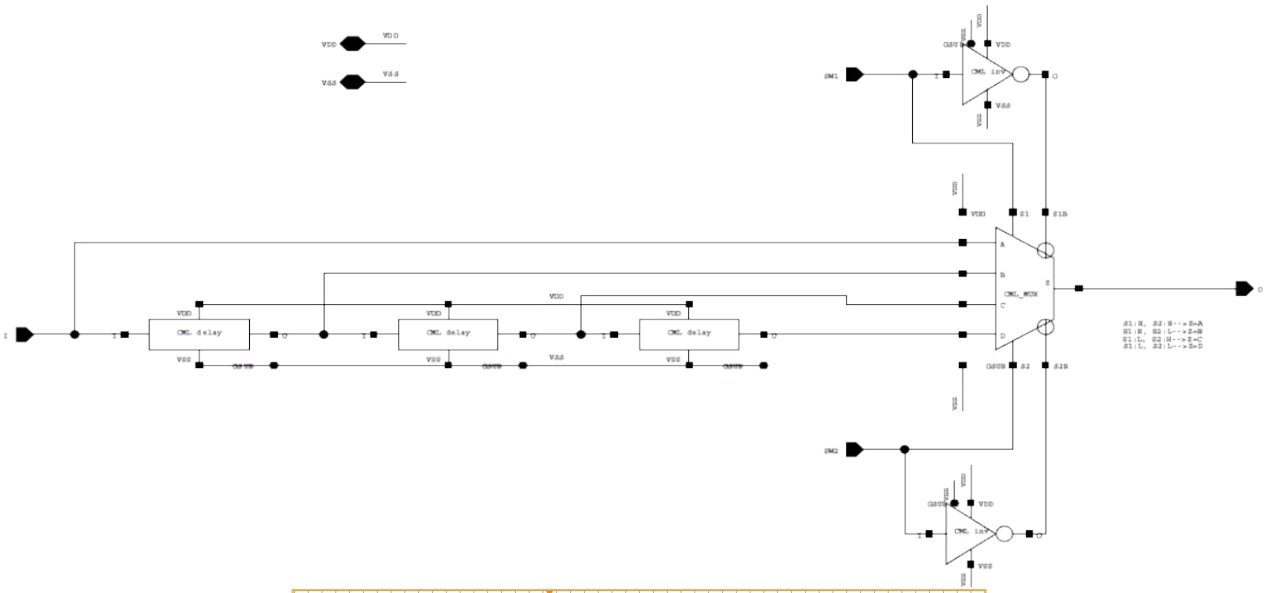


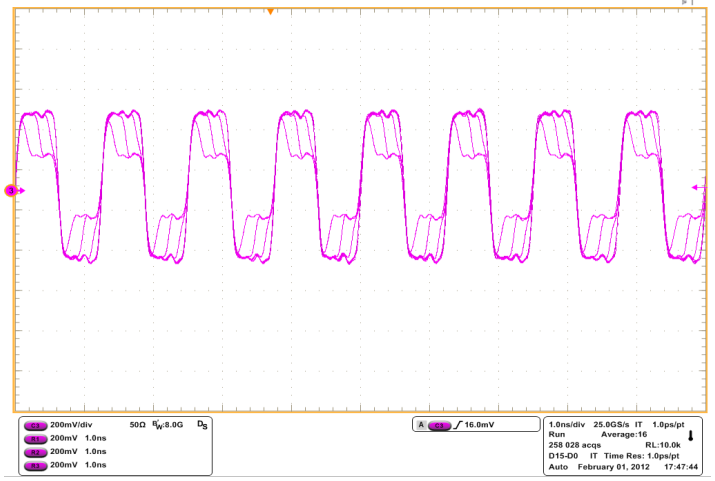
Delay Settings

Setting SW[1:0]	Pulse Width [ps]
11	130
01	300
10	470
00	615

➔ ~170 ps per delay buffer



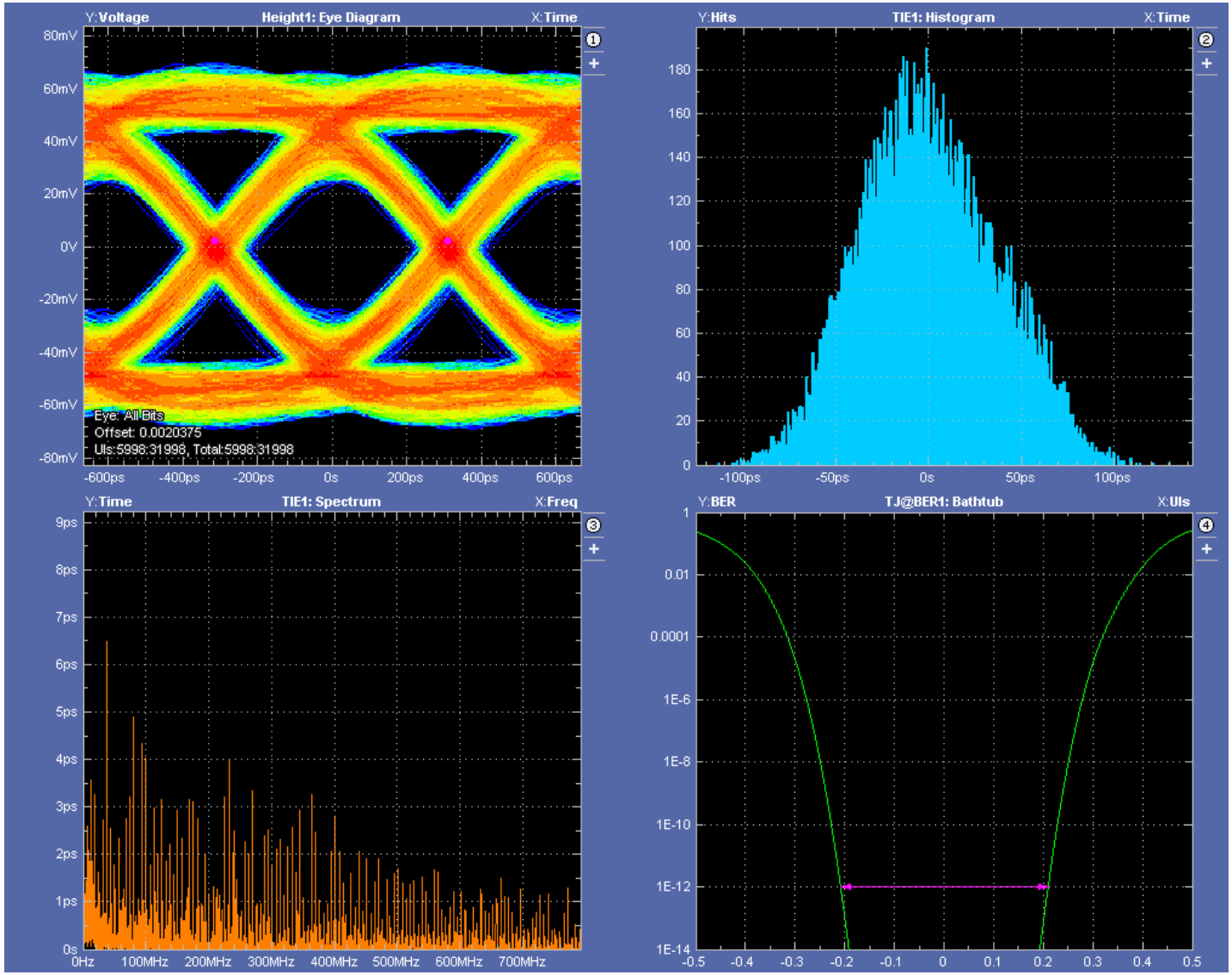




800 MHz clock, different delay settings

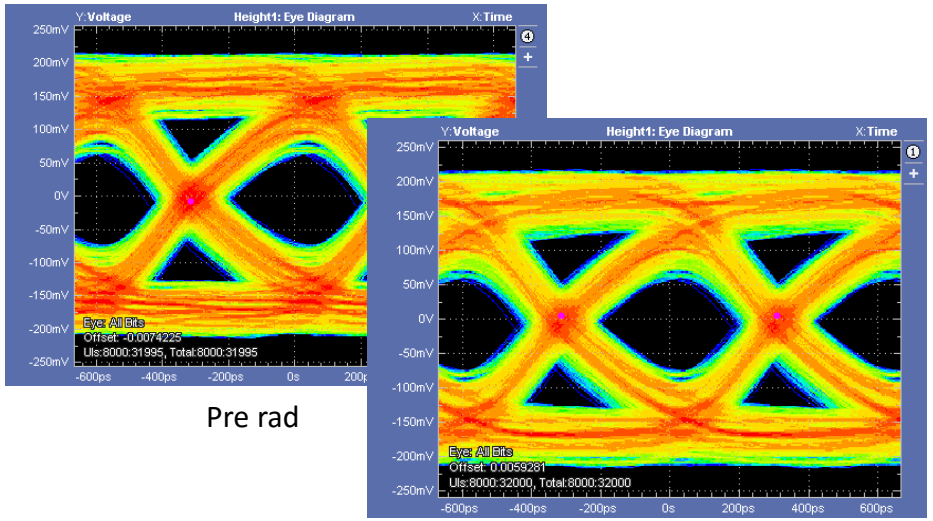
Signal Integrity Characterization

- 1.6 Gbps LFSR-8
- 30 cm kapton cable + 20m AWG26 twisted pair cable



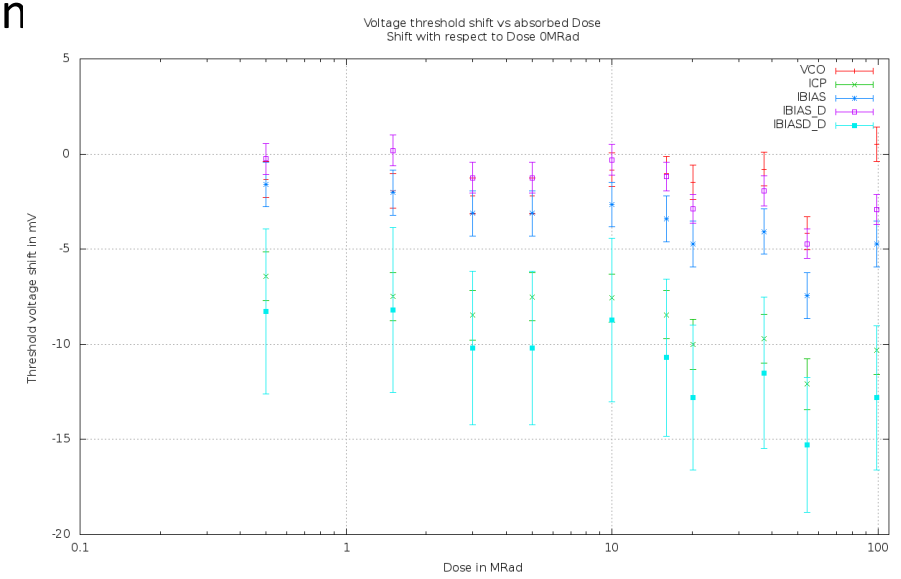
X-ray Irradiation

- TSMC 65nm TID tolerance:
  - V_{THR} shift (wide pMOS and nMOS only)
  - PLL + Gbit link performance
- Up to 100 Mrad (60keV X-ray tube, Karlsruhe)
- Dose rates: ~300 kRad/h (initial) → ~2Mrad/h (end)
- Annealing after each step: 80°C for 100 min



Pre rad

100 Mrad

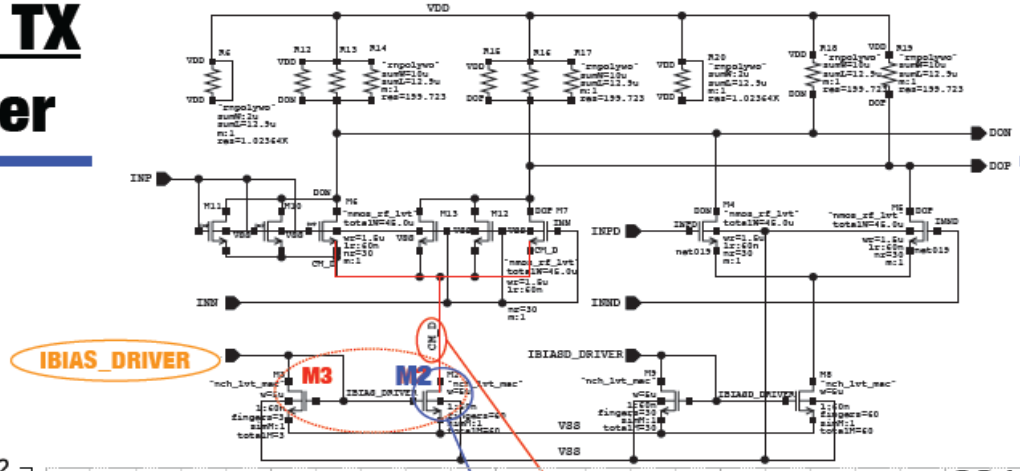


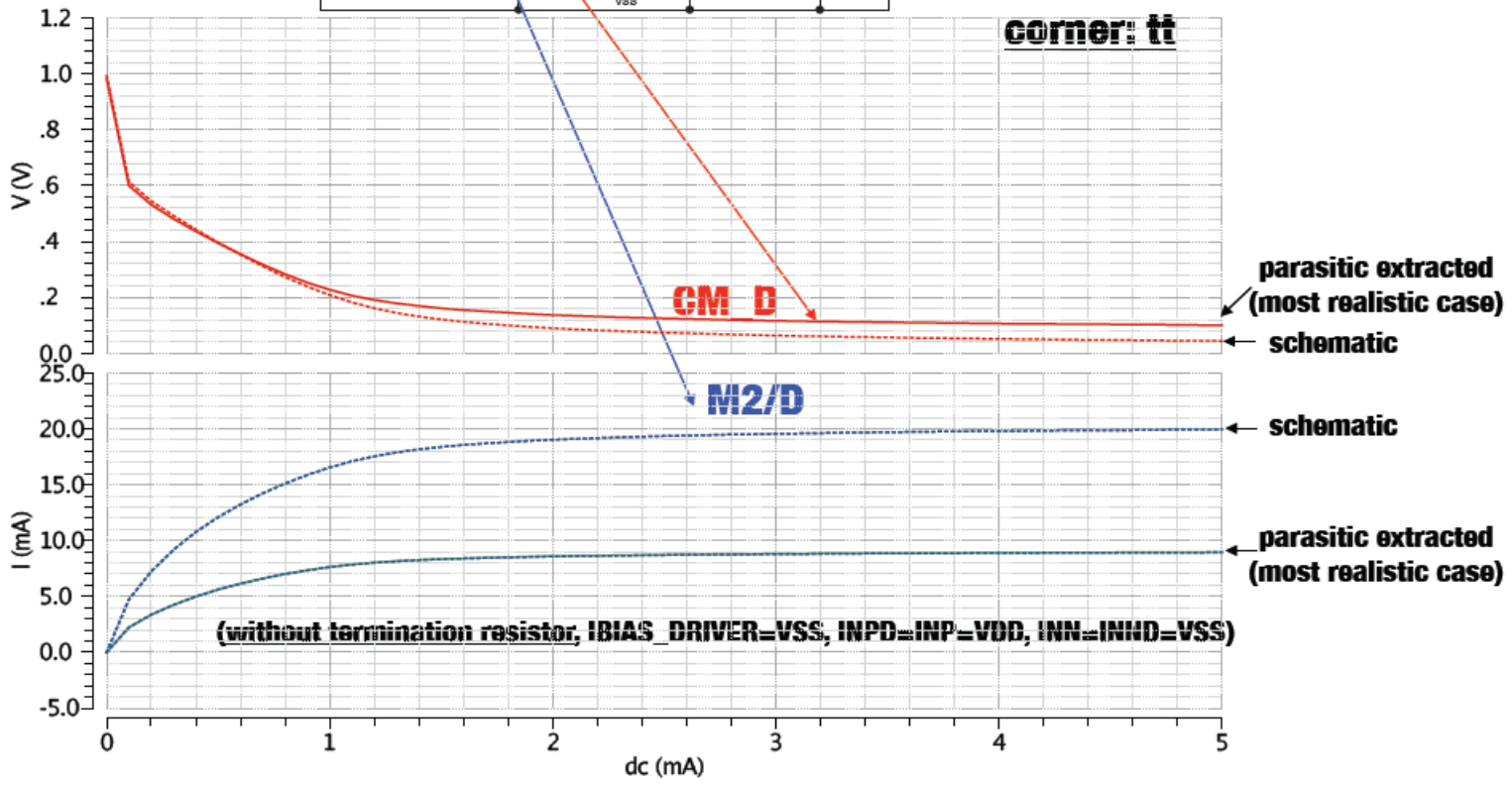
No TID induced degradiation observed up to 100 Mrad

DHPT10 CML TX

Main driver

universitätbonn



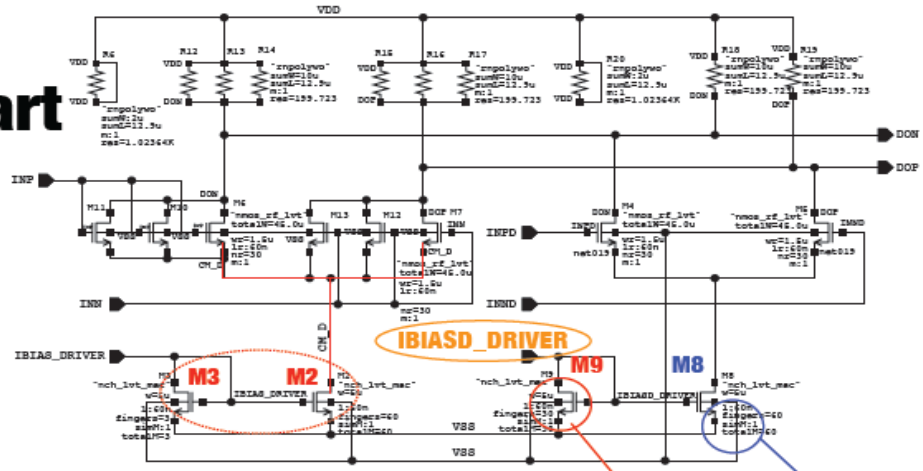


06.05.2015, T.Kishishita

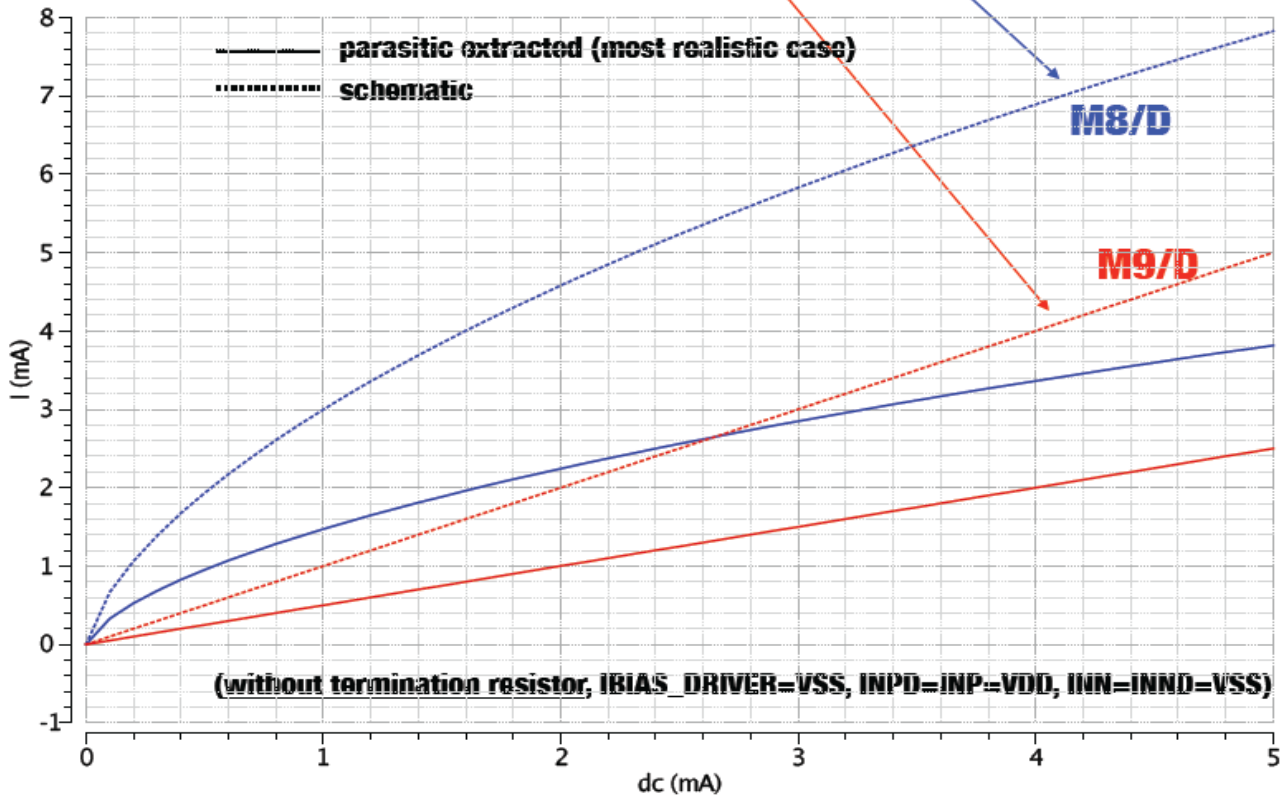
DHPT10 CML_TX

Pre-emphasis part

universitätbonn



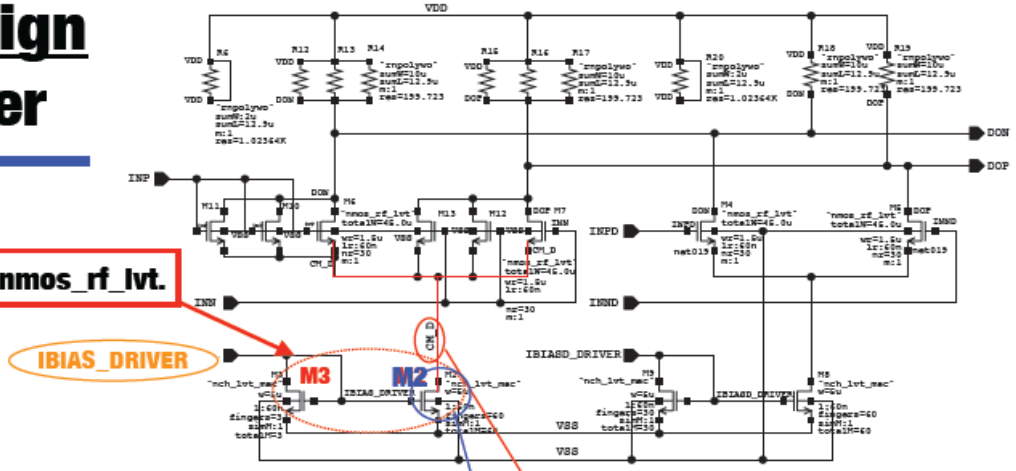
corner: tt



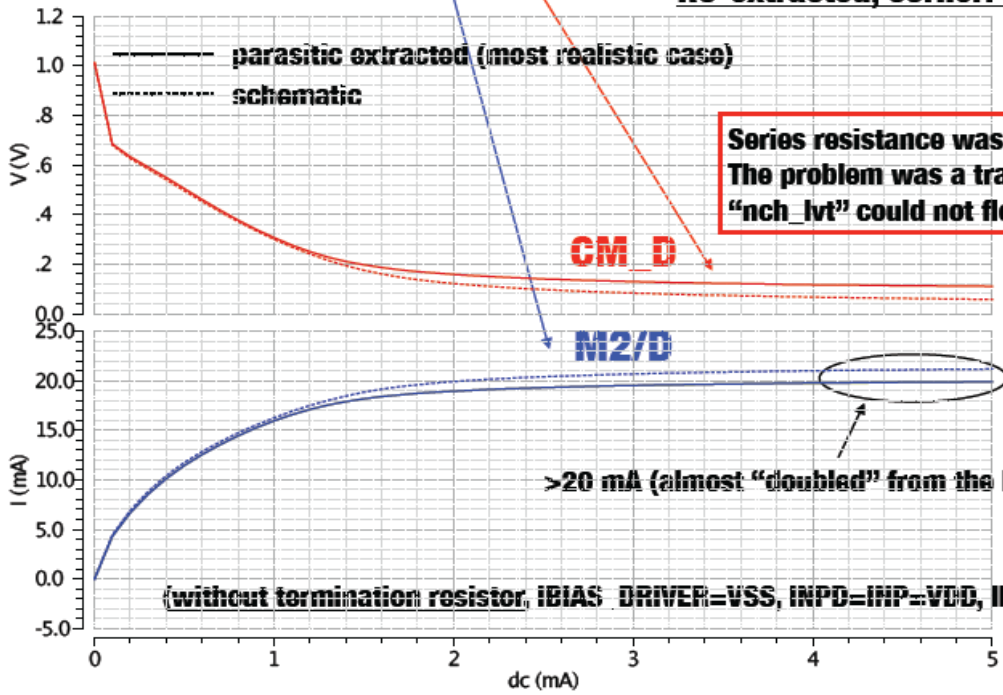
Improved Design
Main driver

universitätbonn

replaced from "nch_lvt" to nmos_rf_lvt.



RC-extracted, corner: tt



Series resistance was not a major problem.
The problem was a transistor type of the current mirror.
"nch_lvt" could not flow much current.

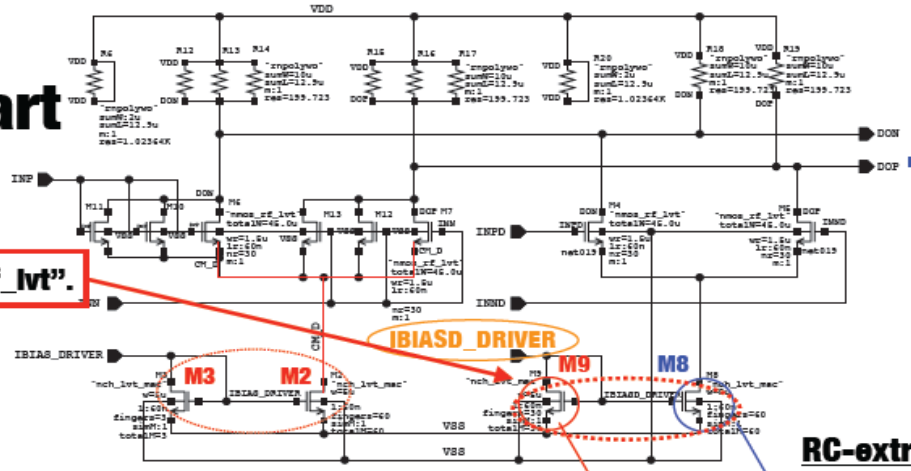
>20 mA (almost "doubled" from the DHPT10 design)

(without termination resistor, IBIAS_DRIVER=VSS, INPD=INP=VDD, INN=INND=VSS)

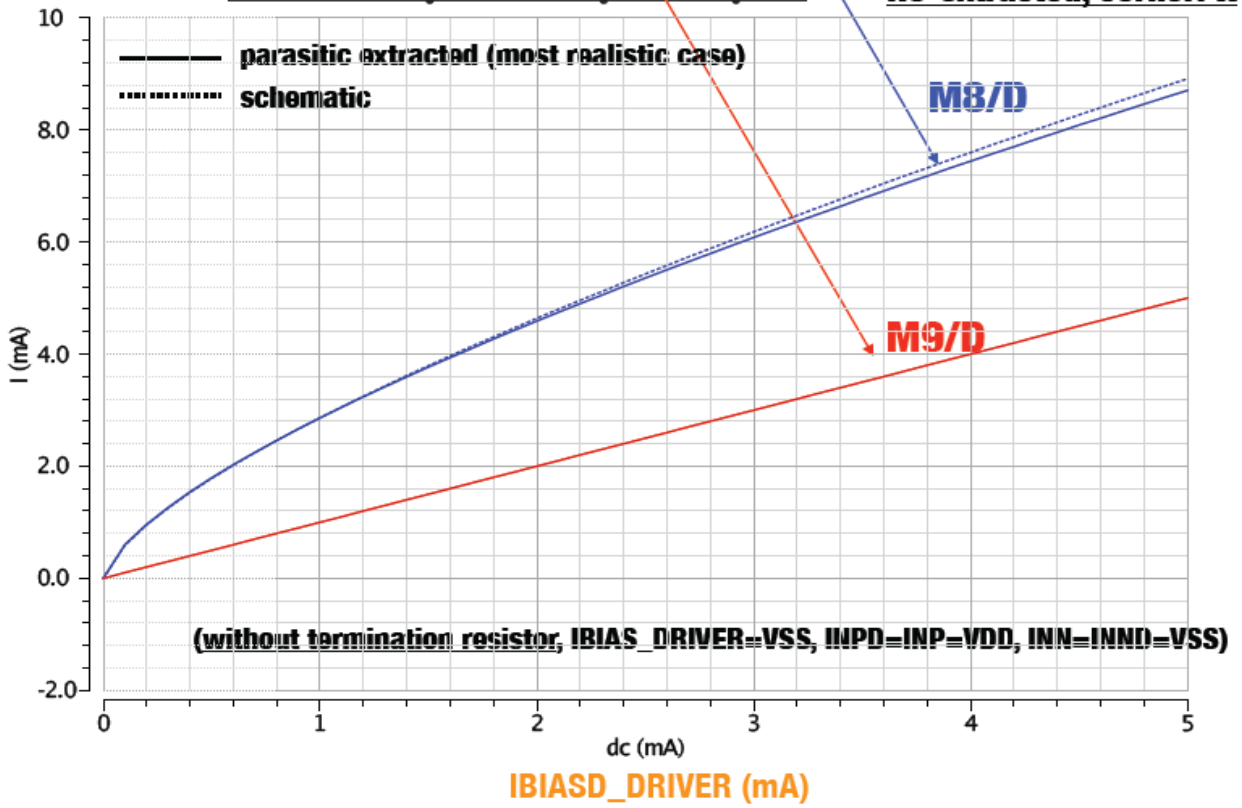
Improved Design
Pre-emphasis part

universitätbonn

replaced from “nch_lvt” to “nmos_rf_lvt”.



RC-extracted, corner: tt



21.04.2015, T.Kishishita

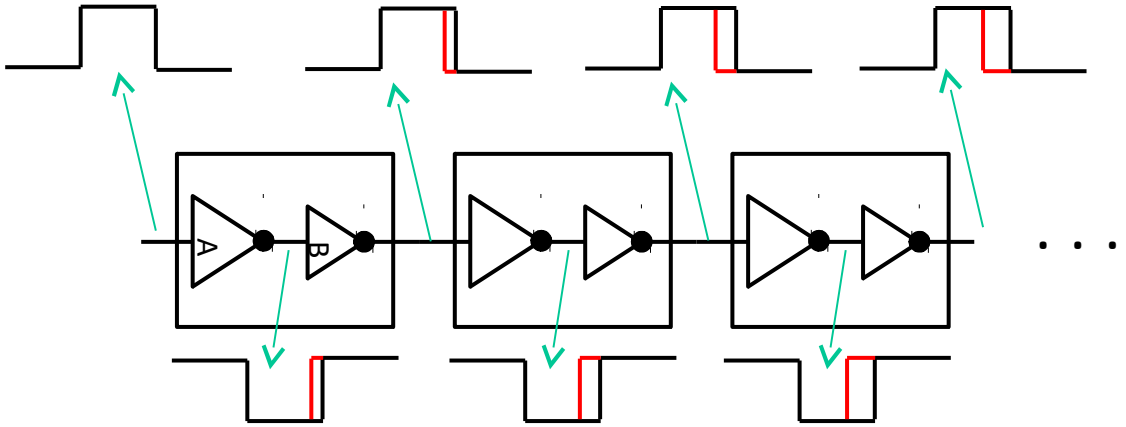
DHPT 1.0

DELAY ELEMENTS

Delay Element Issues

- Programmable delay lines made from std. cell delay elements (dual inverters)
- Inverter have usually unequal propagation delays for rising and falling edges (Asymmetry of PMOS-NMOS drive strength, process corners, W/L…)
- The **std. cell delay** elements consist of **alternating no-equal sized inverters**

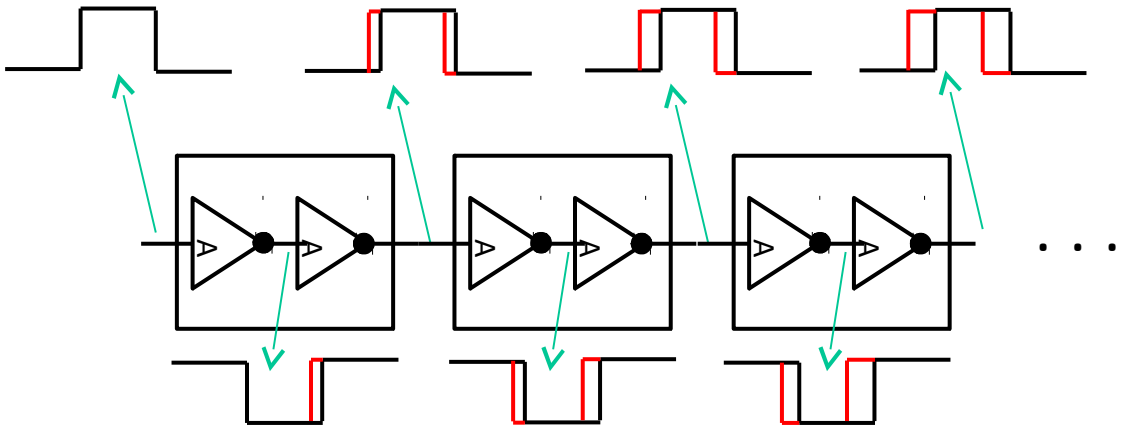
→The difference in t_{pd} for rising and falling edges for inverter A and B is <u>different</u>!



→ Duty cycle distortion increases (accumulates) with the number of delay elements used, i.e. the programmed delay time

Delay Element Issues cont.

- If all **inverters in the delay chain are equal** (and the number of inverters is even), **no duty cycle distortion** occurs (differences in rising and falling edge propagation delay cancel out)

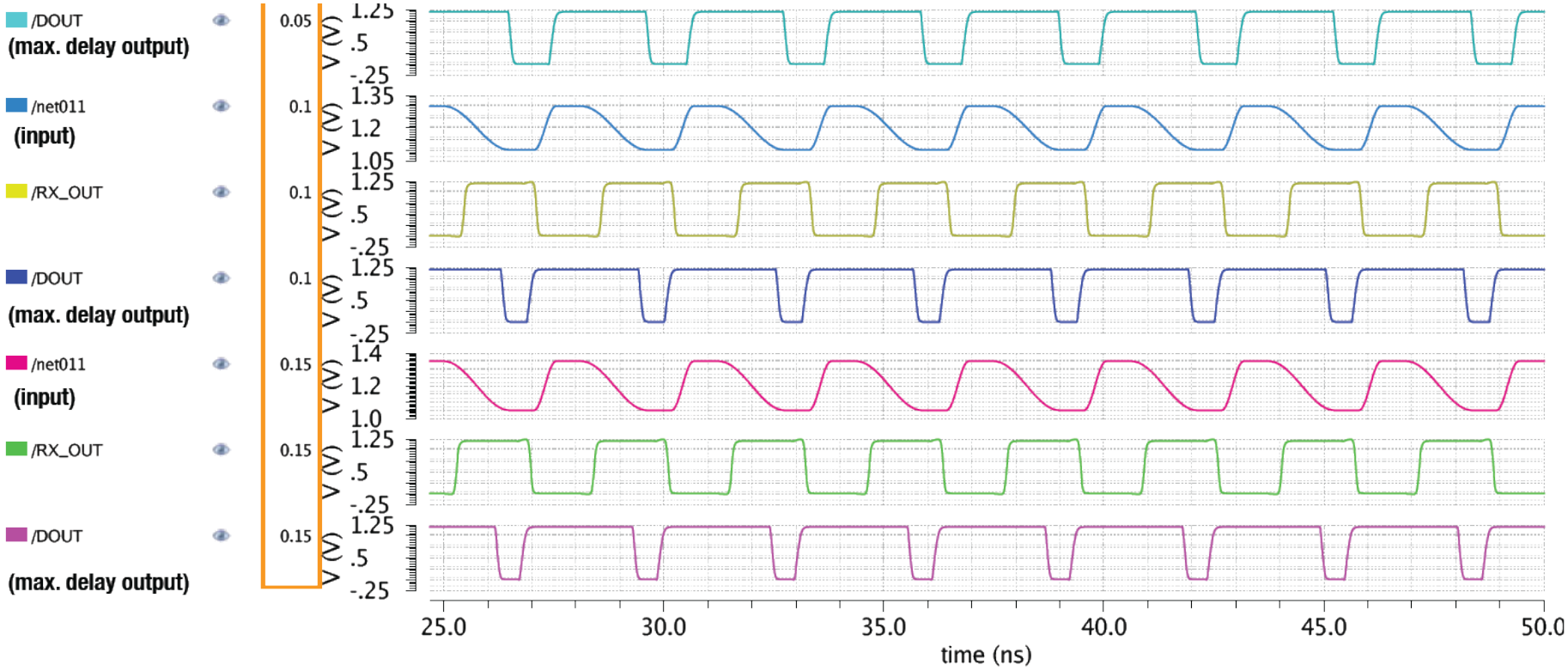


➔ Implemented new, custom made delays based on identical inverters

Duty cycle distortion

universitätbonn

- Duty cycle distortion was overlooked during DHPT 1.0 sign-off



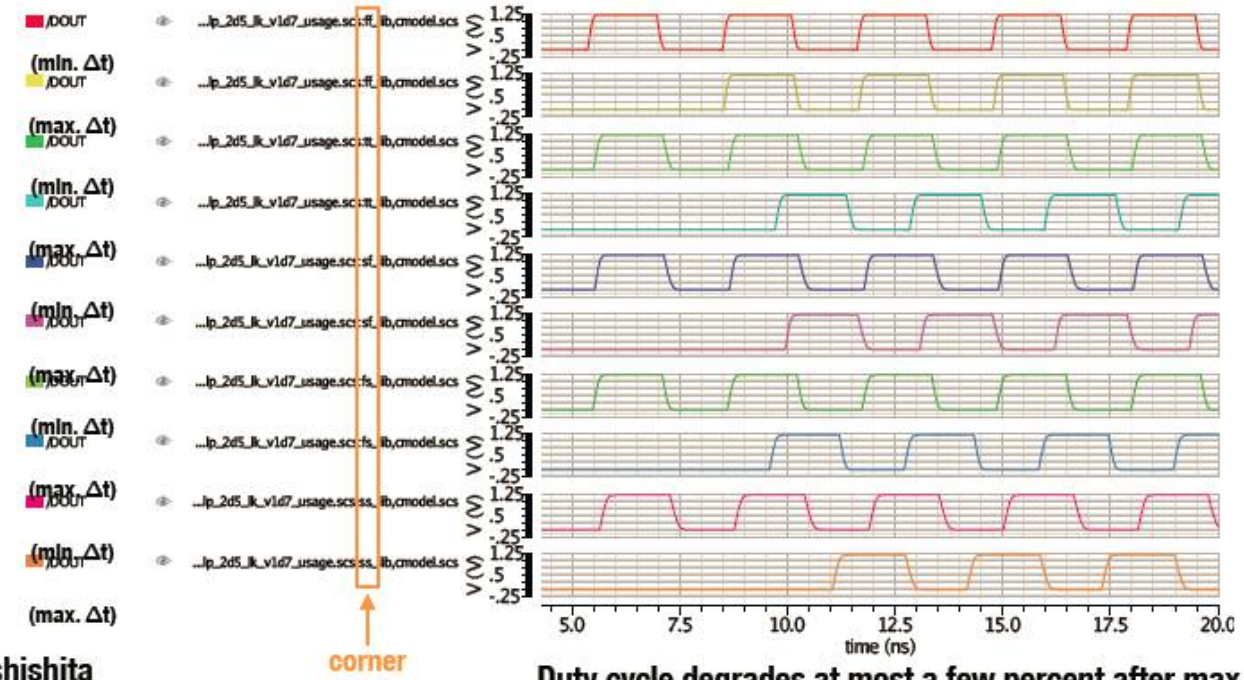
Delay Element Modification

- Custom delay elements made out of identical inverters

All corners covers 3.125 ns (←320 MHz).

Max. delay time with extracted model

	Δt	duty cycle (min. Δt)	duty cycle (max. Δt)
tt	4.20 ns	52.0%	53.3%
ff	3.15 ns	51.4%	52.2%
fs	4.10 ns	51.6%	51.8%
sf	4.43 ns	52.2%	54.9%
ss	5.42 ns	52.8%	54.9%



07.04.2015, T.Kishishita

Duty cycle degrades at most a few percent after max. delay.

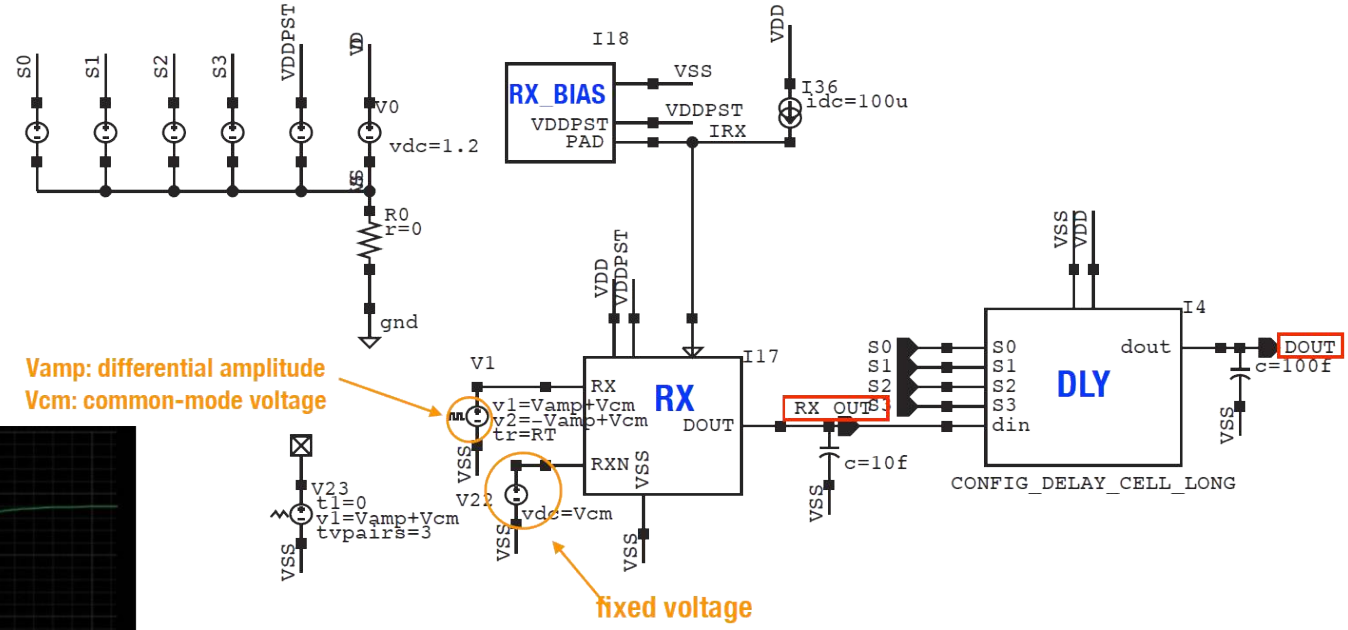
universitätbonn

DHPT 1.0

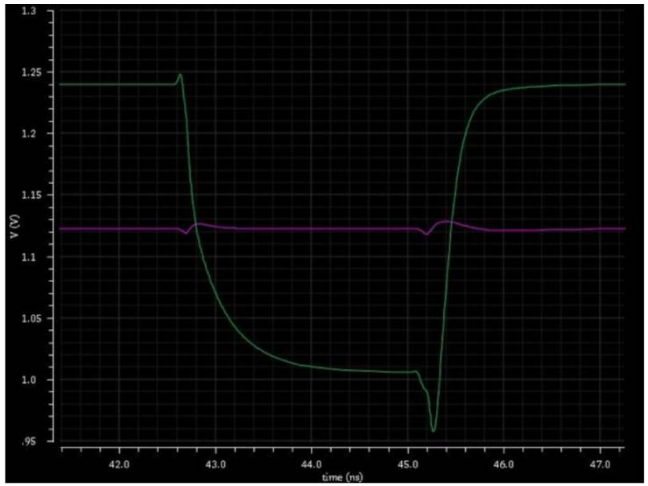
DCD DATA RECEIVER

DCD Data Receiver

- Single ended DCD data receivers based on LVDS receivers → low voltage single ended signaling (LVSE)



DCD LVDS output (from Ivan)

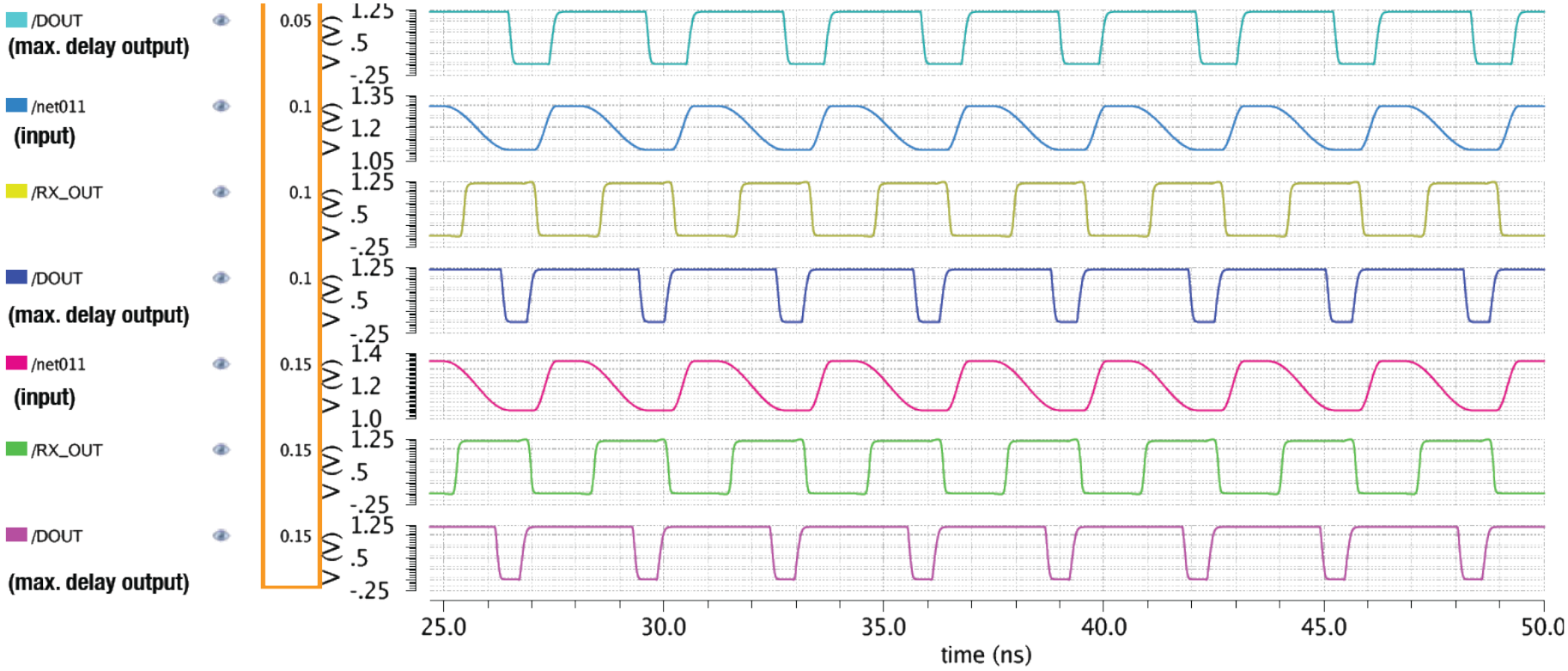


- the falling and rising edges with non-symmetrical shape
- differential amplitude of 120 mV

Duty cycle distortion

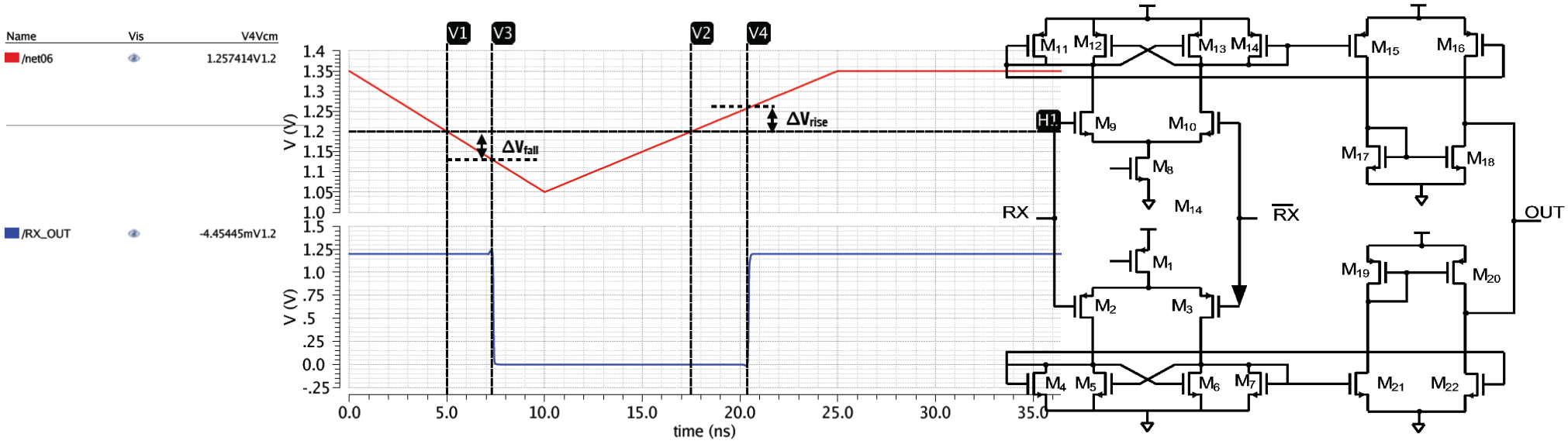
universitätbonn

- Duty cycle distortion was overlooked during DHPT 1.0 sign-off



LVDS Receiver (DHPT 1.0)

- LVDS RX with build-in hysteresis



Markers

	Vcm	V1	V2	V3	V4
x		5.0ns	17.4689ns	7.31256ns	20.3707ns
/net06					
/net06	1.2	1.2V	1.199378V	1.130623V	1.257414V
/RX_OUT					
/RX_OUT	1.2	1.2V	37.1315nV	1.22718V	-4.45445mV

	ΔVfall	ΔVrise
ff	55 mV	46 mV
fs	71 mV	57 mV
sf	68 mV	57 mV
ss	85 mV	68 mV

ΔV_{rise}=57 mV
ΔV_{fall}=70 mV (for nominal corner)

LVDS Receiver Design Modification

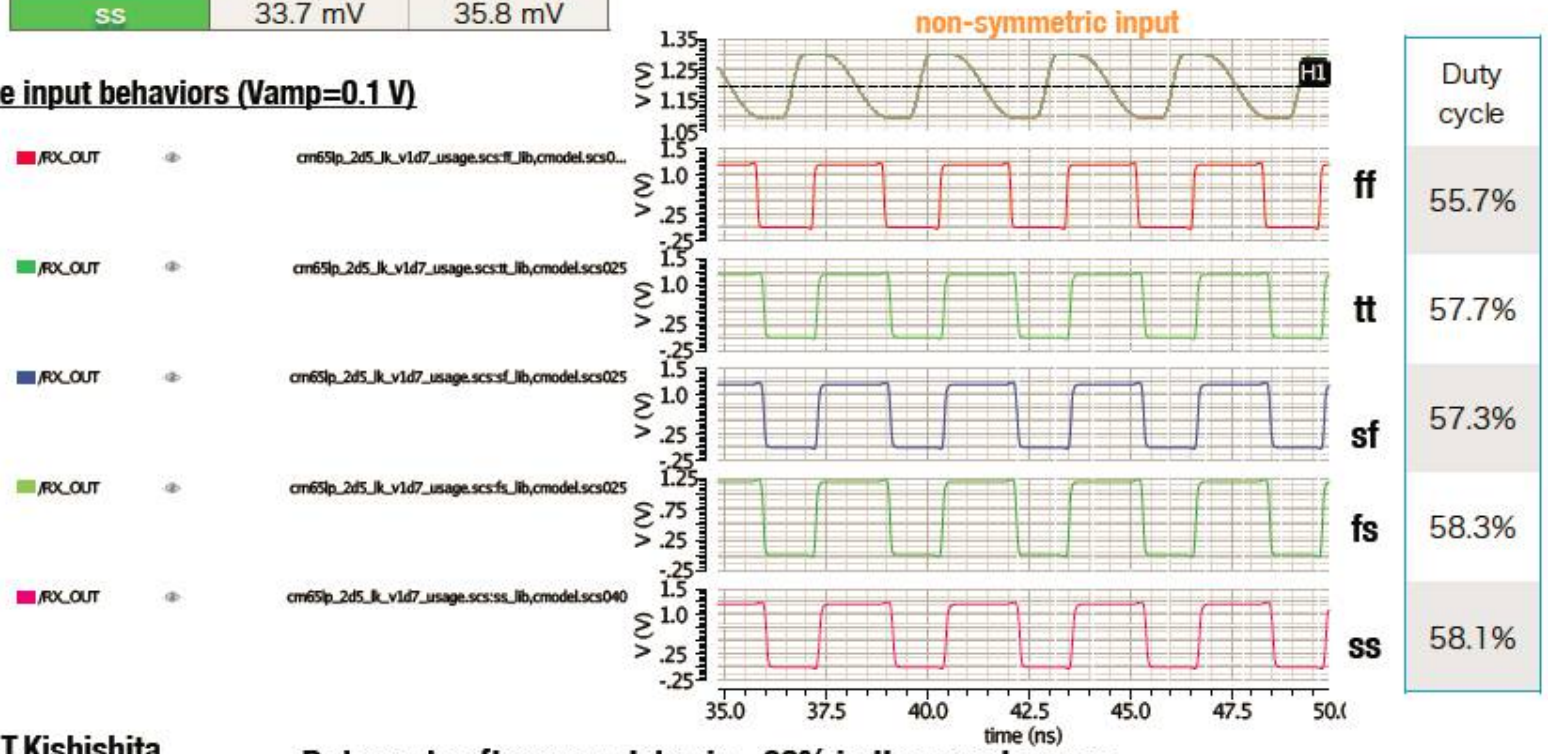
universitätbonn

FET sizes and layout modified to reduce hysteresis (~50% of the current DHPT1.0 design).

Hysteresis values with extracted model

	ΔVfall	ΔVrise
tt	27.5 mV	34.4 mV
ff	19.8 mV	30.0 mV
fs	29.1 mV	33.4 mV
sf	26.3 mV	34.1 mV
ss	33.7 mV	35.8 mV

DCD-like input behaviors (Vamp=0.1 V)



07.04.2015, T.Kishishita

Duty cycle after max. delay is ~60% in the worst corner.