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SI LAB
Silizium Labor Bonn

DHPT1.0/1.1 and PXD9 Tests on Hybrid 5 Systems

9th Belle II VXD workshop
13th-15th January 2016, IFIC Valencia

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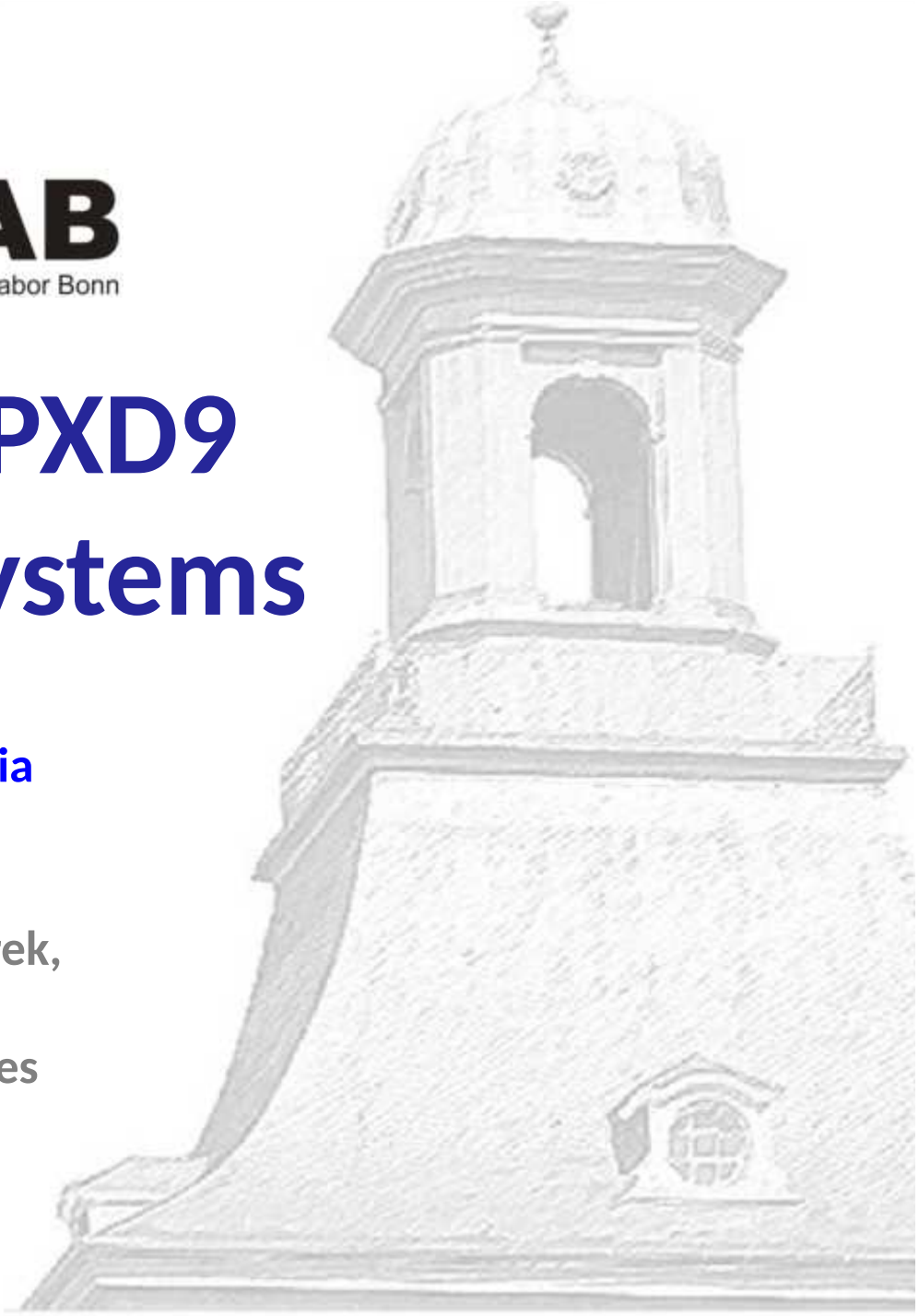

Contents

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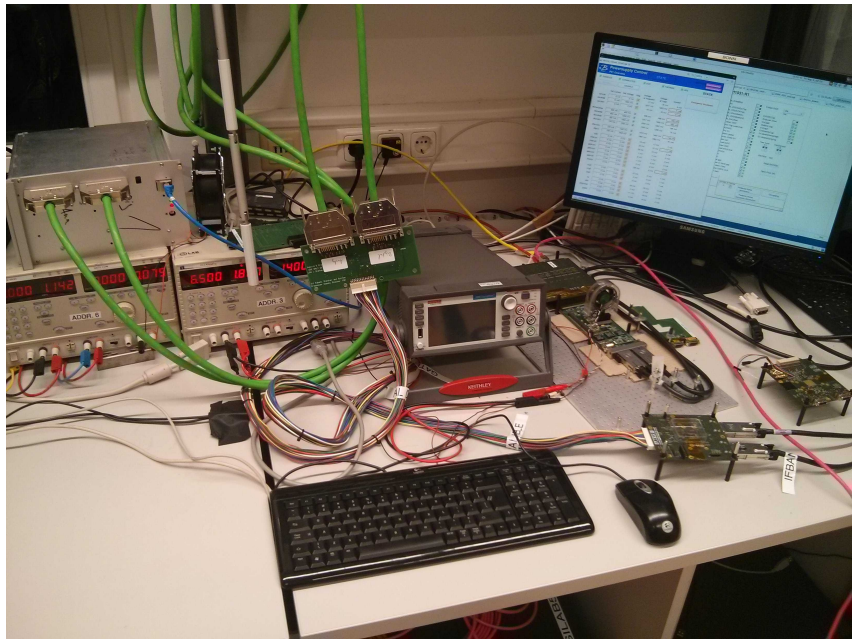
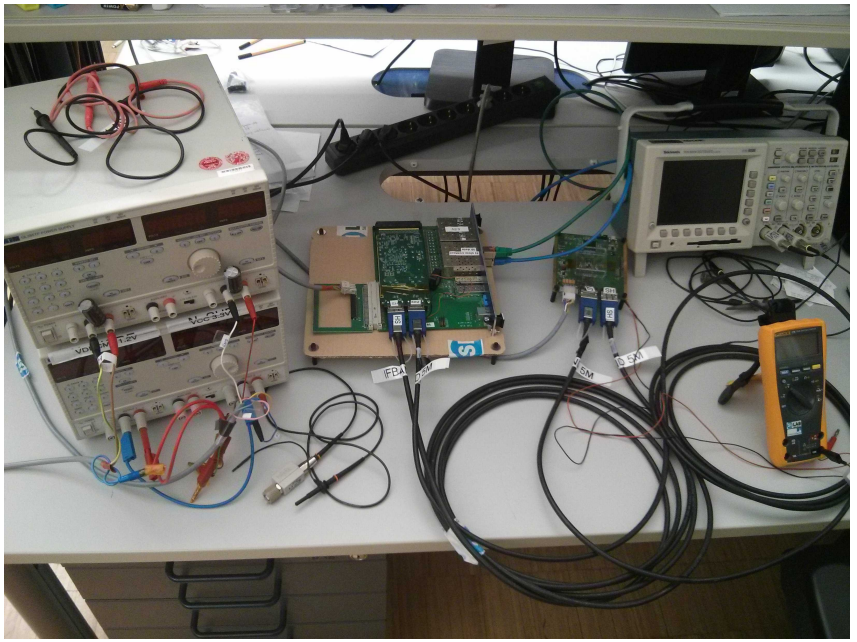
- Setups in Bonn
- Hybrid 5 test system optimization
- PXD9 small matrix laboratory test
- DHPT1.1 ↔ DCD communication

Setups in Bonn

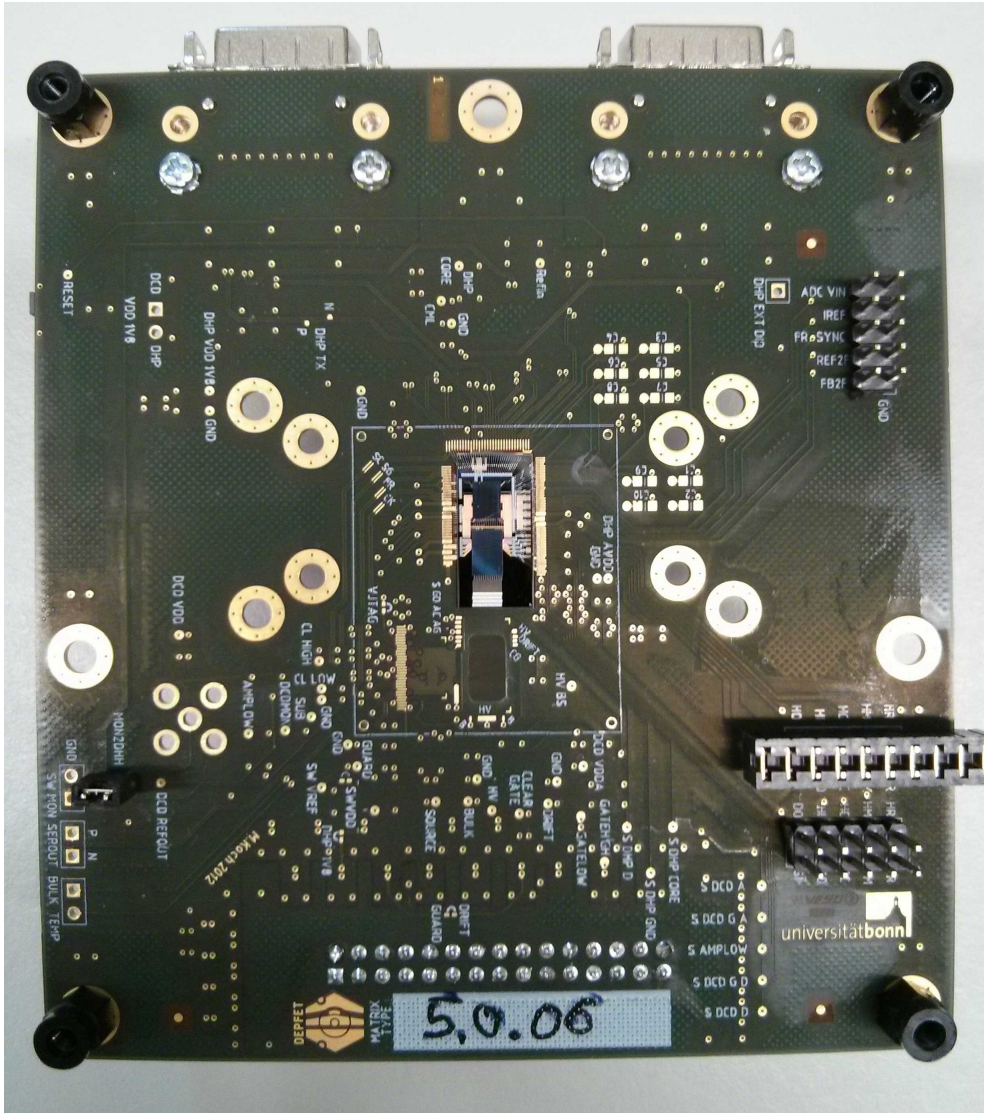
- Setup 1:
  DHH and LMU-PS
  for Hybrid 6 testing
- Setup 2:
  DHH and LMU-PS
  for Hybrid 5 testing
- Setup 3:
  DHH
  for debug cart (bonded DHP + FPGA)
  or needle cart (contacted DHP + FPGA)



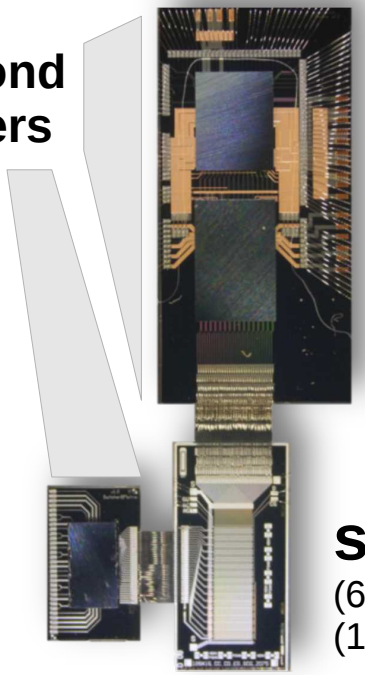


- Additional DHH for dedicated Switcher/Gated Mode tests requested

The Hybrid 5



[Hybrid 5.0.06]



wirebond adapters

switcher

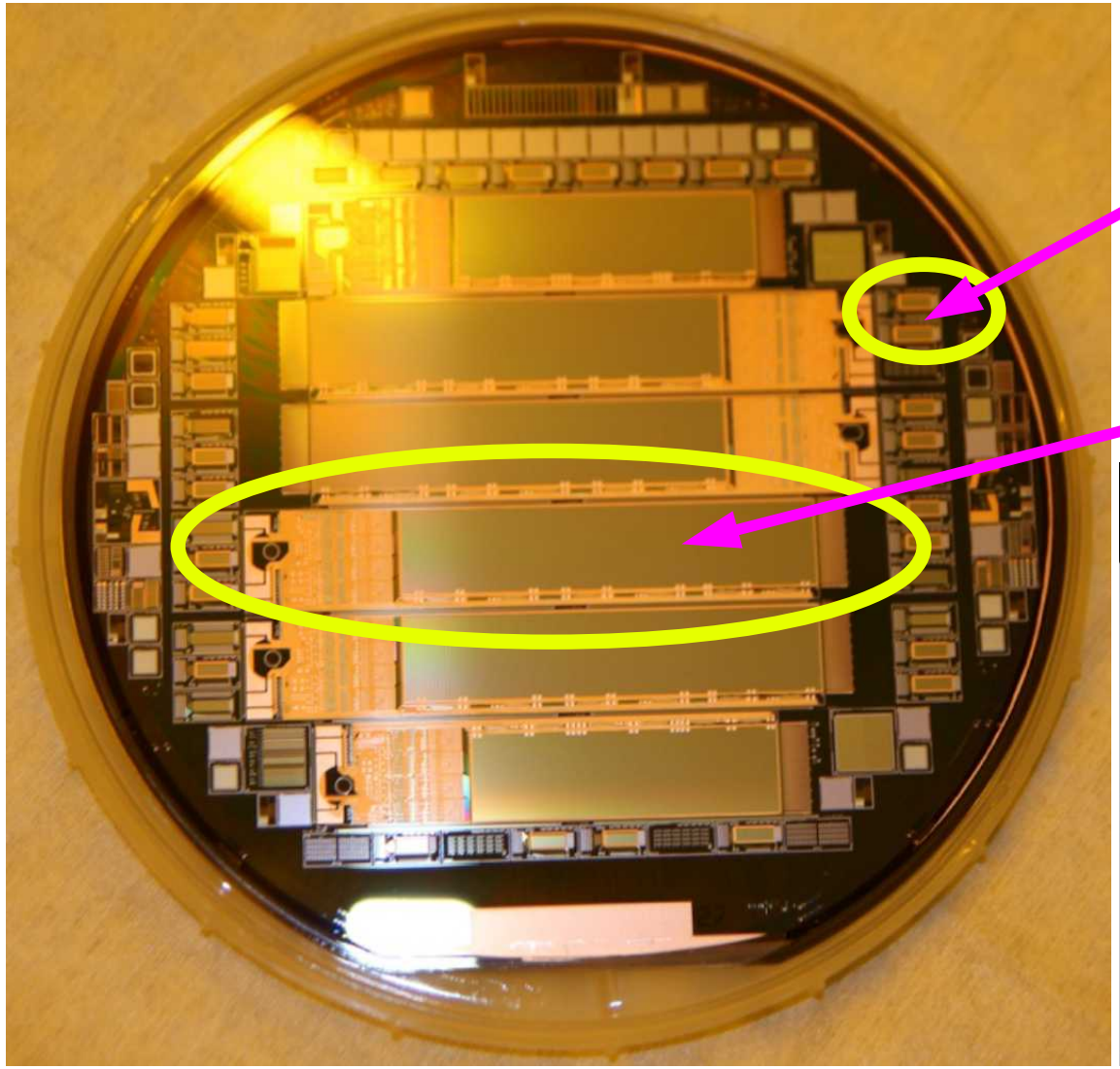
DHP
(Data Handling Processor)

DCD
(Drain Current Digitizer)

small matrix
(64x32 DEPFET pixels)
(16 gates, 128 drain lines)

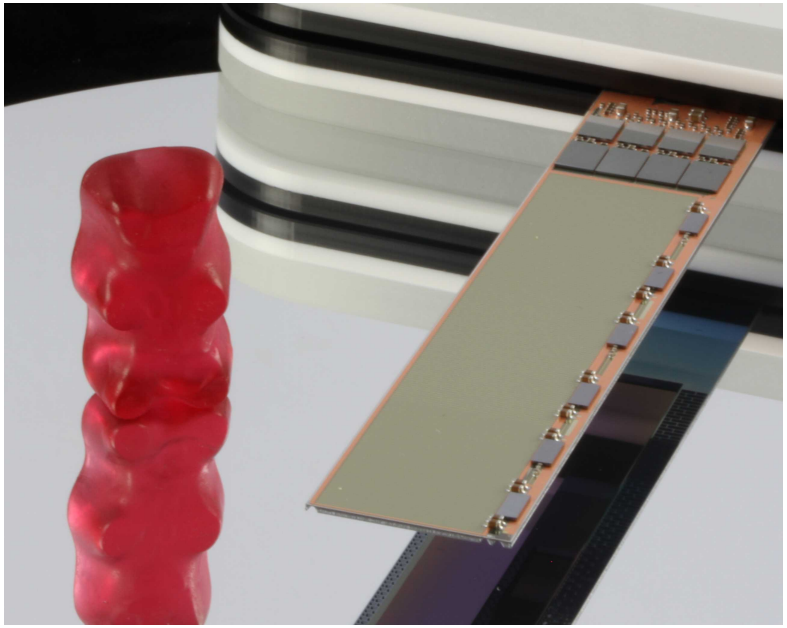
- Can be equipped with
  1 DHP, 1 DCD, 1 Switcher and 1 small matrix
- ASICs are bump-bonded to wirebond adapters
- Connection via 2 Infiniband cables and one Samtec multipole power connection

PXD 9



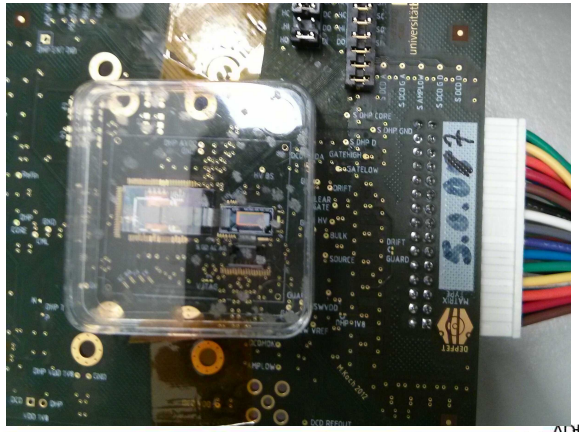
Small matrices
(80 x 32 pixels)
(16 gates, 128 drainlines)

Full modules with
Large matrices
(768 x 250 pixels)
(192 gates, 1000 drainlines)



Fully equipped Hybrid 5.0.07 (and 5.0.06)

- Two Hybrid 5 boards assembled with by then most recent ASICs (DHPT1.0, DCDpp, SwitcherB) and small PXD9 matrix in October 2015
- Test beam preparation campaign in Bonn with GOE and HLL



Laser pointer on PXD9 matrix (slightly wrong mapping)

Two full Hybrid 5 setups operated in parallel on one desk

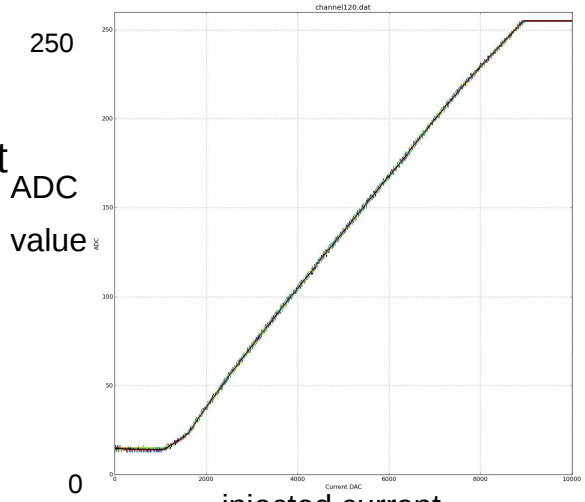
Optimization of ADCs

- ADC parameters of DCD optimized

  256 8 bit ADCs per DCD

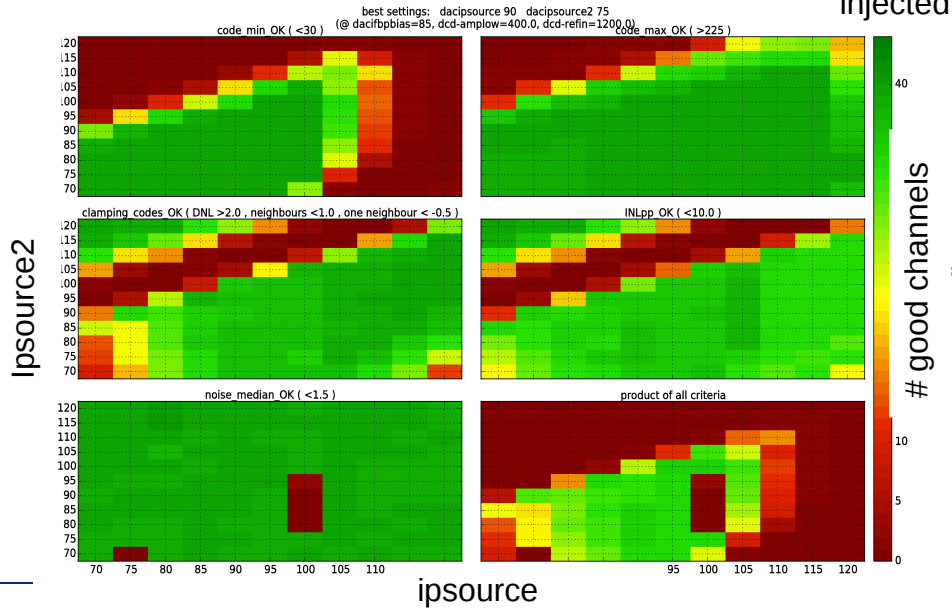
- Scans over two parameters at a time for a representative number of channels

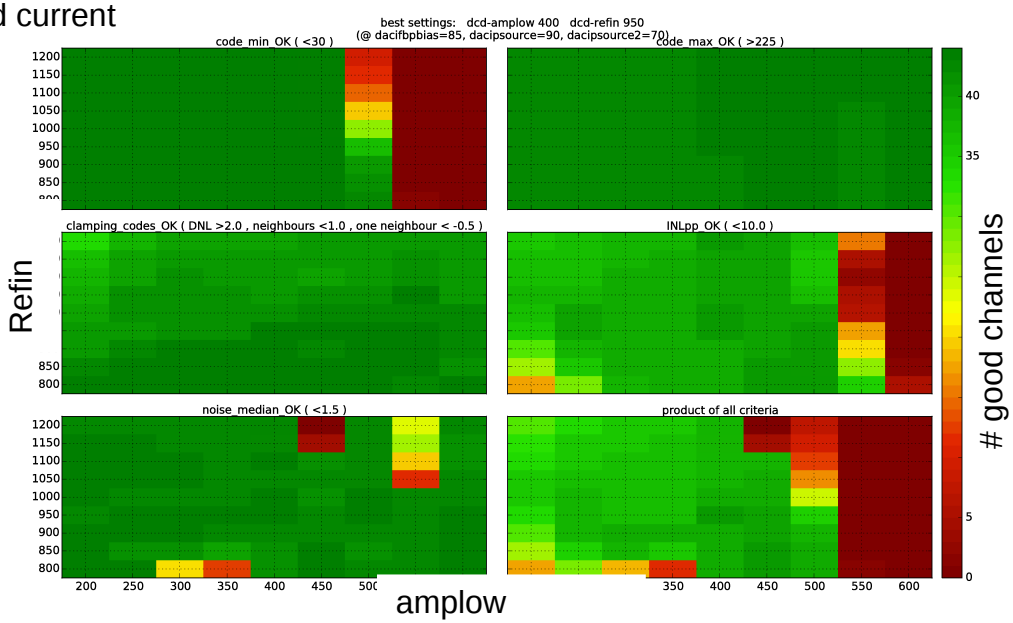
- Automated analysis:



Main DCD parameters:

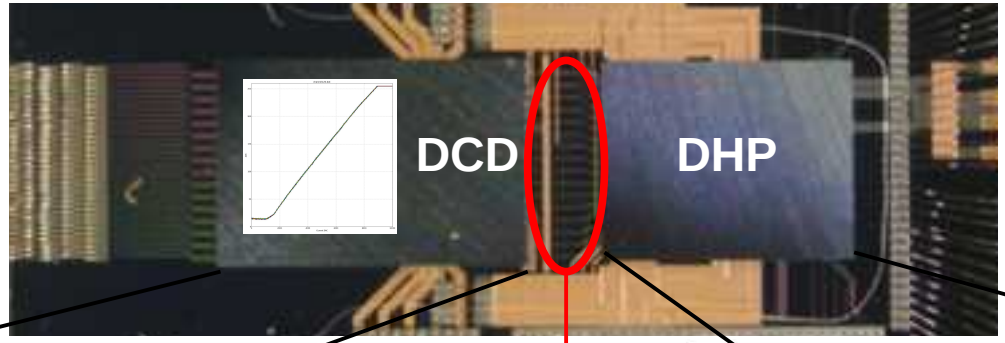
- Amplow (PS voltage)
- Refin (PS voltage)
- Ipsource (DAC)
- Ipsource2 (DAC)
- Ifbpbias (DAC)

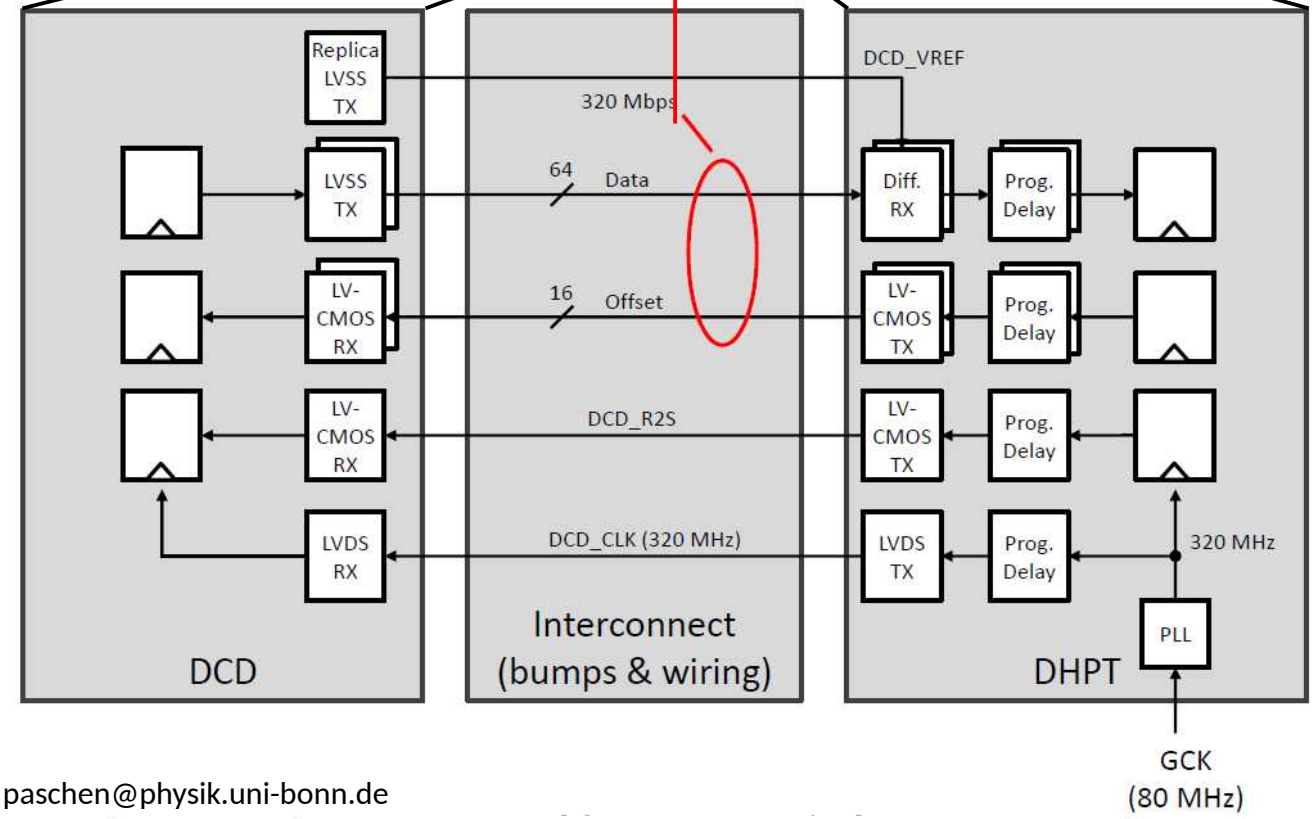


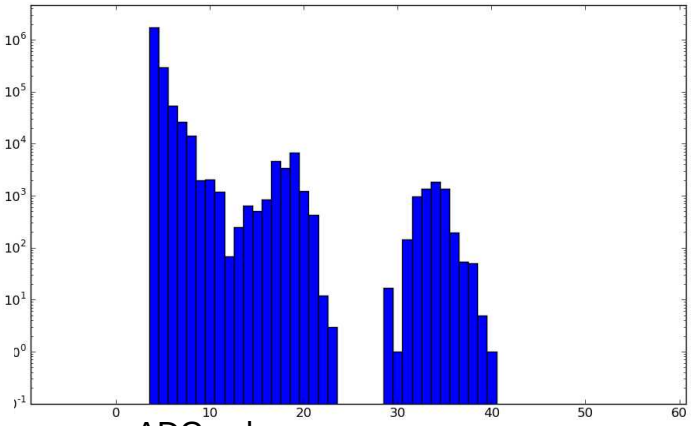


Optimization of DCD ↔ DHP communication

- Transmission of ADC values disturbed by digital errors (see previous talk by Benjamin)







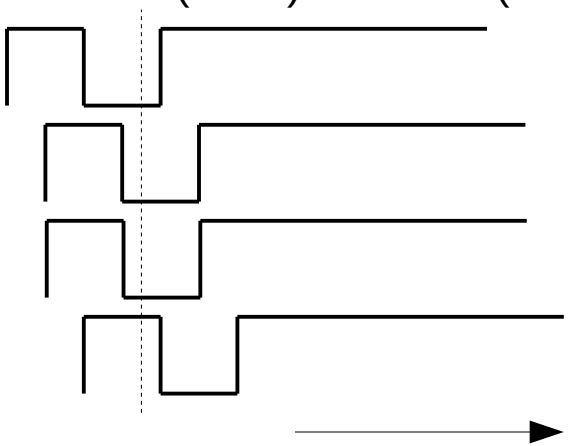
ADC values
of zero suppressed data taking
dominated by digital errors

- Programmable delay in DHP for every transmission line
- All delay registers 4 bit
  → 16 settings
- One replica LVDS driver providing reference voltage

Optimization of DCD ↔ DHP communication

- **Delay lines**
  - Known problem in DHPT1.0: asymmetric delays → duty cycle distortion
    - Worse distortion for higher delays

    → **minimize delays for data lines (local delays)**
  - Global (clock) and local (data) delays work “in the same direction”:



DCD output signal with undelayed clock

global delay (shifts clock)

DHP input signal after global delay

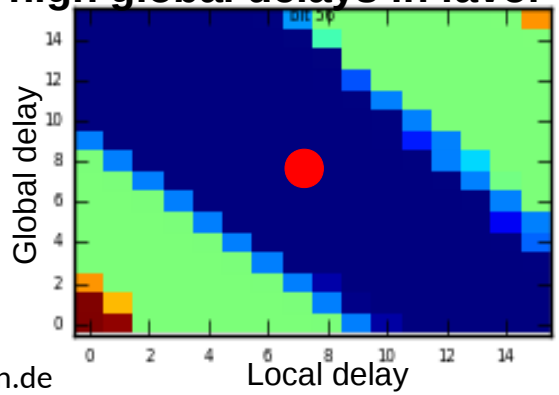
internal DHP input signal after additional local delay

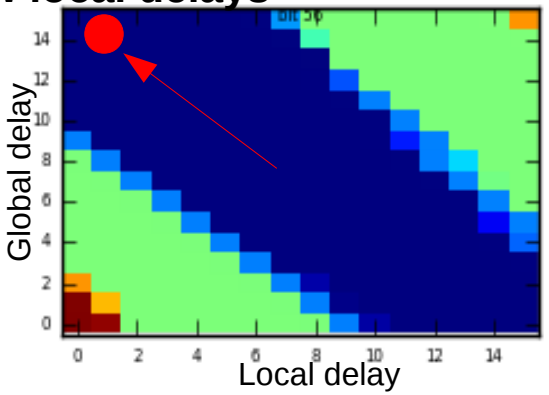
local delay (shifts data)

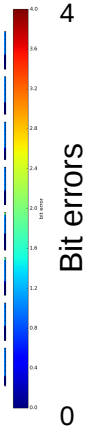
  - → **go to high global delays in favor of low local delays**

Working point

Solution of automatic script: ->



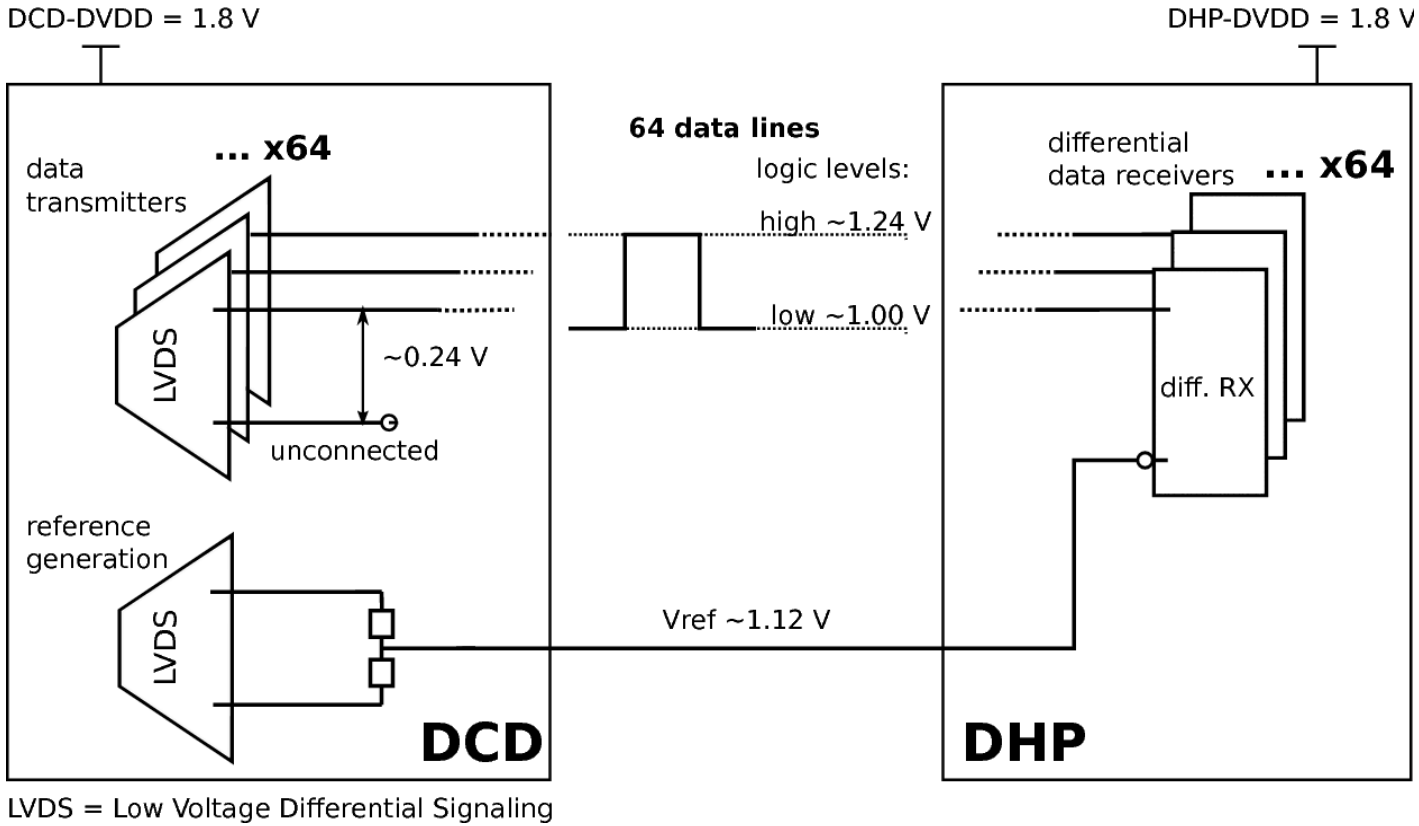




← Better solution for DHPT1.0

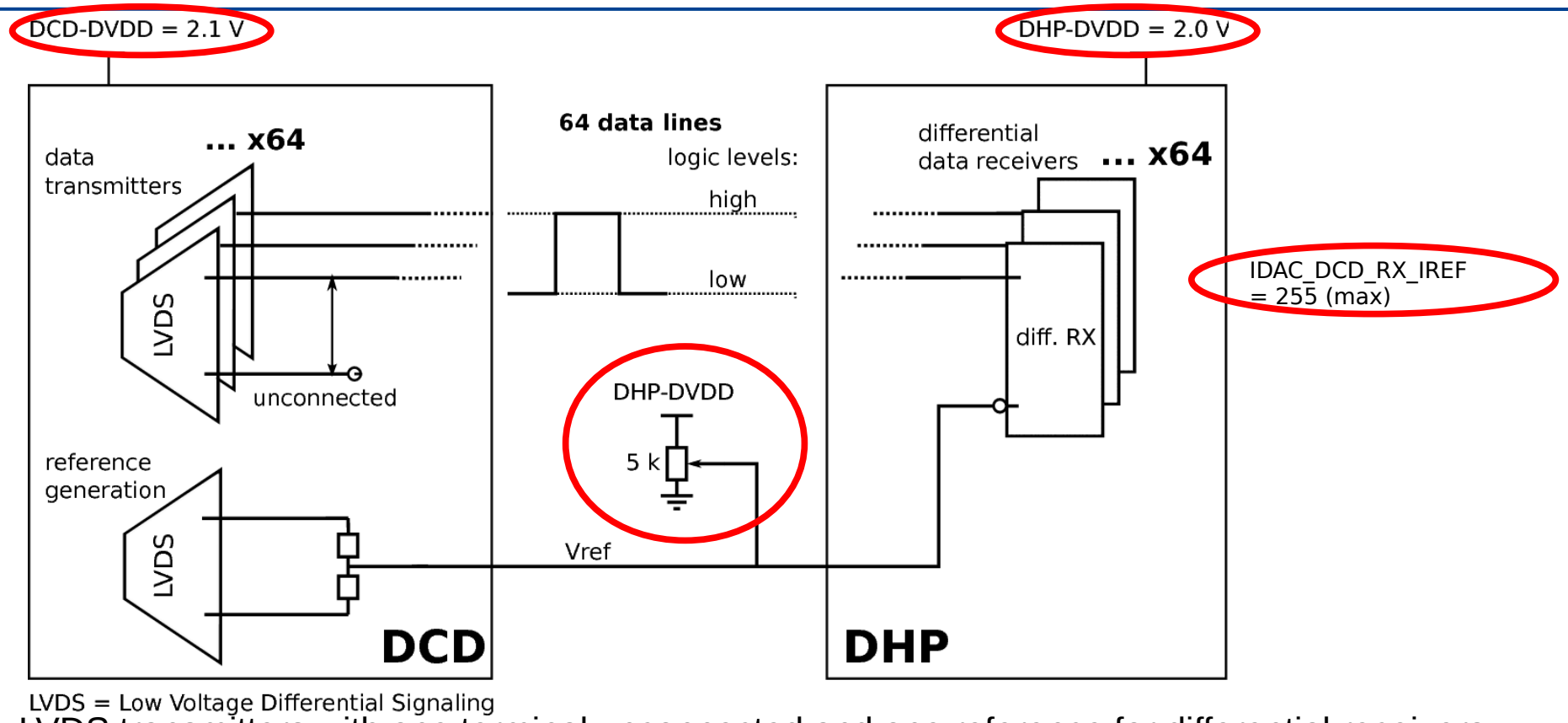
For more detail on delay tests see Hybrid 5 talk of Trieste workshop

Optimization of DCD ↔ DHP communication



- LVDS transmitters with one terminal unconnected and one reference for differential receivers
- Possible problems:
  - High/low levels not reached due to long rise/fall times → **use higher supply voltages (DVDD)**
    → **use slower clock** with DHPT1.0
  - Mismatch of Vref w.r.t. logic levels of data lines → **modify Vref** (only Hybrid 5)

Optimization of DCD ↔ DHP communication



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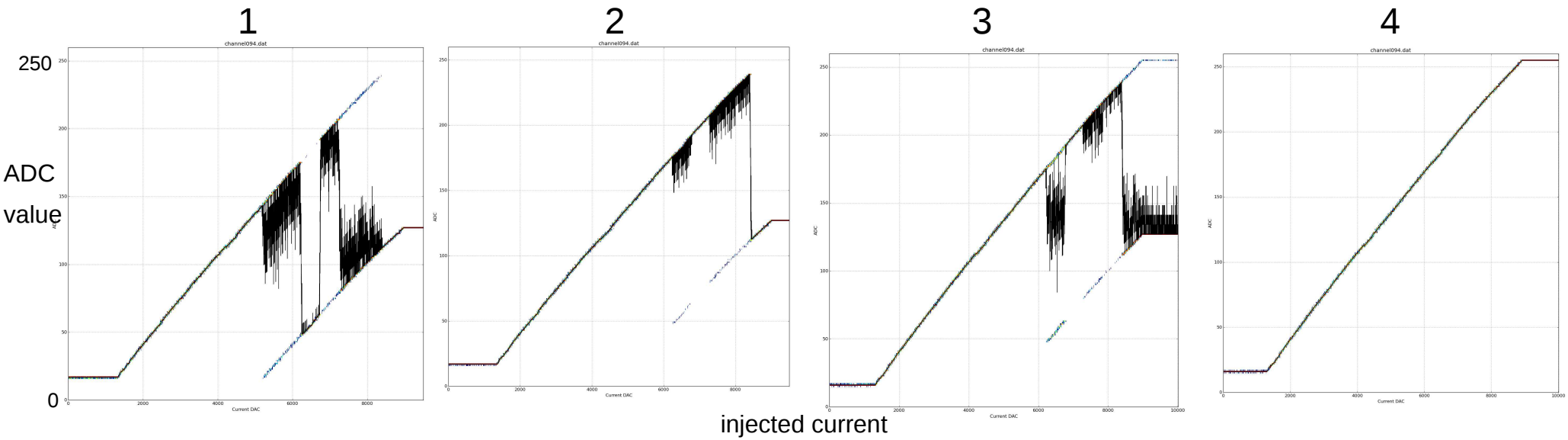
Optimization of DCD ↔ DHP communication

Example of procedure:

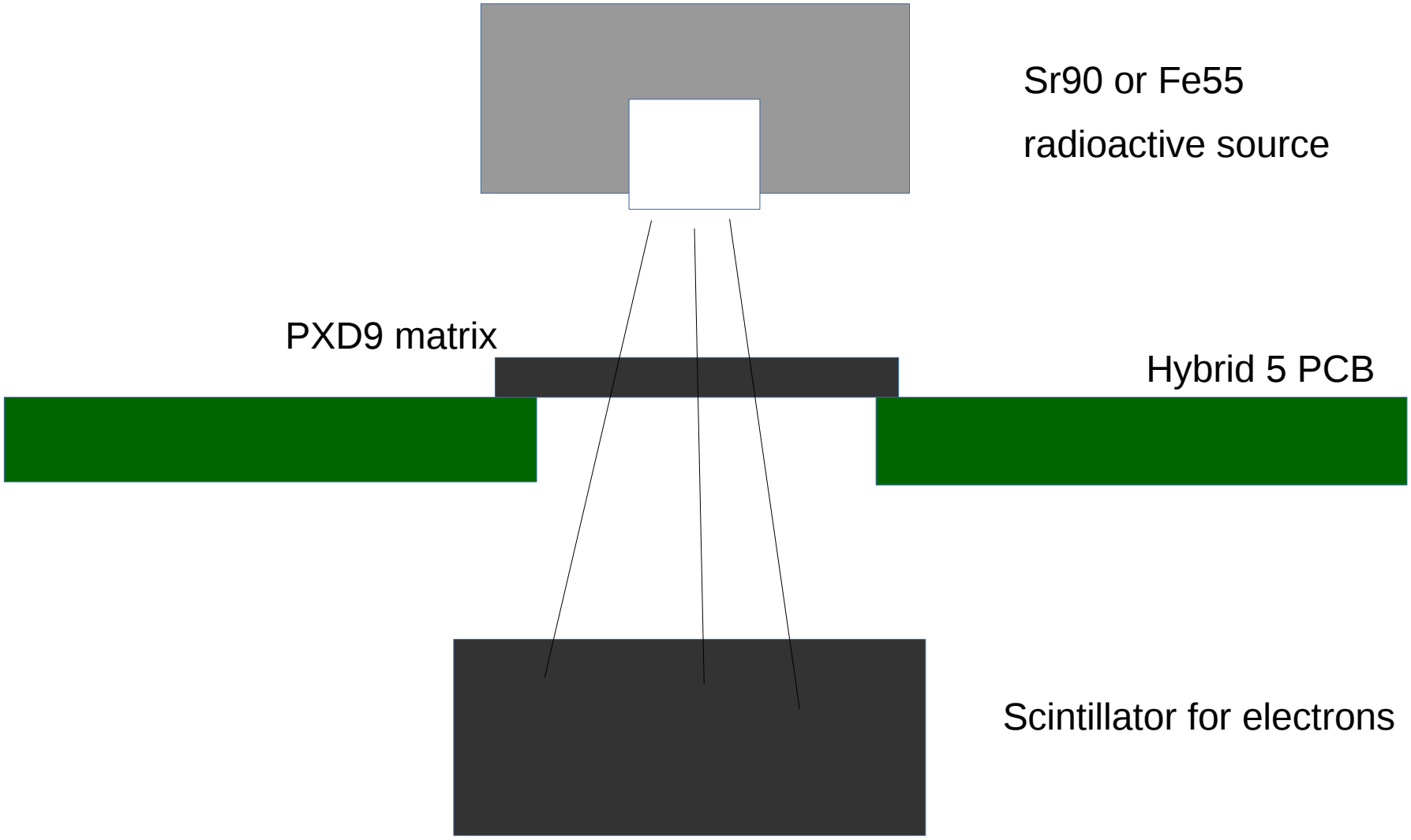
- **1**: Initial curve after standard delay optimization
- **2**: Increase digital supply voltages and RX bias current (DCD-DVDD = 2.1 V)
- **3**: Decrease local delay and increase global delay (GD = 14)
- **4**: Increase Vref by 27 mV



Hybrid 5.0.07 DCD channel 94 with MSB toggling (bit 8 = 127 ADU) @ 62 MHz

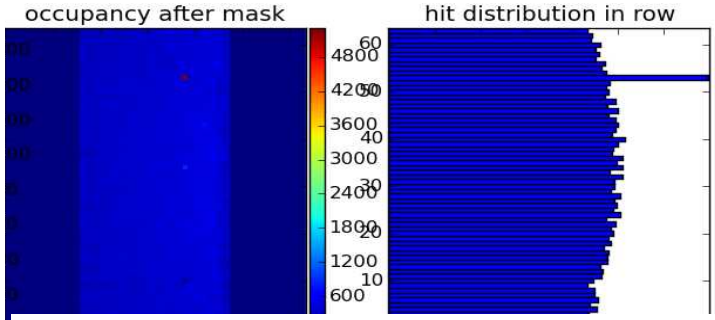
Radioactive Source Tests

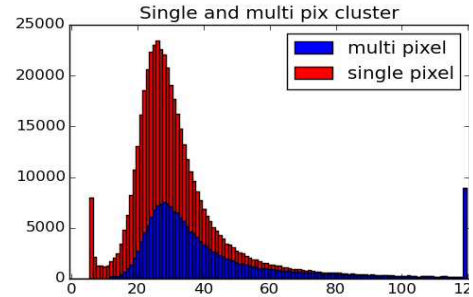
- Setup for source measurements:



HV: -80 V

Drift: -7 V





CCG: -1 V

Clear-low: 3 V

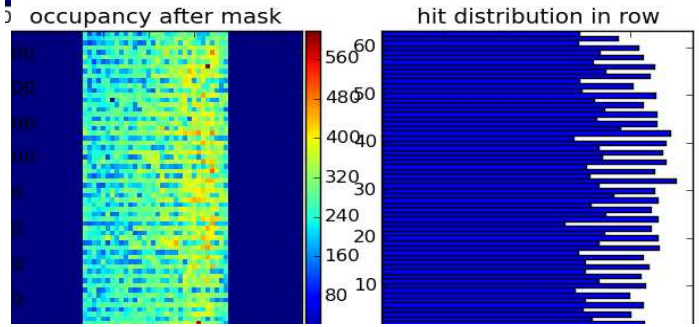
Clear-high: 20 V

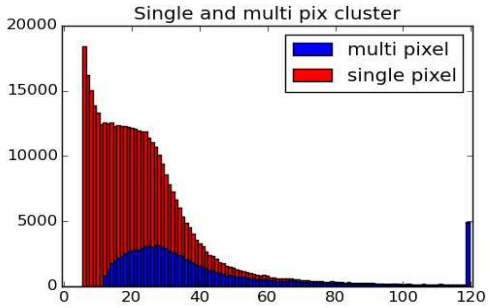
Gate-on: -2.5 V

Gate-off: 3 V

HV: -76 V

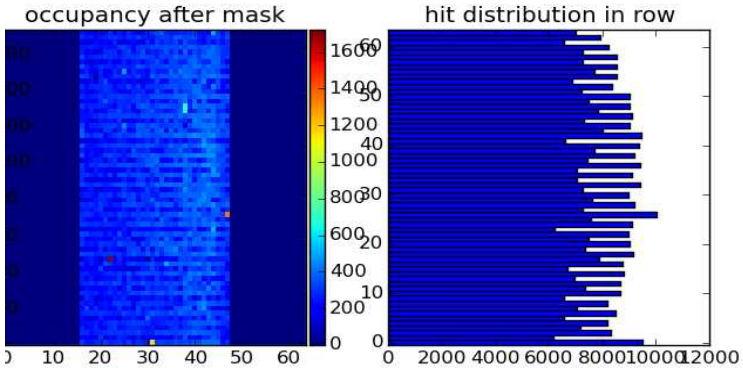
Drift: -7 V

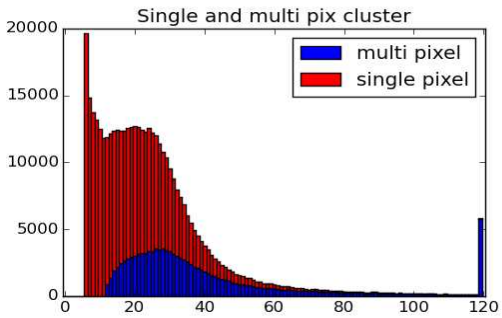




HV: -70 V

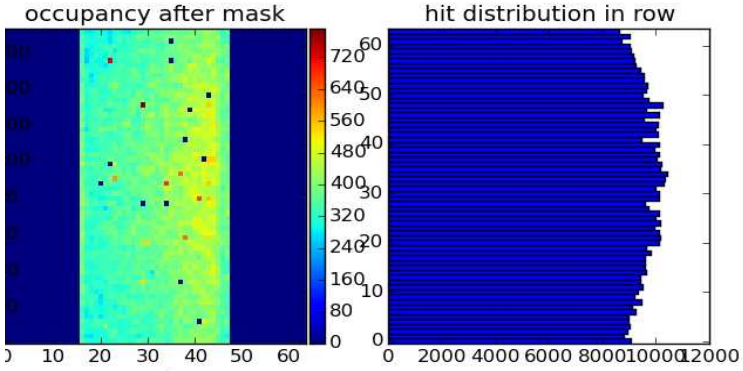
Drift: -7 V

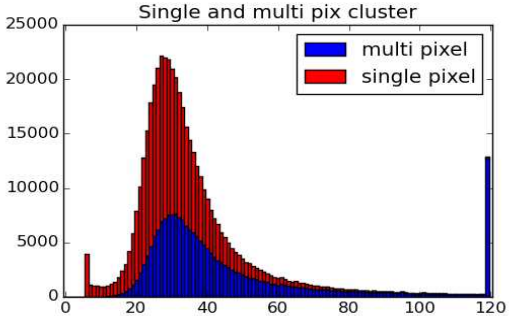




HV: -66 V

Drift: -7 V





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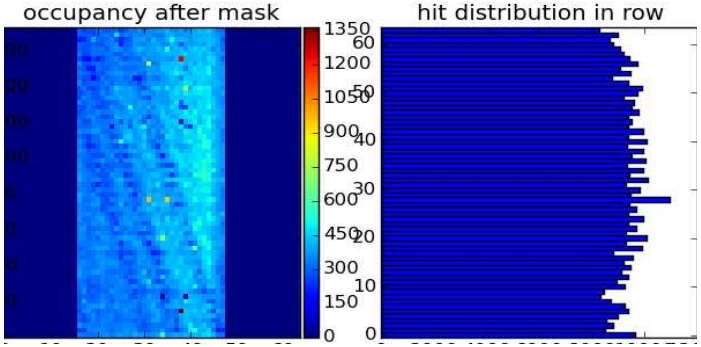

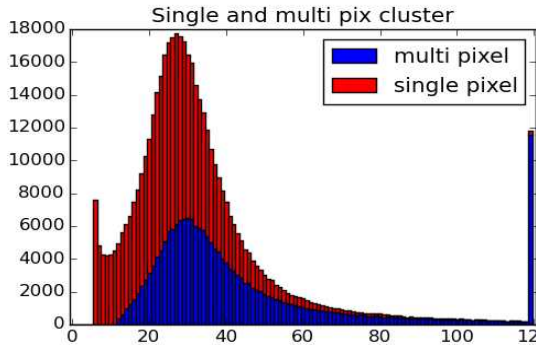

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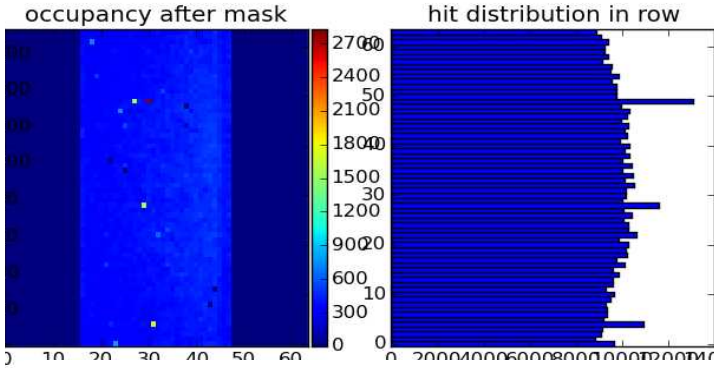

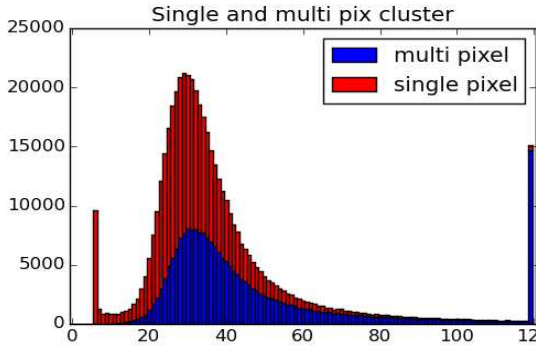

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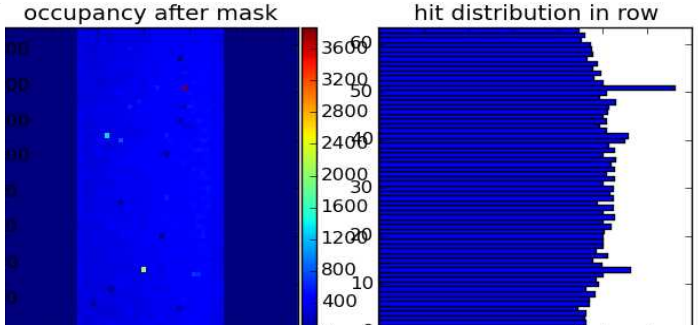

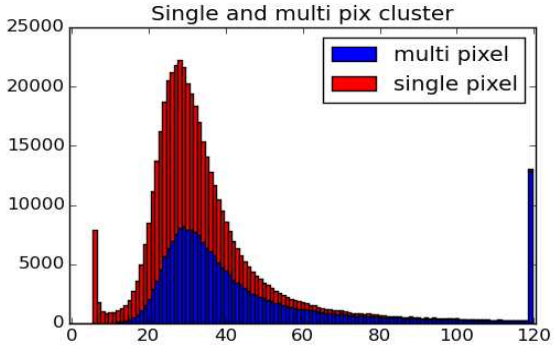

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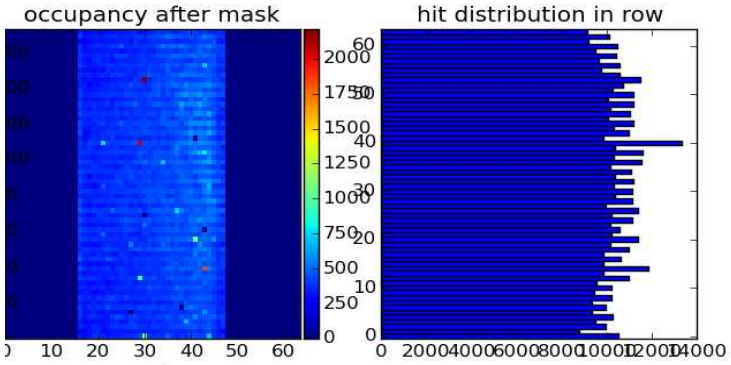
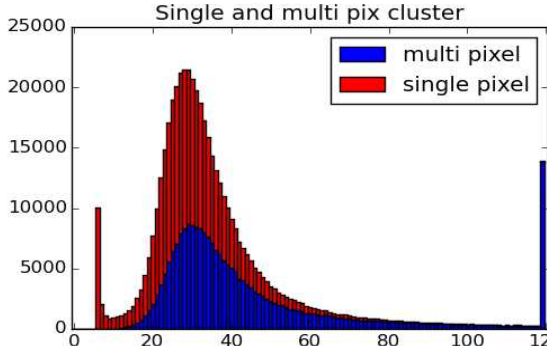
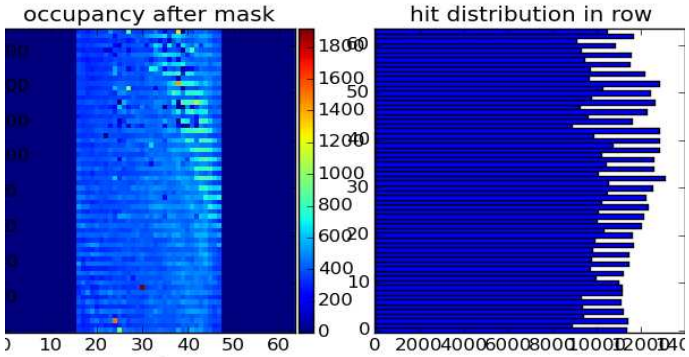
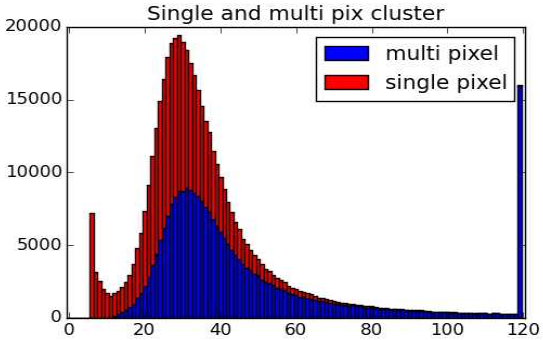




HV: -80 V

Drift: -3 V





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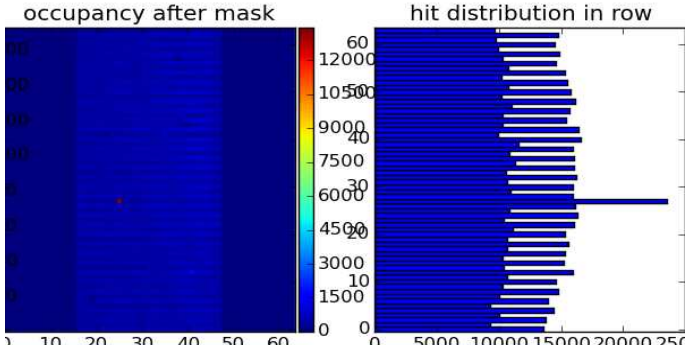

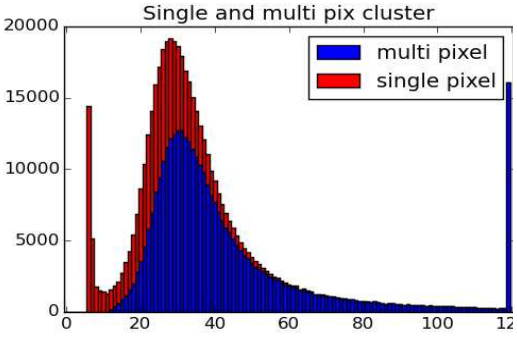

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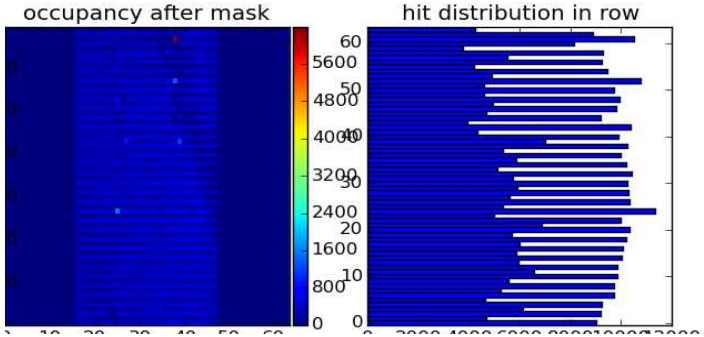

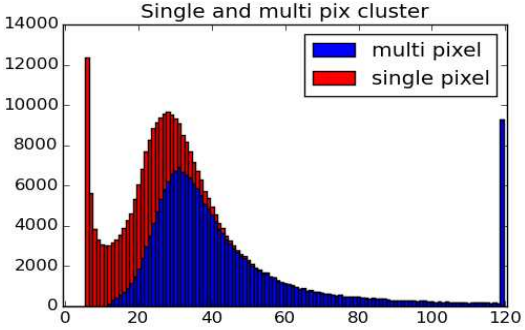

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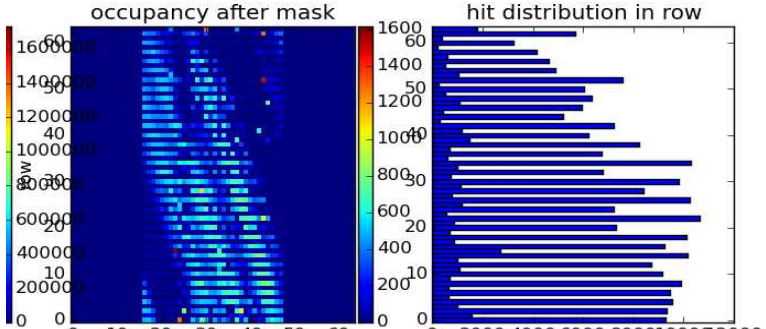
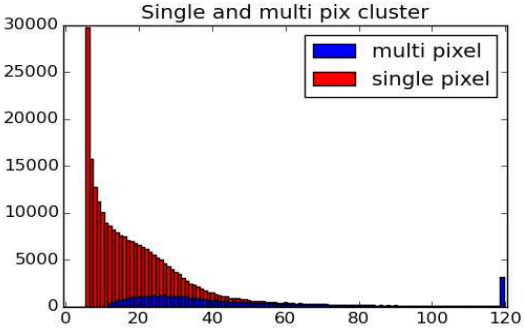
Drift: -3 V



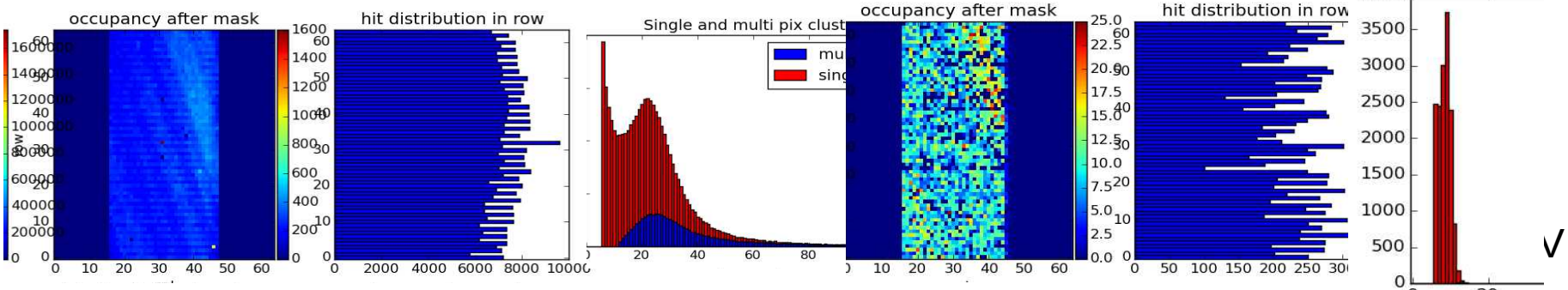


Sr90

Fe55

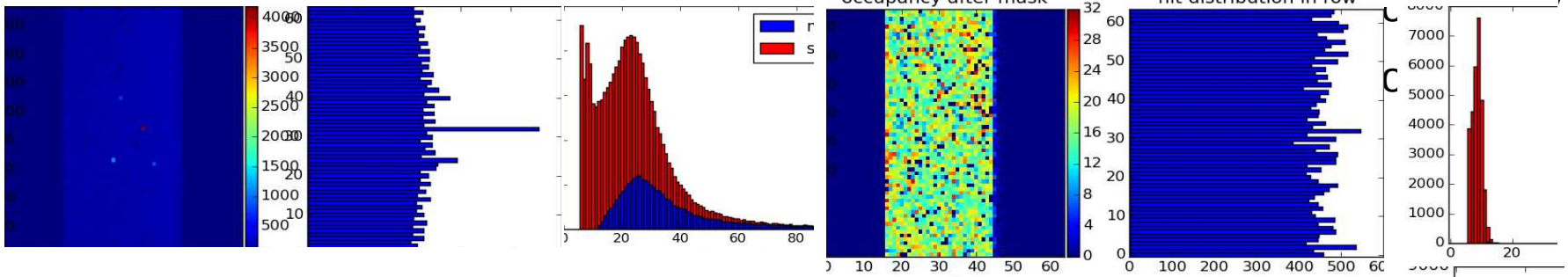
HV: -80 V

Drift: -5 V



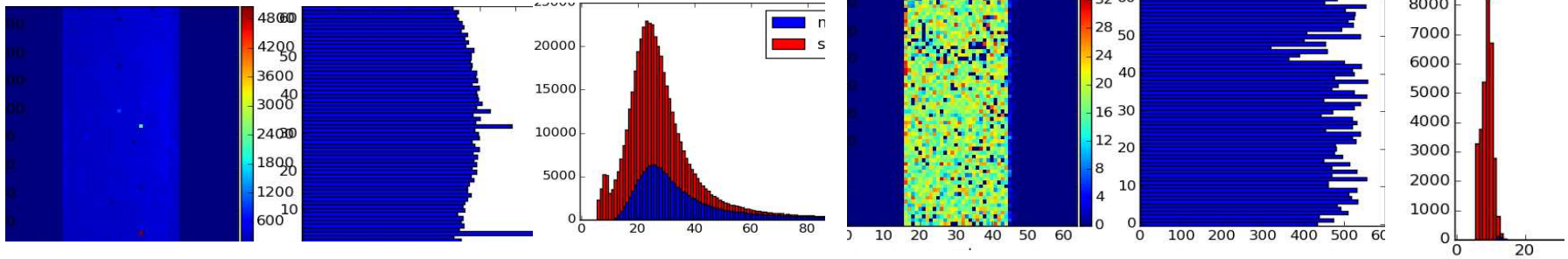
HV: -75 V

Drift: -5 V



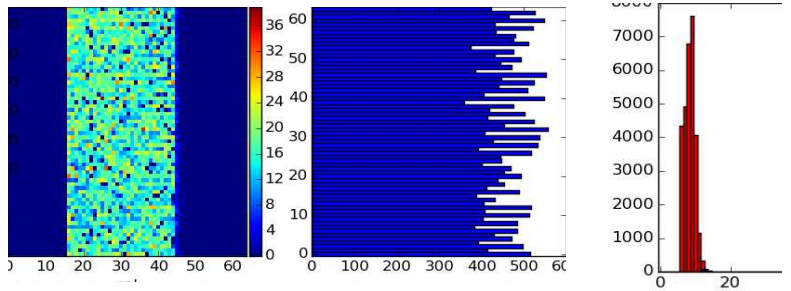
HV: -70 V

Drift: -5 V



HV: -65 V

Drift: -5 V

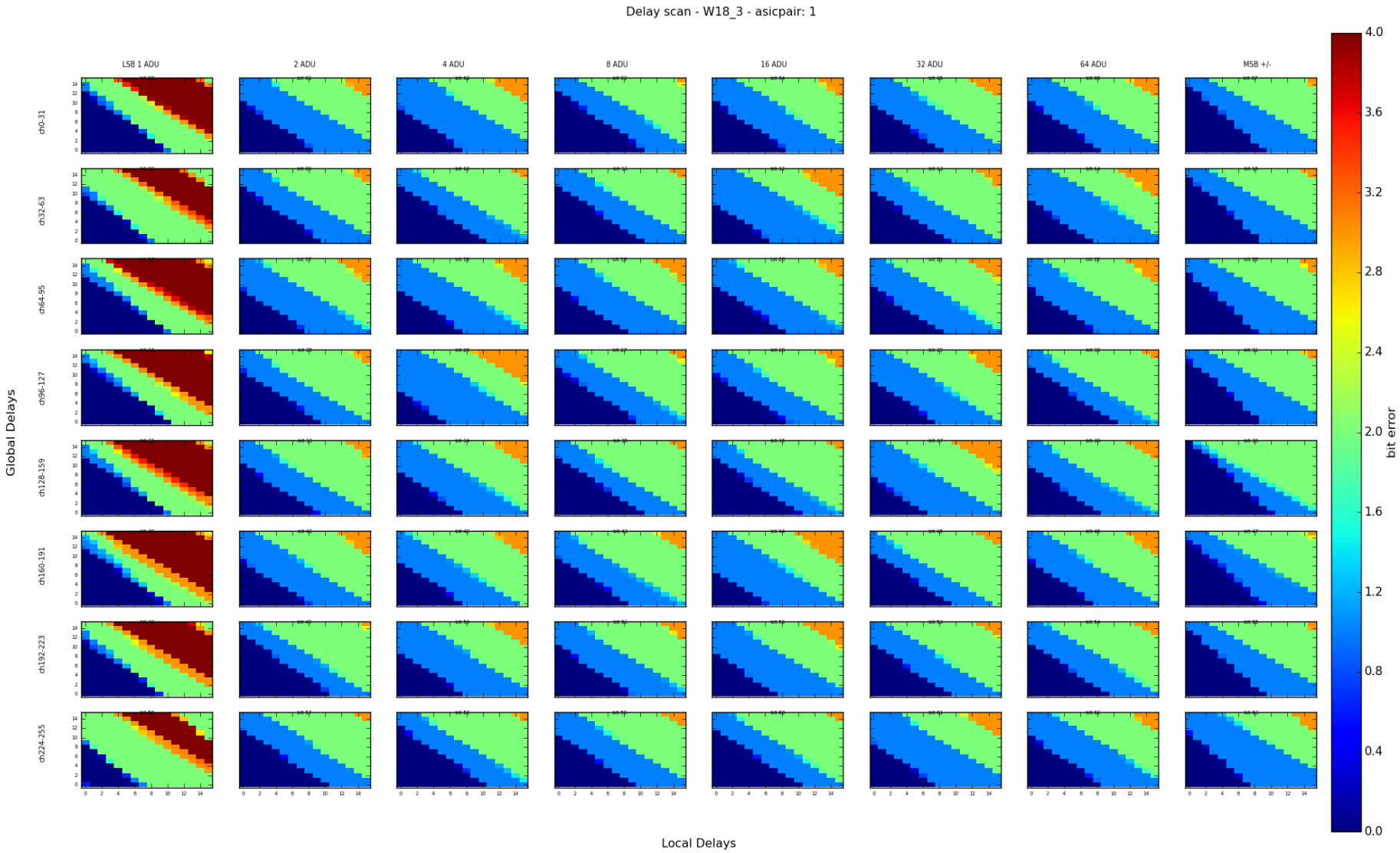


New DHPT1.1 on Hybrid 5

- Two Hybrid 5 assemblies with new DHPT1.1 and DCDpp have been assembled (Hybrid 5.0.08, 5.0.09)

- High speed link to DHH is improved (see Leo's talks)
- DCD ↔ DHP communication should be improved due to lower capacitances

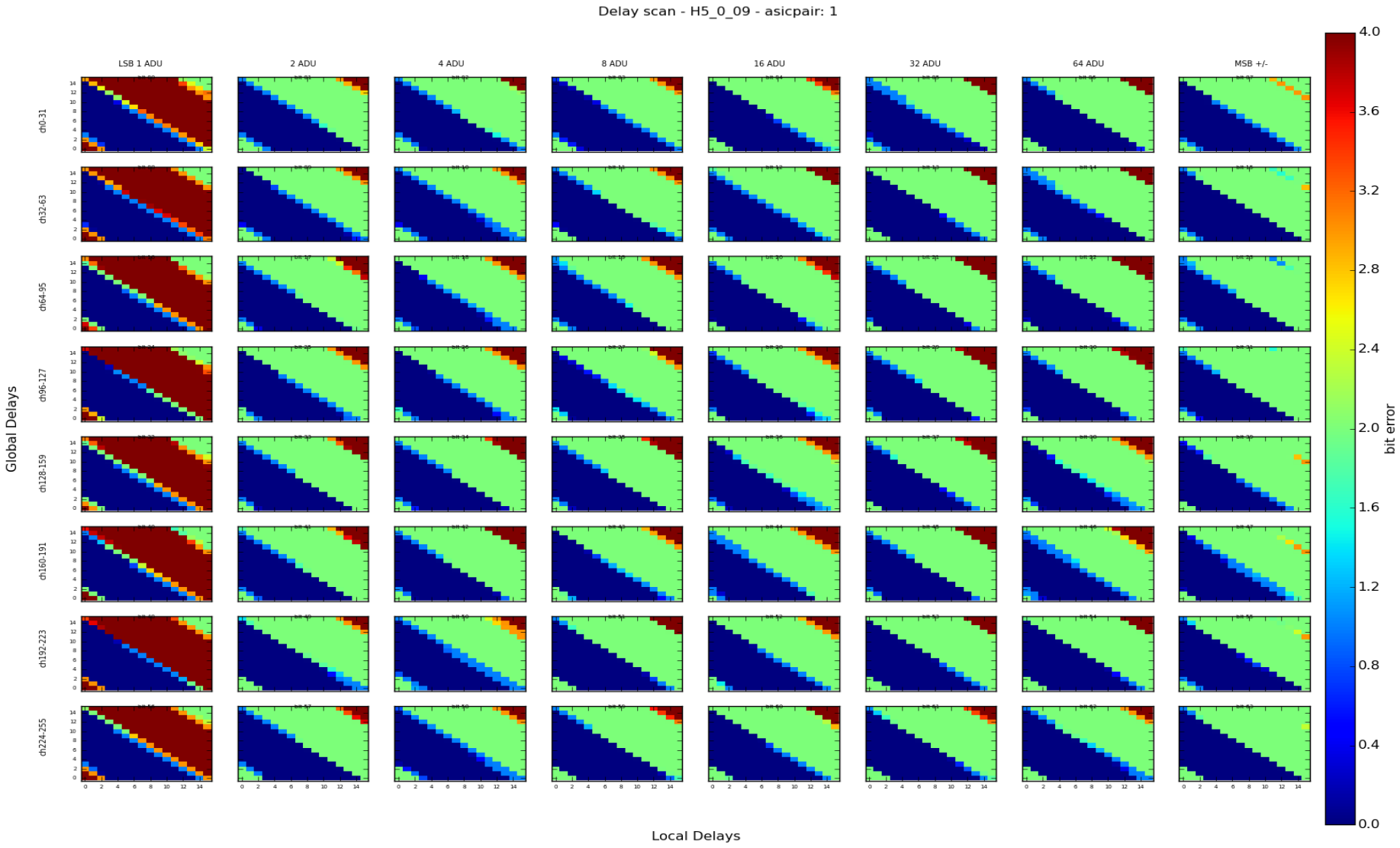
Test Pattern Hybrid 5.0.07 with DHPT1.0 at 76.2 MHz



dcd-dvdd = 1900 mV, dhp-core = 1620 mV

asymmetric...

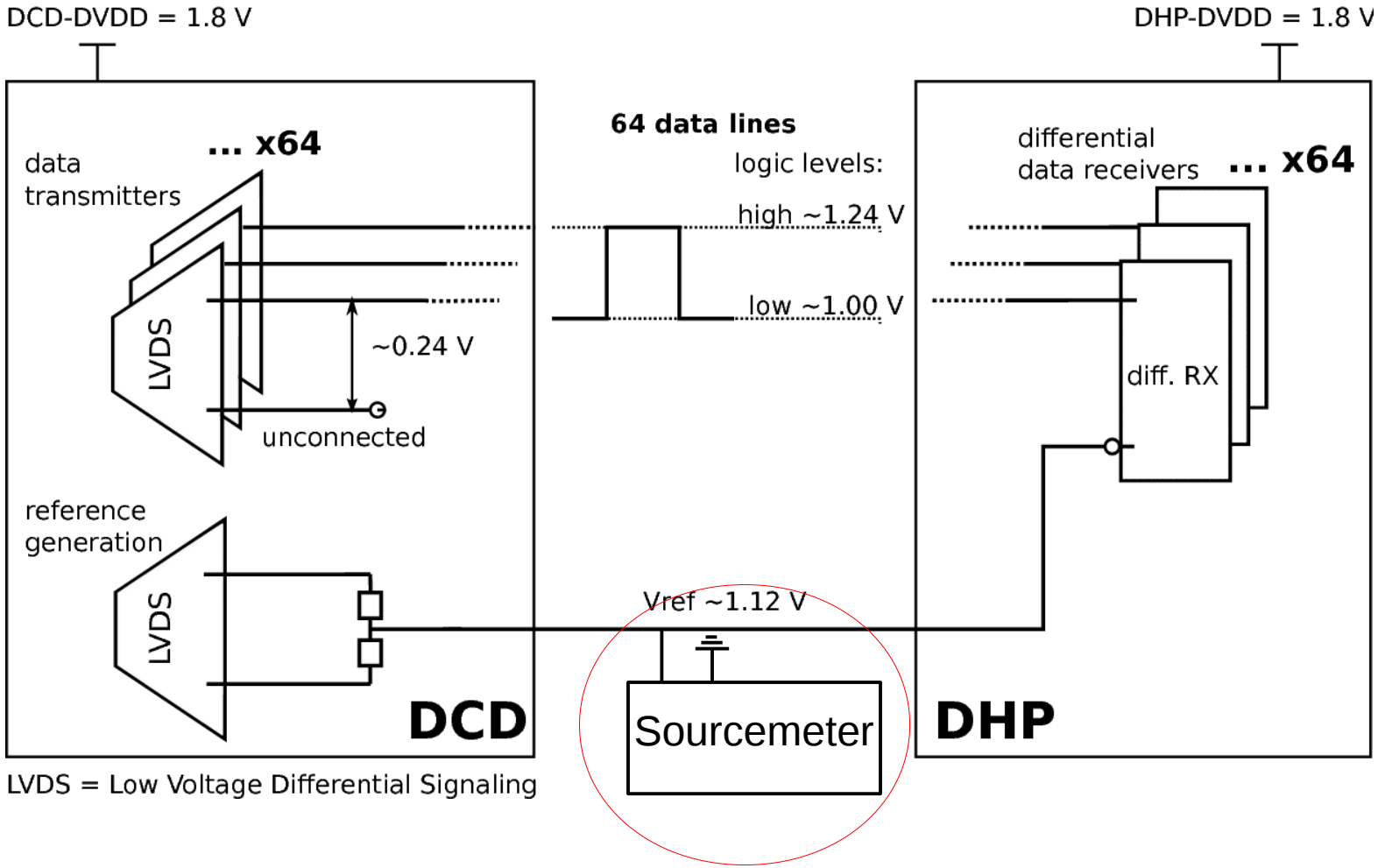
Test Pattern Hybrid 5.0.09 with DHPT1.1 at 76.2 MHz



dcd-dvdd = 1900 mV, dhp-core = 1300 mV

SYMMETRIC!

Comparison of Test Pattern with DHPT1.0 and 1.1 with Vref variation

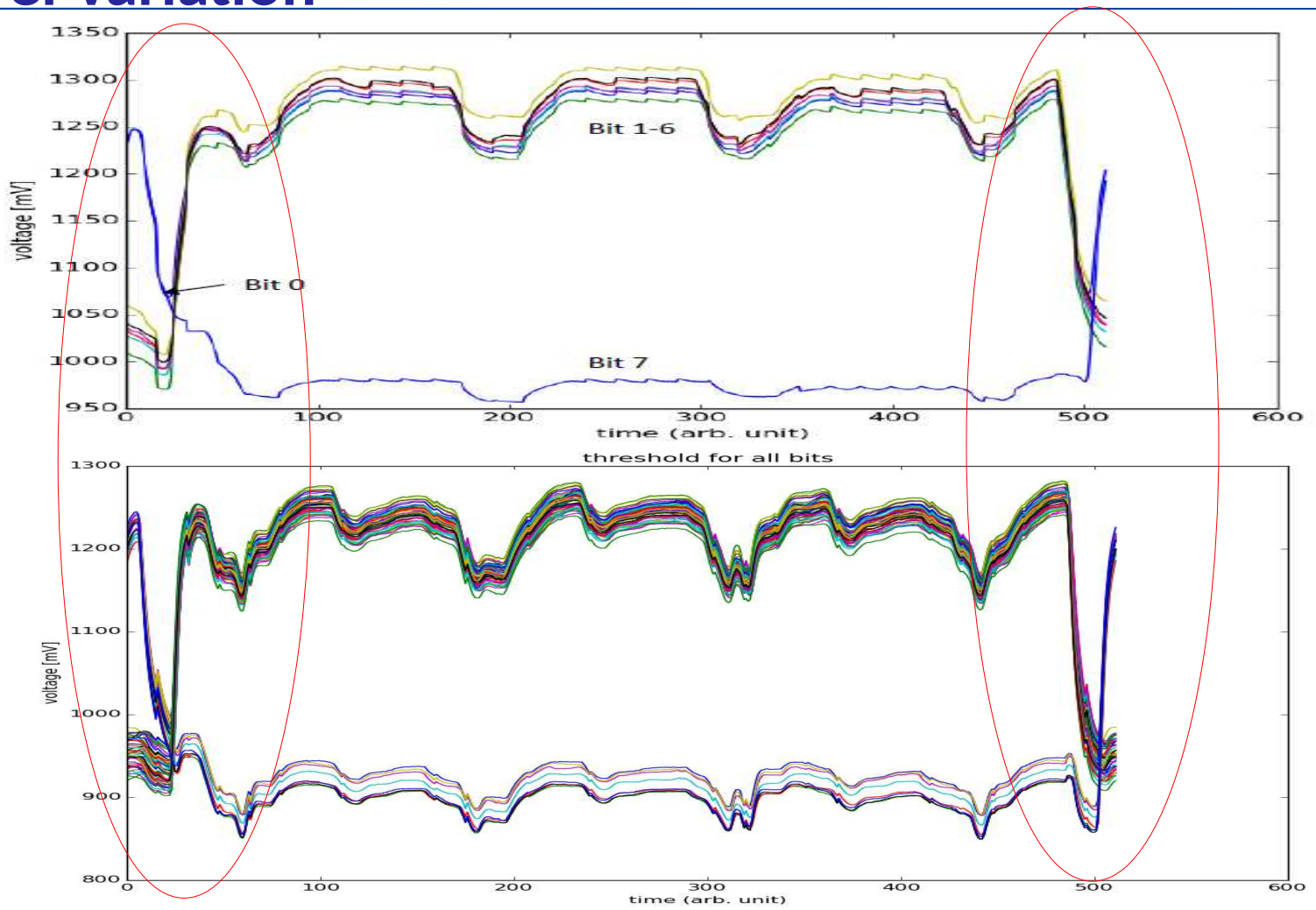


- Overwrite Vref with a sourcemeter and measure for every point in time of the test pattern for which values the signal flips from 0 to 1 or vice versa
- Emulates sampling oscilloscope when integrating all measurements

Comparison of Test Pattern with DHPT1.0 and 1.1 with Vref variation

DHPT 1.0

DHPT 1.1



- Edges rise and fall more quickly

Conclusion

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- Hybrid 5 with DHPT and DCD is a valuable device for examining the communication between the ASICs

- DHPT1.1 improves the communication already with the unchanged DCDpp
  - Next step:
    - Irradiation campaign in February

- At low clockspeeds (62 MHz instead of 76 MHz) a small PXD9 matrix could successfully be optimized and read out for the first time on a test beam
  - Next steps:
    - Laser scan with sub pixel resolution for detailed charge collection analysis
    - Gated mode investigation with laser setup

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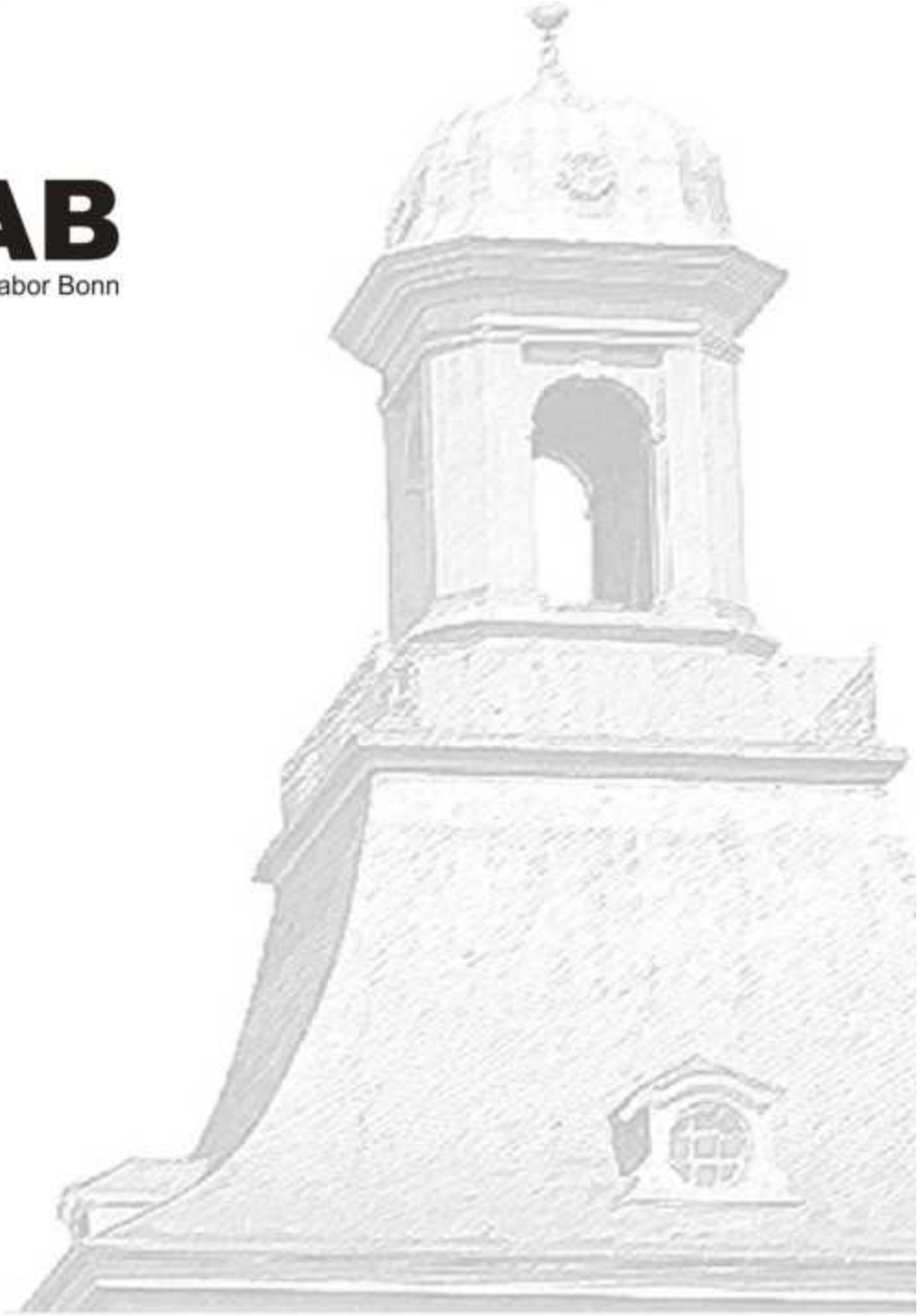

Thank you

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DHE half rate mode

- half rate DHP ↔ DHE communication

  → DHP doubles all output bits, DHE running at effectively half frequency