Summary of TB results for the small PXD9 matrix

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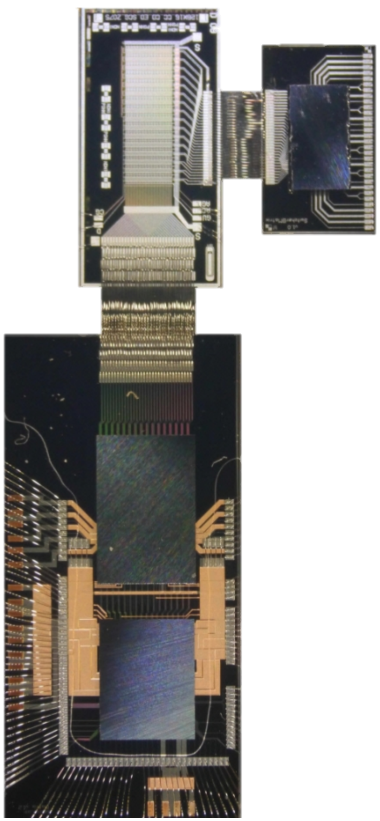
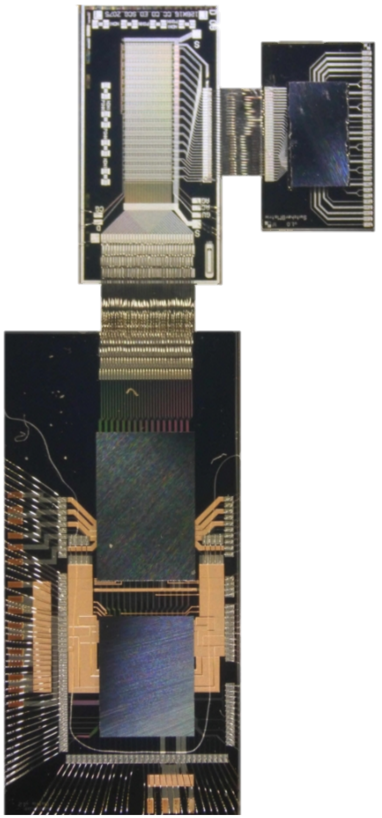
For the test beam crew

Small PXD9 @ DESY 2015



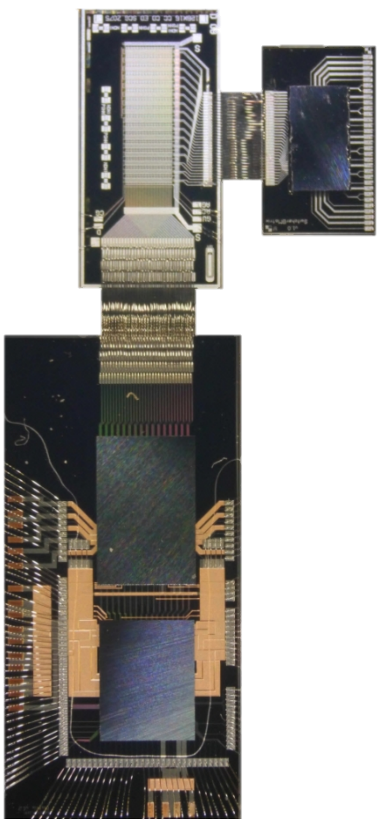
- First Belle II type matrix in a test beam integrated into EUDET telescope
- PXD9 small Belle II type matrix
  - Pixel pitch: 50x55 μm^2
  - Gate length: 5µm
  - 32x64 pixels readout @250MHz
- Readout chain
  - DCDBpipeline
  - DHPT1.0,
  - SwitcherB.1.8Gated
  - DHP->DHE->BonnDAQ PC-> EUDAQ PC
- Optimization and testing before going to DESY

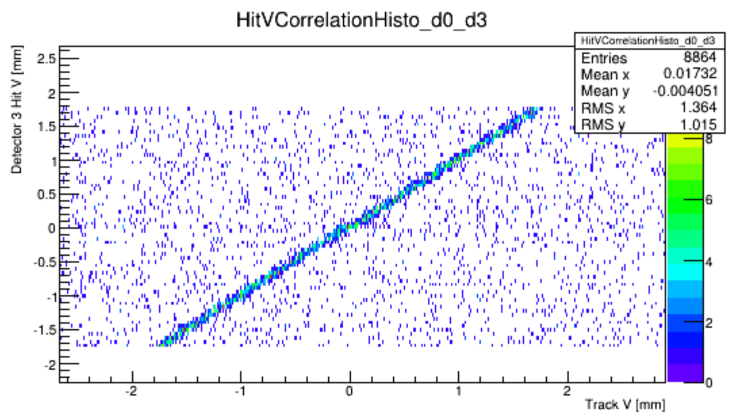
Many open questions to study

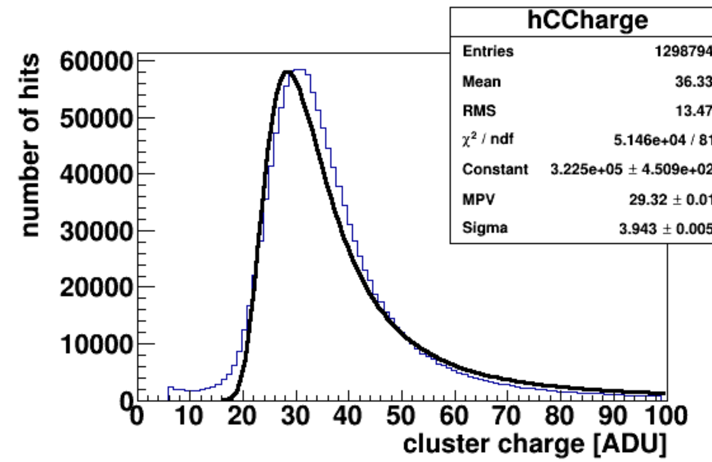


- What is the amplification or g_q for PXD9?
  - Gate oxide reduced x2 compared to PXD6
  - Different layout of pixel cell (Rainers talk)
- Can we rely on our PXD digitizer?
  - Spatial resolution?
  - Cluster shapes?
  - Hit efficiency?
  - For different track incidence angles
- Understanding of charge collection on in-pixel level?
- Number of hot/bad readout channels?
  - Impact of bit errors and long codes?
  - Smallest ZS threshold for good operation?

First TB results from Hybrid 5





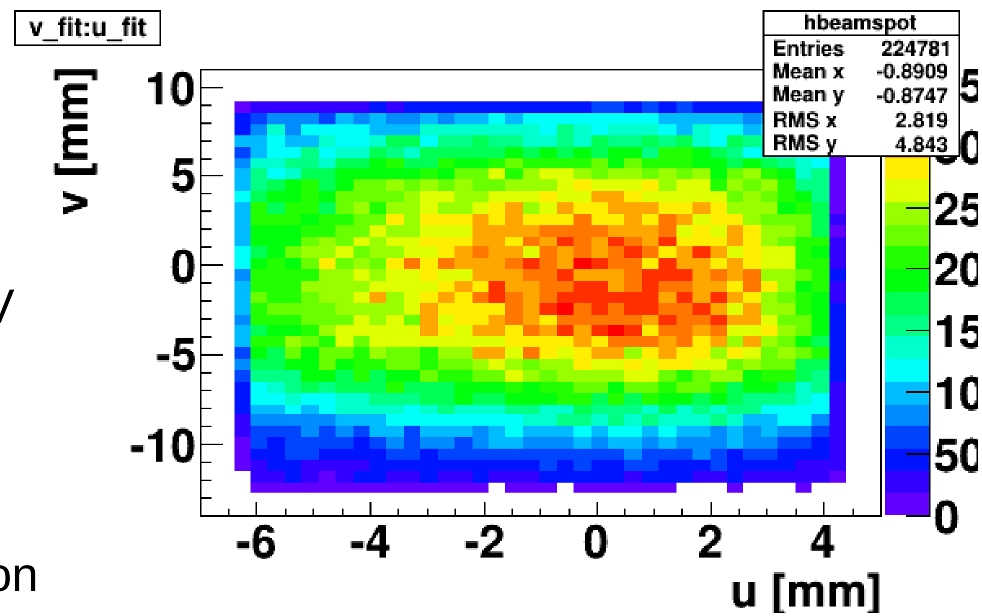


:- Correlations with
Eudet telescope

:- Beam spot with 4GeV
Electrons

:- Landau peak

→ Successful integration

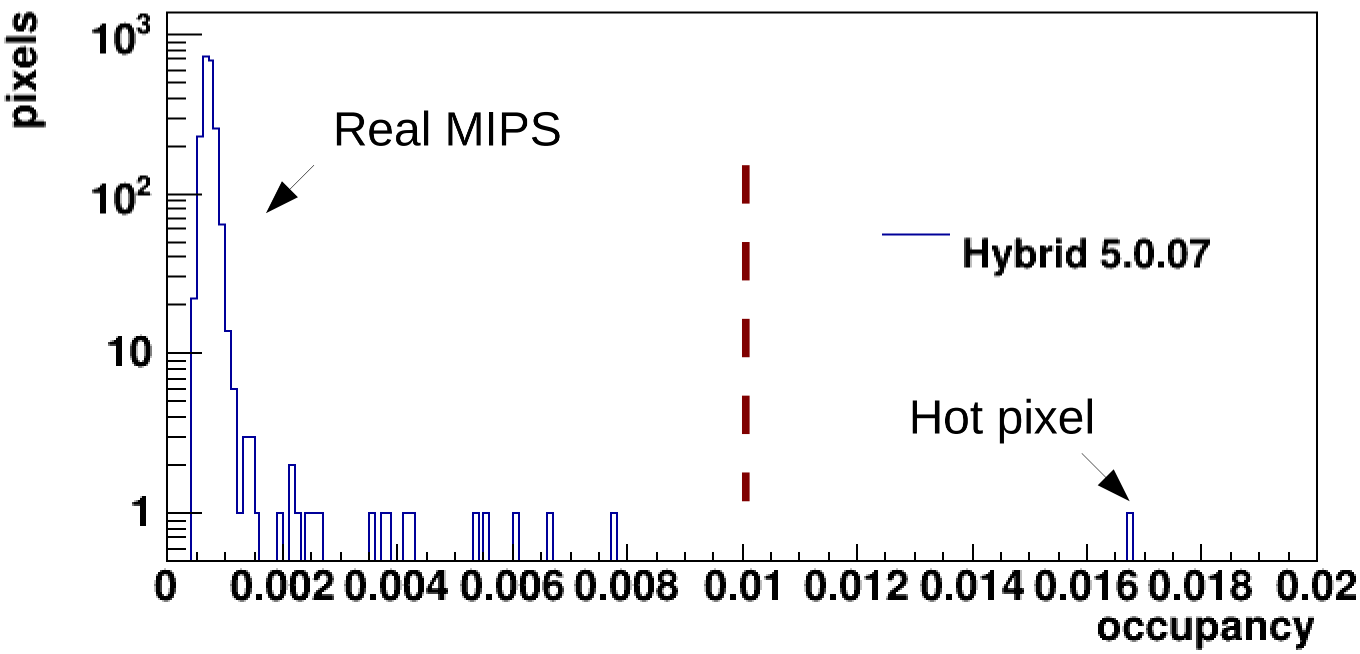


Hot pixels and zero suppression

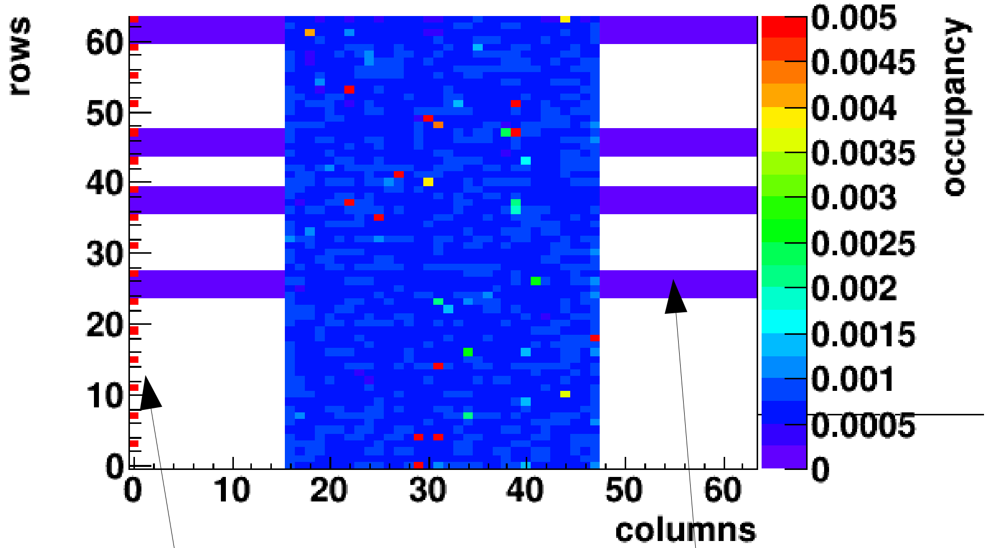
:- smallest DHP hit threshold was 4

:- pixel occupancy == #hits/#triggers

:- “hot pixel” == occupancy > 0.01



2D occupancy maps



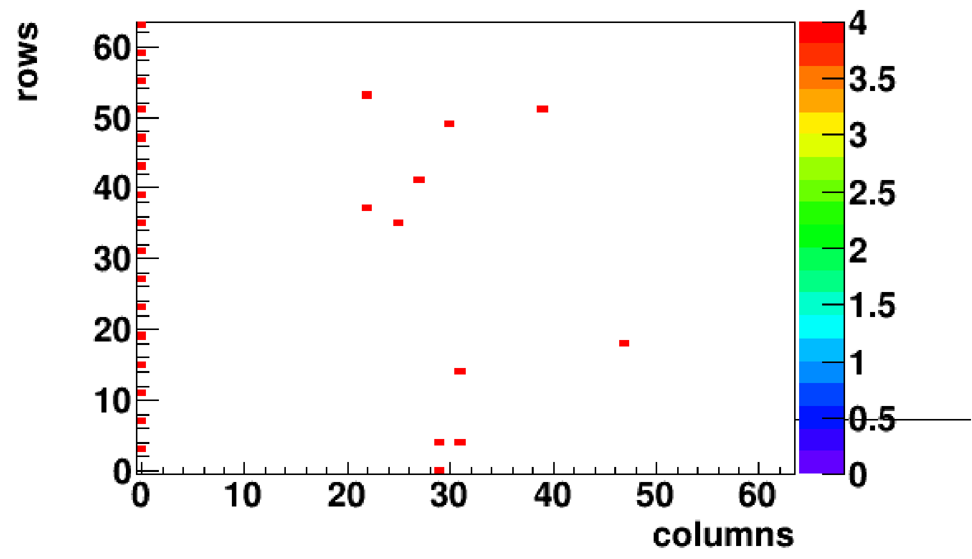
:- only pixel columns 16-47 readout

:- outer columns were masked in DHP

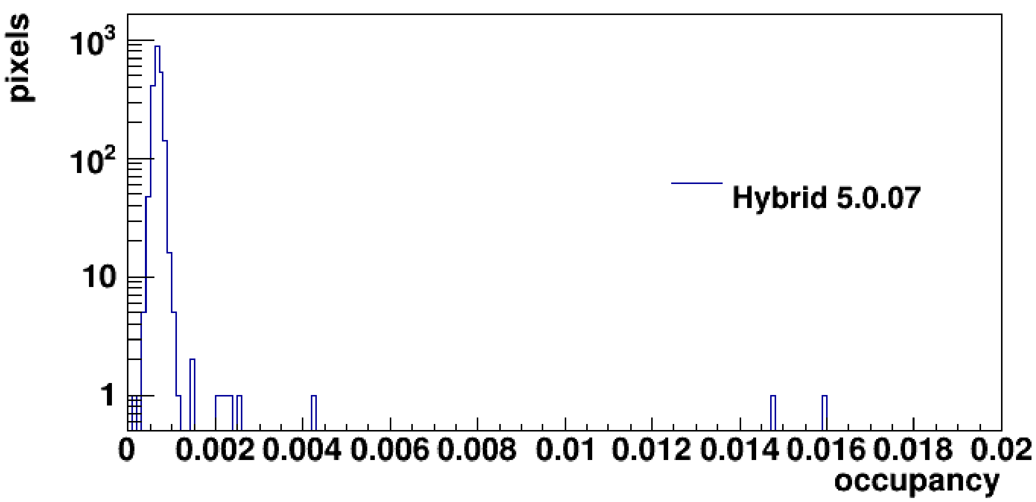
Despite masking some hits from column 0

Sometimes whole gate fires

Total of 11 channels masked



Raising DHP ZS threshold to 5...

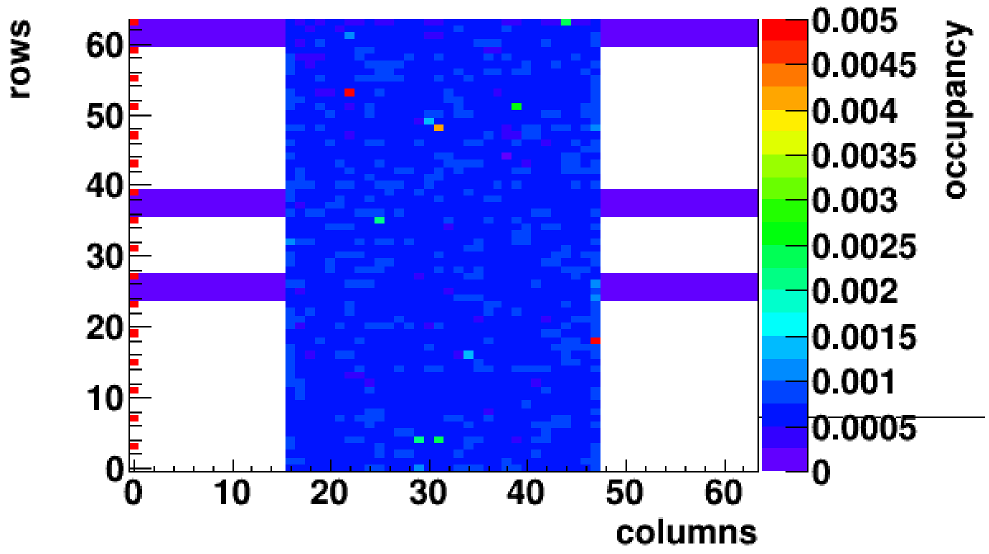


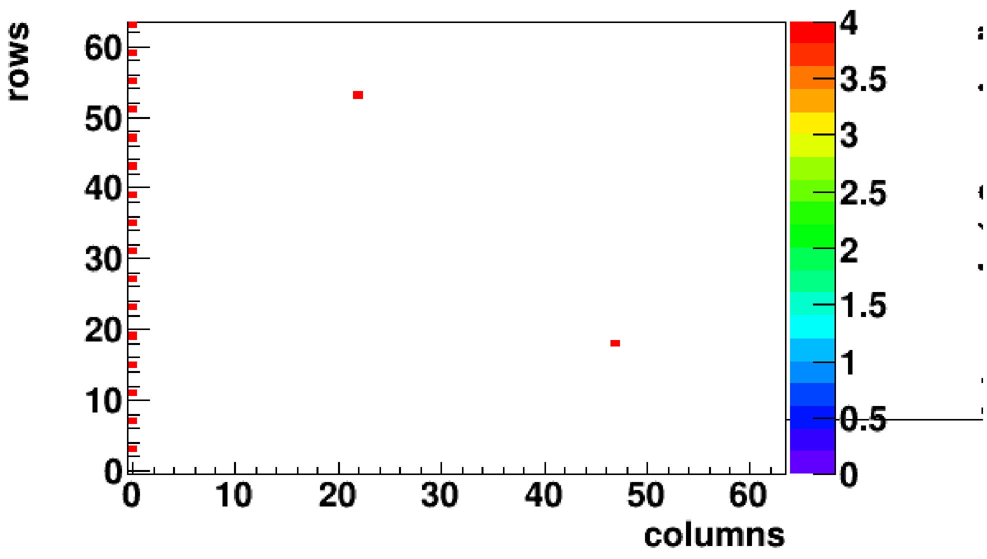
:- Threshold 5 chosen as default for offline study.

:- Only 2 readout channels masked as “hot” pixels

→ “hot” pixels turn normal at slightly higher threshold.

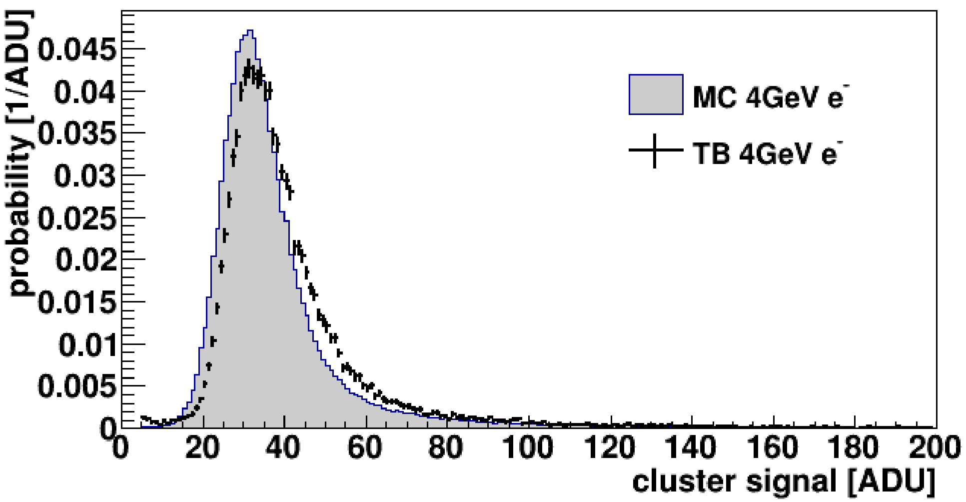
:- Strange artefacts still there...





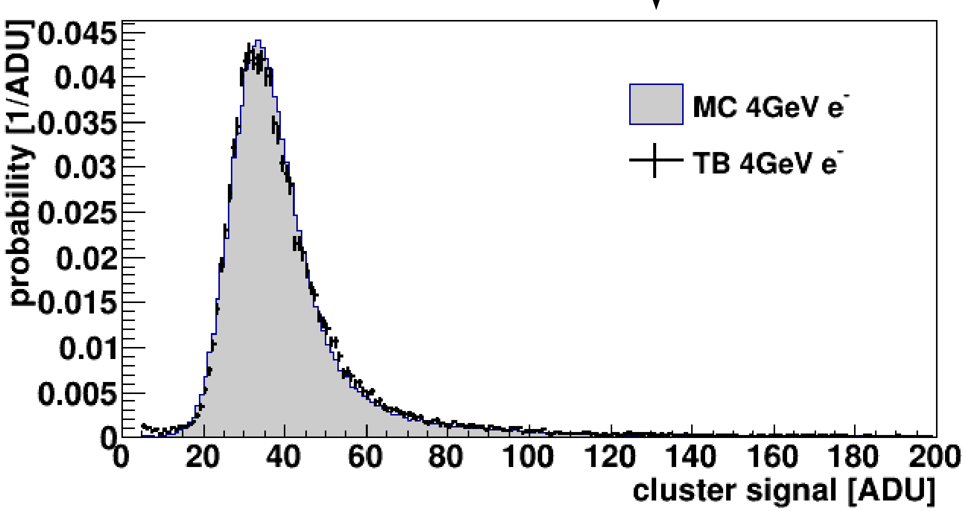
Calibration of the gq using MC

g_{tot} = 1/175 ADU/e



g_{tot} = 1/162 ADU/e

fitting



:- Geant4 gives energy loss in 75um Si.

:- DEPFET digitizer gives collected charge (e-) in internal gate.

:- Ideal 8bit ADC turning charge in digital output code

:- What is width of ADC code in number of electrons??

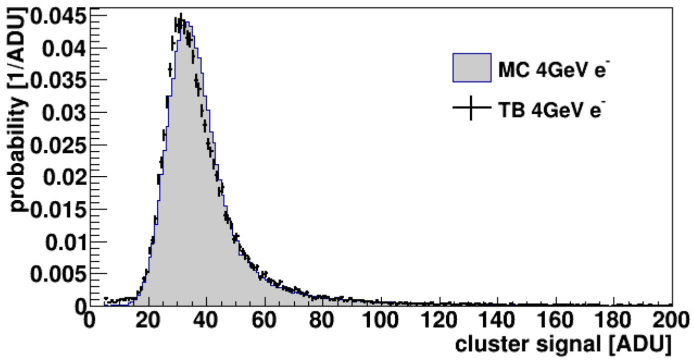
→ Fit against measured spectra!

→ Result: g_{tot} = 1/162 ADU/e

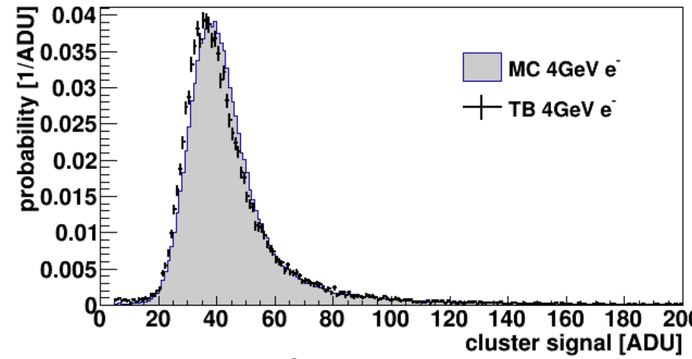
:- For test beam there is more data also from different angles.

Fitted spectra for different tilt angles

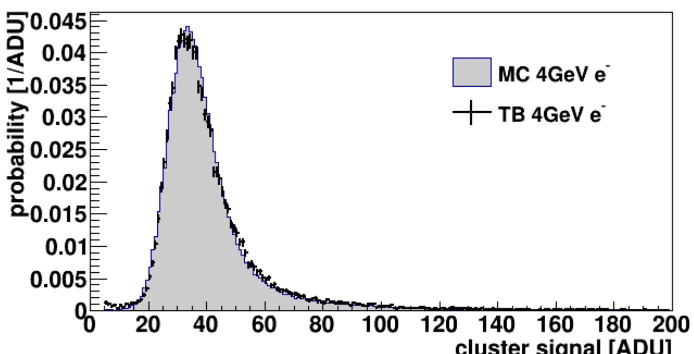
0 degree



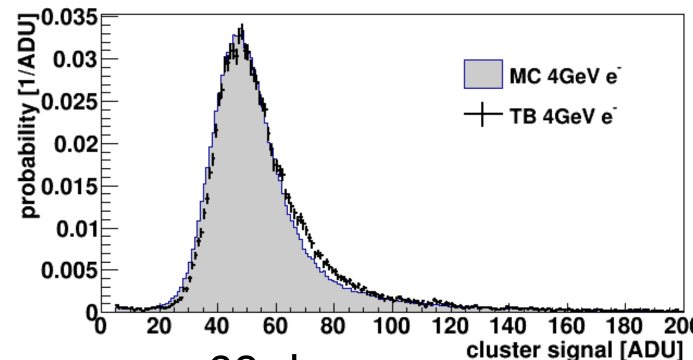
30 degree



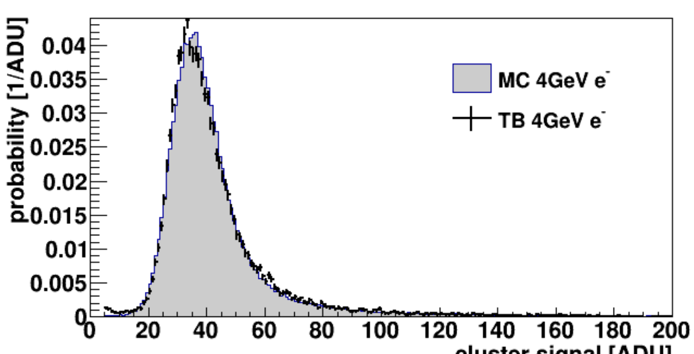
10 degree



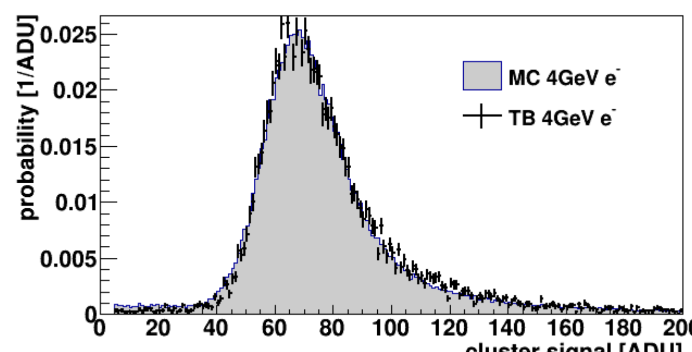
45 degree



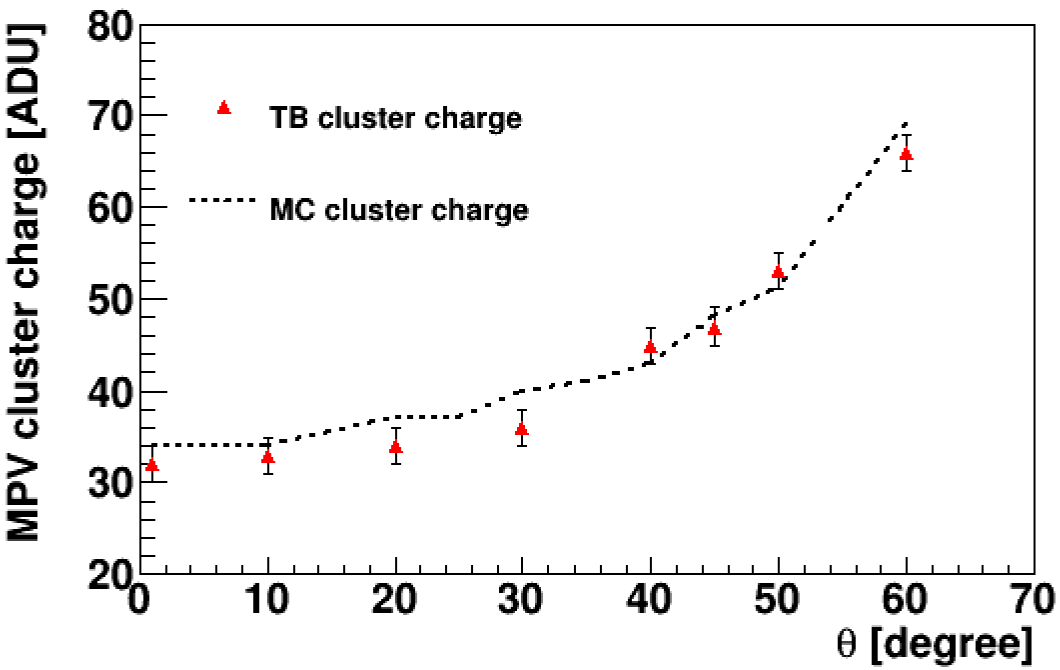
20 degree



60 degree



Calibration of the gq – part two



:- Consider g_q as total gain

$g_t = g_q \times g_{ADC}$

g_q takes charge to current

g_{ADC} takes current to codes

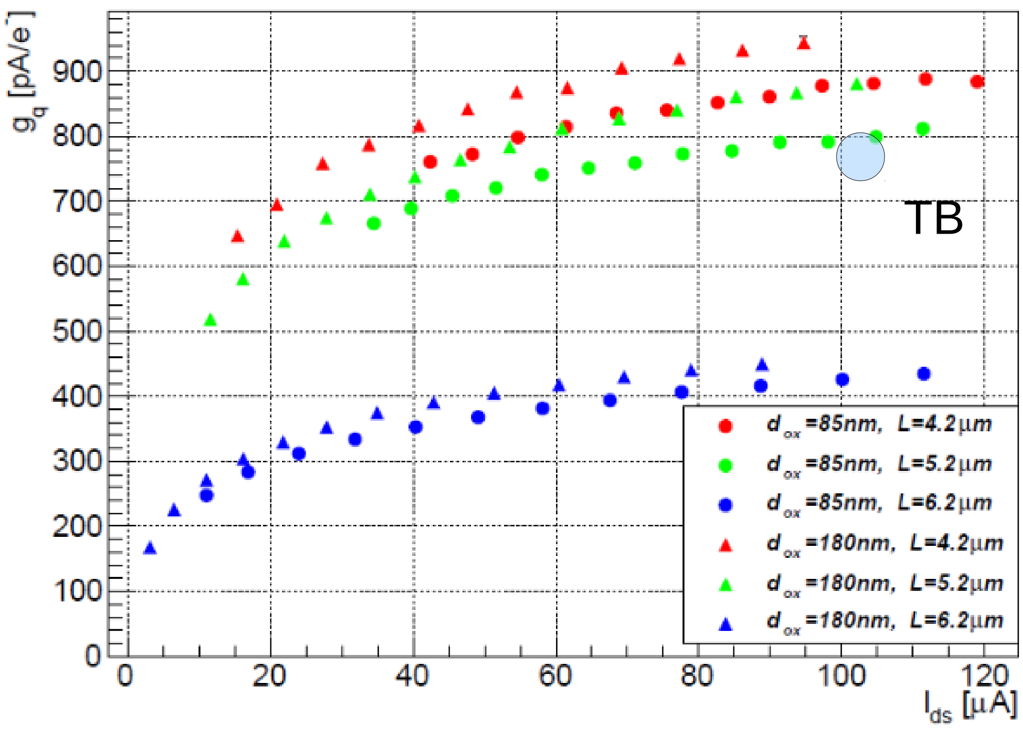
:- Take g_{ADC} from ADC curves (slope)

$g_{ADC} = 1/120$ ADU/nA

:- Final result:

$g_q = g_t / g_{ADC} = 740 \pm 50$ pA/e

Comparison with other results



[measurements presented by Stefan Rummel
In Prague meeting]

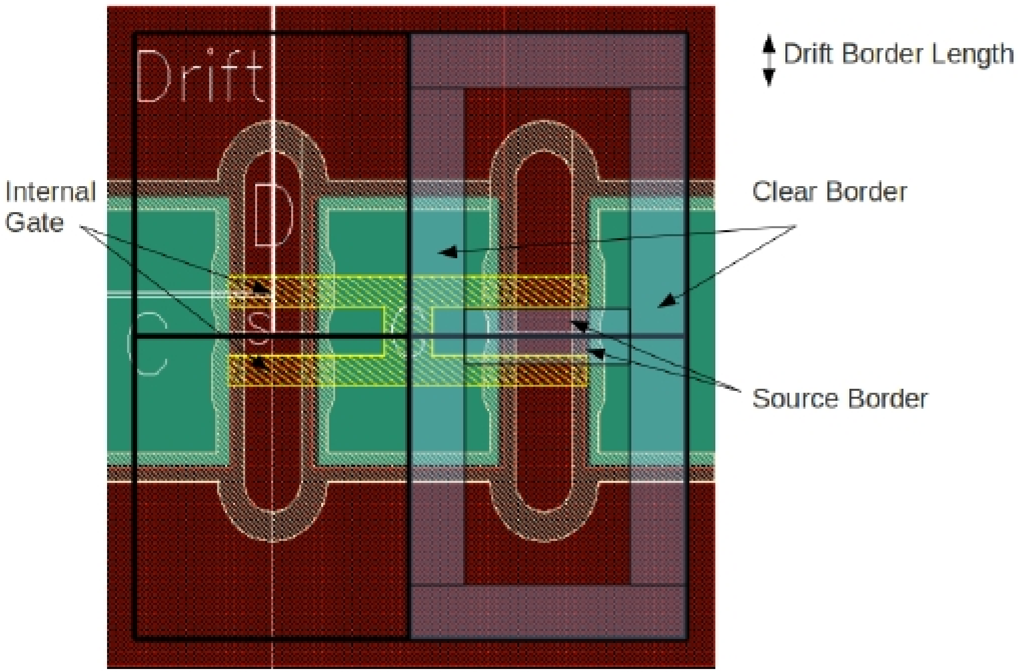
:- PXD9 design value ~500 pA/e

:- g_q of 740 pA/e is rather high

:- In test beam:

- gate on -2.5V
- gate length 5um
- oxide thickness 100nm
- I_ds ~100uA

Charge sharing model in digitizer (short reminder)



:- 2x2 unit pixel cell

:- Lateral charge transport in
In pixel edges dominated by diffusion.

:- Size of borders can be from
from Rainer's simulations

List of Digitizer Parameter Values

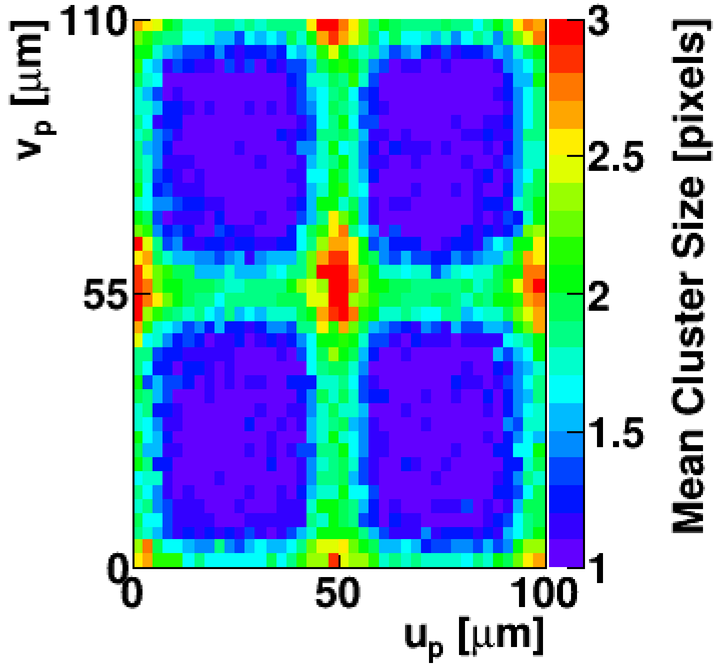
[Slide shown in DEPFET workshop in Valencia 2010]

	PXD 5 (TB2009)	PXD 6 (BelleII PXD)
Noise (in ENC)	~290	~100
Bulk Doping (in $10^{12}cm^{-3}$)	0.85	10
Backplane Voltage (in V)	-180	-20
Drain Border Length (in μm)	3	~10
Clear Border Length (in μm)	3	~10
Source Border Length (in μm)	3	~10

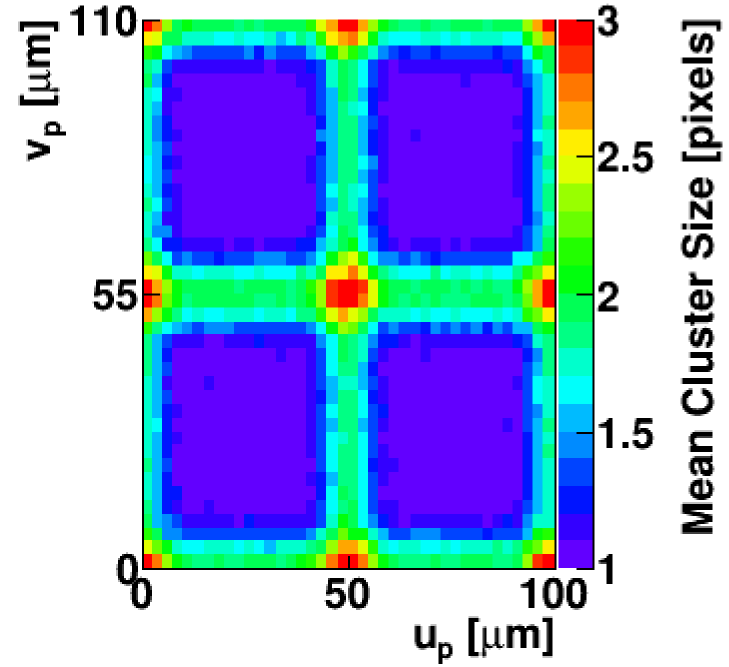
Table 1: Preliminary listing of DEPFET digitizer parameters for TB and Belle II.

Inter pixel charge sharing

Small PXD9 in test beam



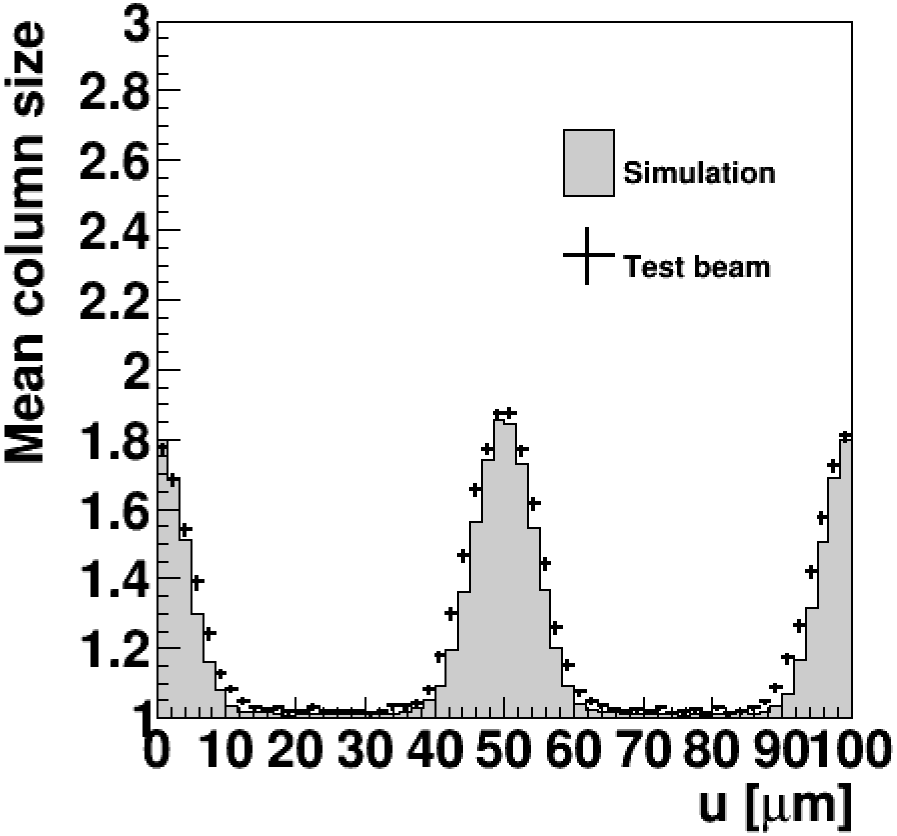
“Tuned” PXD9 Digitizer

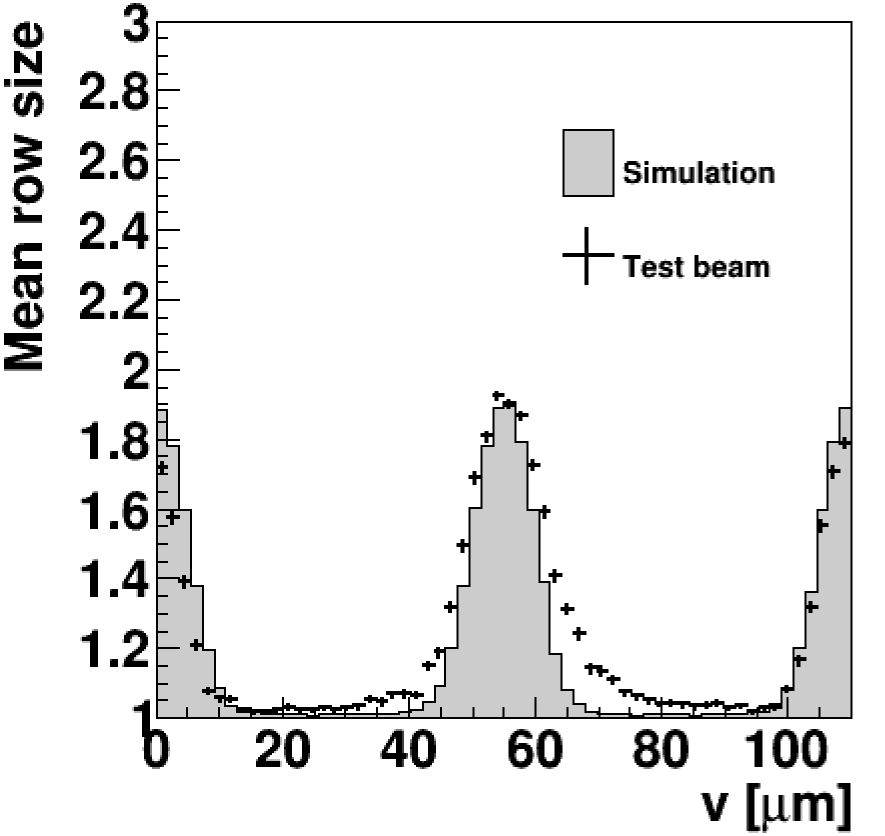


Summary of “tuned” digitizer parameters PXD9 50x55:

:- Source / Drift border length ~6um
:- Clear border length ~4um

Inter pixel charge sharing

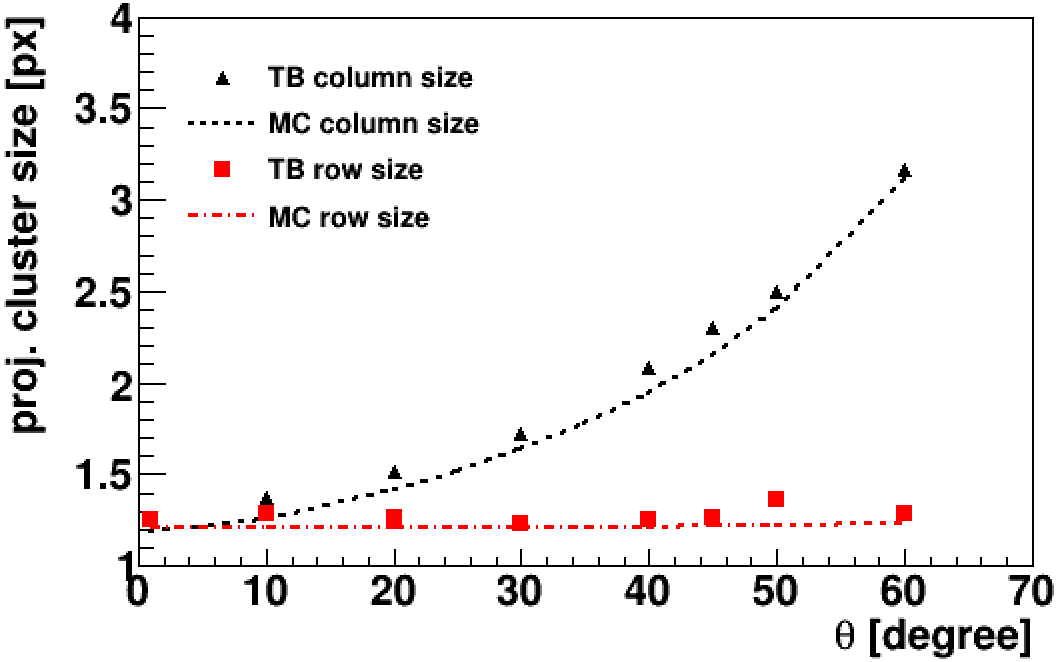




Summary of “tuned” digitizer parameters PXD9 50x55:

:- Source / Drift border length ~6um
:- Clear border length ~4um

Good test: cluster sizes vs angle



:- Module tilted against the beam axis up to 60° around v-axis

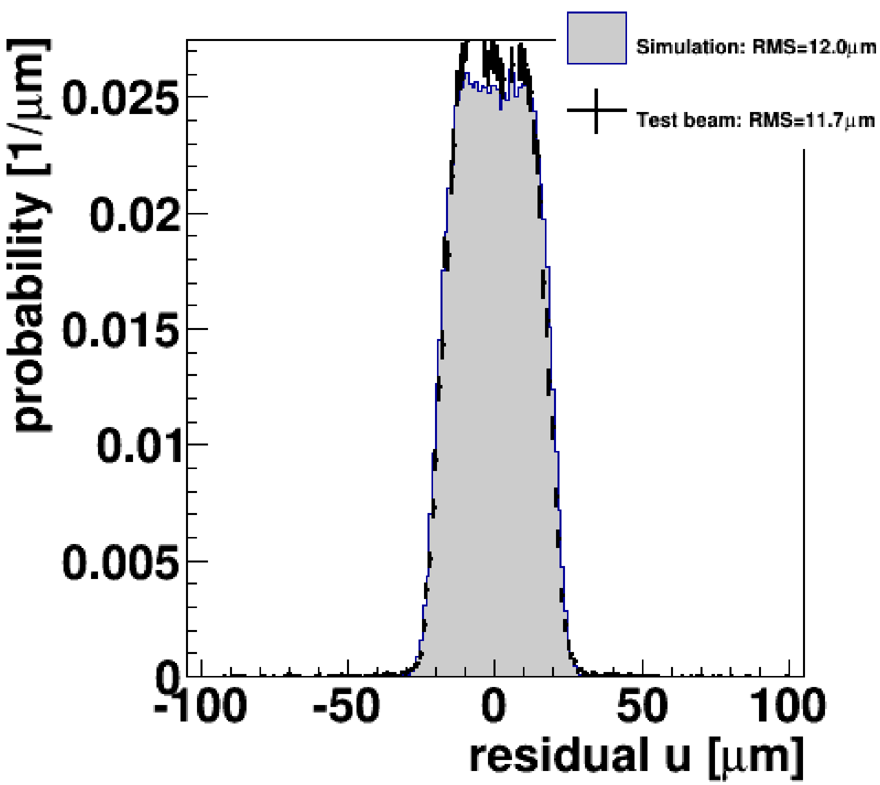
:- Elongated clusters along u axis (multi-column clusters)

:- Only clusters matched to telescope track used

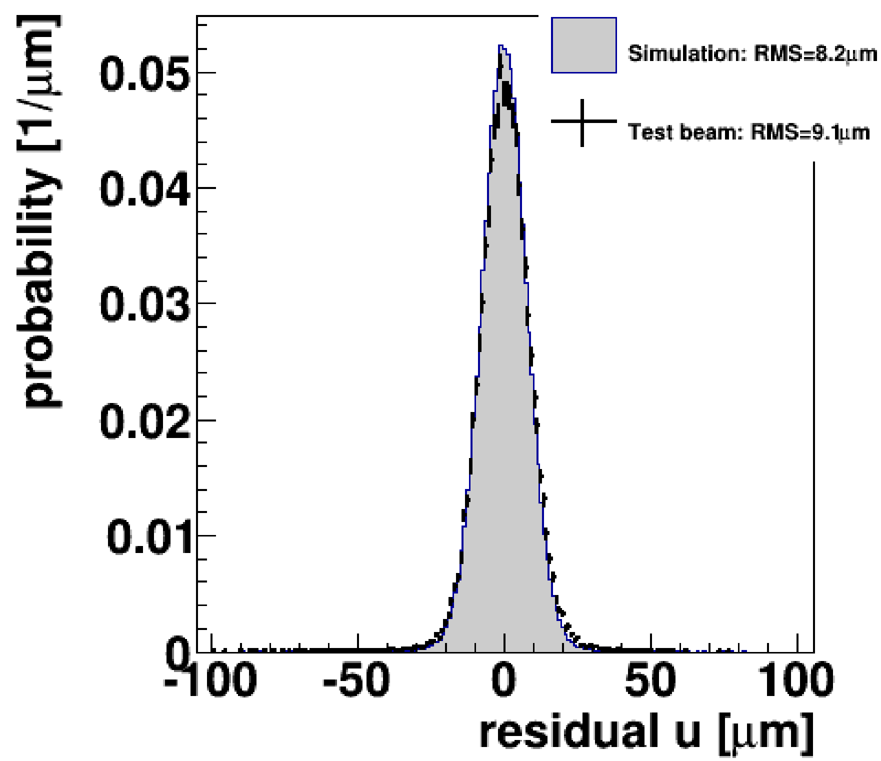
:- **Digitizer model matches cluster shapes for all tilts :)**

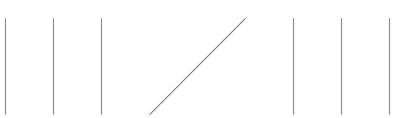
Looking at u - residuals

0° tilt: perp. incidence



30° tilt: many two column clusters



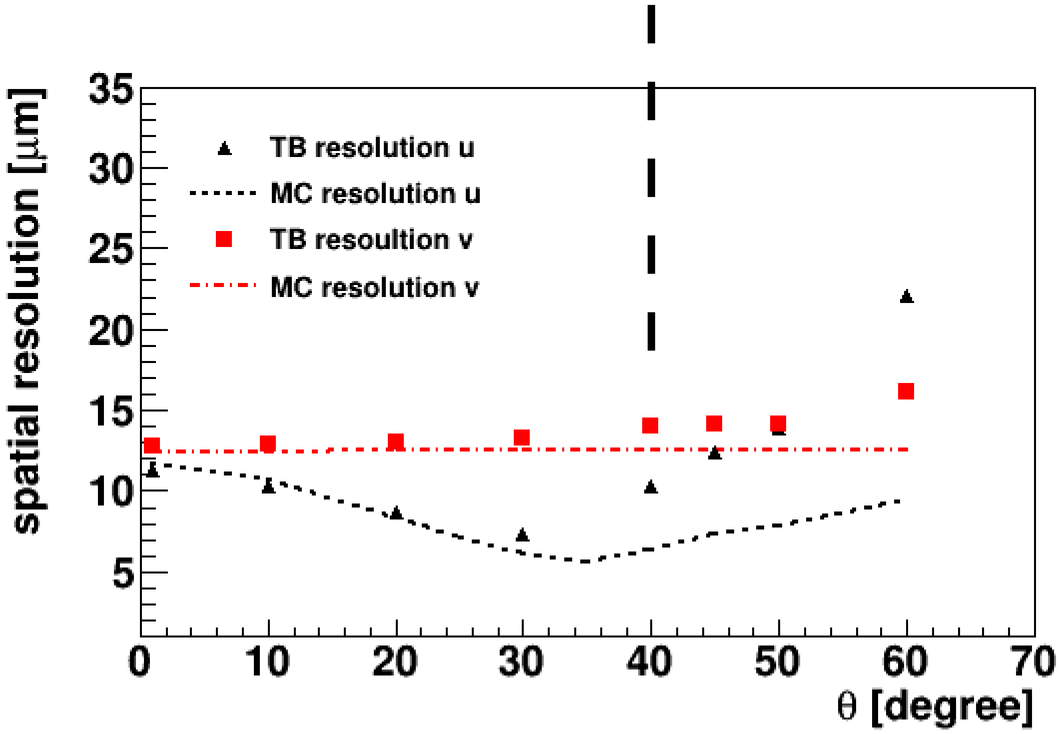


:- Hit coordinates computed as center of gravity
:- Digitizer truth hit smeared by estimated EUDET resolution
:- Telescope resolution grows with angle ()
:- tel. resolution @ 0°:   ~2.8um (RMS)
:- tel. resolution @ 30°: ~5.3um (RMS)

Extraction of spatial resolution

TB extraction ok

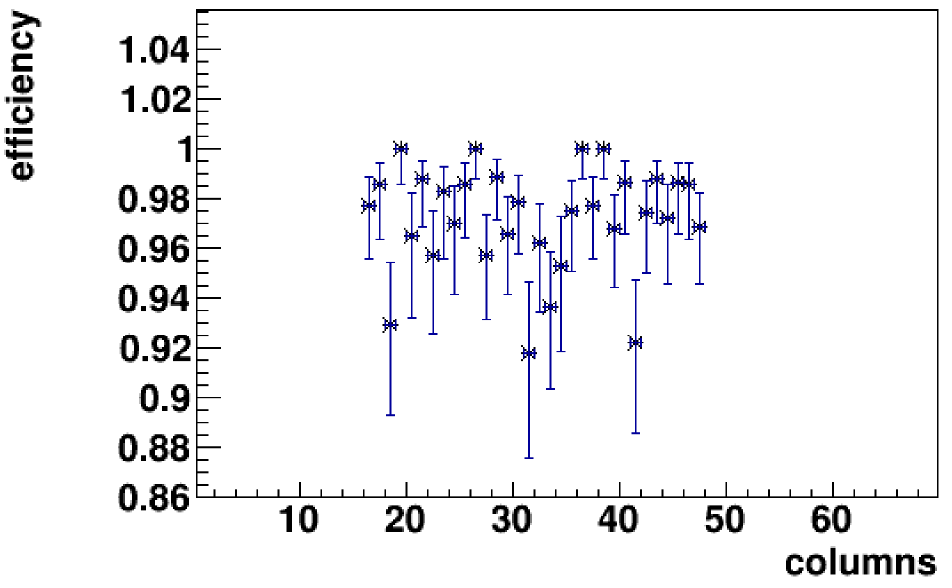
TB extraction troubsome

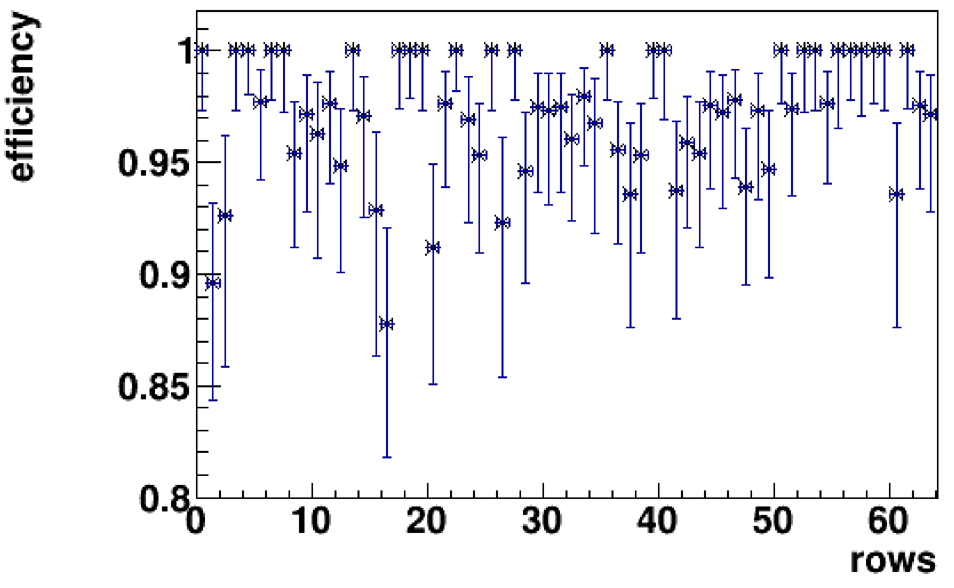


Telescope resolution >8um for tilts >40°

→ large spacings between Eudet arms
→ at some point start hitting Al frame
→ large and hard to estimate EUDET resolution

Efficiency estimation





:- TB data at ZS threshold 5

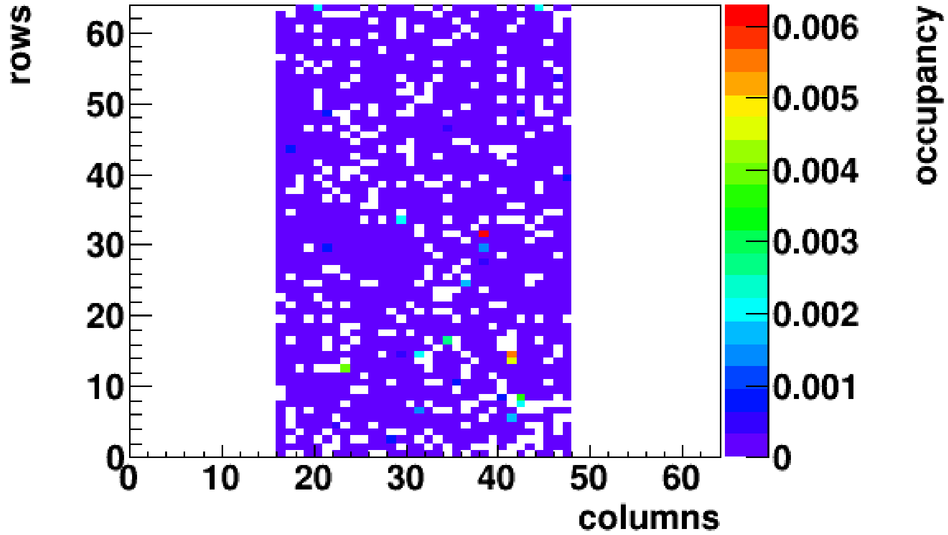
:- efficiency = matched tracks / all tracks

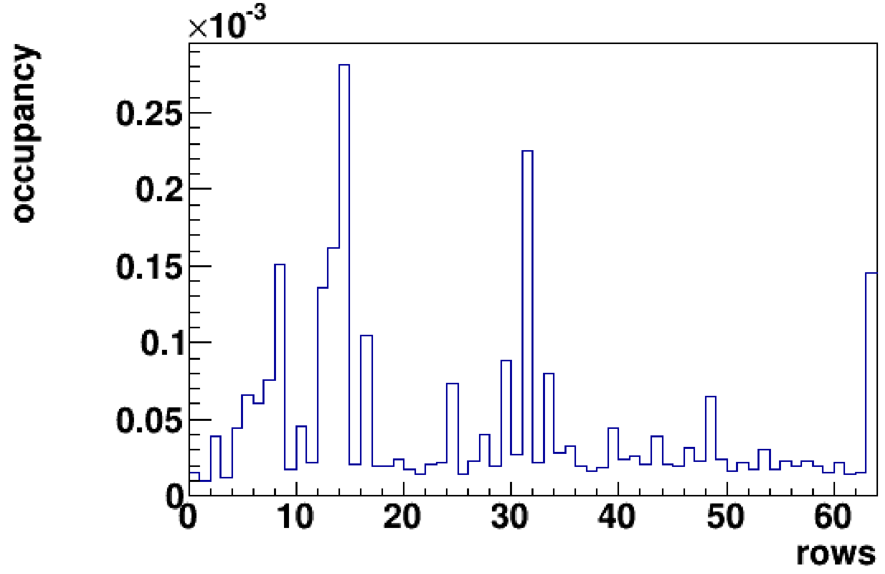
:- skip events with more than one telescope tracks

→ if all events are used: efficiency drops 5%

:- seems that there is some few percent loss

Noise occupancy @ ZS threshold 5





:- noise occupancy = #noise hits / # triggers

:- noise hits = hits not matched to track (masking real signal hits)

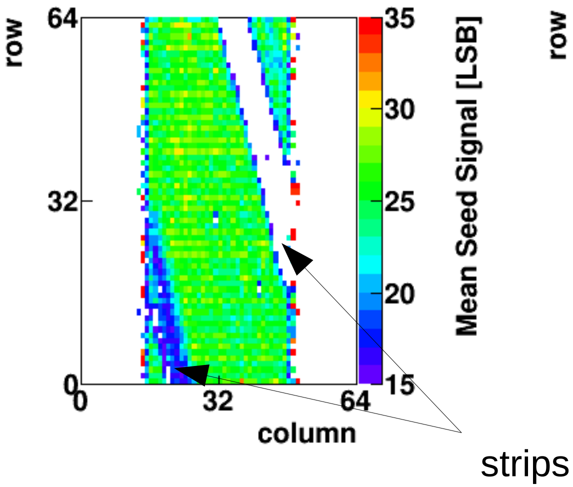
:- noise occupancy on level ~10^-5

HV scan and matrix uniformity

Charge Collection Uniformity

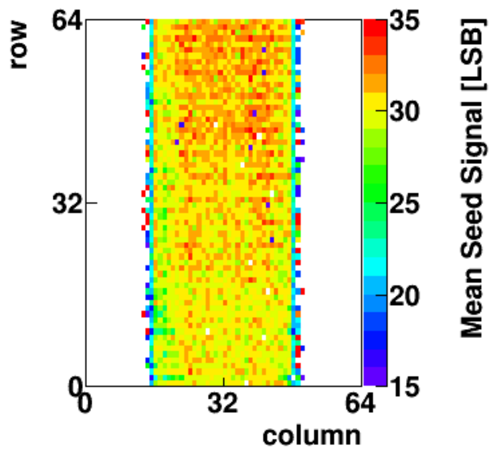
:- 90° incidence on PXD9 @4GeV
:- Looking at mean seed signal per pixel

HV 60V / Drift 5V

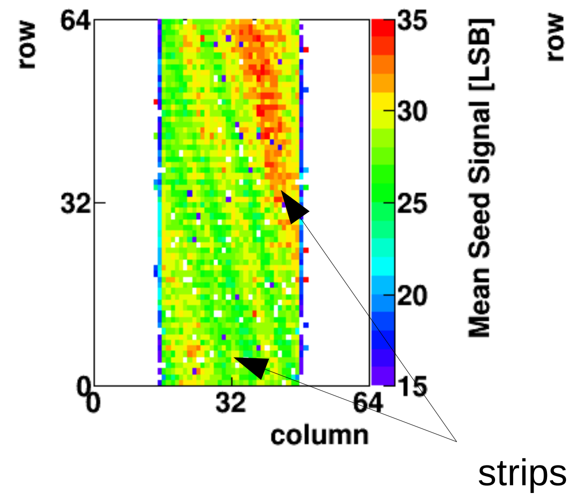


HV 70V / Drift 5V

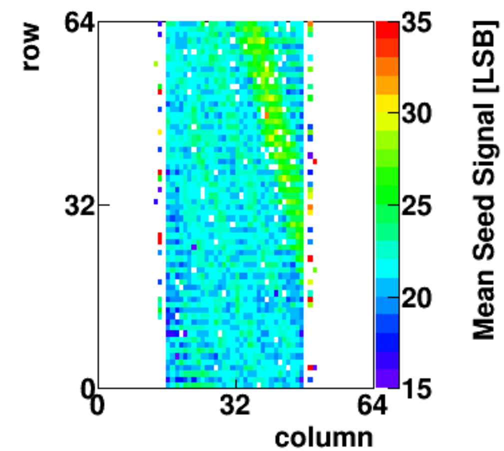
(best)



HV 75V / Drift -5V



HV 80V / Drift 5V



:- HV 60V too low
:- Two strips with small collected charge.
:- Between strips not all signal collected (mean signal ~25LSB)

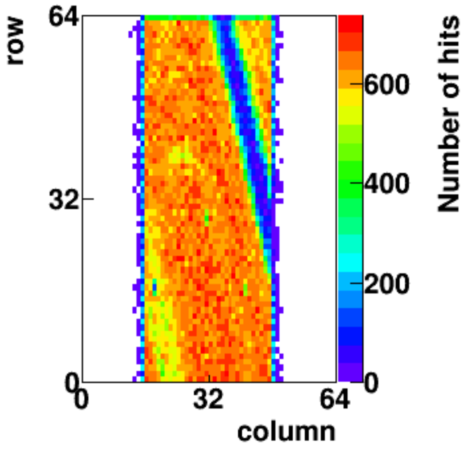
:- HV 70V best
:- most uniform charge collection
:- highest mean signal >30LSB

:- HV >75V too high
:- Strips appear again
:- Between strips charge is lost

Hit occupancy (efficiency)

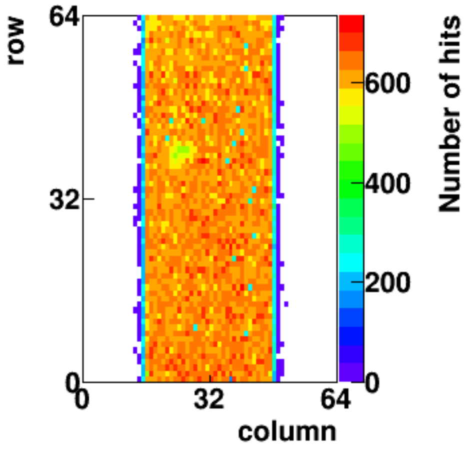
:- 90° incidence on PXD9 @4GeV
:- number of pxd9 hits matched to tracks
→ proxi for hit efficiency!

HV 60V / Drift 5V

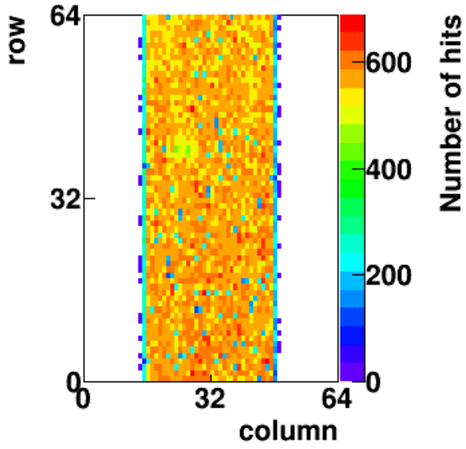


HV 70V / Drift 5V

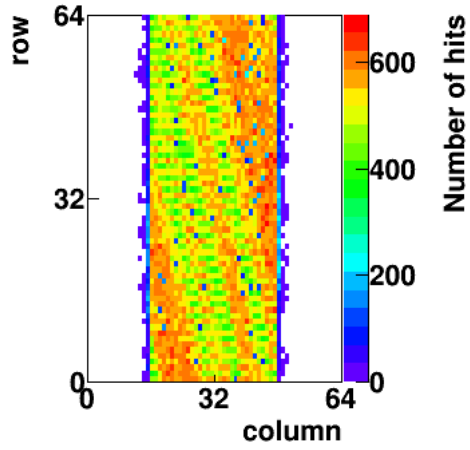
(best)



HV 75V / Drift -5V



HV 80V / Drift 5V



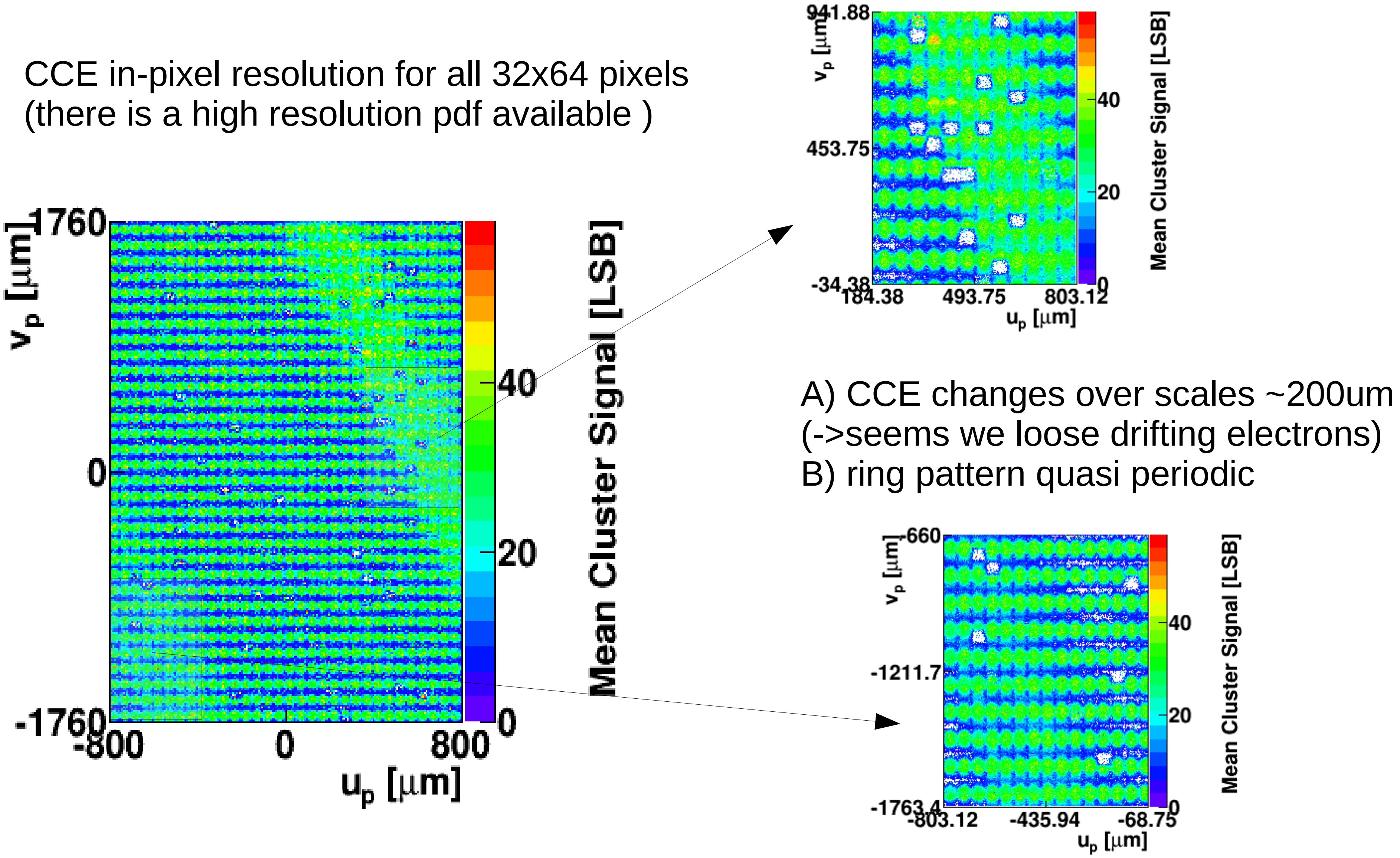
:- similar pattern as before

:- for HV 60V and HV >75V: ineffecient regions observed

H5: HV -80V and Drift -5V

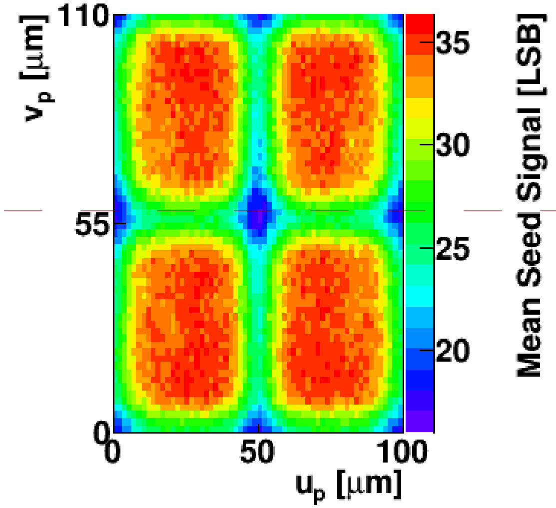
CCE in-pixel resolution for all 32x64 pixels
(there is a high resolution pdf available)

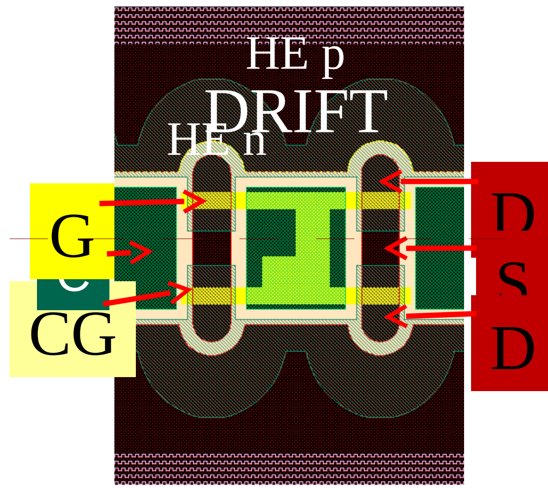
A) CCE changes over scales ~200um
(->seems we loose drifting electrons)
B) ring pattern quasi periodic

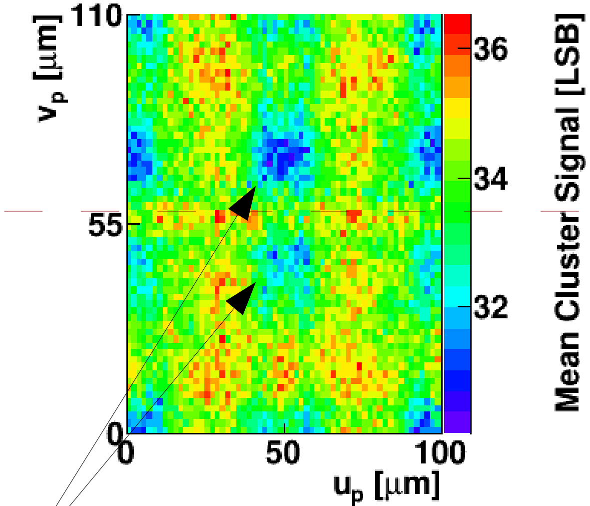


In-pixel charge collection

Optimal point: HV -70V / Drift -5V







Charge loss

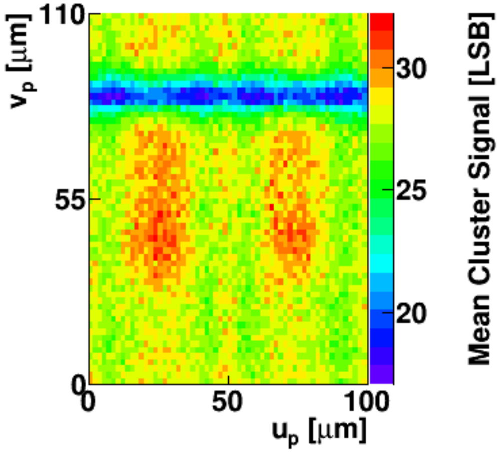
:- 2 double pixle structures (2x2 pixels)
:- charge loss at interface of clear implant and clear gate

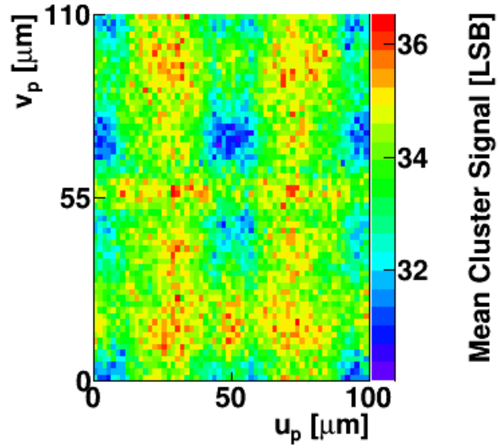
Summary

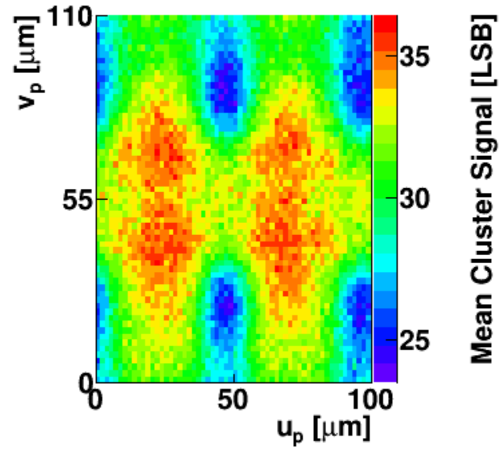
- First time to see MIPs with PXD9 sensors ;)
- Thanks to well trained team: we managed to carry out systematic studies and obtain huge statistic.
- Results are mostly as expected (also according to simulations):
  - Cluster size ok
  - Residuals ok
  - Landau ok
- Uniformity and in-pixel charge collection studies revealed “rings”
  - Optimal settings for HV / Drift under discussion
  - Underlying reason not fully understood (bulk doping)

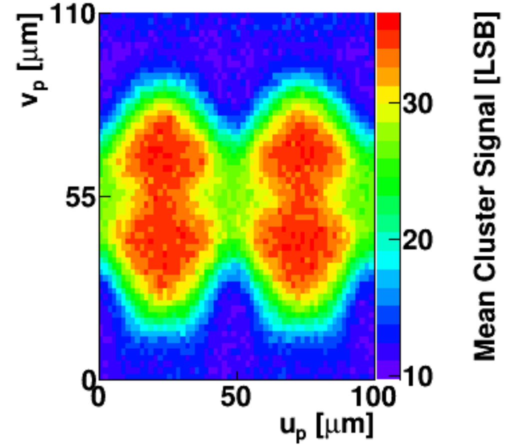
HV -60V / Drift -5V | HV -70V / Drift -5V | HV -75V / Drift -5V | HV -80V / Drift -5V

(best)







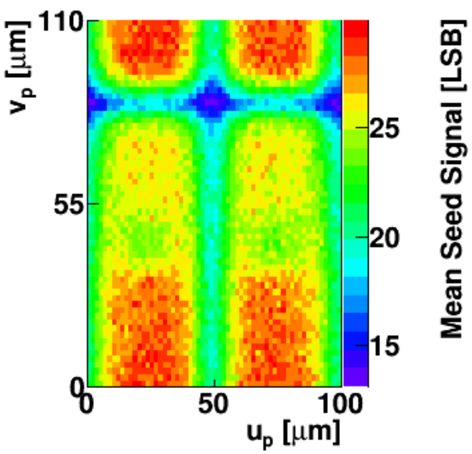


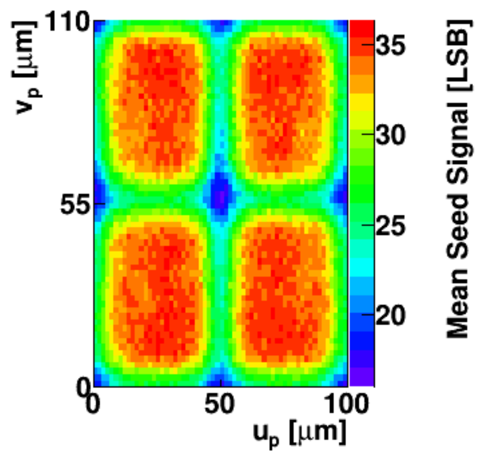
:- Not fully depleted
:- No charge seperation between
pixels sharing source

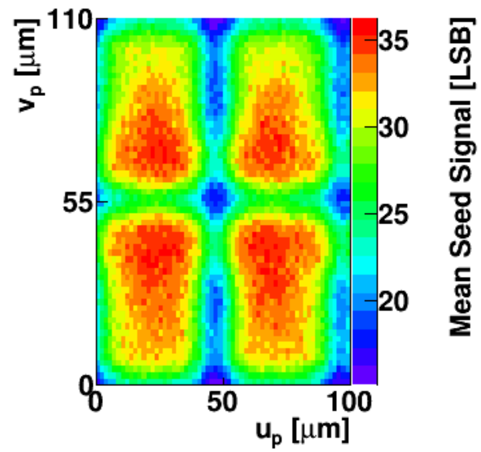
Cluster Charge

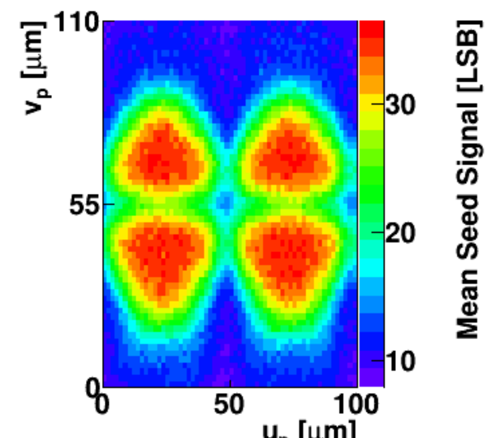
:- too much HV
:- electrons lost
in clear gate

(best)







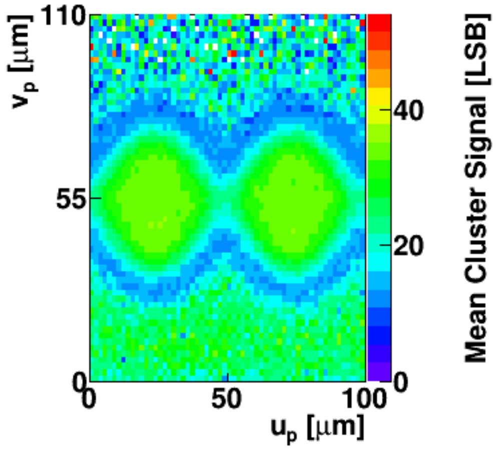


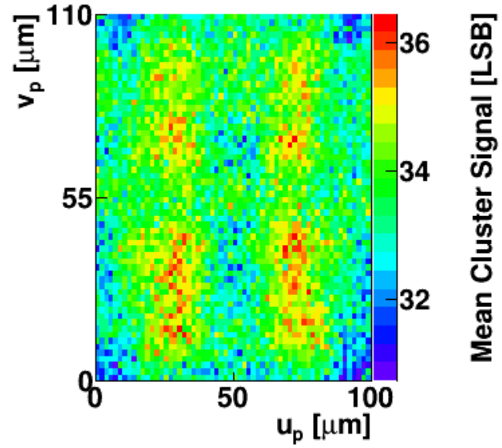
Seed Charge

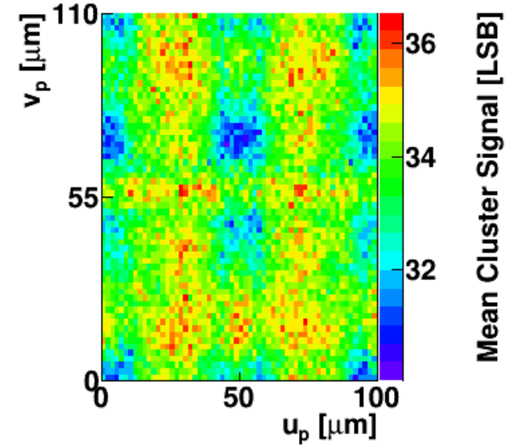
HV -70V / Drift -1V

HV -70V / Drift -3V

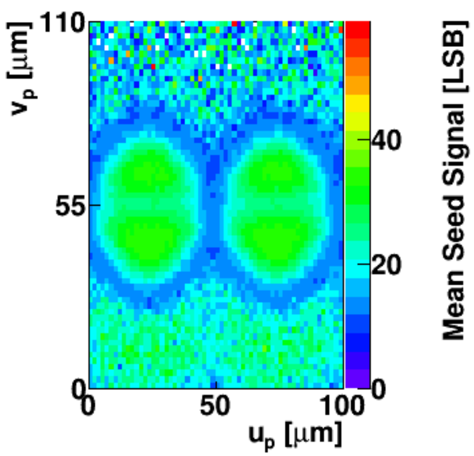
HV -70V / Drift -5V

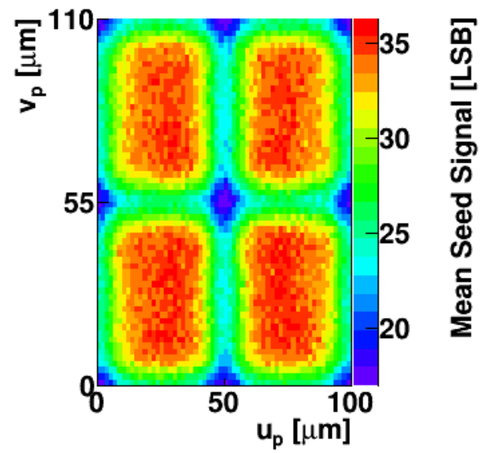


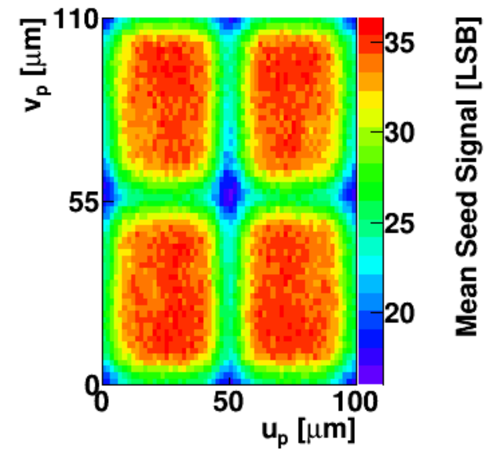




:- crift voltage too small
:- not all charge from drift region collected
:- charge loss below clear gate

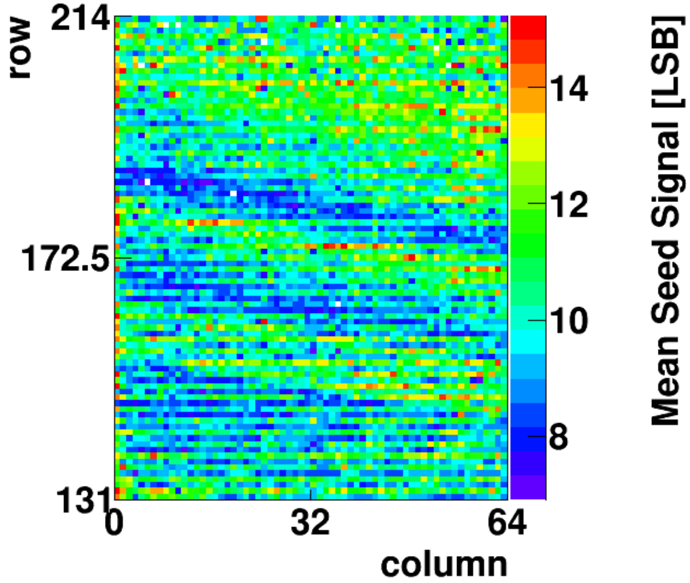




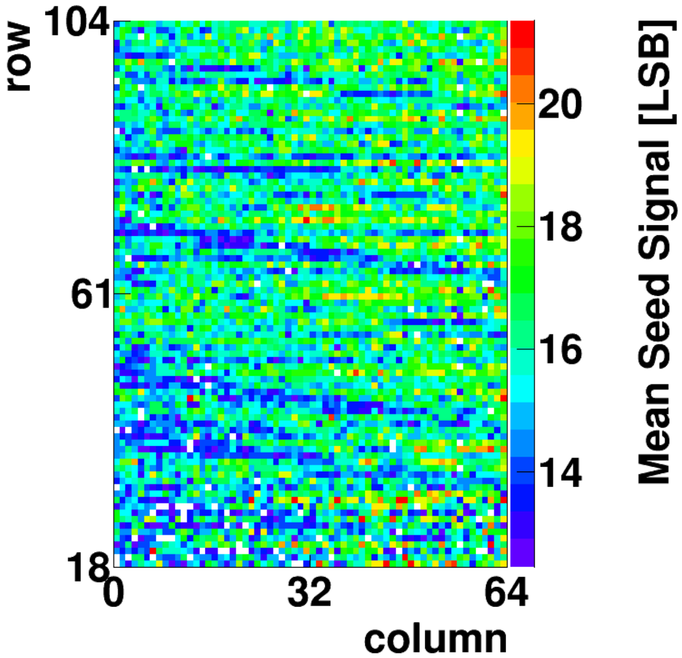


Looking at large PXD6 (Hybrid 6)

HV -16V / Drift -1V



HV -20V / Drift -1V



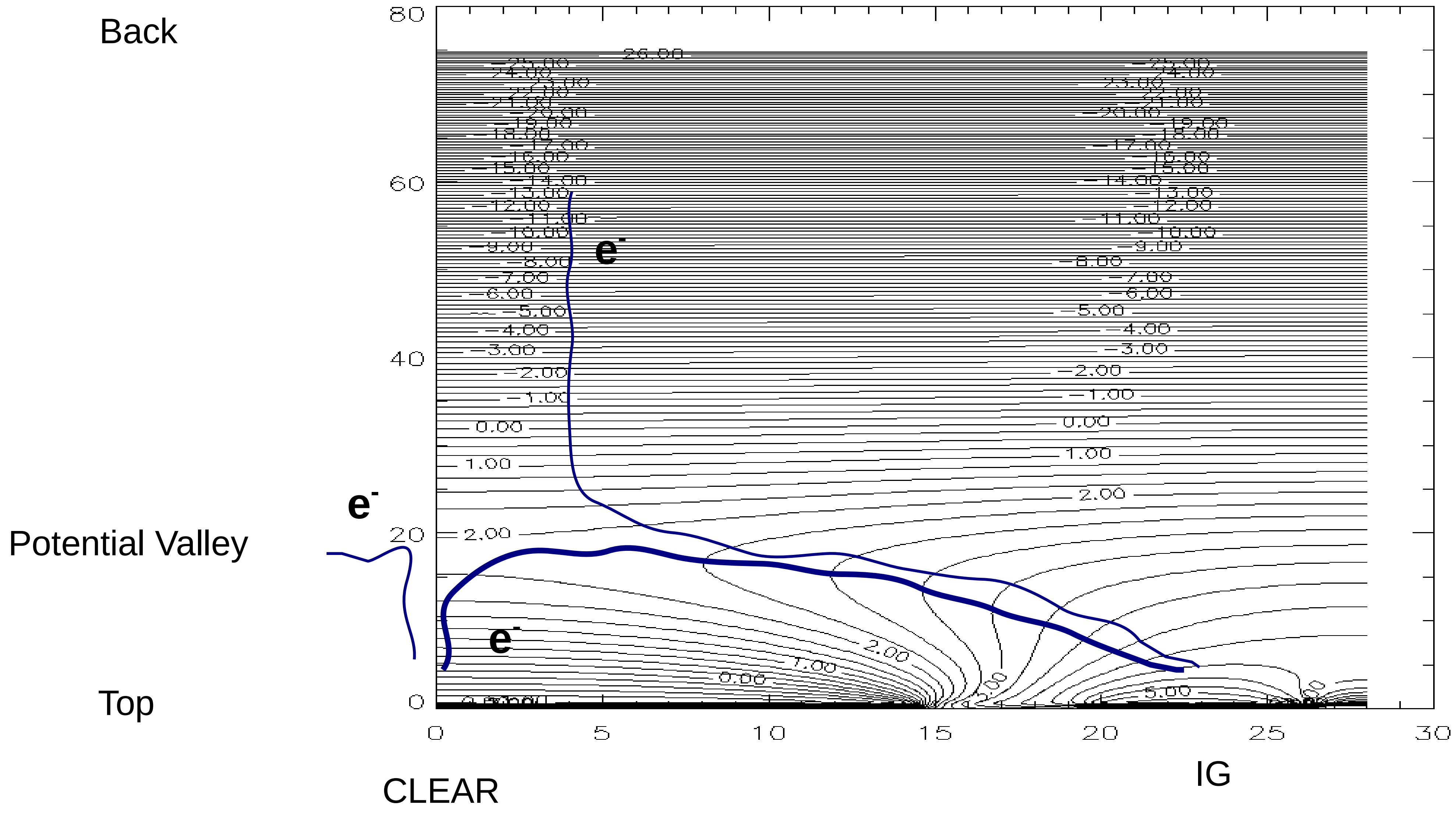
In the HV range -16V to -20V: no sign of rings for Drift -3V or -5V

→ rings depend on balance HV / Drift
→ also present in PXD6
→ bulk doping variation possible root cause

H5 voltages during TB

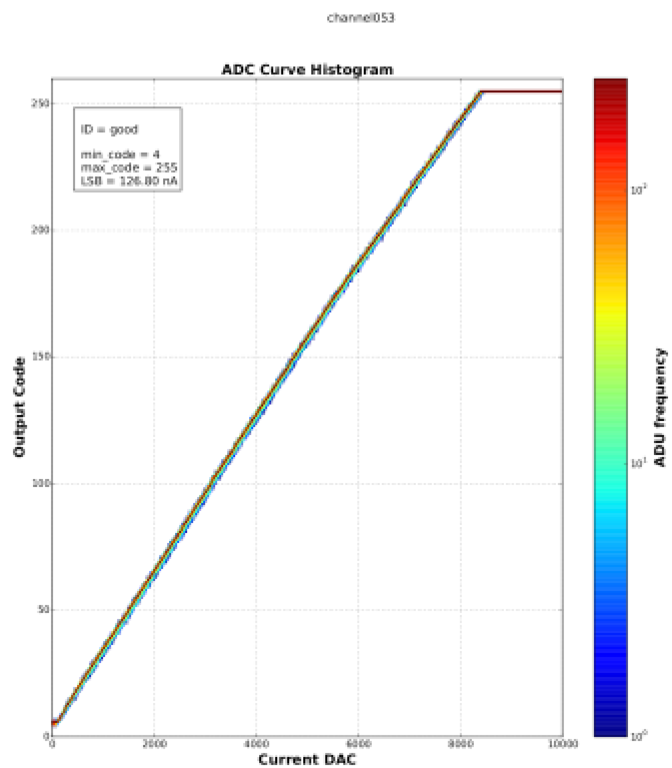
- CCG: -1V
- Clear-low: 5V
- Clear-high: 20V
- Gate-on: -2.5V
- Gate-off: 3V
- HV: scanned from -60V to -80V
- Drift: scanned from -1V to -5V

2D Potential Map in R-Φ Cut: Clear – Clear Gate – IG



Testing results Hybrid 5

All testing results EMCM/Hybrid5 collected here:
http://twiki.hll.mpg.de/bin/view/DepfetInternal/Emcmresults



:- ADC curve with DHE current source after optimization

:- large dynanic range: 127nA per ADU

:- low noise noise: ~0.7ADU

:- no missing code / no bit errors