

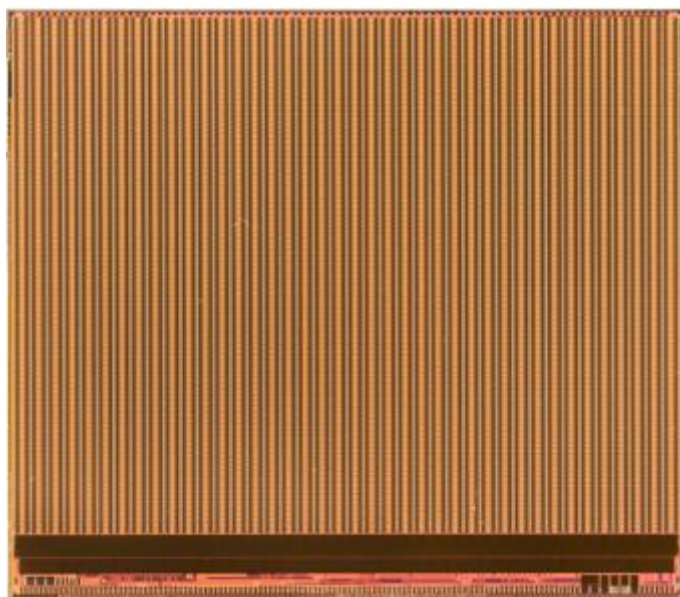


# FANGS

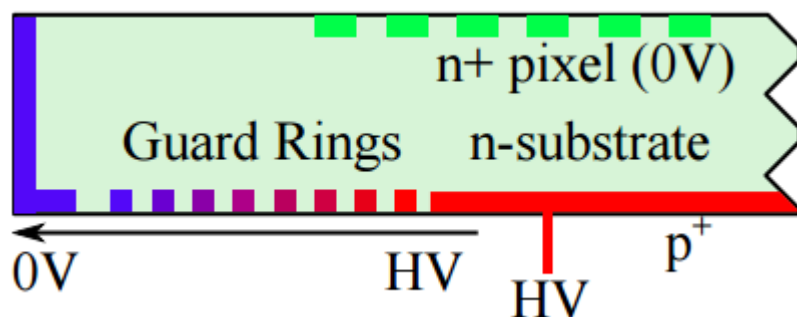
P. Ahlburg, J. Dingfelder, A. Eyring, V. Filimonov,  
H. Krüger, L. Mari, C. Marinas, D. Pohl

University of Bonn

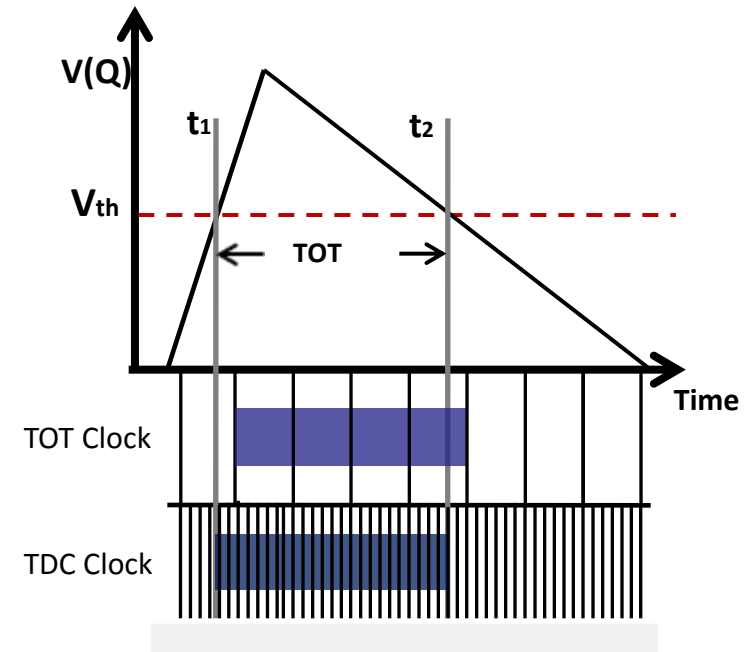
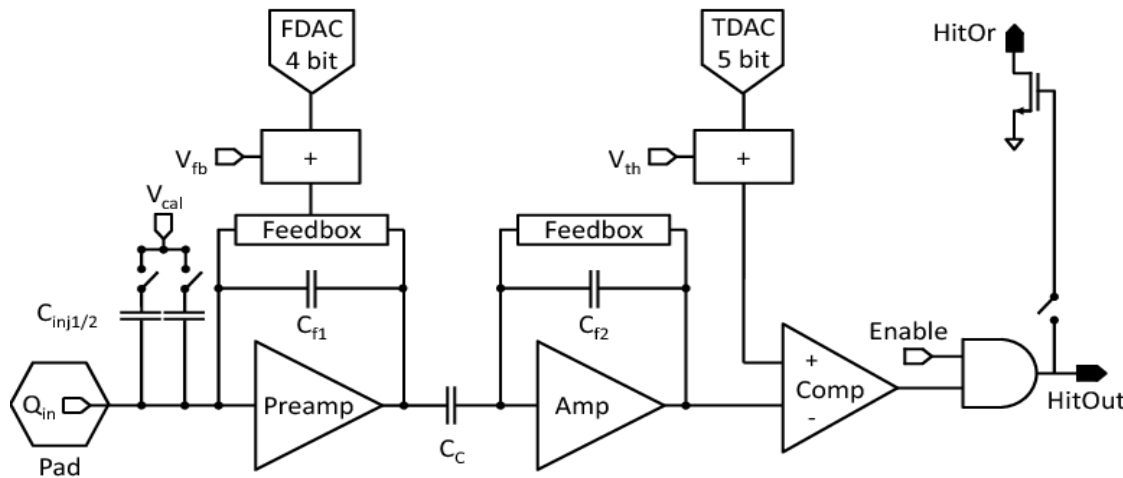




- FE-I4 read out chip
  - High hit rates and radiation hard**
  - IBM 130 nm CMOS process
  - Read out for 80x336 pixels
  - Thickness=150  $\mu\text{m}$
  - Physical size=**21x19 mm<sup>2</sup>**
- Sensor:
  - n-in-n planar
  - Pitch=**50x250  $\mu\text{m}^2$**
  - Thickness=200  $\mu\text{m}$
  - Physical size=19x20 mm<sup>2</sup>
  - HV=60 V
  - Power=1.2 W

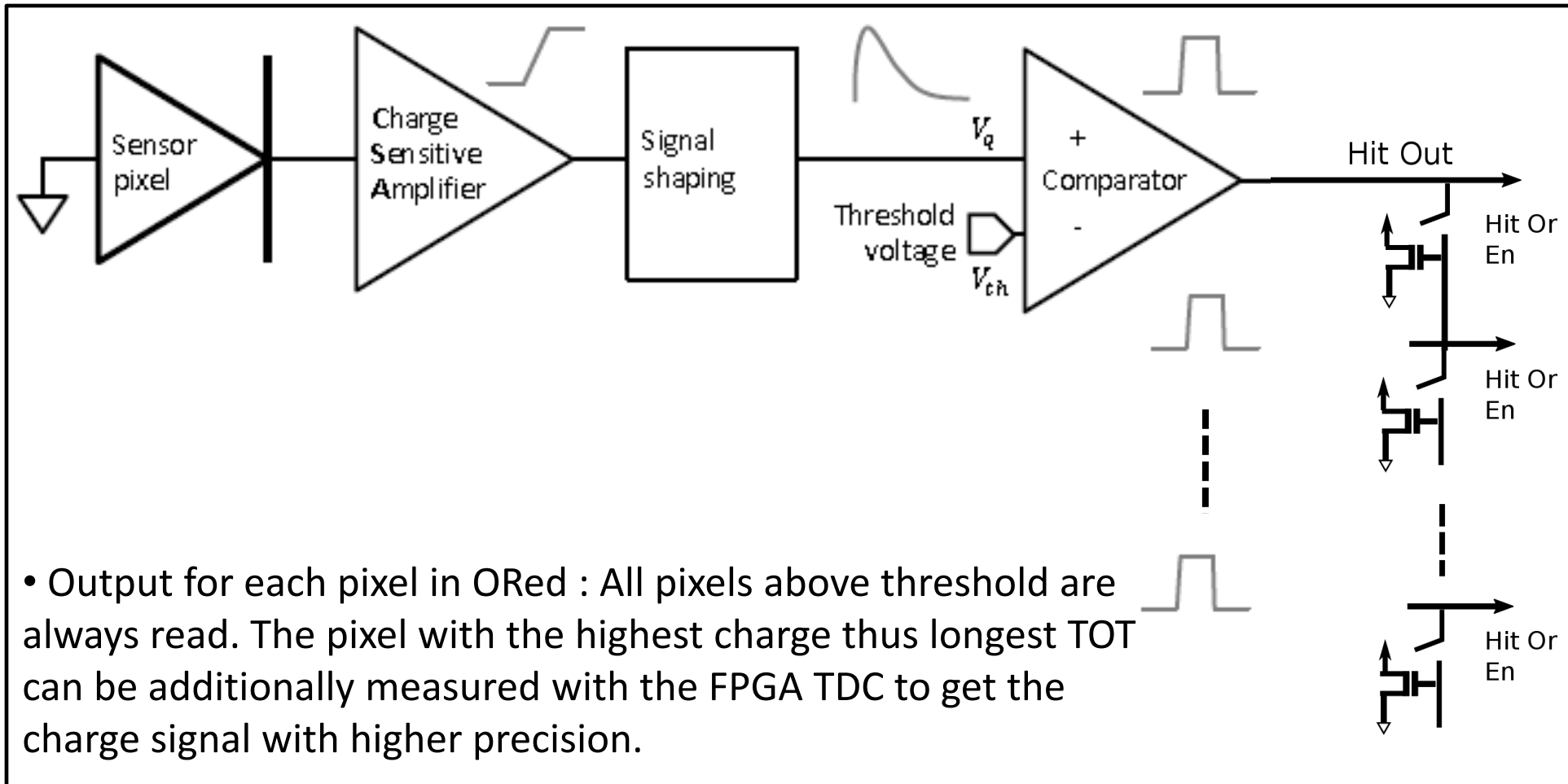


- **Background radiation measurements in Phase 2:**
  - Sensitive to low keV X-rays
  - Ability to measure high particle rates



- Two stage amplifier → Discriminator with adjustable threshold.
- Time over threshold (**TOT**) with 40 MHz clock.
- Time to digital converter (**TDC**) uses 640 MHz FPGA clock.
- Output of each pixel is ORed.
- Internal charge injection circuit for threshold tuning and calibration

→ Both, high speed and adequate energy resolution achieved at the same time

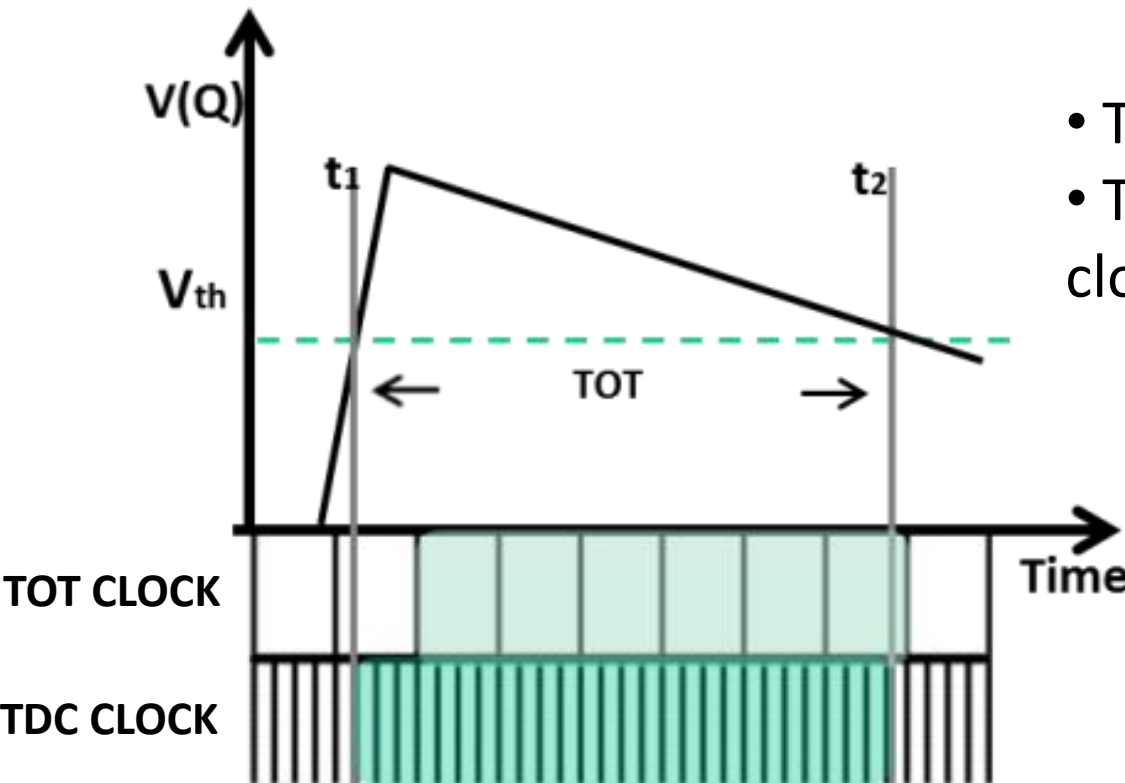


- Output for each pixel in ORed : All pixels above threshold are always read. The pixel with the highest charge thus longest TOT can be additionally measured with the FPGA TDC to get the charge signal with higher precision.

- Hit Bus also used as self trigger

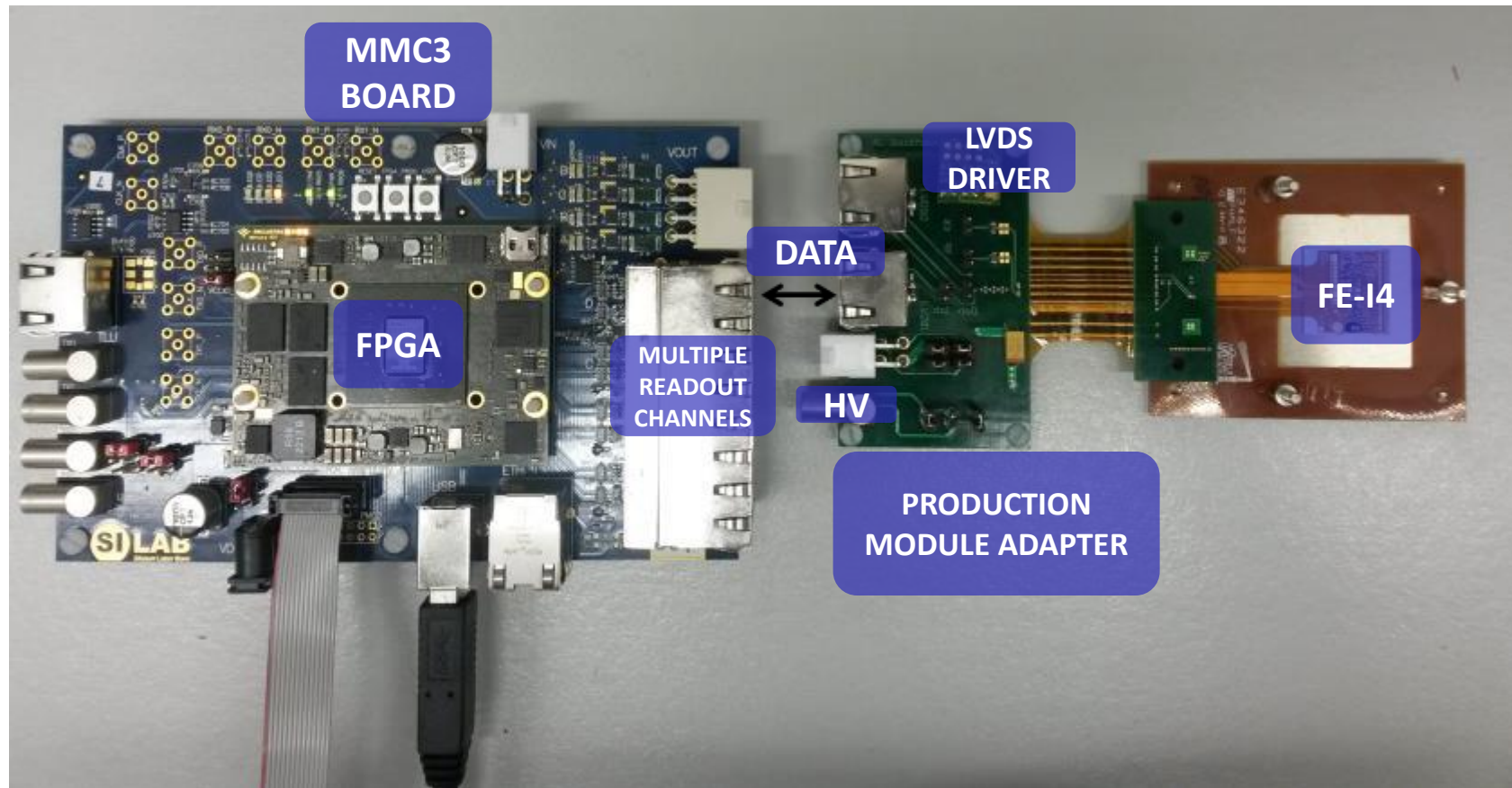
**Hit Bus**



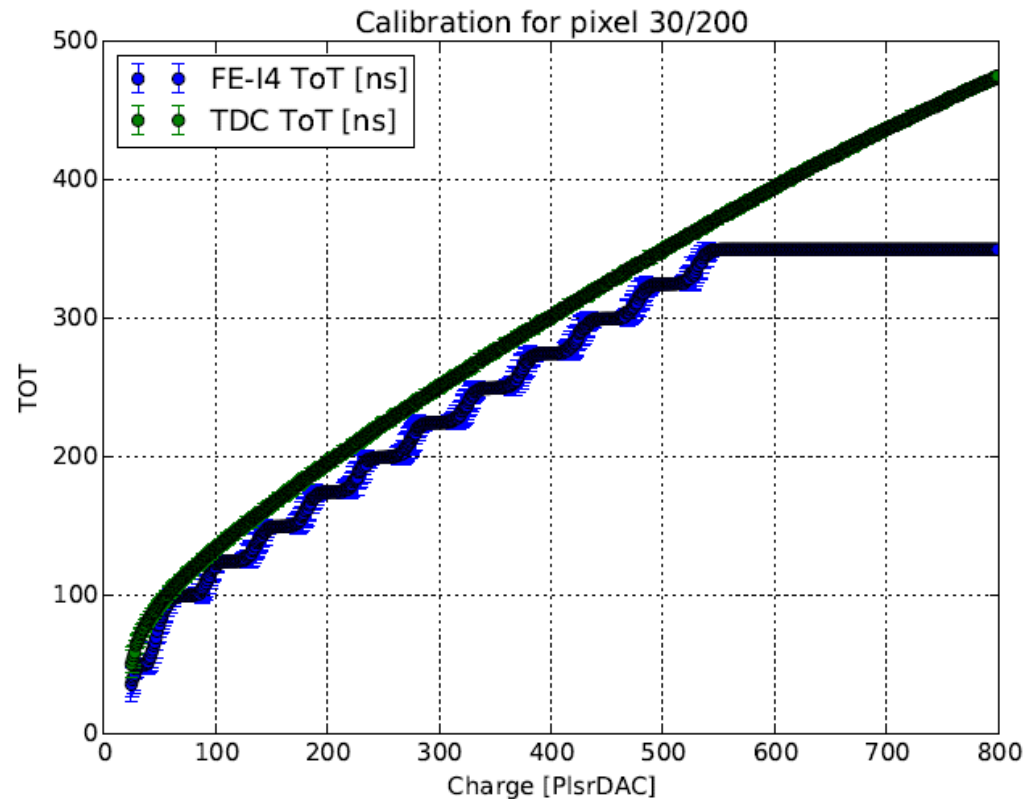


- TOT Method uses 40MHz clock:4 bit
- TDC Method uses FPGA's 640 MHz clock:16 bit

- Improved resolution
- Limited to **one** pixel per readout
- HitOr signal transmitted separately

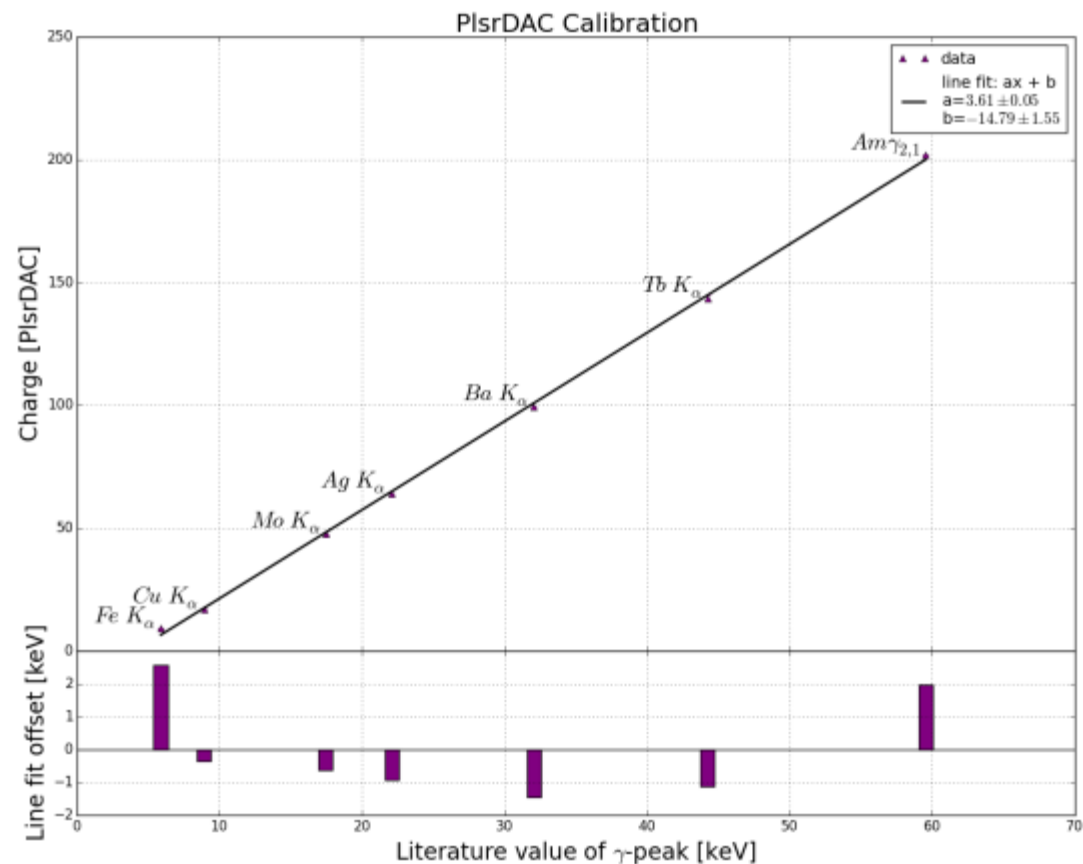
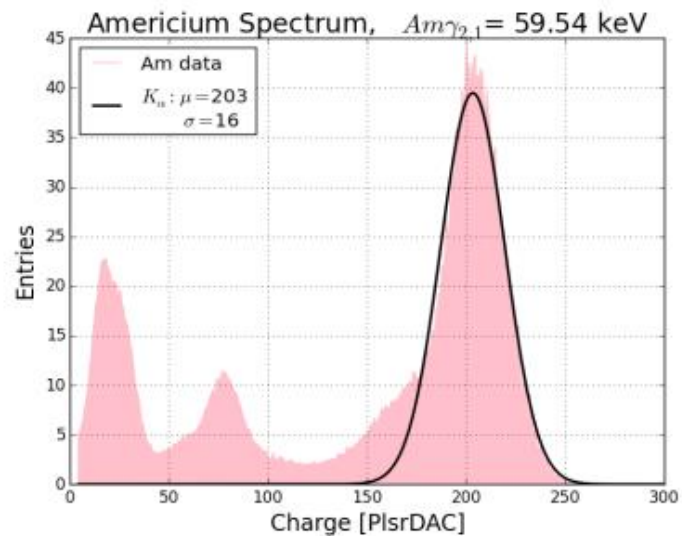
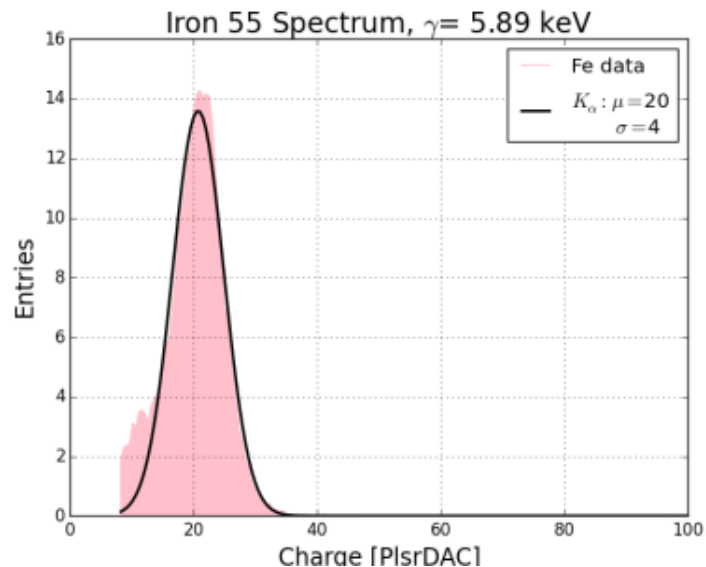


- MMC3: New data acquisition system for the BEAST experiment
  - Multiple FE read out in parallel
  - Faster FPGA; TDC Method may be improved
- Single ended HitOr signal converted to an LVDS signal.



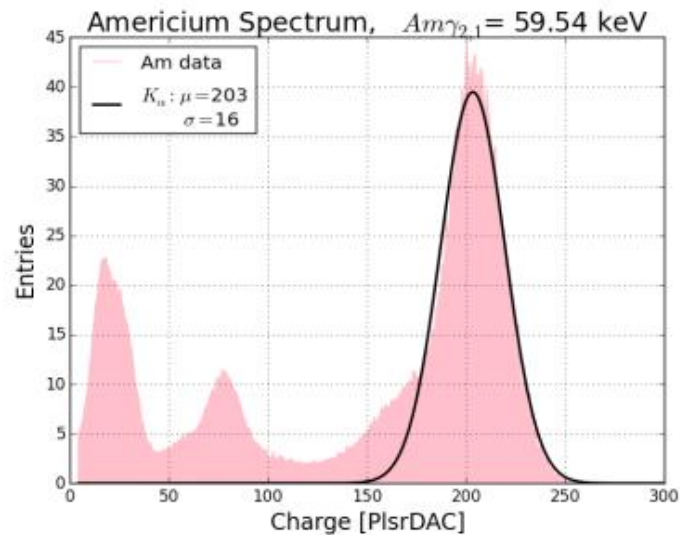
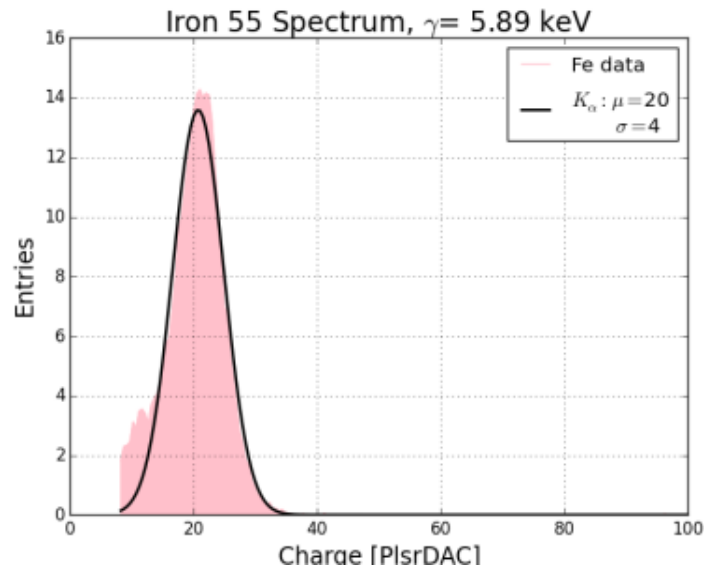
- Precise energy resolution requires pixel per pixel calibration
- Internal charge injection in units of PlsrDAC
- $V_{th}$  and TDC as a function of charge different for each pixel.

# Calibration and Dynamic Range

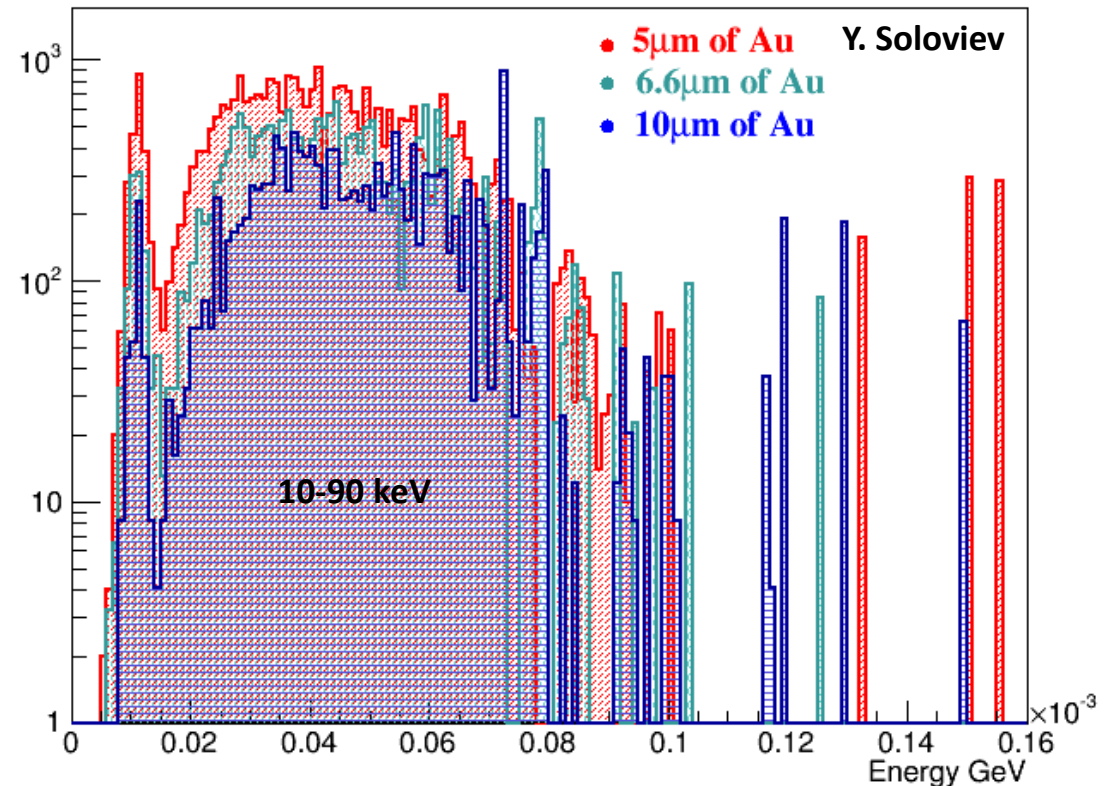


- Dynamic range 10-60 keV (wider also possible)
- Lowest measured plsrDAC value  $\sim 7$ 
  - Threshold of  $\sim 1000$  electrons feasible

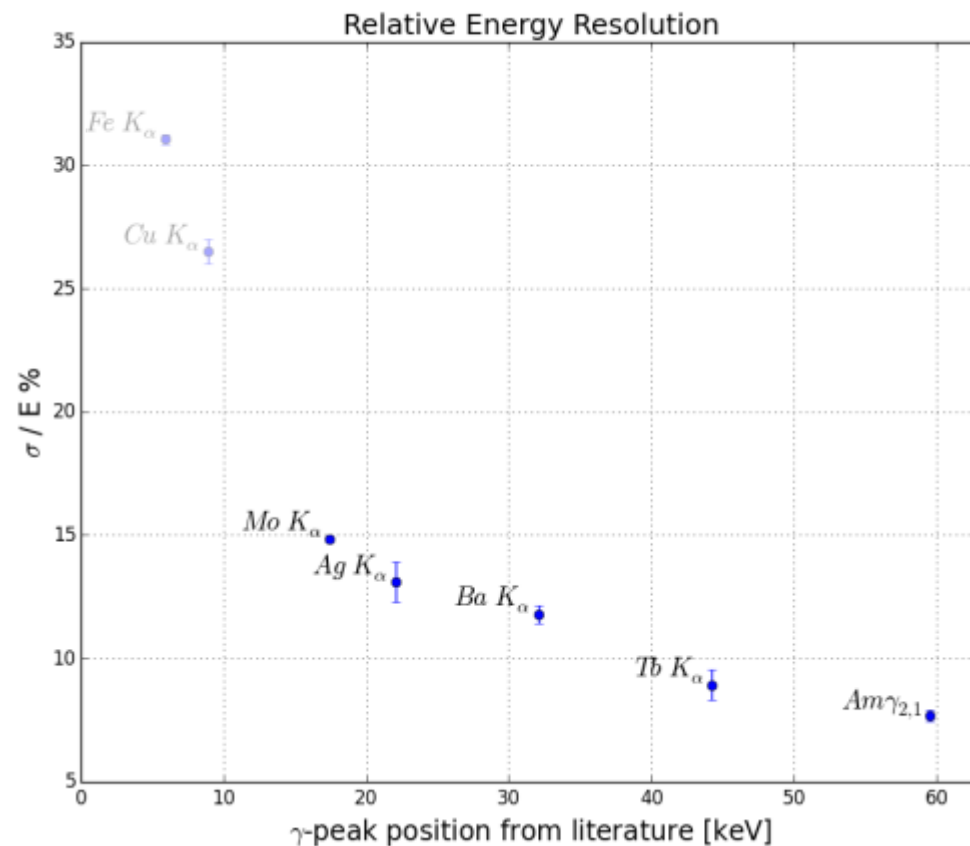
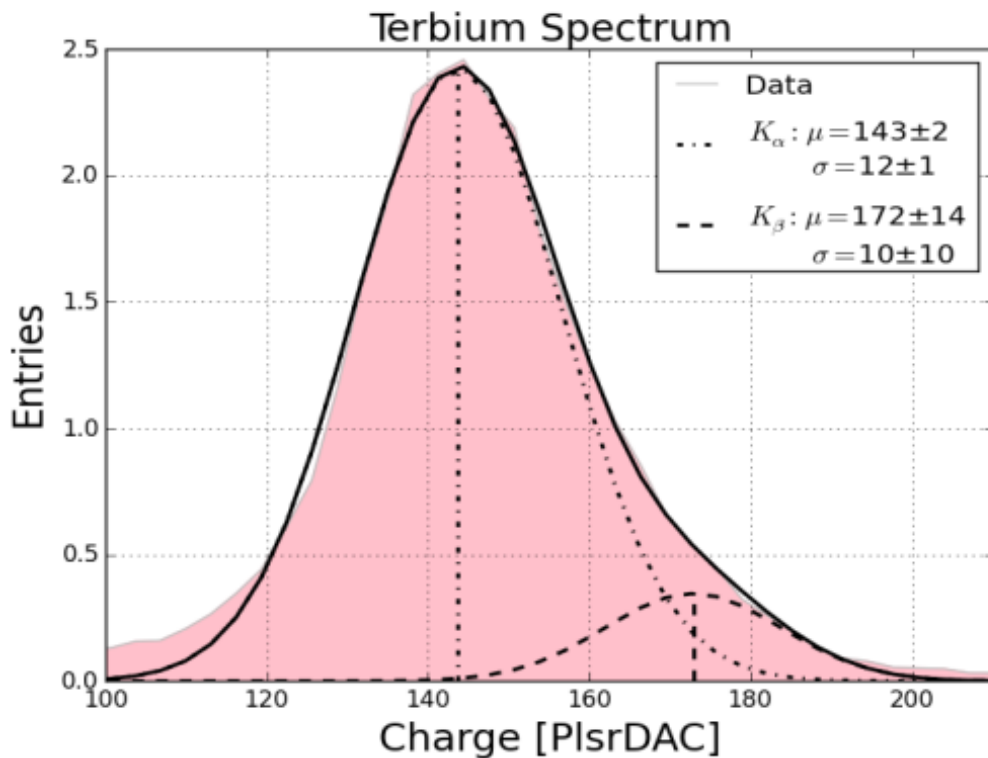




## Energy of SR photons in PXD

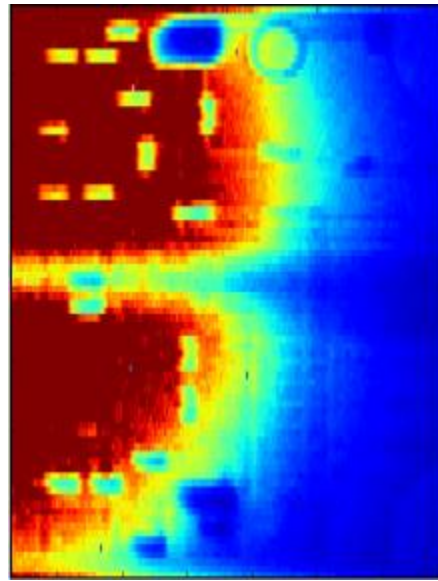
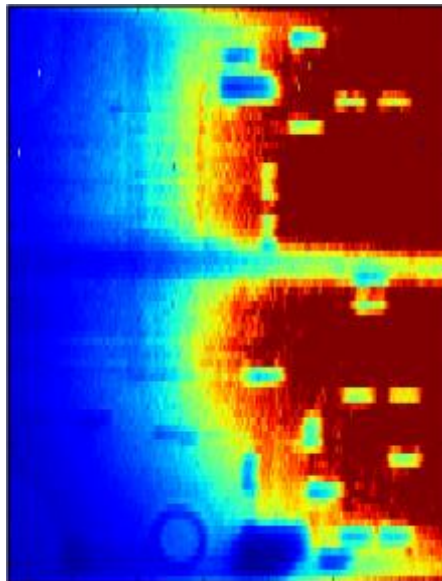
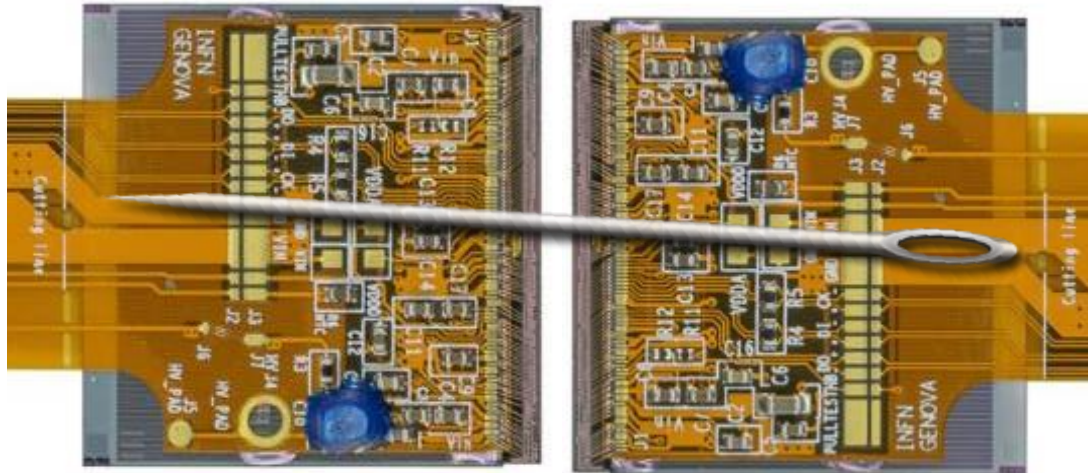


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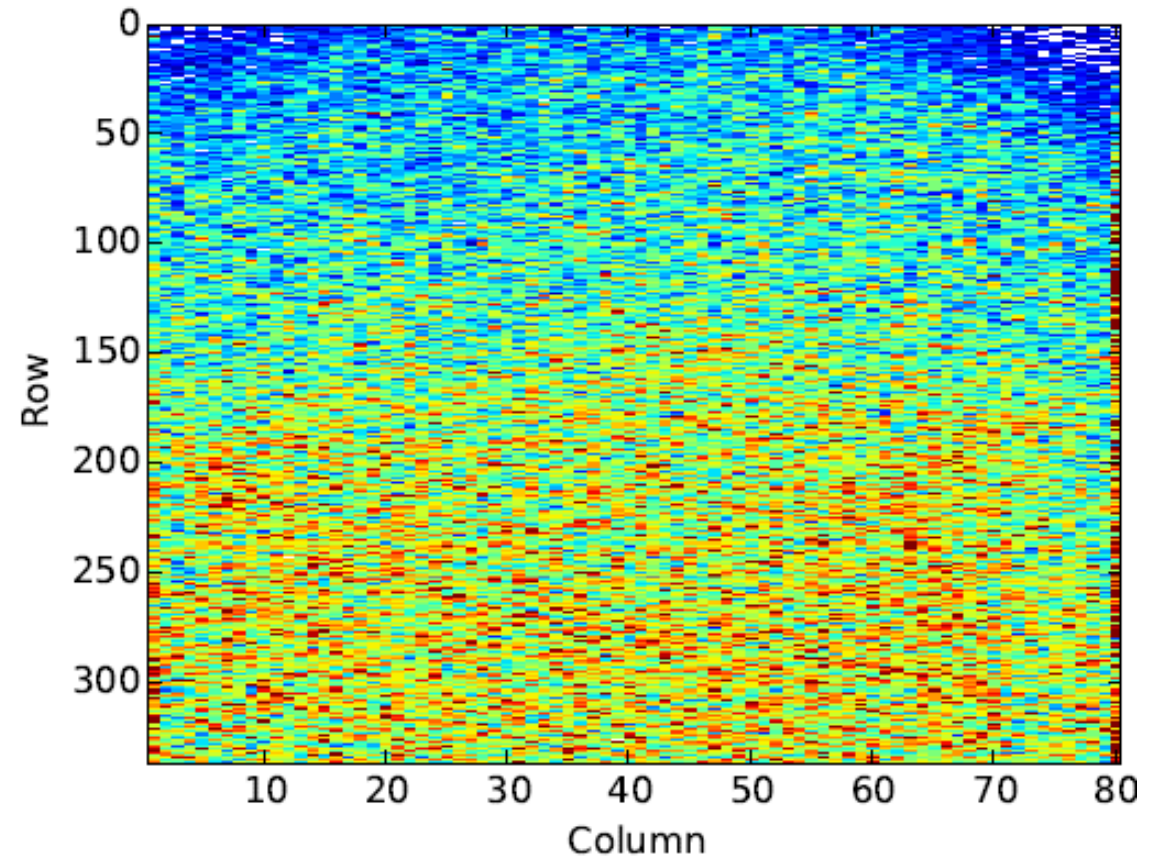


- Terbium  $K_\alpha = 44.2$  keV,  $K_\beta = 50.7$  keV
- $\Delta E = 6.4$  keV

- Adequate energy resolution
- Better than 15 % above 10 keV

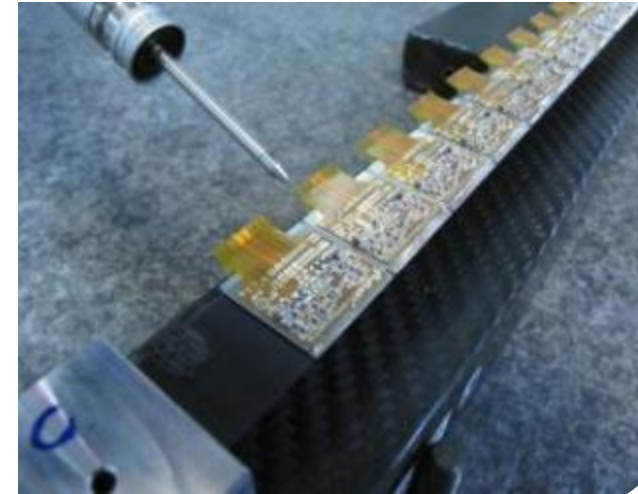
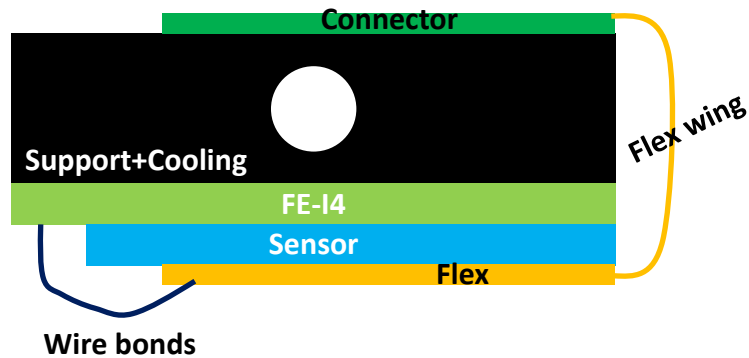


- Hit map two FE under Sr90 illumination
- Multiple module parallel readout with MMC3
- Current stave design prompted by absorption of flex components

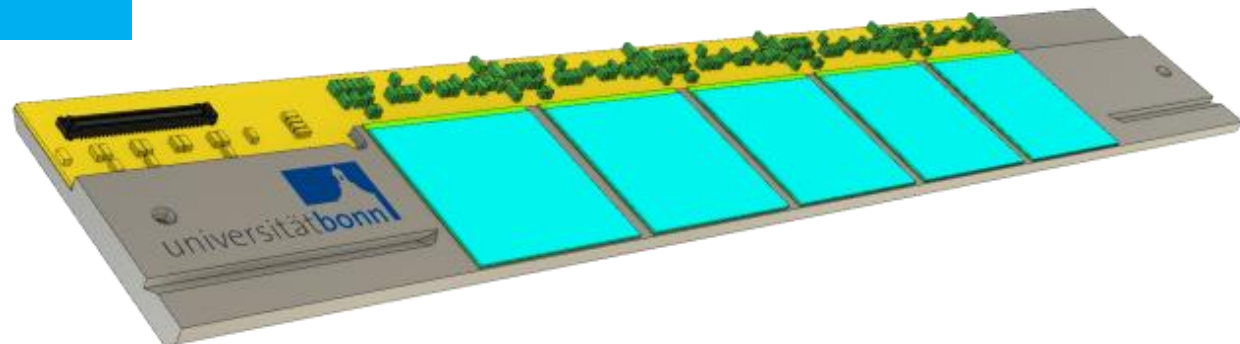
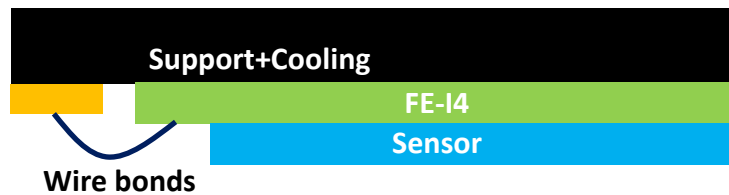


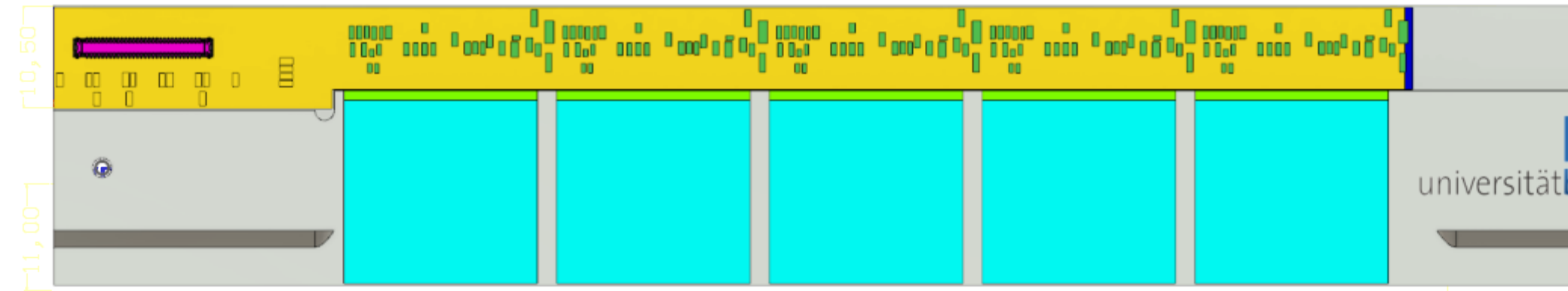
- Effect of components is eliminated by taking a source scan via backside (FE) illumination
- For BEAST, no material in front of the sensor; kapton running parallel to the modules

- Initial concept, following IBL stave design

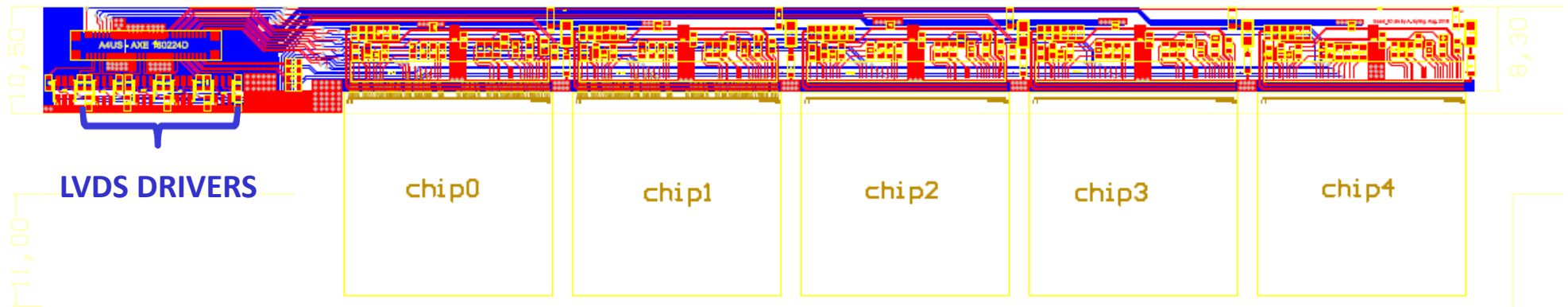


- Revised design, adapted to BEAST needs

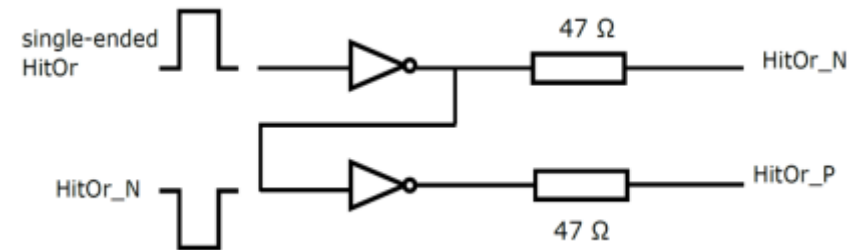
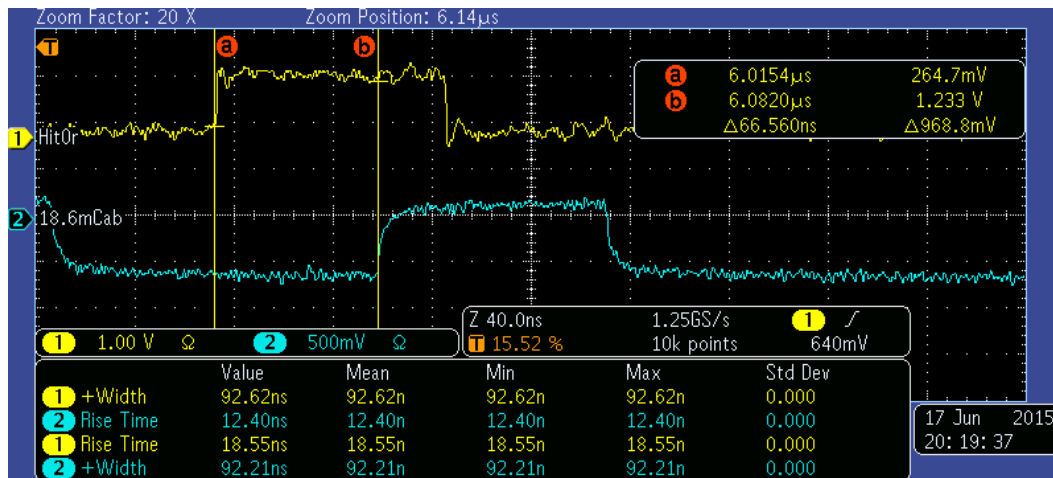




- Flex design for a single stave of 5 FE-I4 chips
- LVDS drivers converting single ended HitOr signal to differential signal for propagation over long cables
- Drivers positioned in backward direction shielded from radiation behind the PXD cooling block
- Radiation hardness to be investigated



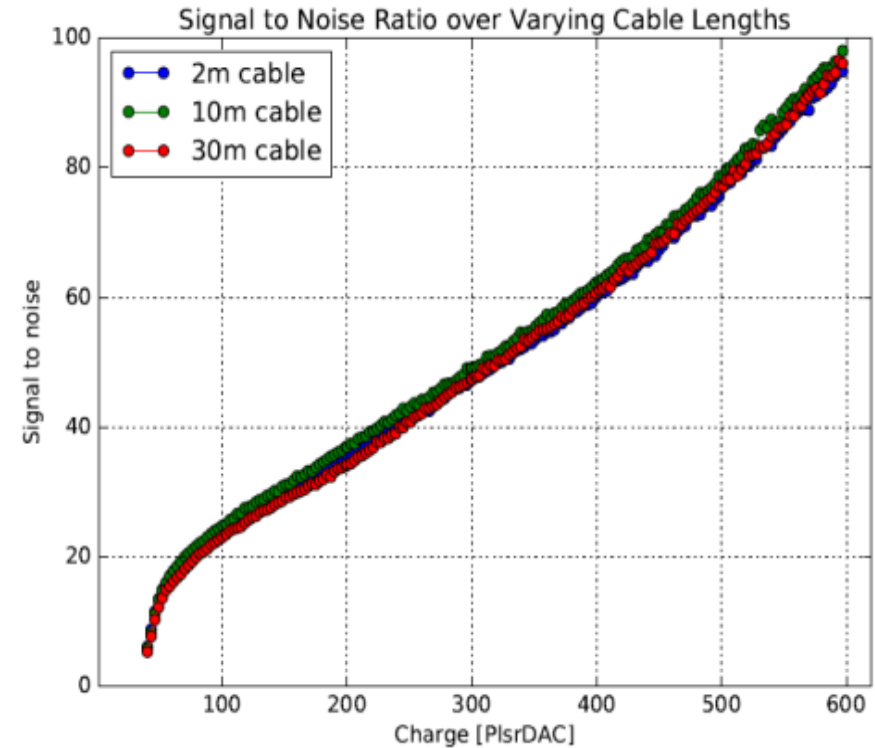
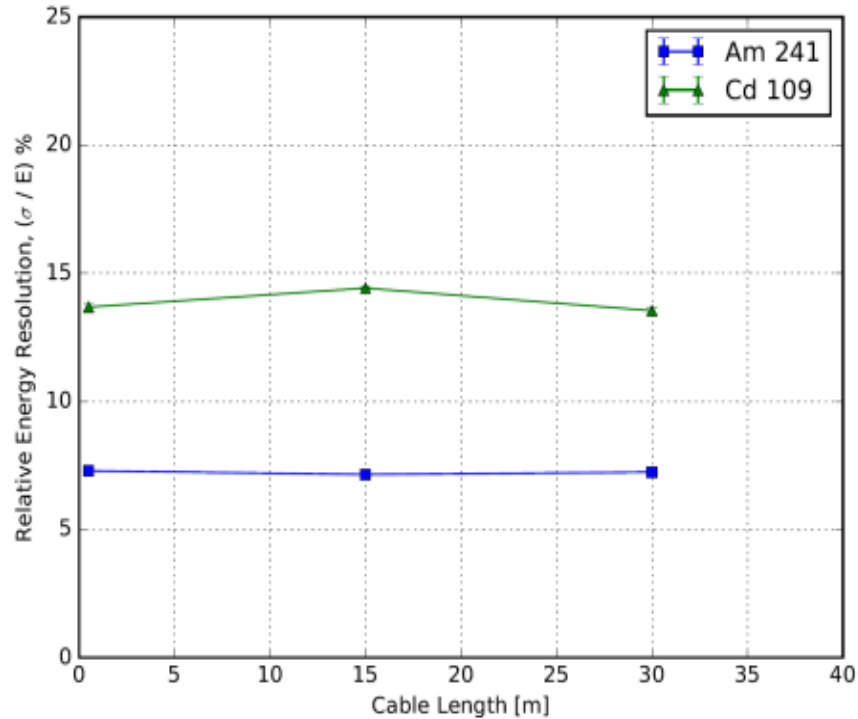
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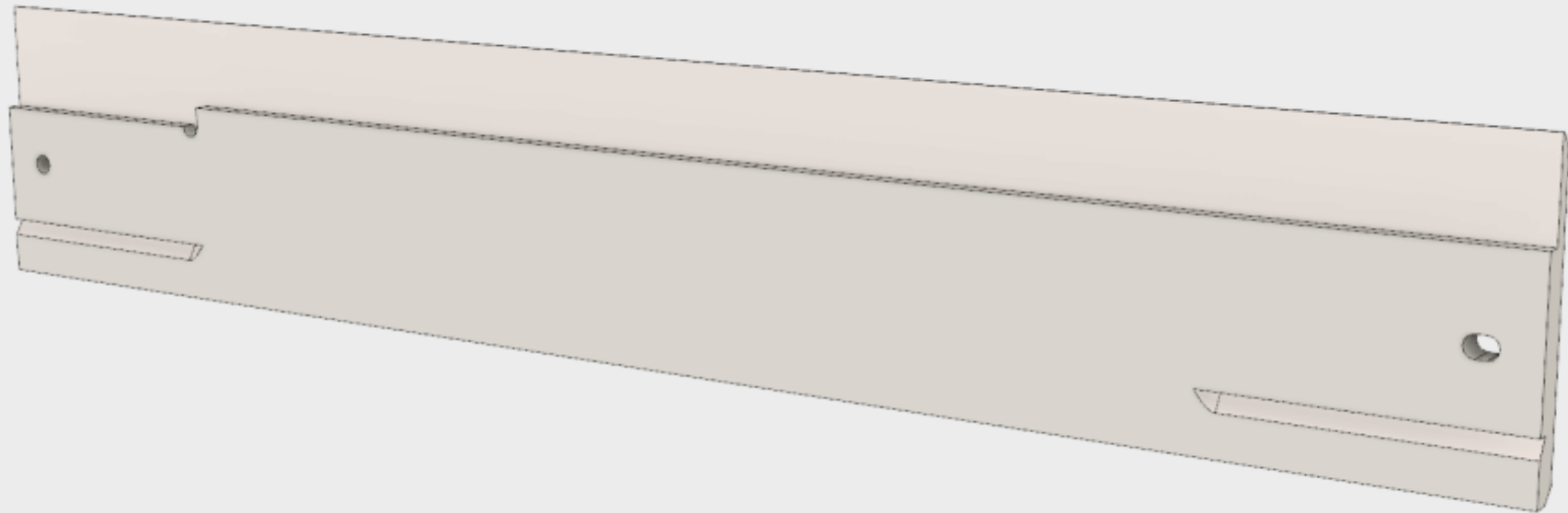
- Convert single ended HitOr to differential

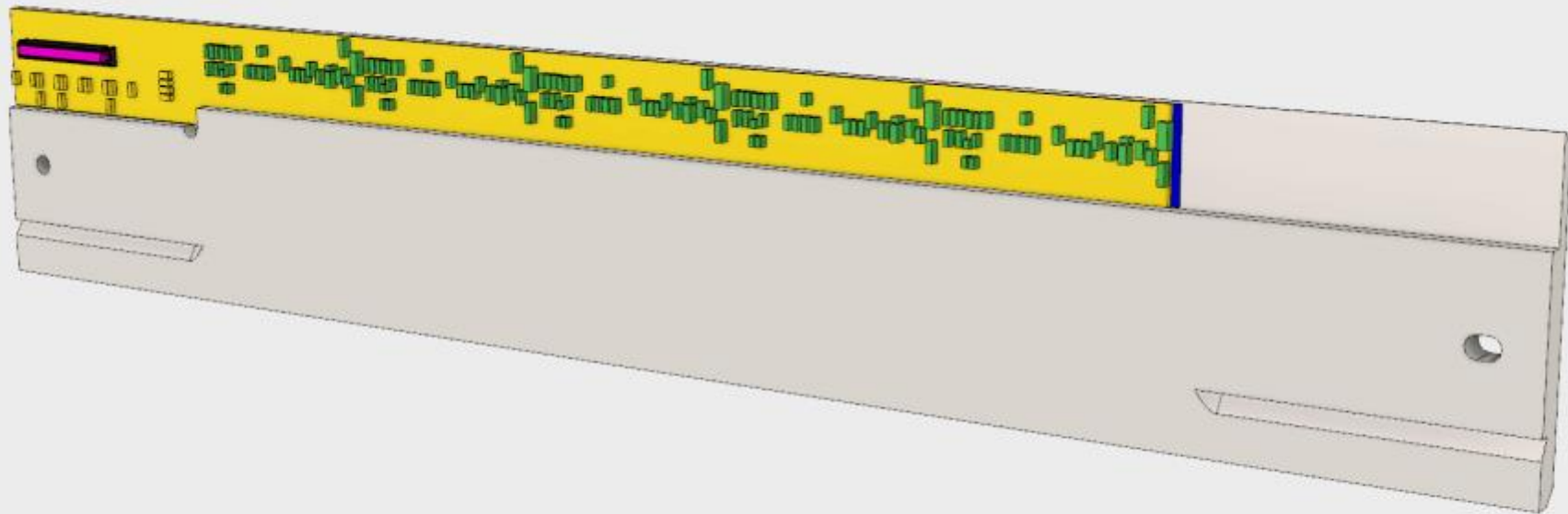
- Propagation delay of HitOr over a 19 m CAT 7
- Signal integrity maintained with delay of  $\sim 60$  ns
- Improvement pulse shape under investigation

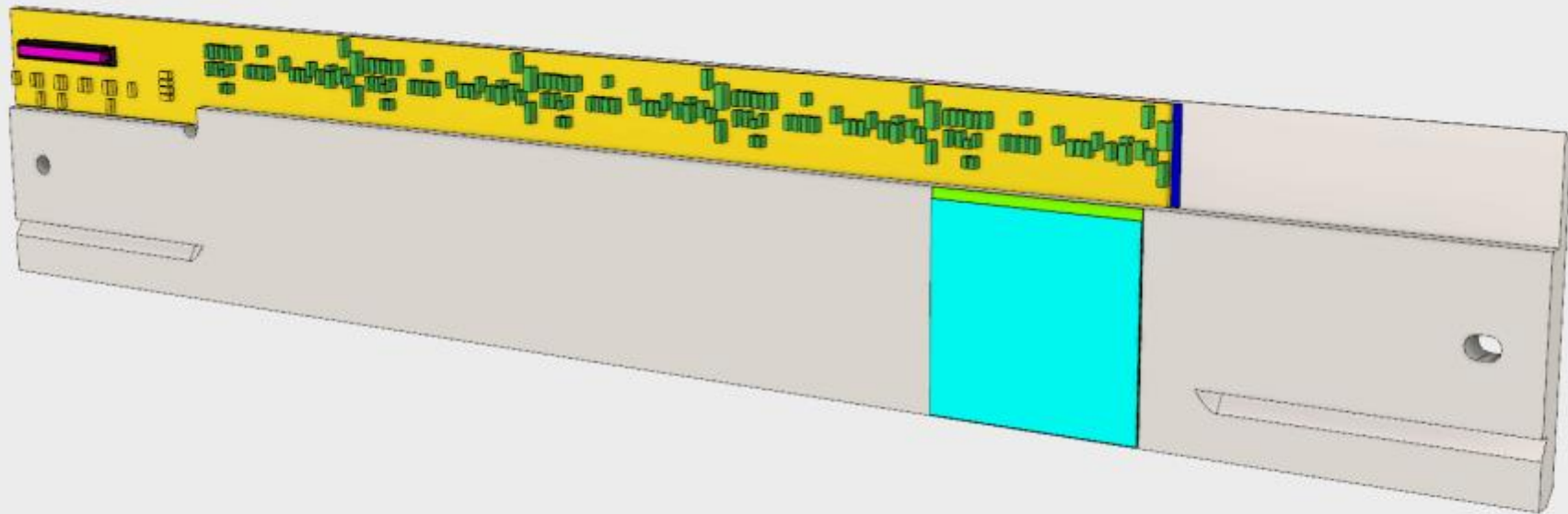


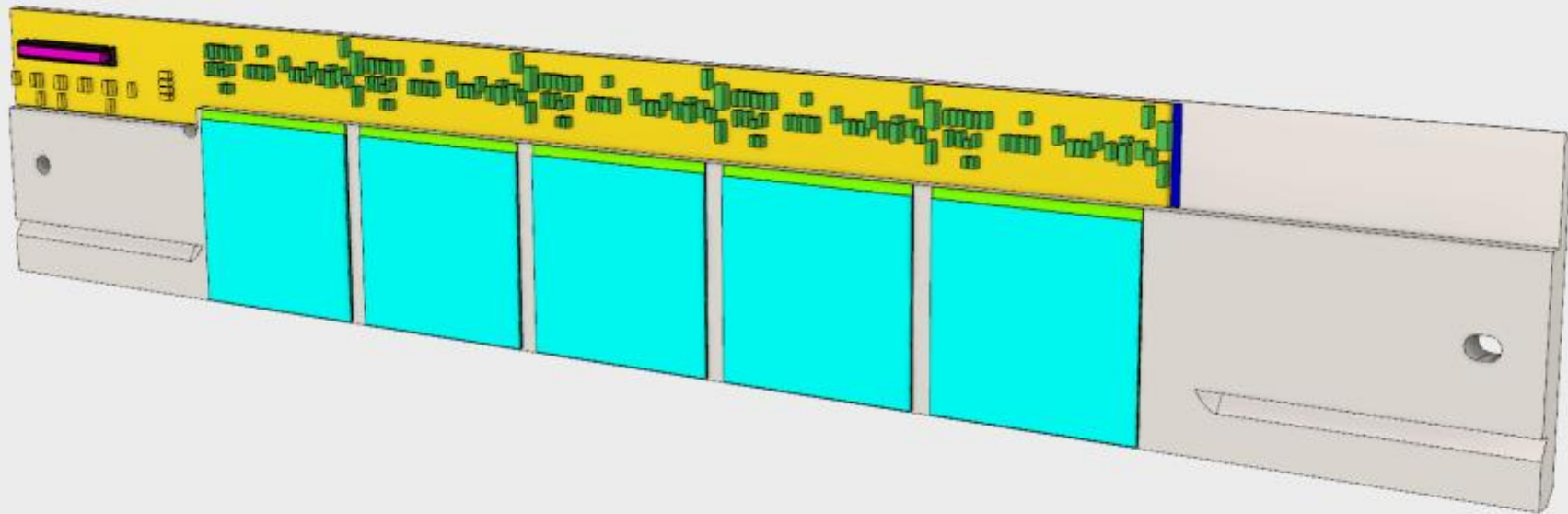


- Signal integrity maintained over 20 m cable
- Proper resolution over this range

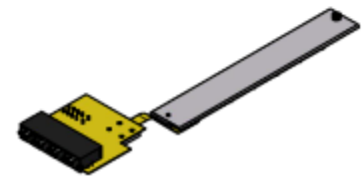
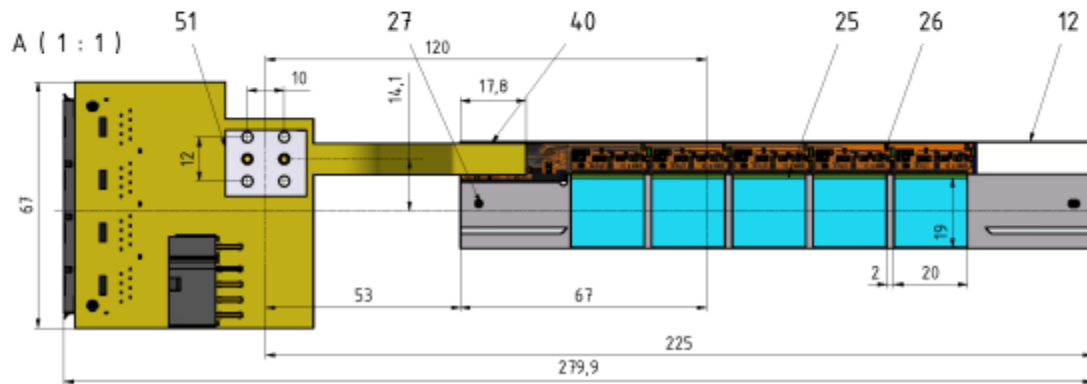
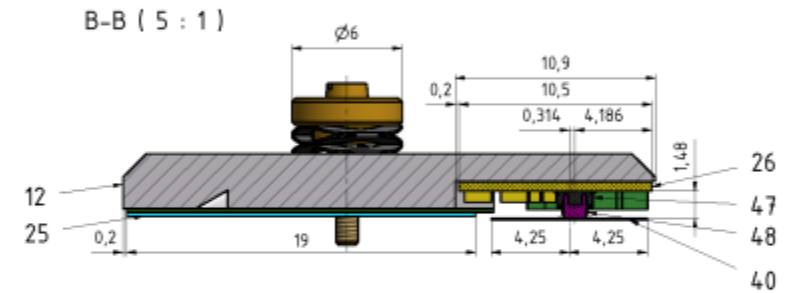
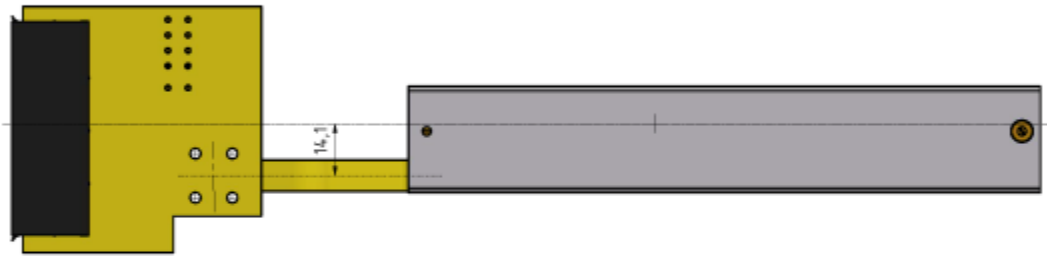
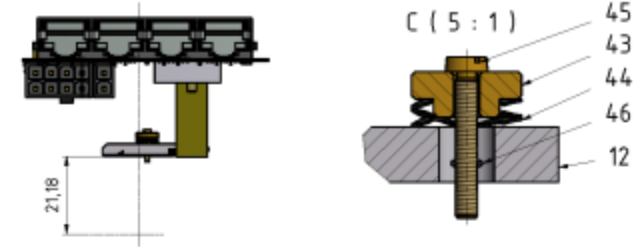
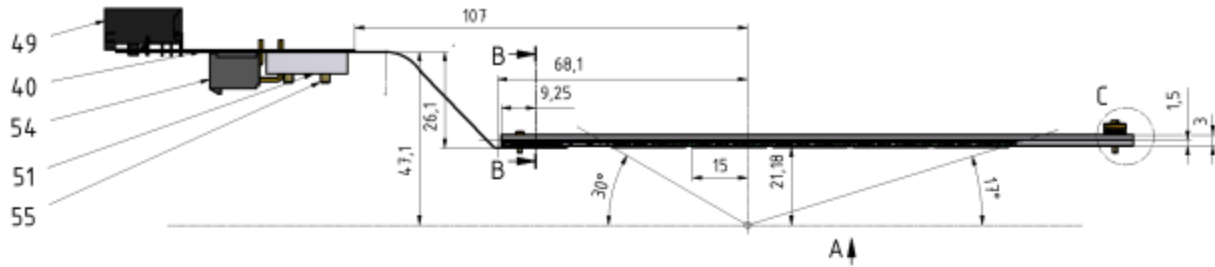




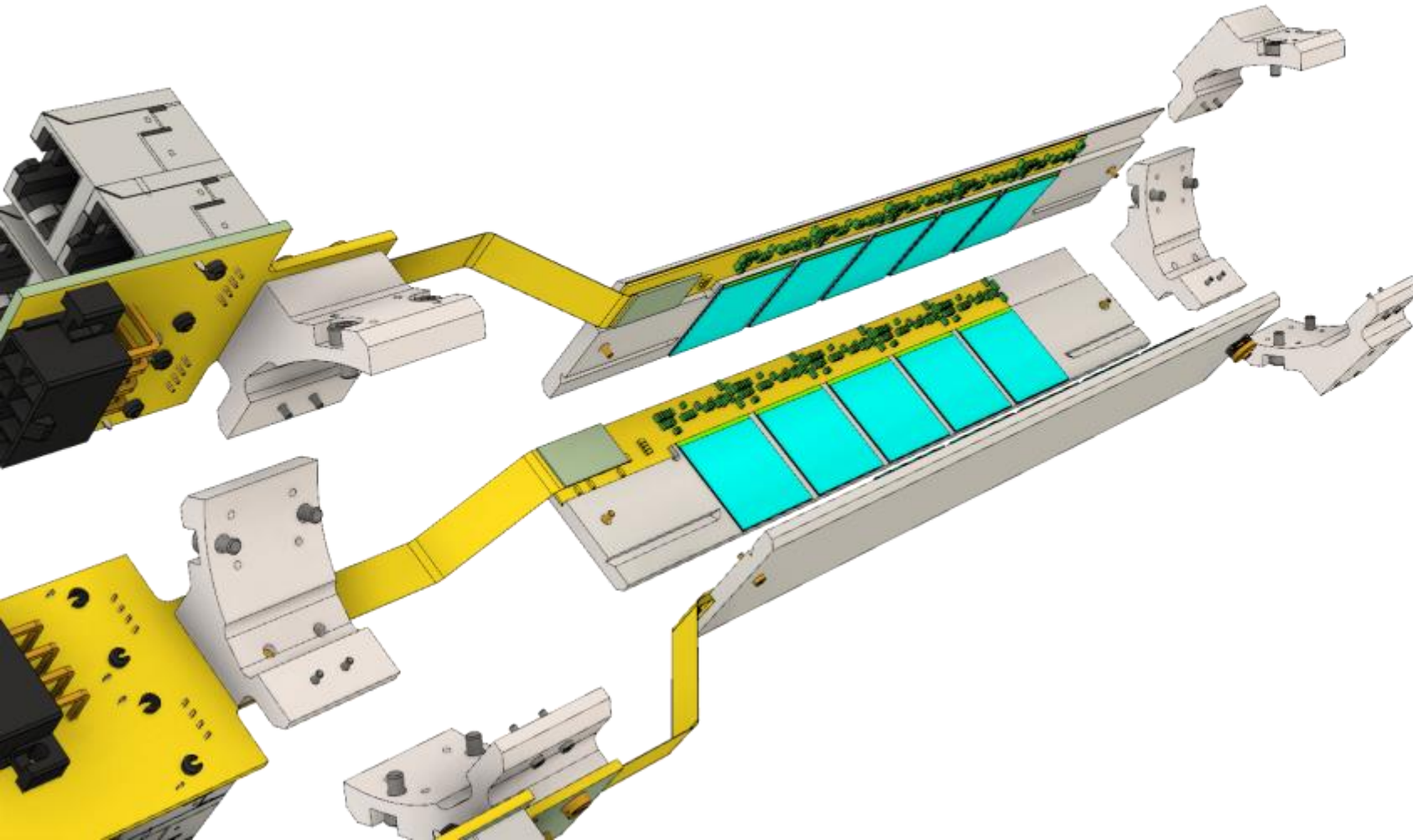




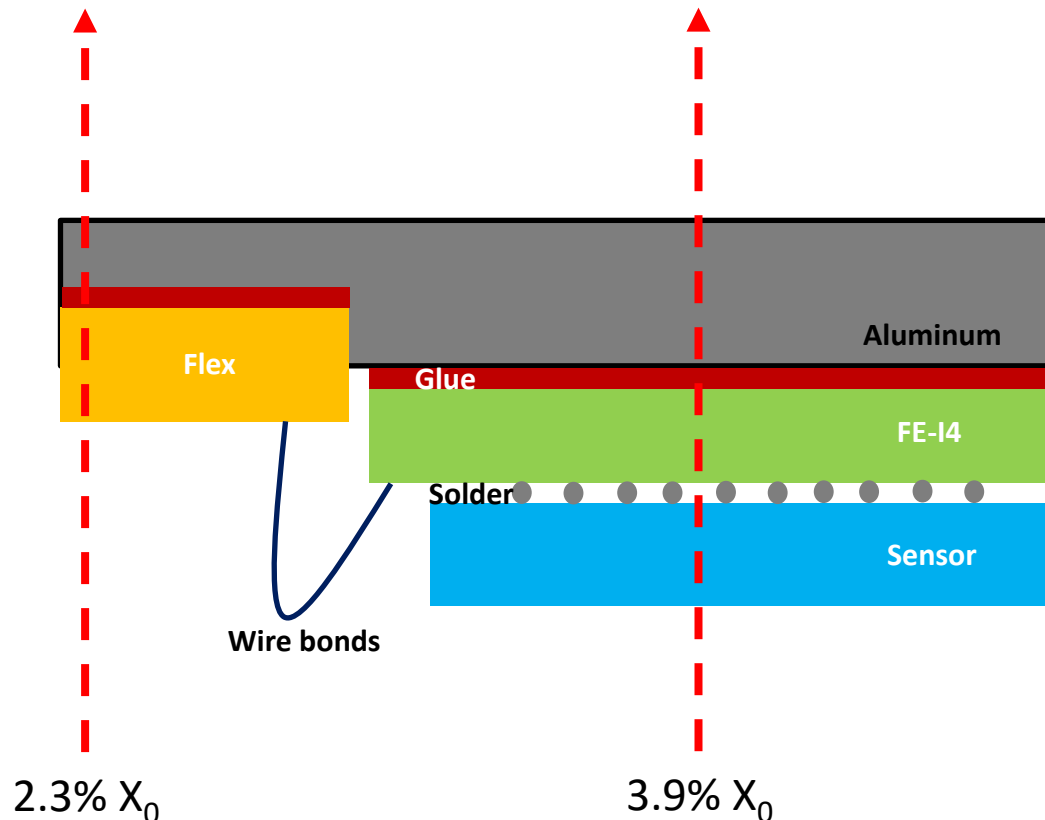
# FANGS Stave Fully Equipped



3 Staves: Covering  $90^\circ$ ,  $180^\circ$ ,  $270^\circ$  in  $\phi$ , *full* acceptance in  $\theta$



# Aluminum Stave Material Budget

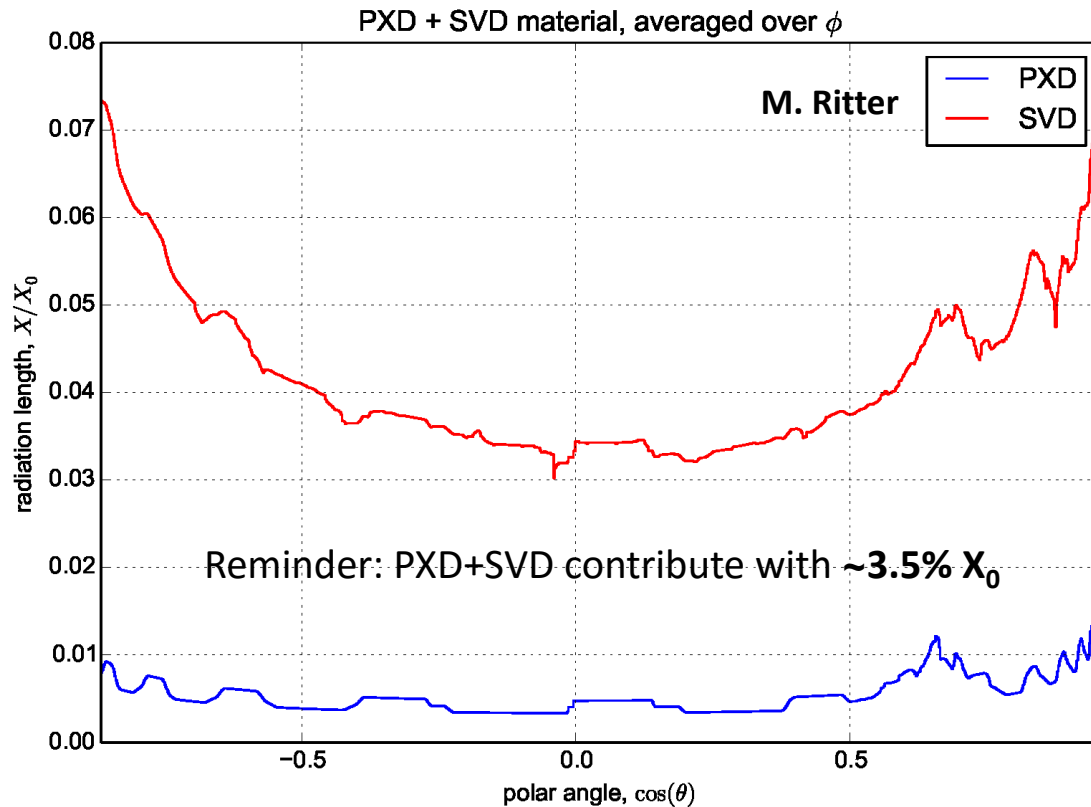


- Low and flat material budget distribution
- No impact in outer detectors
- Further reduction possible if strong physics arguments

- Support:  
3 mm thick Aluminum  $\rightarrow 3.4\%X_0$
- Glue:  
50  $\mu\text{m}$  thick Epoxy  $\rightarrow 0.014\%X_0$
- FE-I4  
150  $\mu\text{m}$  thick Silicon  $\rightarrow 0.16\%X_0$
- Sensor:  
200  $\mu\text{m}$  thick Silicon  $\rightarrow 0.21\%X_0$
- Solder balls  
25  $\mu\text{m}$  thick SnAg  $\rightarrow 0.17\%X_0$  (3.3% of the area)
- Flex  
100  $\mu\text{m}$  thick polyimide  $\rightarrow 0.035\%X_0$   
70  $\mu\text{m}$  Cu (2 layers)  $\rightarrow 0.50\%X_0$   
50  $\mu\text{m}$  thick Epoxy  $\rightarrow 0.014\%X_0$

Total<sub>Max</sub>:  $3.9\% X_0$

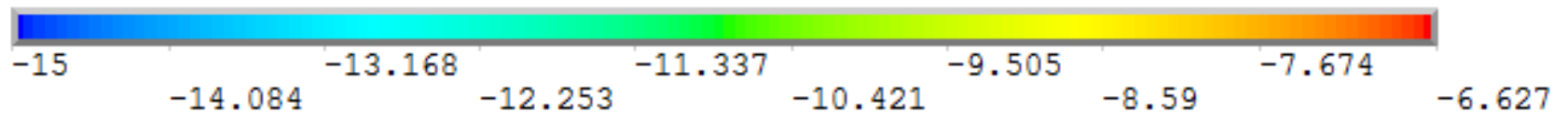
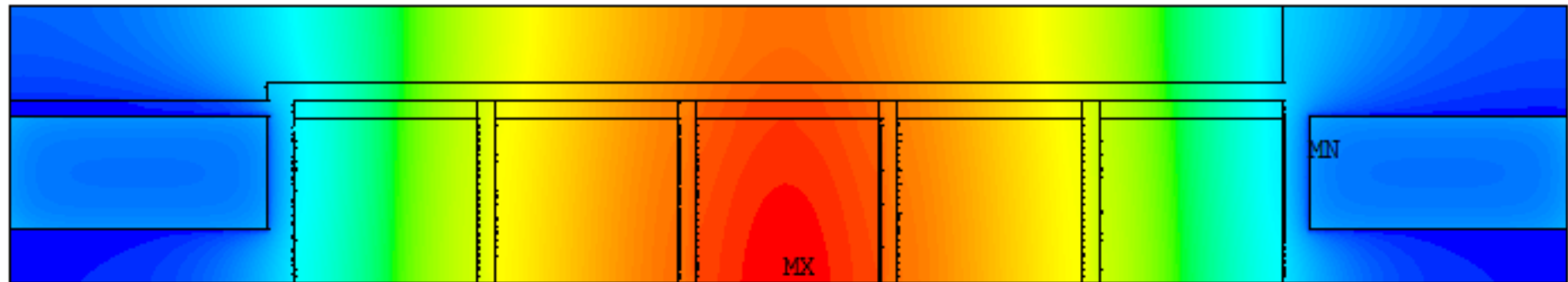




- Low and flat material budget distribution
- No impact in outer detectors

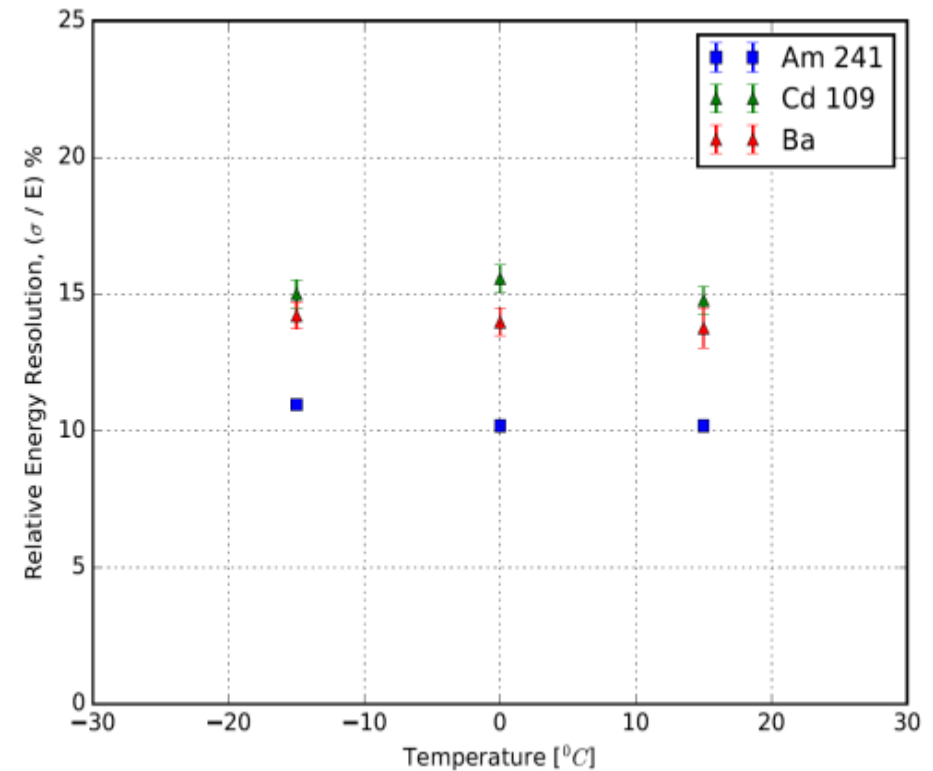
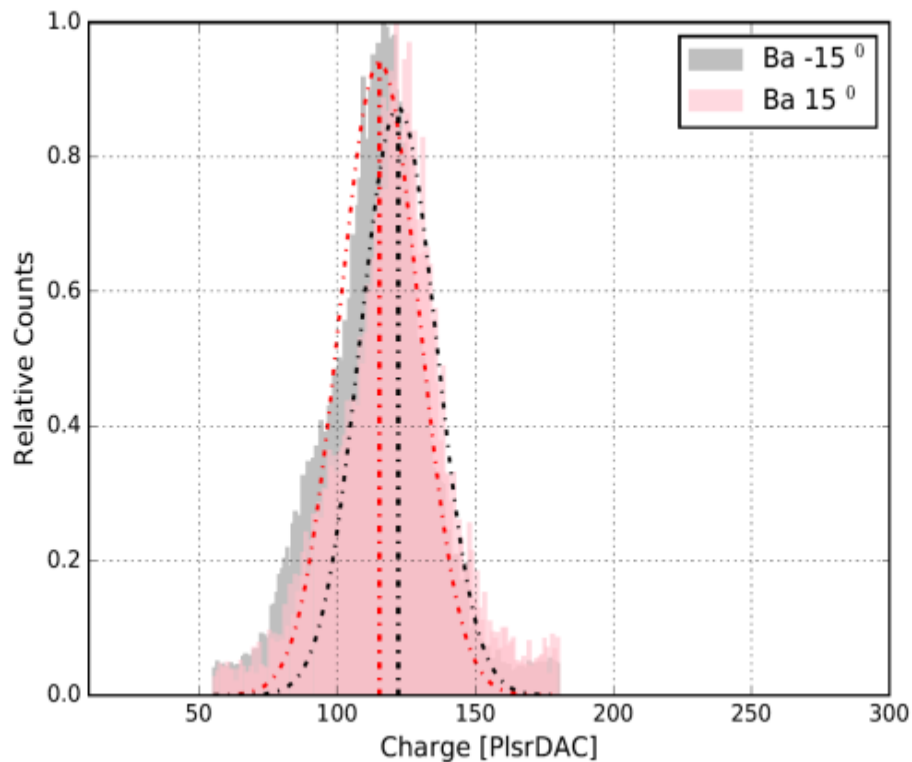
- Support:  
3 mm thick Aluminum  $\rightarrow 3.4\% X_0$
- Glue:  
50  $\mu\text{m}$  thick Epoxy  $\rightarrow 0.014\% X_0$
- FE-I4  
150  $\mu\text{m}$  thick Silicon  $\rightarrow 0.16\% X_0$
- Sensor:  
200  $\mu\text{m}$  thick Silicon  $\rightarrow 0.21\% X_0$
- Solder balls  
25  $\mu\text{m}$  thick SnAg  $\rightarrow 0.17\% X_0$  (3.3% of the area)
- Flex  
66  $\mu\text{m}$  thick polyimide  $\rightarrow 0.023\% X_0$   
24  $\mu\text{m}$  Cu (2 layers)  $\rightarrow 0.17\% X_0$

Total<sub>Max</sub>: 3.9%  $X_0$



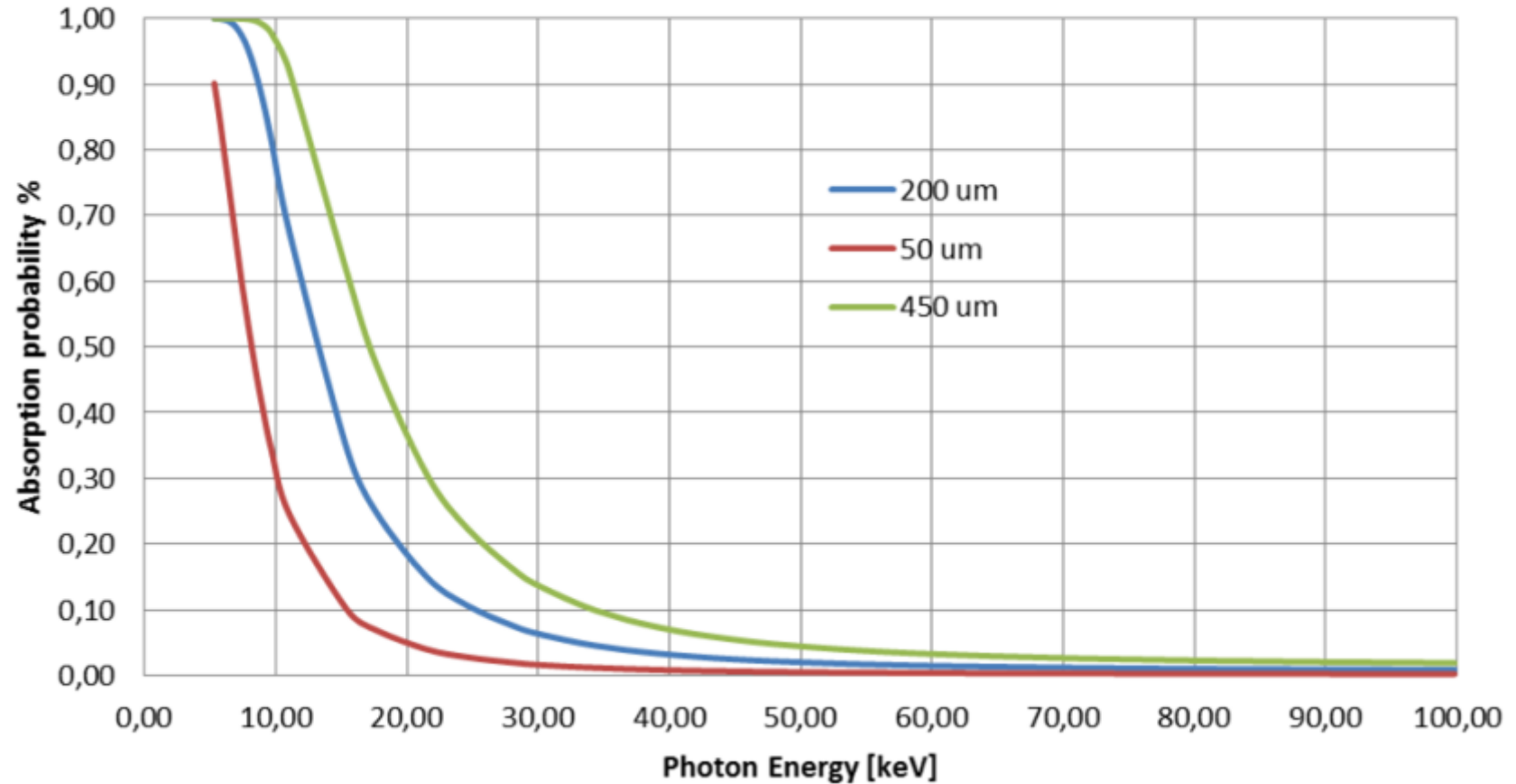
FANGS for BEAST, C. Marinas (University of Bonn)

- Maximum temperature = -7 °C
- Maximum  $\Delta T$  within one sensor = 5 °C
- Power = 1.2 W each FE
- Cooling block = -15 °C
- Environment = 20 °C at 2 m/s
- Proper heat handling
- Low and flat temperature profile

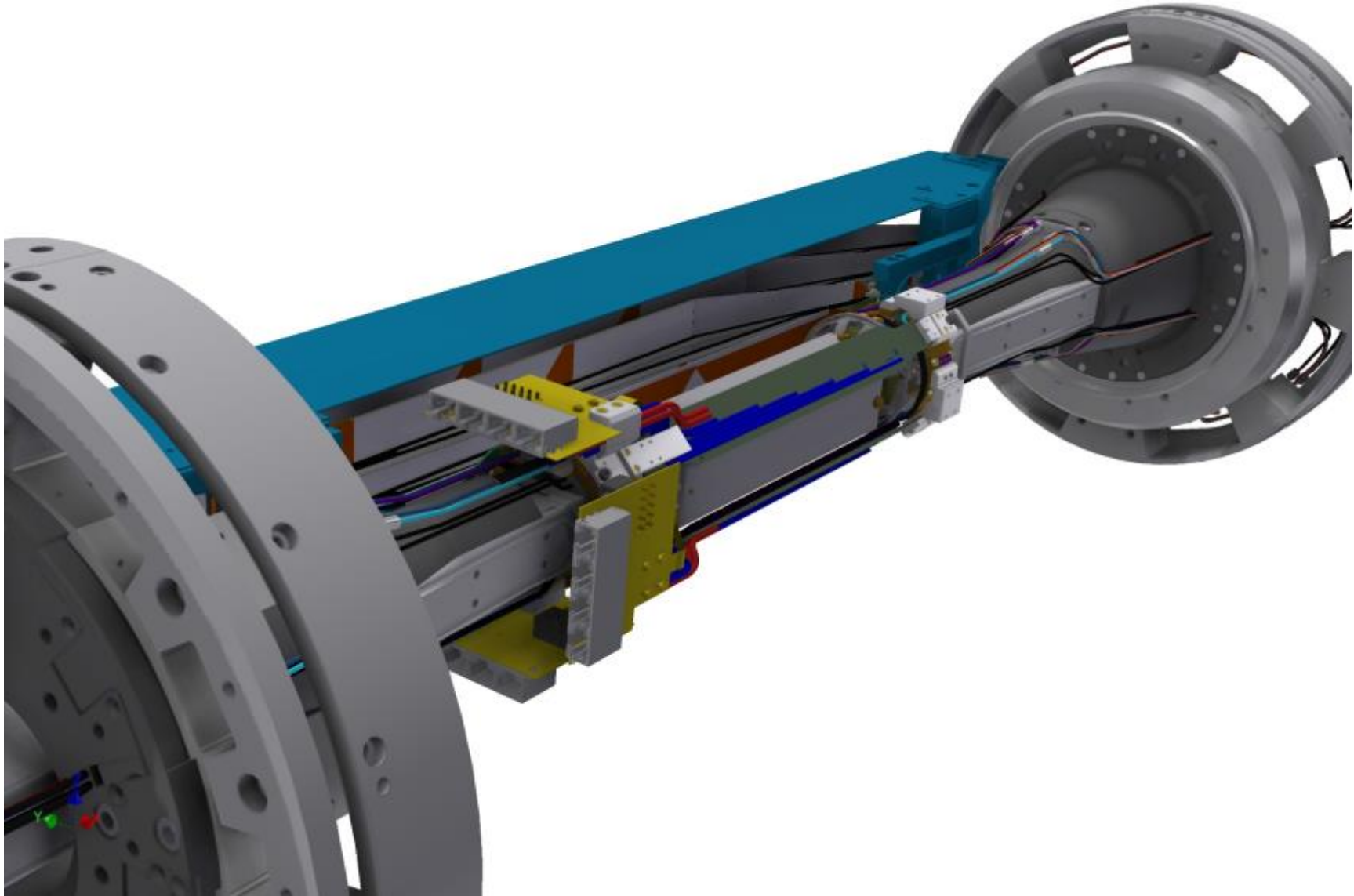


- No performance degradation is observed over the expected temperature range

## Absorption in Silicon



# Phase 2 Set Up



- Front end has been tuned to cover the expected energy range with sufficient **resolution** for Beast Phase 2
  - **Multiple-FE DAQ** demonstrated
  - **20 m long cables** tested
  - Finalized design of Kapton flex and intermediate boards.
  - **Mechanical** concept and **cooling** management are finalized
  - Mass production will follow. FANGS to be ready by the end of the year for integration
- NEXT:**
- Radiation hardness flex electrical components
  - More realistic environment

# Thank you

