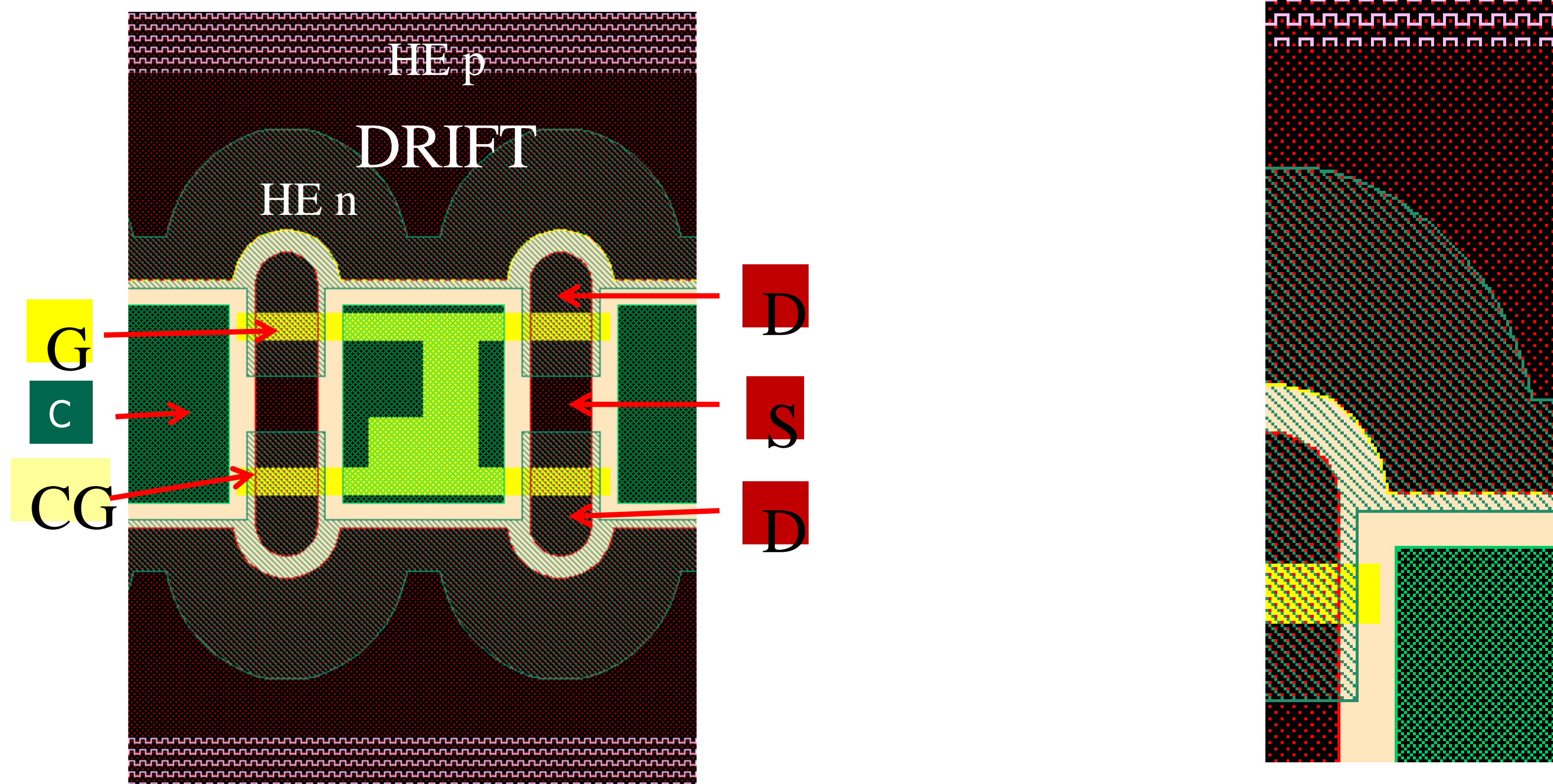
Charge collection of PXD9 Depfets

Charge loss mechanisms
Ring pattern
Operation windows
Recommendations

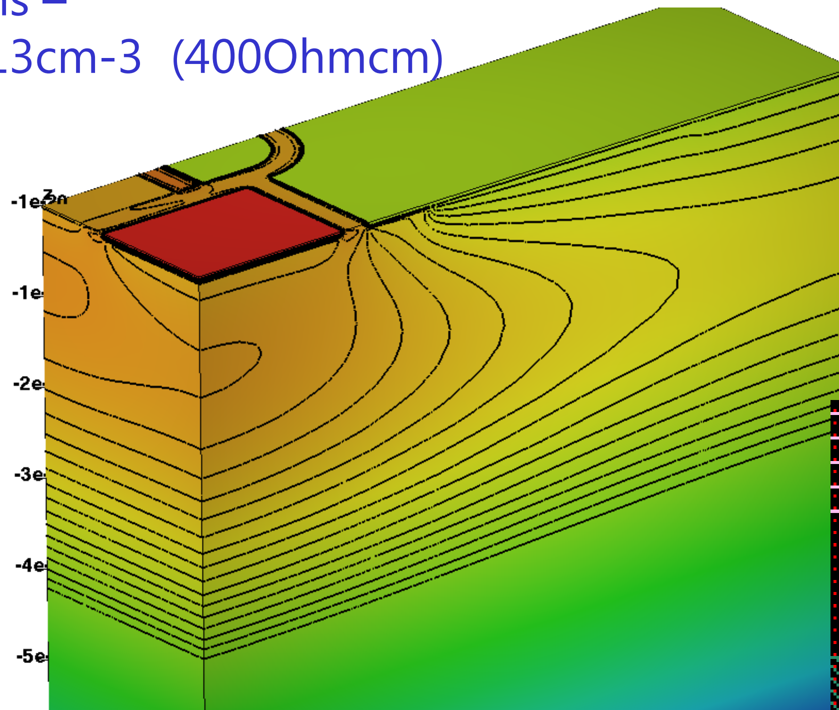
Charge loss mechanisms vs bias voltages

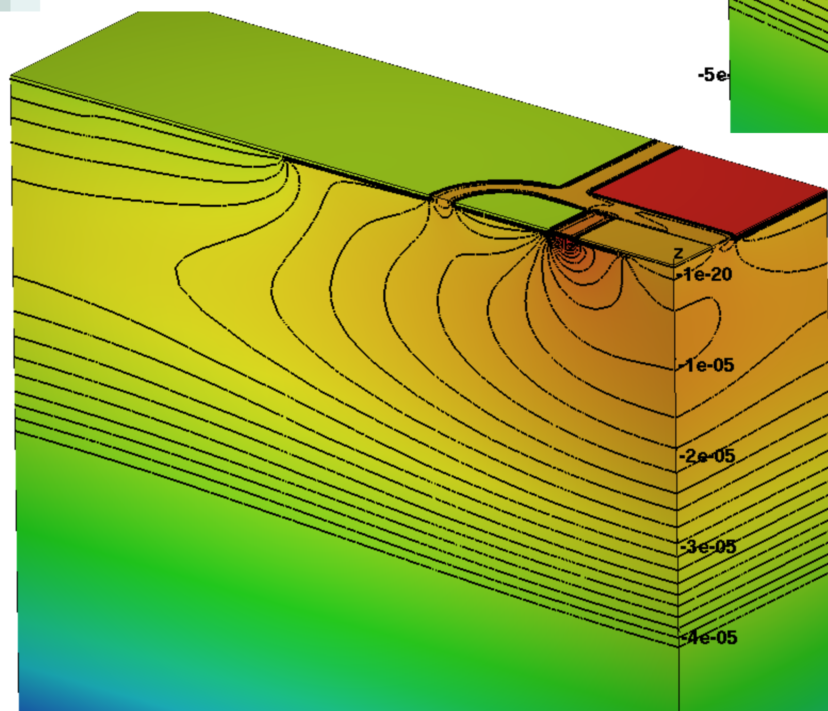
A reminder: layout outer module large pixels – 85µm x 50µm (4 pixels)

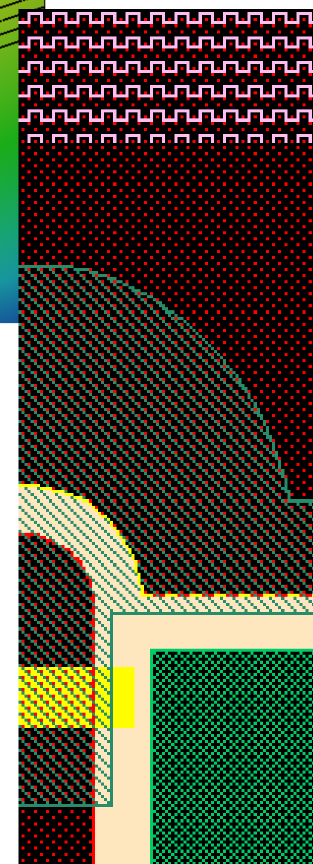


Testbeam bias conditions – Normal bulk doping 1e13cm-3 (400Ohmcm)

Drain -5V
Drift -5V
Clear 5V
ClearGate -0.5V
Back -30V

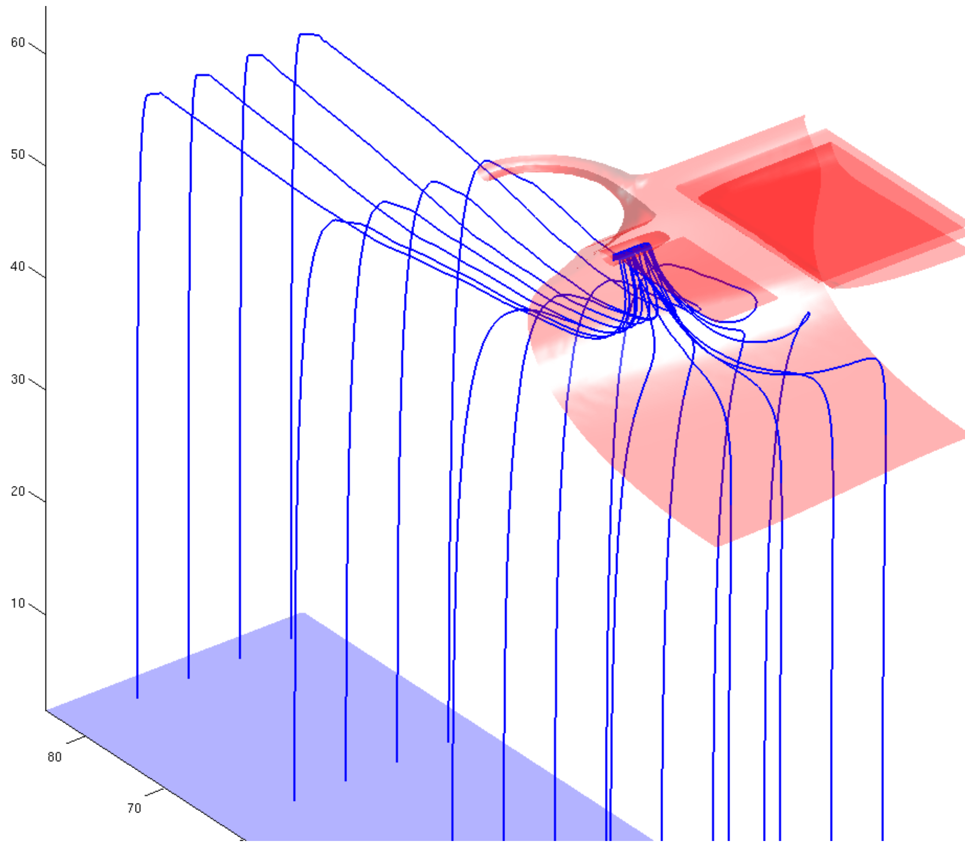


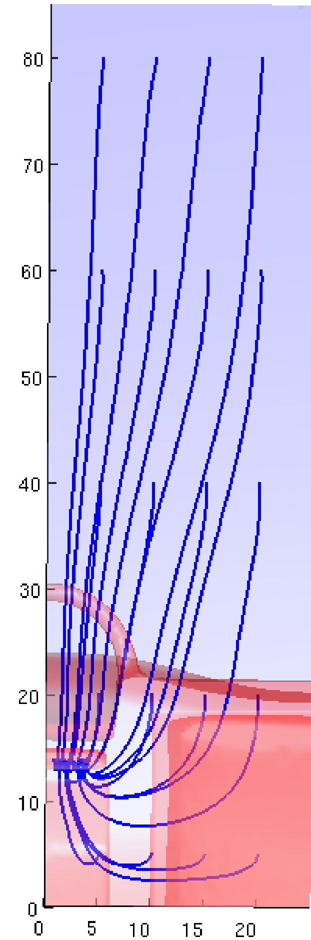




Simulator : Oskar3
(Klaus Gärtner)

Test beam bias conditions - normal bulk doping





Very nice !

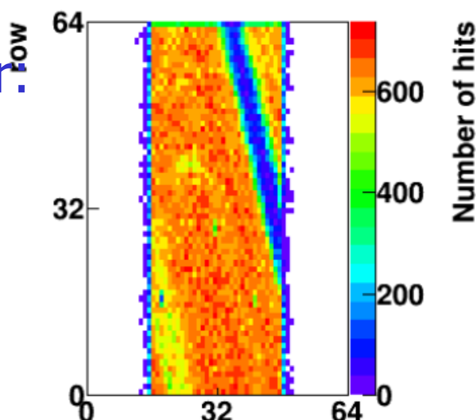
But we see strips in the charge collection

Small testbeam sensor:
(see Benjamins talk)

Strips change their behavior:

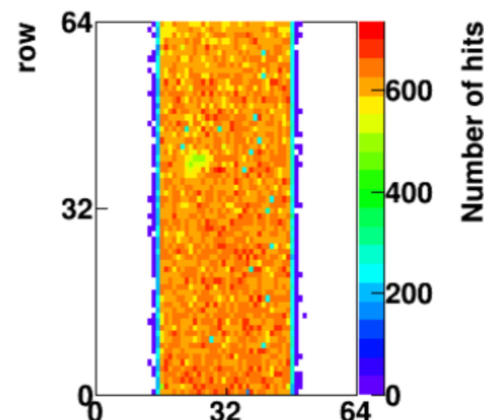
Dead strips at low HV show
best charge collection
on very high HV
and vice versa

HV 60V / Drift 5V



HV 70V / Drift 5V

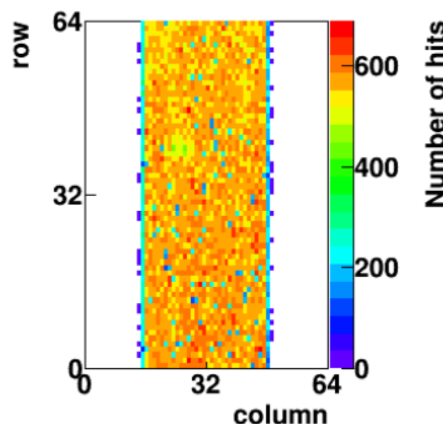
(best)



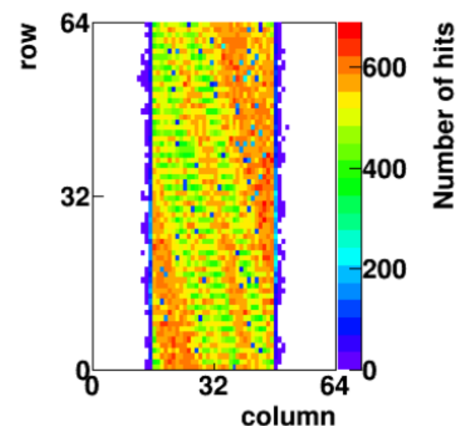
Strips are inclined:
cannot be assigned, neither to
columns nor to rows

Must be a sensor property

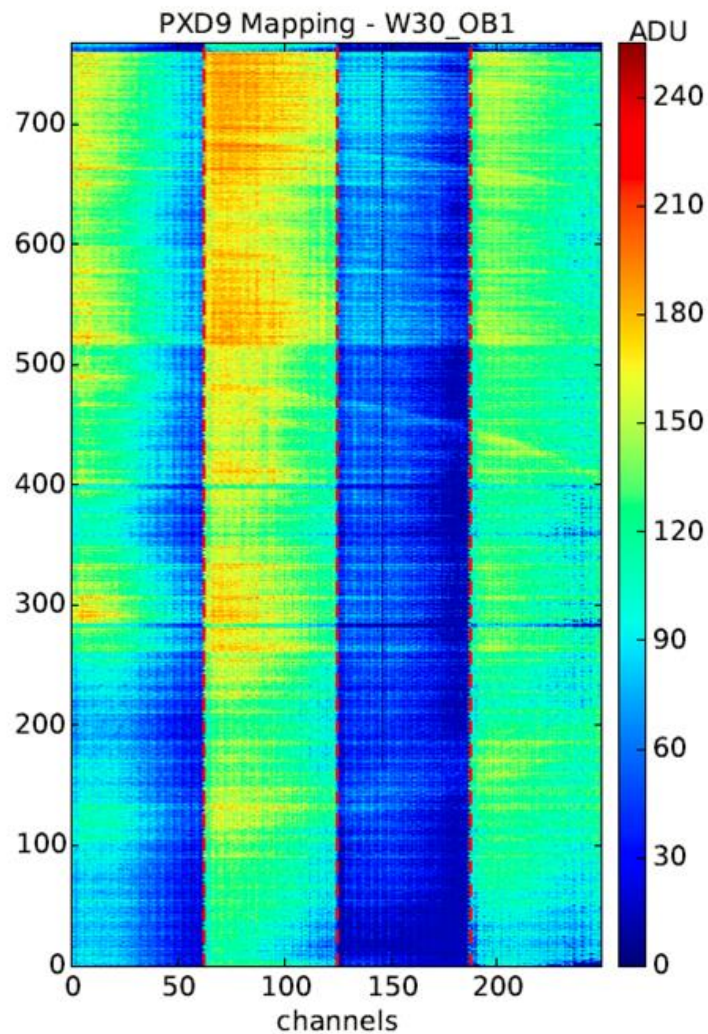
HV 75V / Drift -5V



HV 80V / Drift 5V



Pedestal Map



measured by Christian and Felix

Possible reason ?

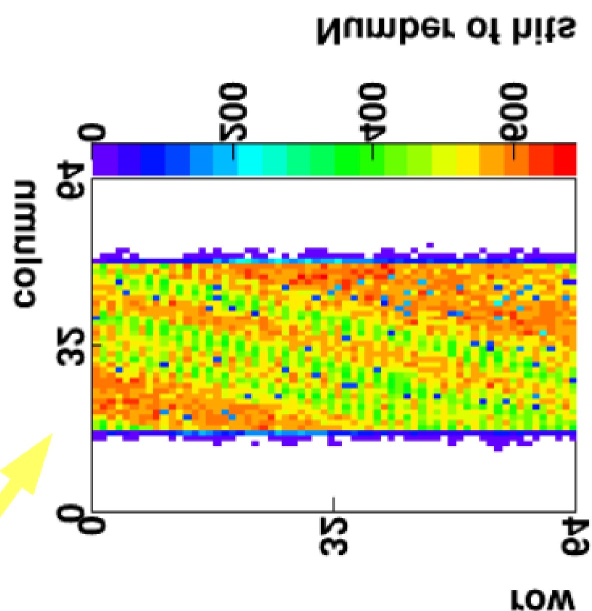
Only explanation (up to now) :

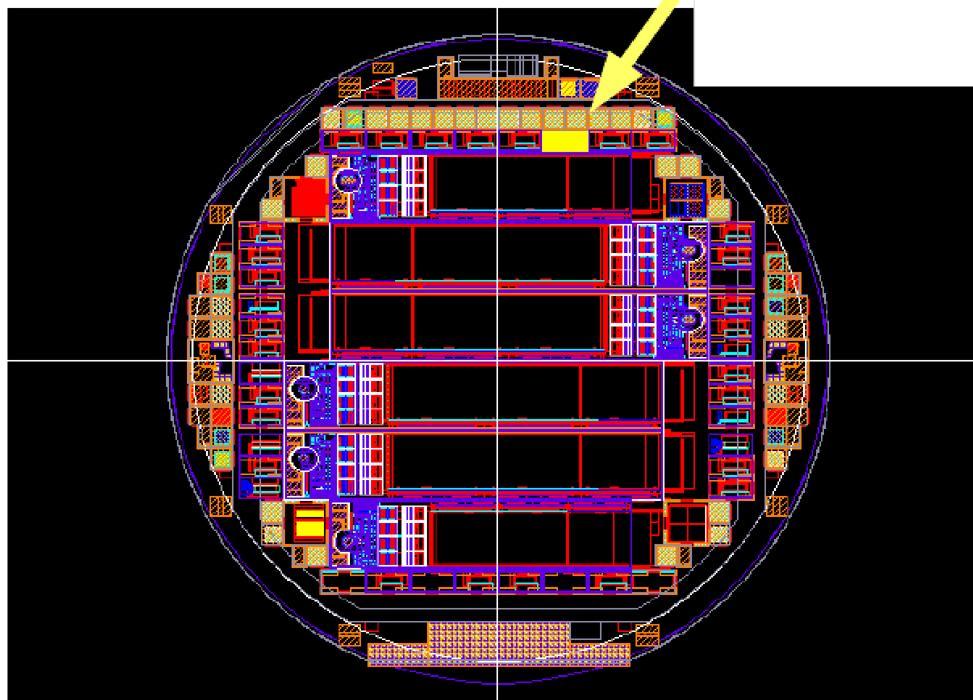
variations in the bulk doping

Any kind of damage due to polishing, etching or other rotating procedures cannot be repaired by just another backside voltage !

Must be strong and on a short lateral scale

What is the origin?





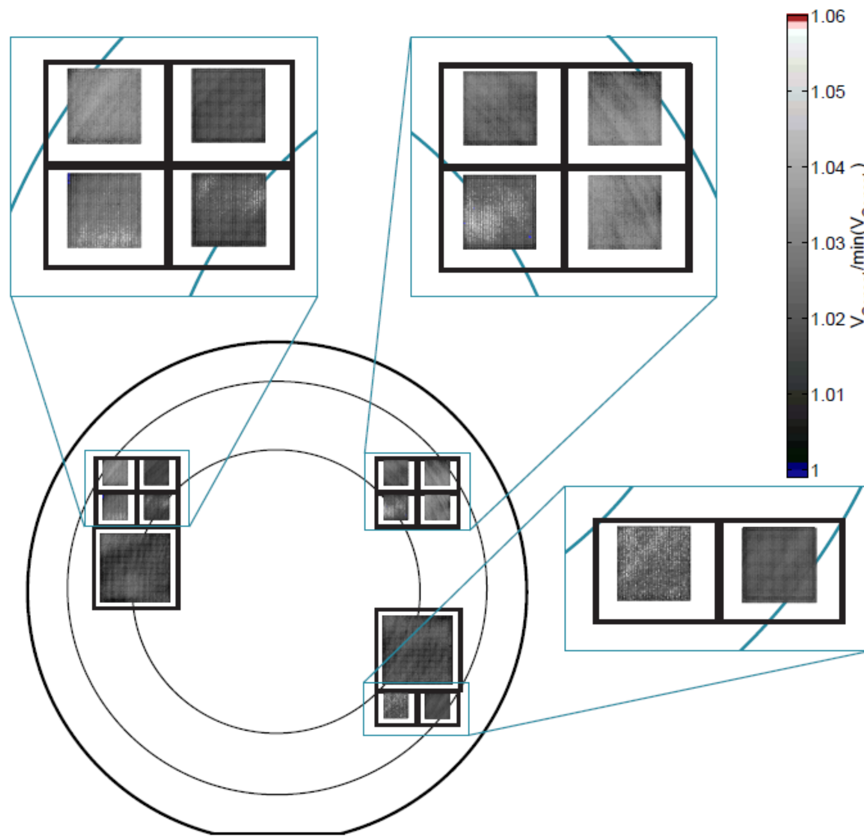
Chip number: PXD9-6 W30 A05

:- Idea: variation of bulk doping in concentric rings around wafer center

:- yellow area on wafer: tb sensor

:- hit occupancy mirrored to match orientation of chip on wafer.

Already observed on DEPFETs produced for the Bepi Colombo mission



Variations of the clear behavior

No quantitative conclusions

about the degree of doping variations

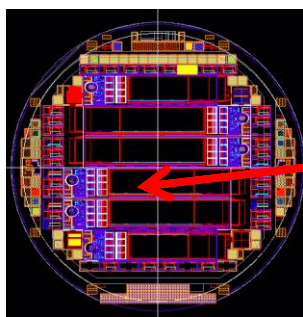
But also concentric

PhD: Bettina Bergbauer

Figure 3.3.29.: Maps of the onset voltage of the clear V_{Conset} for two MIXS macropixel matrices and the surrounding 10 IS prototypes with respect to their position on the wafer 35. V_{Conset} is normalized to the minimum value for every die. A concentric structure is visible due to the resistivity variation of the high ohmic float zone silicon wafer material [9].

with some phantasy ....

wafer center



OB1

What can we do?

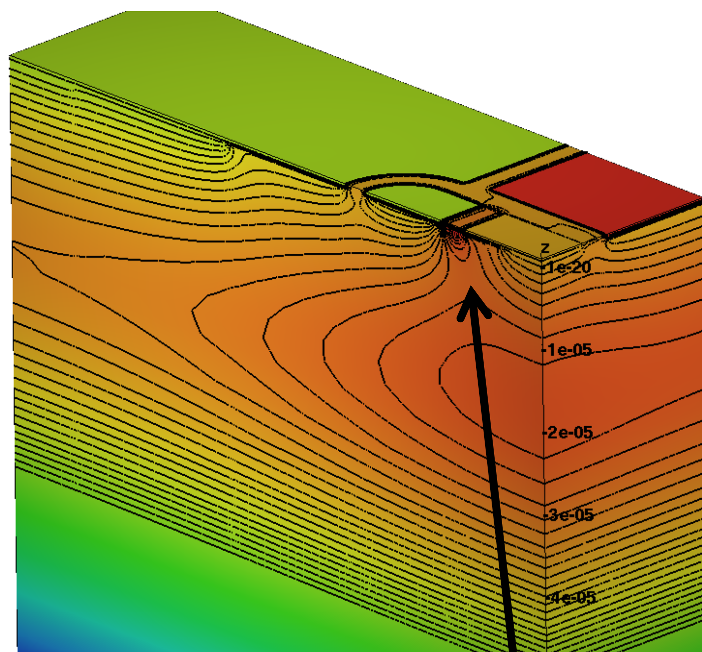
Either we throw the data coming from the ring regions away

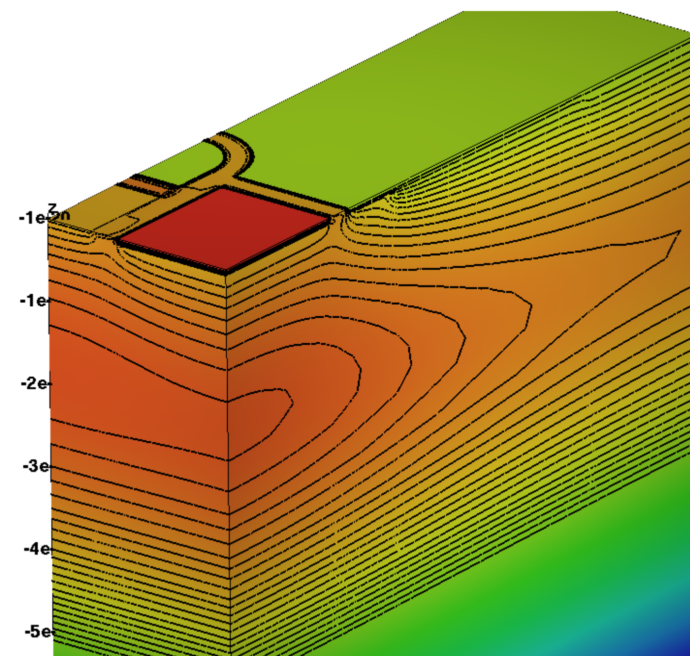
or we try to get all regions running

with an adapted bias parameter set

If we increase the bulk doping by 50% - 1.5e13cm-3

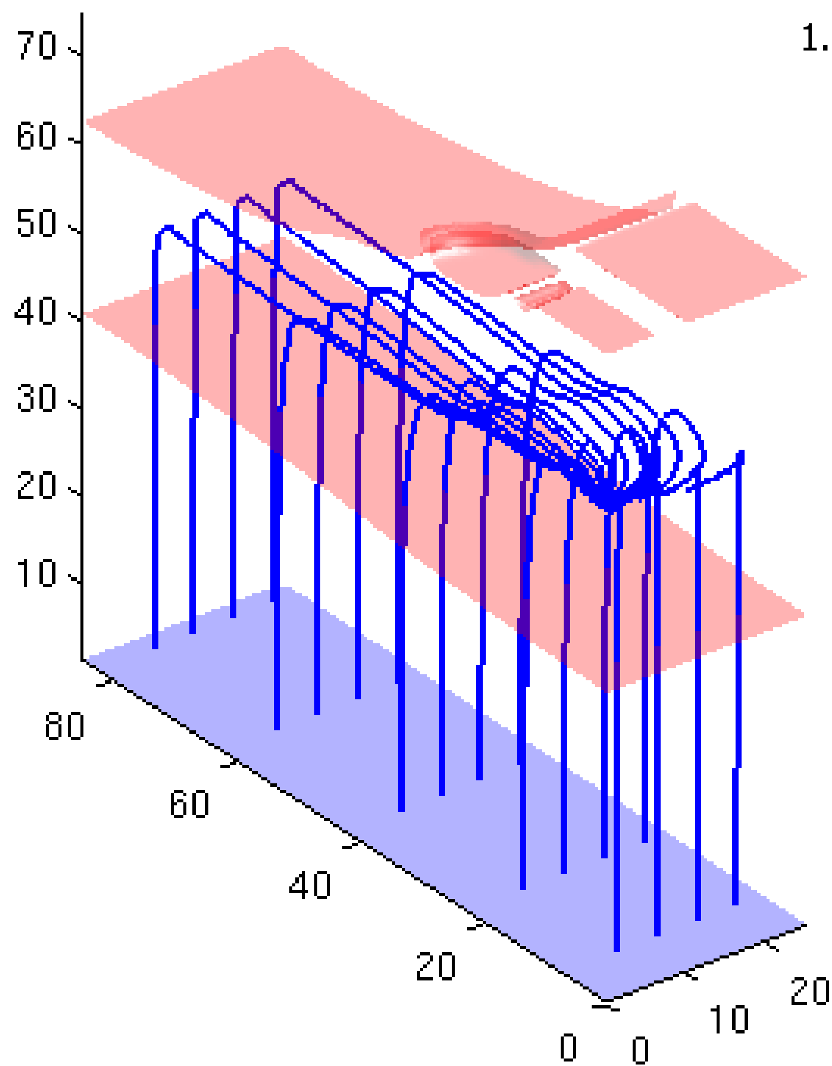
Testbeam bias conditions
Drain -5V
Drift -5V
Clear 5V
ClearGate -0.5V
Back -30V





Saddle point pinchs off the Internal Gate

No charge collection possible



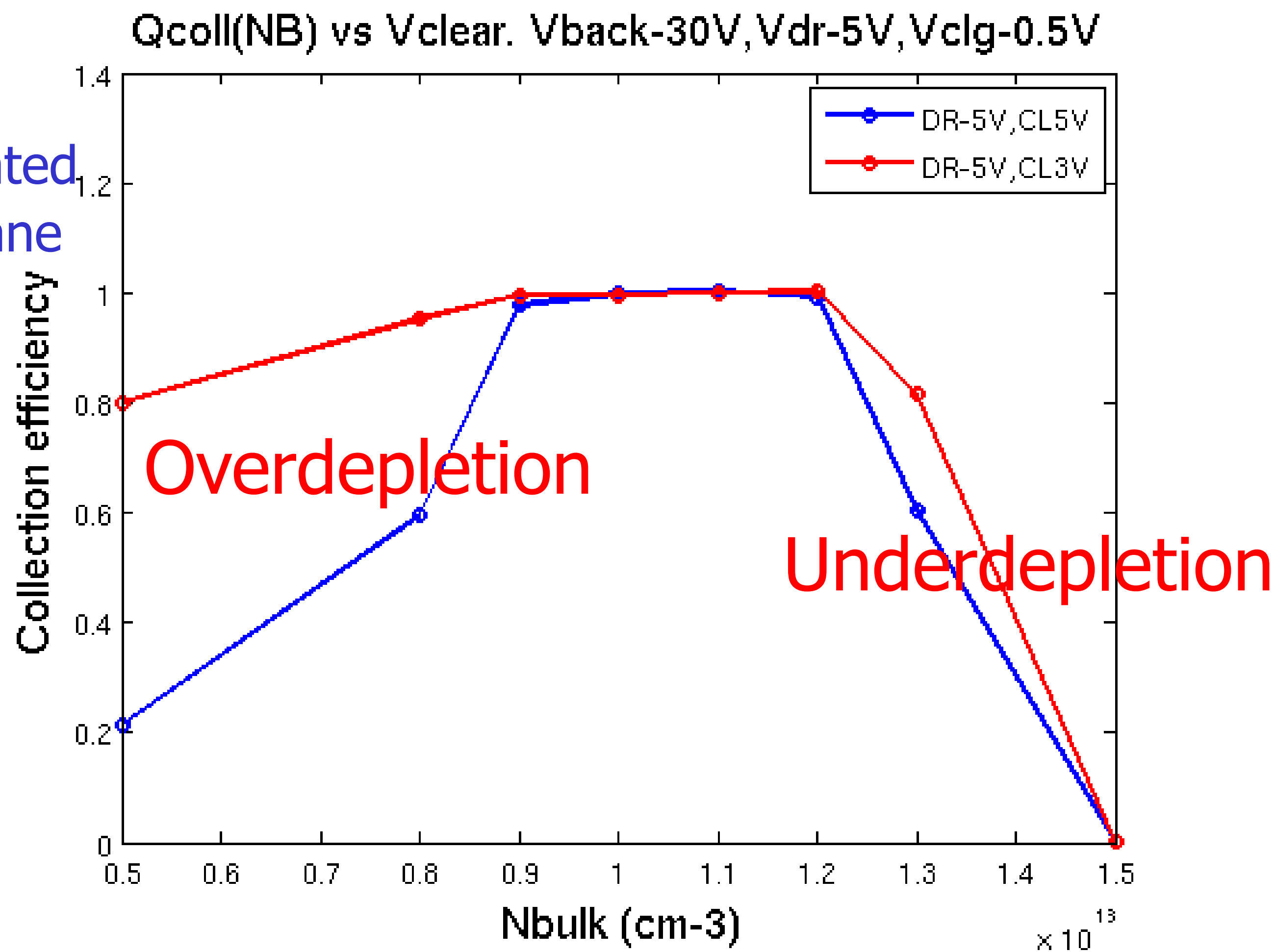
1. charge loss mechanism

under depletion

Charge collected in the Internal Gate

Test charge generation
10k electron/hole pairs

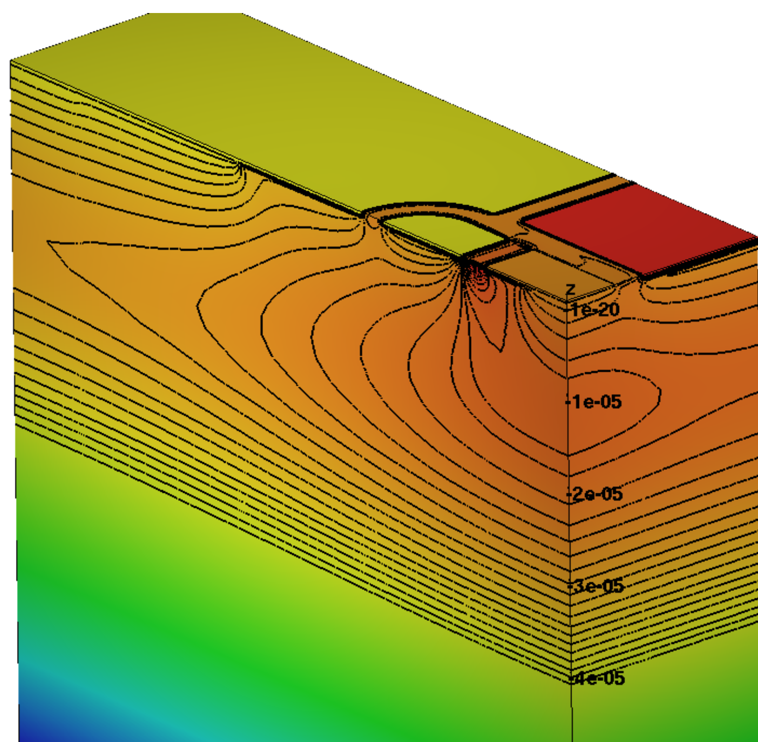
homogeneously generated
2µm above the backplane

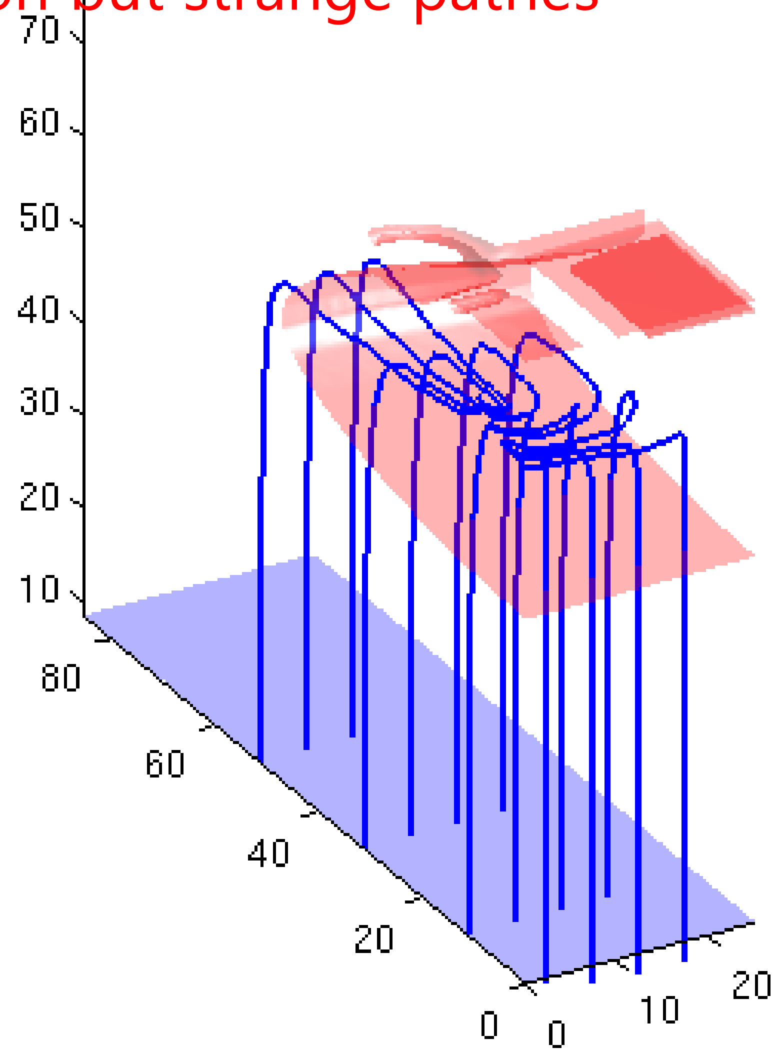


Nbulk 1.5e13cm-3: Can the charge lost be repaired ?

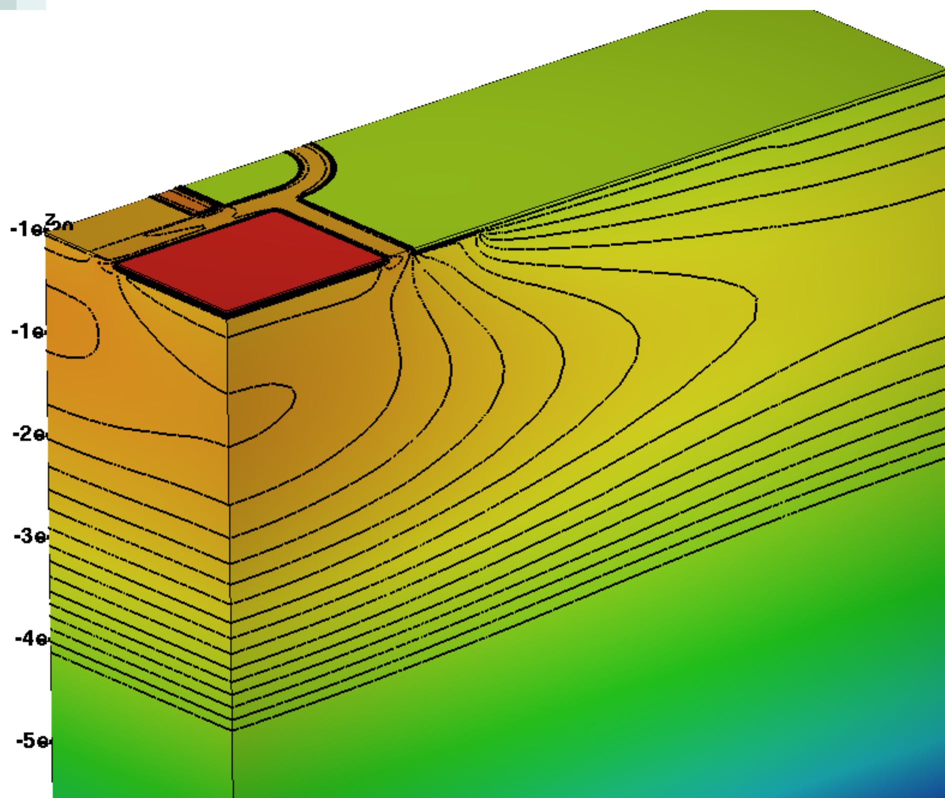
Decrease Vback down to-39V

-> good charge collection but strange pathes

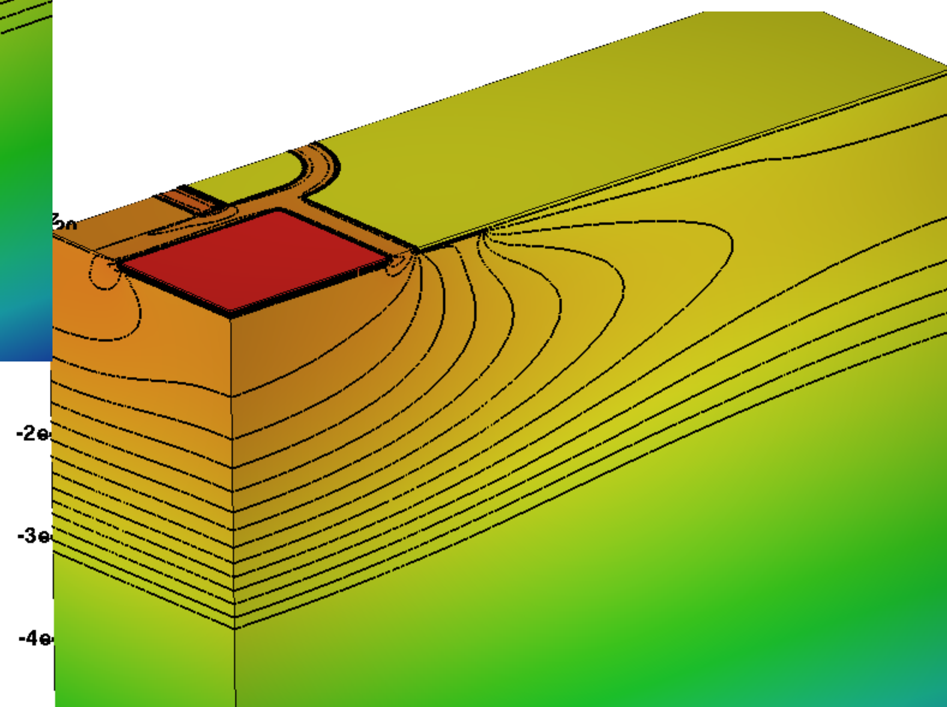




But what happens to the normal doped pixels

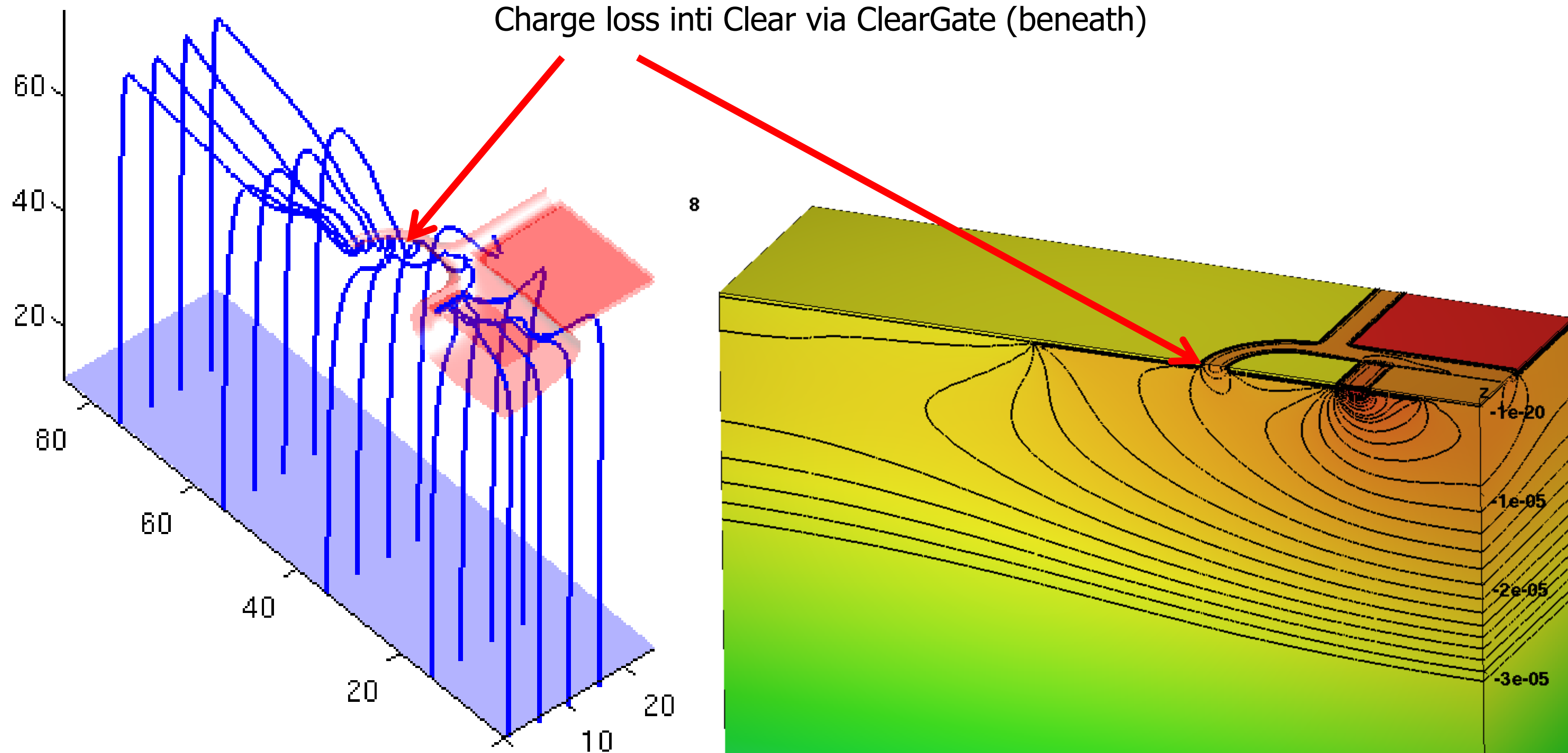


Vback=-39V



Vback=-30V

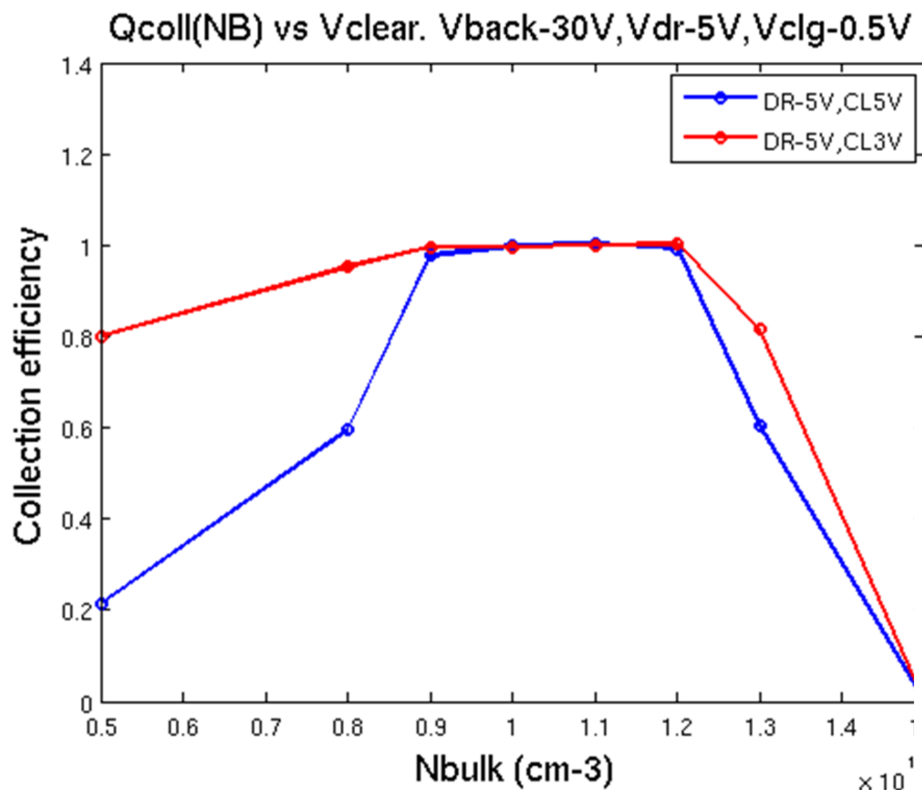
Normal bulk doping at Vnack=-39V



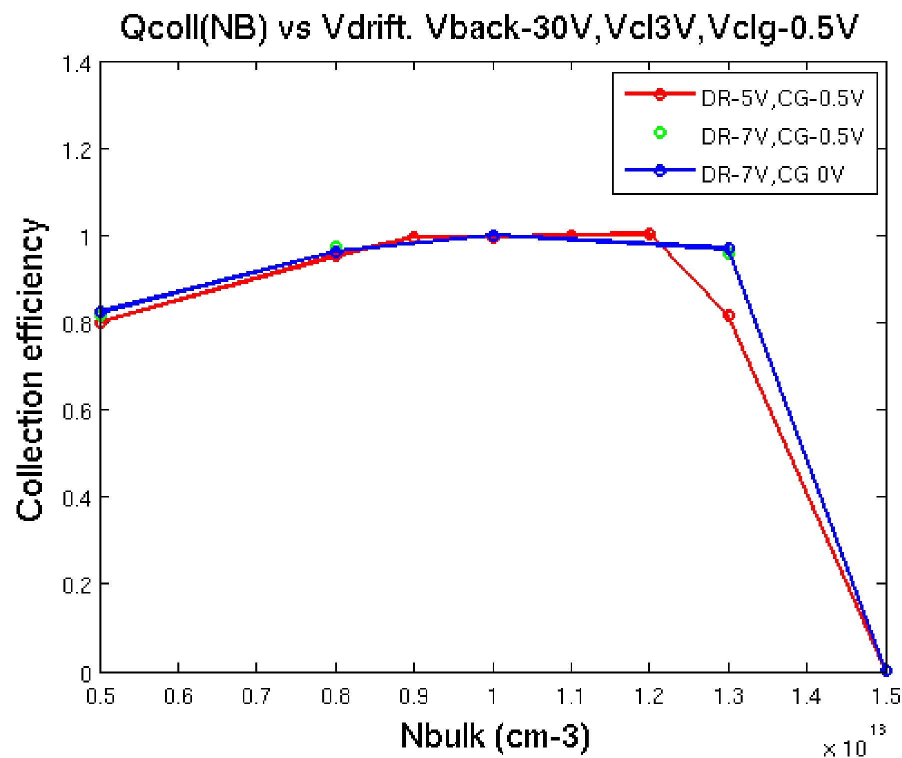
Conclusion: for the test beam bias voltage set:

A local bulk doping increase of 50% cannot be compensated by a more neg. bias voltage

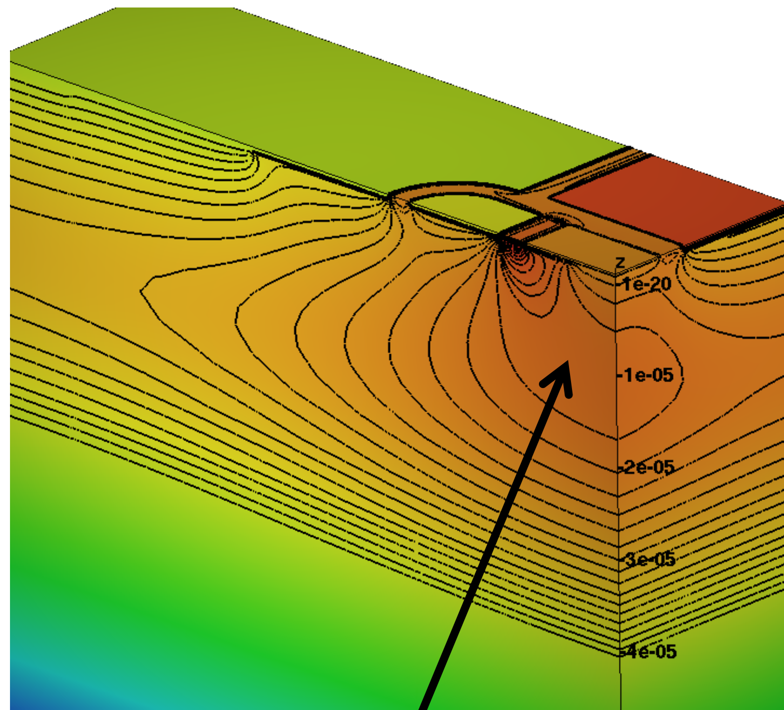
Are there better bias conditions?

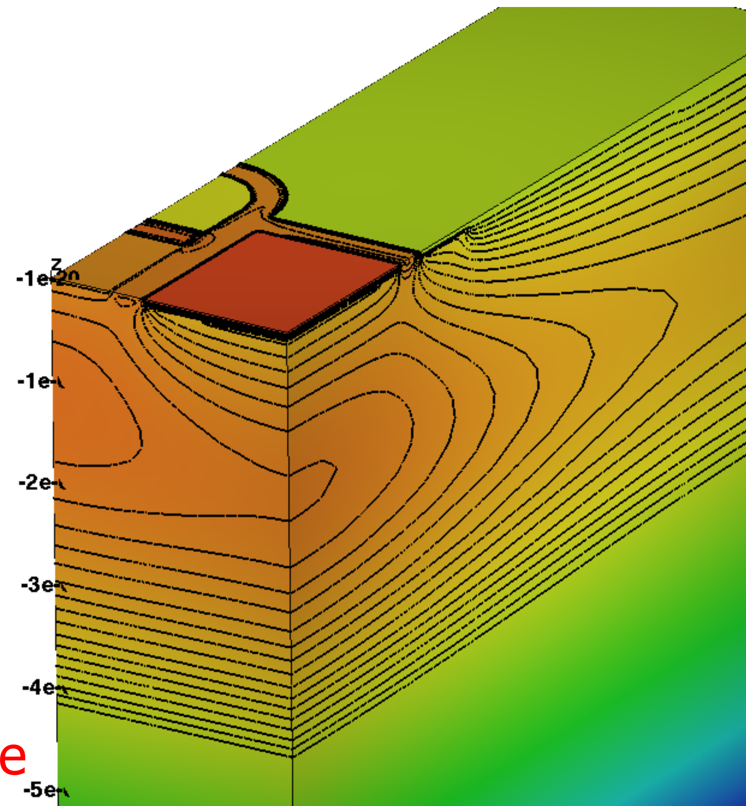


Vclear=3V and Vdrift=-7V



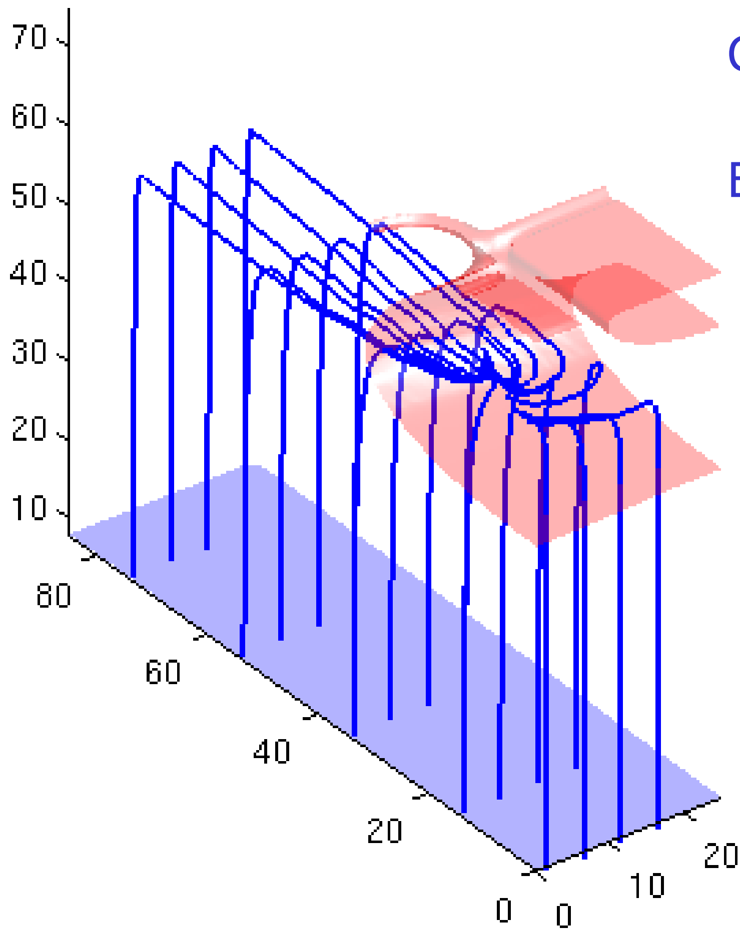
- Vclear-low =3V , Vdrift = -7V, Vback =-38V, Nb= 1.5e13cm-3





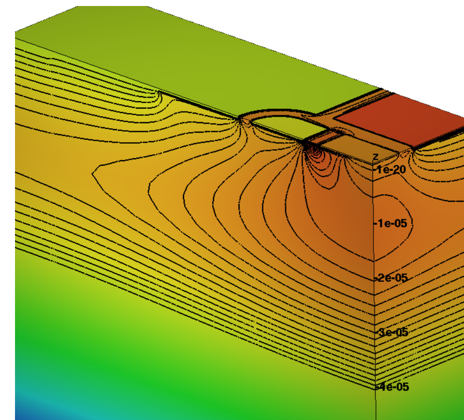
Low field region beneath the Source
But no pinch off

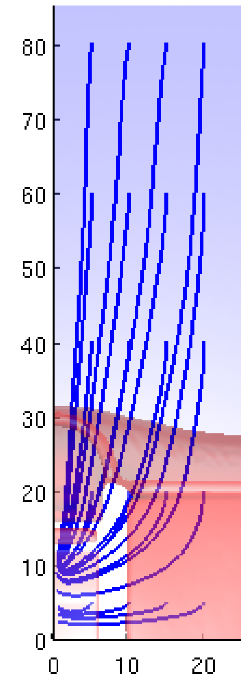
Vclear-low =3V , Vdrift = -7V, Vback =-38V, Nb= 1.5e13cm-3



Good charge collection

But strange drift path





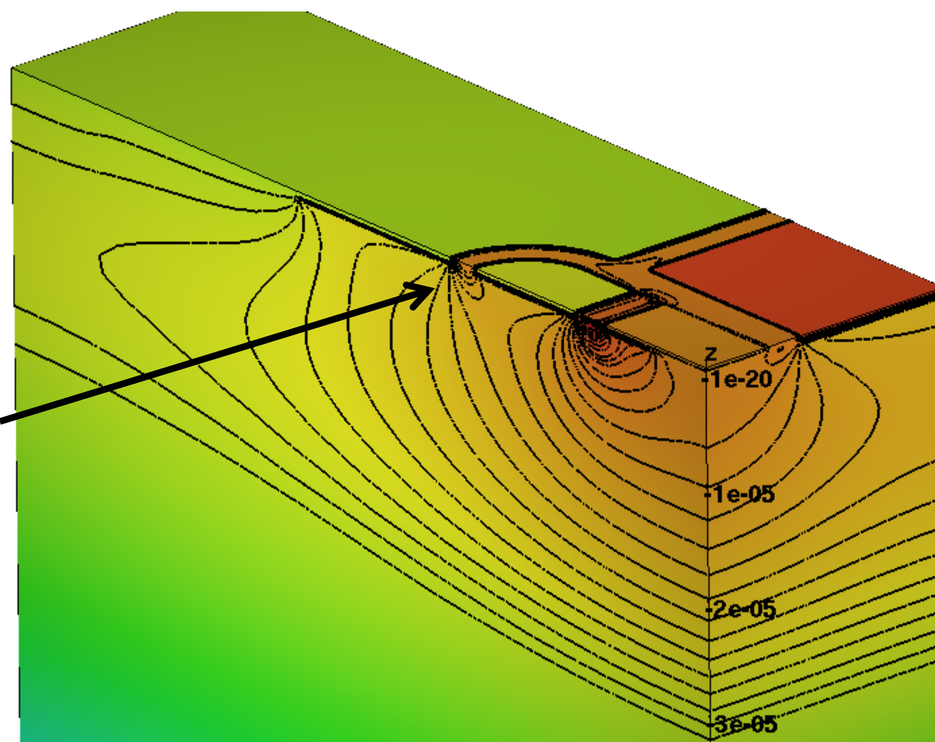
Charge is pressed to pixel center
But does not reach the southern pixel boundary!

Vclear-low =3V , Vdrift = -7V, Vback =-38V, Nb= 1e13cm-3

Normally doped regions have to run with more neg. backside

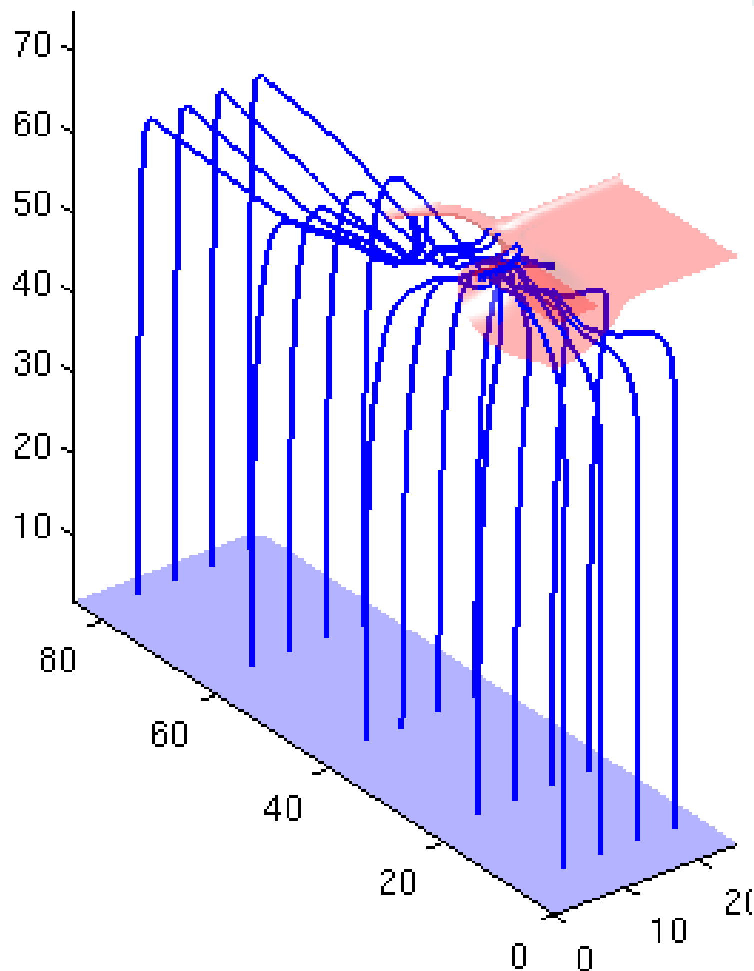
Drift path is pushed toward the topside

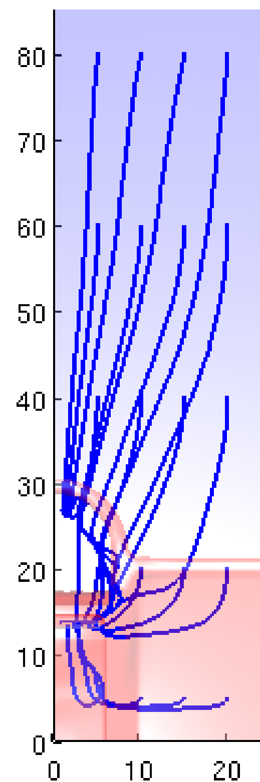
Electrons could be trapped by ClearGate regions

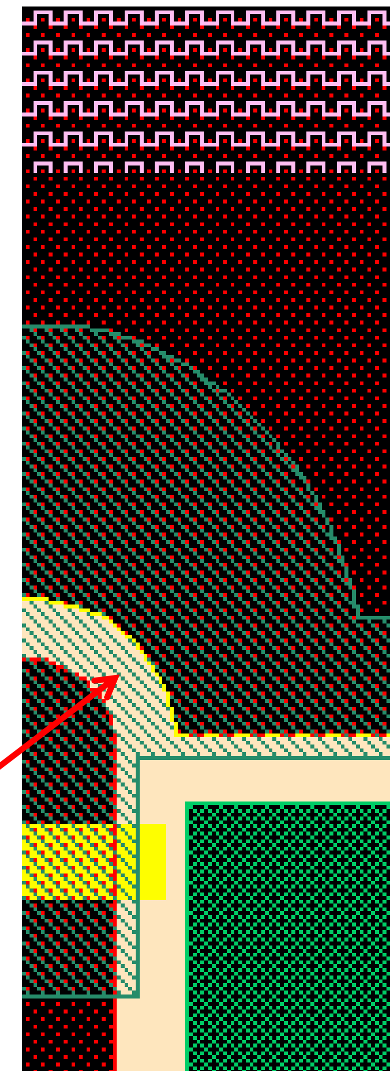


But contrary to the opld bias conditions we don`t see charge loss in the simulations – due to lower Vclear (charge does not go into the Clear)

Charge in the ClearGate Region





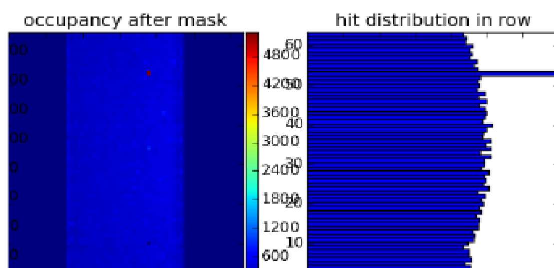


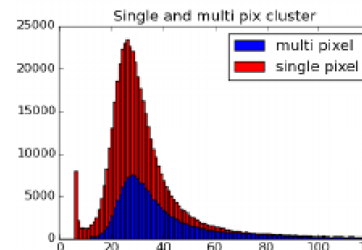
Shaped ClearGate

Charge should drift slowly to the Internal Gate
if Vclear (3V) is not too positve -> no significant loss
to be tested

Laser measurements – B. Paschen (Bonn)

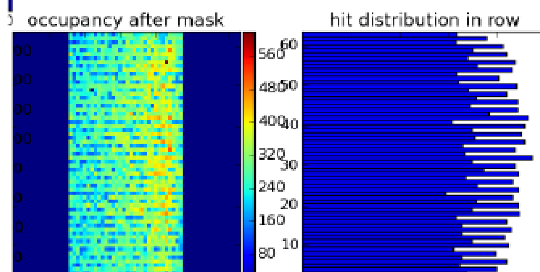
HV: -80 V
Drift: -7 V

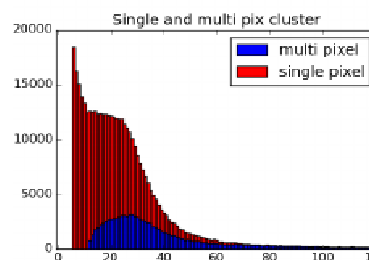




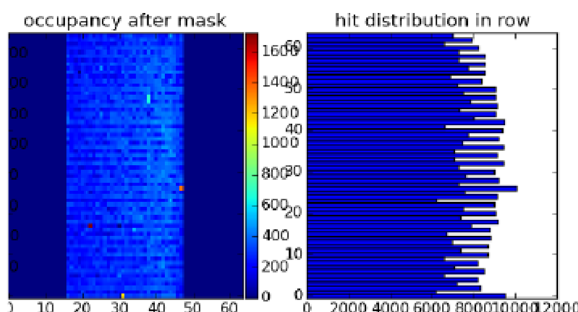
CCG: -1 V
Clear-low: 3 V
Clear-high: 20 V
Gate-on: -2.5 V
Gate-off: 3 V

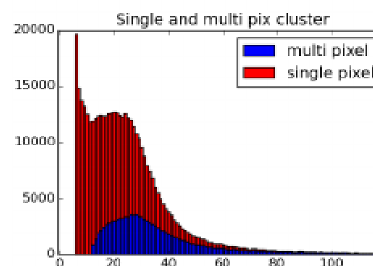
HV: -76 V
Drift: -7 V



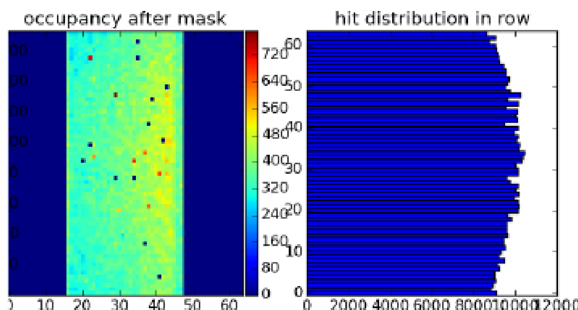


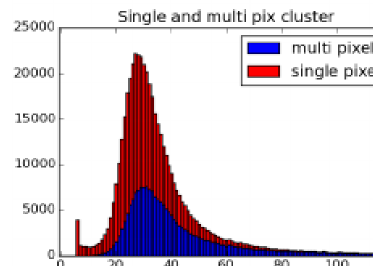
HV: -70 V
Drift: -7 V





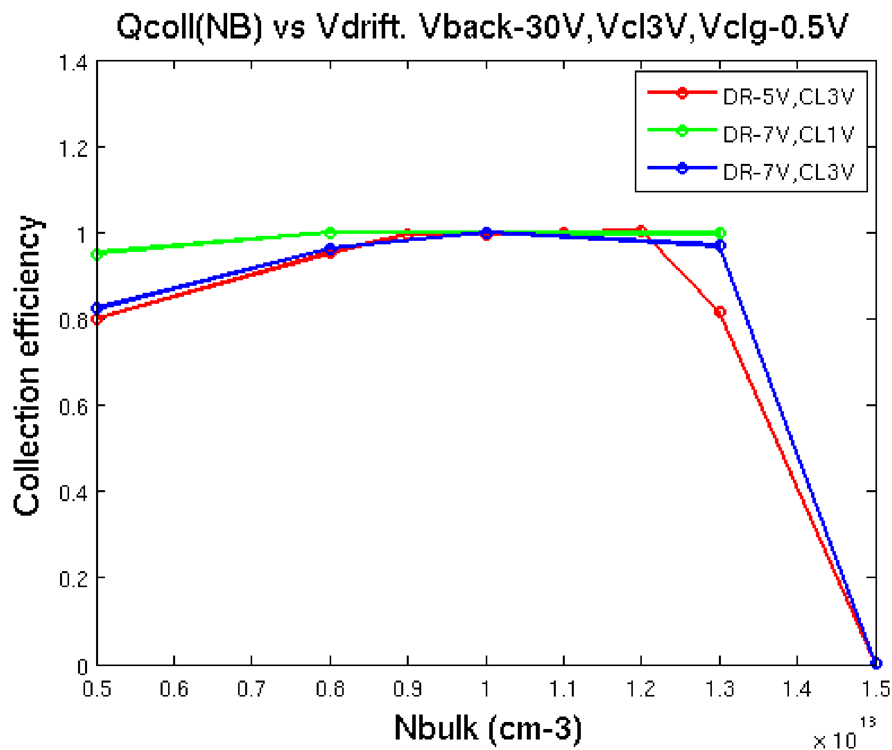
HV: -66 V
Drift: -7 V

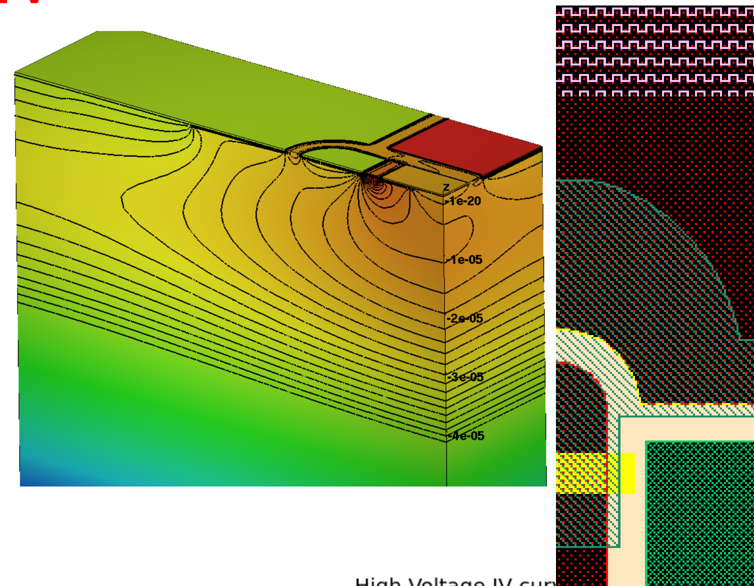


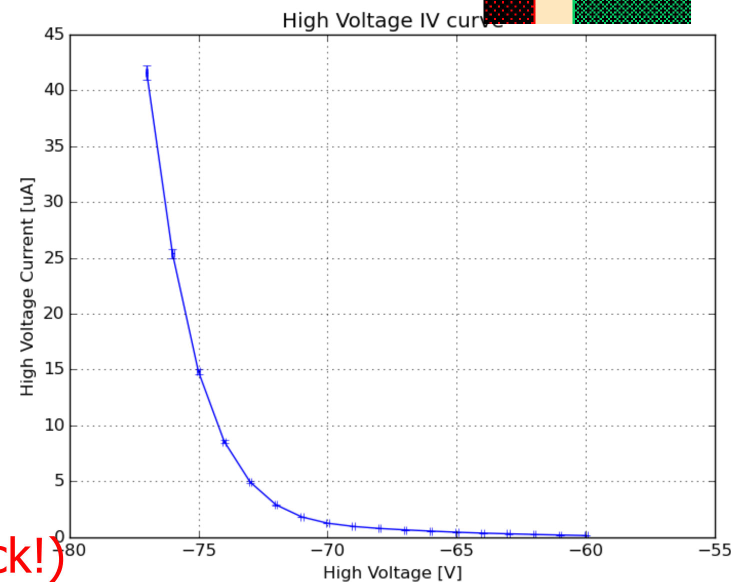


Good response over a wide HV range

Qcoll@Vdrift-7V,Vback=-30V Vclear3V -> 1V







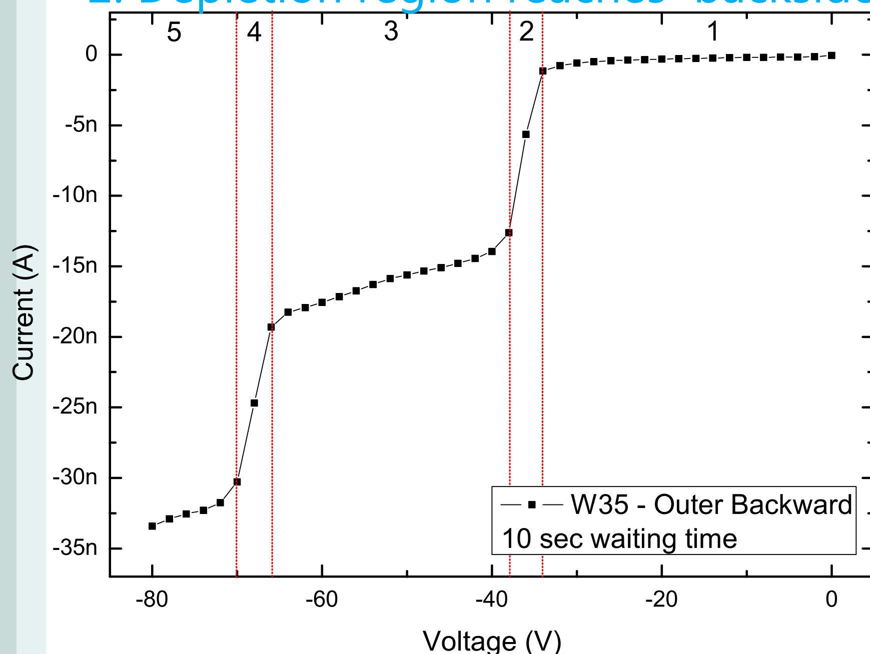
The lower Vclear the earlier the onset of hole emission from Source to Back

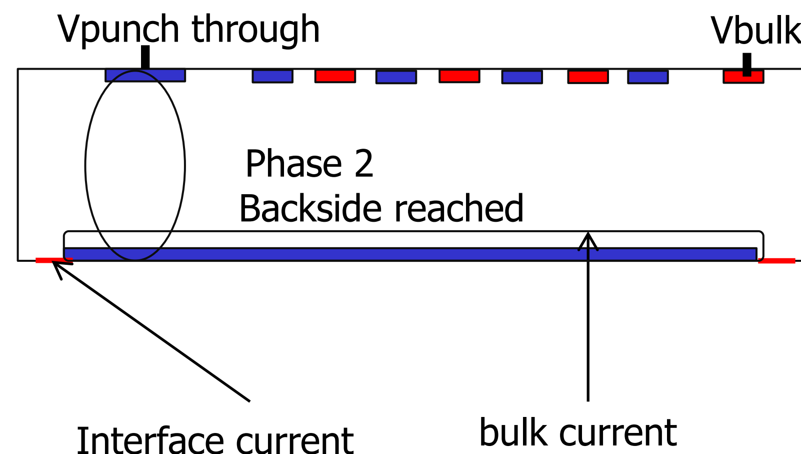
No Problem as long it does not affect the power consumption (measurement of Iback!)

Some words according - HV

Backside voltage is applied via punch through structure
Not directly !

2. Depletion region reaches backside





About 35V of HV drops over the punchthrough structure (this is constant if Iback is in an acceptable range. Another (about) 25-30V is required for depletion of the sensor region

Any further increase of HV increases directly Vback of the sensor

Keep in mind: a HV change has to be refered to -30V(Vback) not to HV

Please use smaller steps for HV optimization (2V instead of 5V) !

Bias - Recommendations

More robust charge collection:

Vclear_low has to be lowered from 5V -> 3V (or even lower but look at backside currents)

Vdrift :   -5V -> -7V …

HV scan: in steps of 2V (not 5V)

Parasitic hole channel from Source to Drift /Drain:

(subthreshold current but in every pixel of 200.000 pixels, measured on W30-OB1)

VclearGate :   -1V -> -0.5V (solves this issue)

Summary

MPG HLL

- Charge collection inefficiencies has been observed in the November testbeam

- Reason is most likely a significant localized increase of doping shaped in small concentric rings

-Do we find a set of operation voltages where these ring do not harm?

3d simulations and measurements (see Benjamin' s talk) suggest that this is possible

- But we don't yet know the full picture … some other areas or wafers !

- A new bias voltage set is proposed.