PXD9 Pilot Module

Status Pilot Module Testing

VXD Meeting – January 13, 2016

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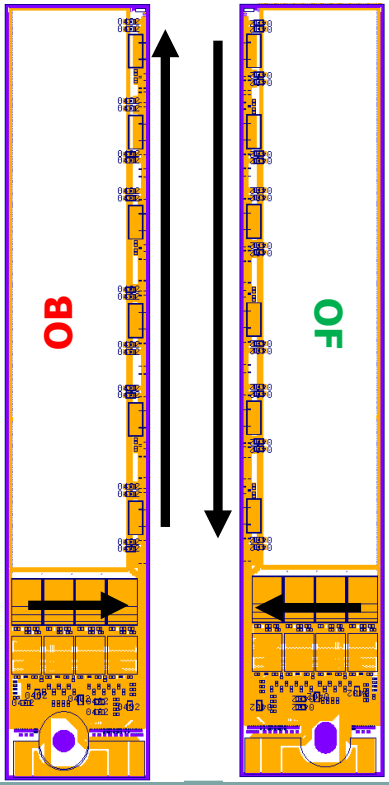
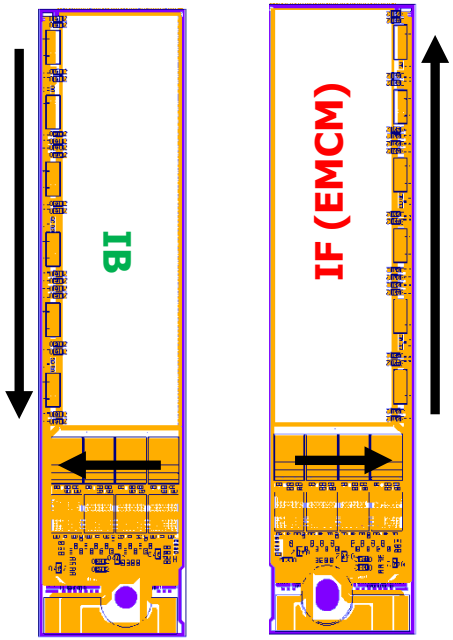
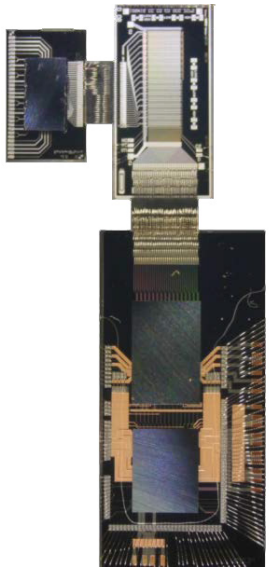
What do we need to proceed with PXD-9 processing?

- PXD9 pilot module full speed operation with acceptable performance (Cd109/Sr90 spectrum)
  - normal and gated mode (with laser)
  - **for metal1: full speed operation (with laser)**
- available devices (with **current ASIC** versions and their known features….)
  - W30-OB1, W30-OB2: outer backward modules with kapton attached
  - W30-OF1: outer forward module on Hybrid7
  - small PXD9 matrices : Hybrid5 □beam tests



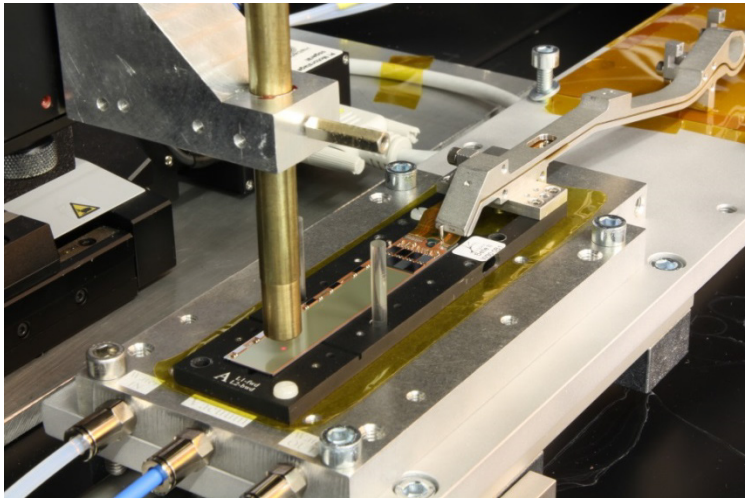


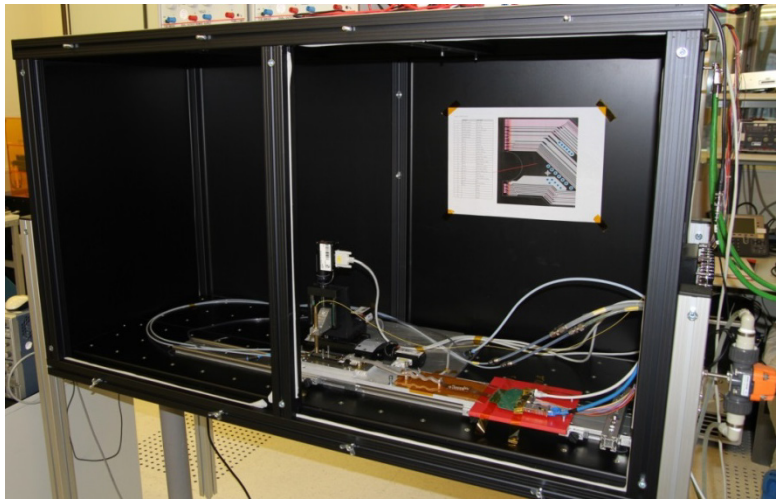


→ Small PXD9 @ DESY Beam Test talk by B. Schwenker on Thursday

Pilot run modules on the test bench

- Successful assembly of 3 modules (2 OB, 1 OF), all modules without faults (boundary scan)
- One was broken by operator (handling mistake)



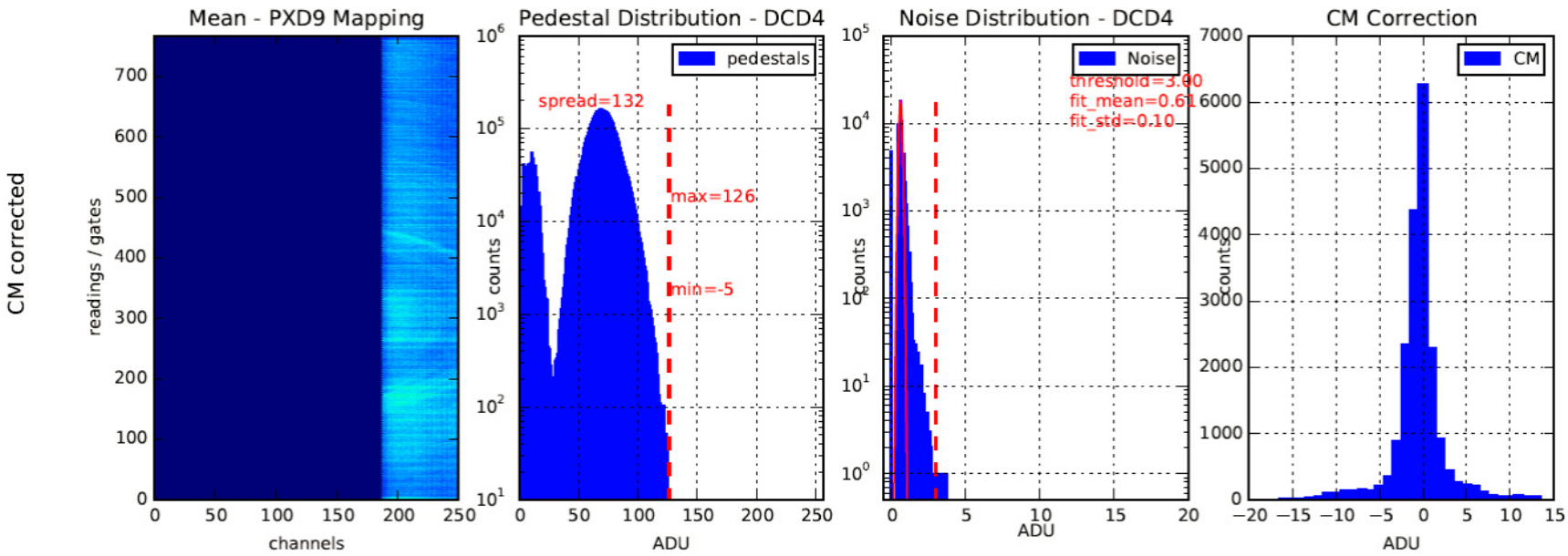


- Power-up ASICs – sanity check voltages + currents
- Boundary Scan
- DCD <-> DHPT communication – timing adjustment
- Sampling point scan
- Measure DEPFET response (Source, Laser spot)

→ Main focus at the moment: **response (clear performance) over the entire matrix**

4x DHPT1.0
4x DCDpp
6x SwitcherB18v2

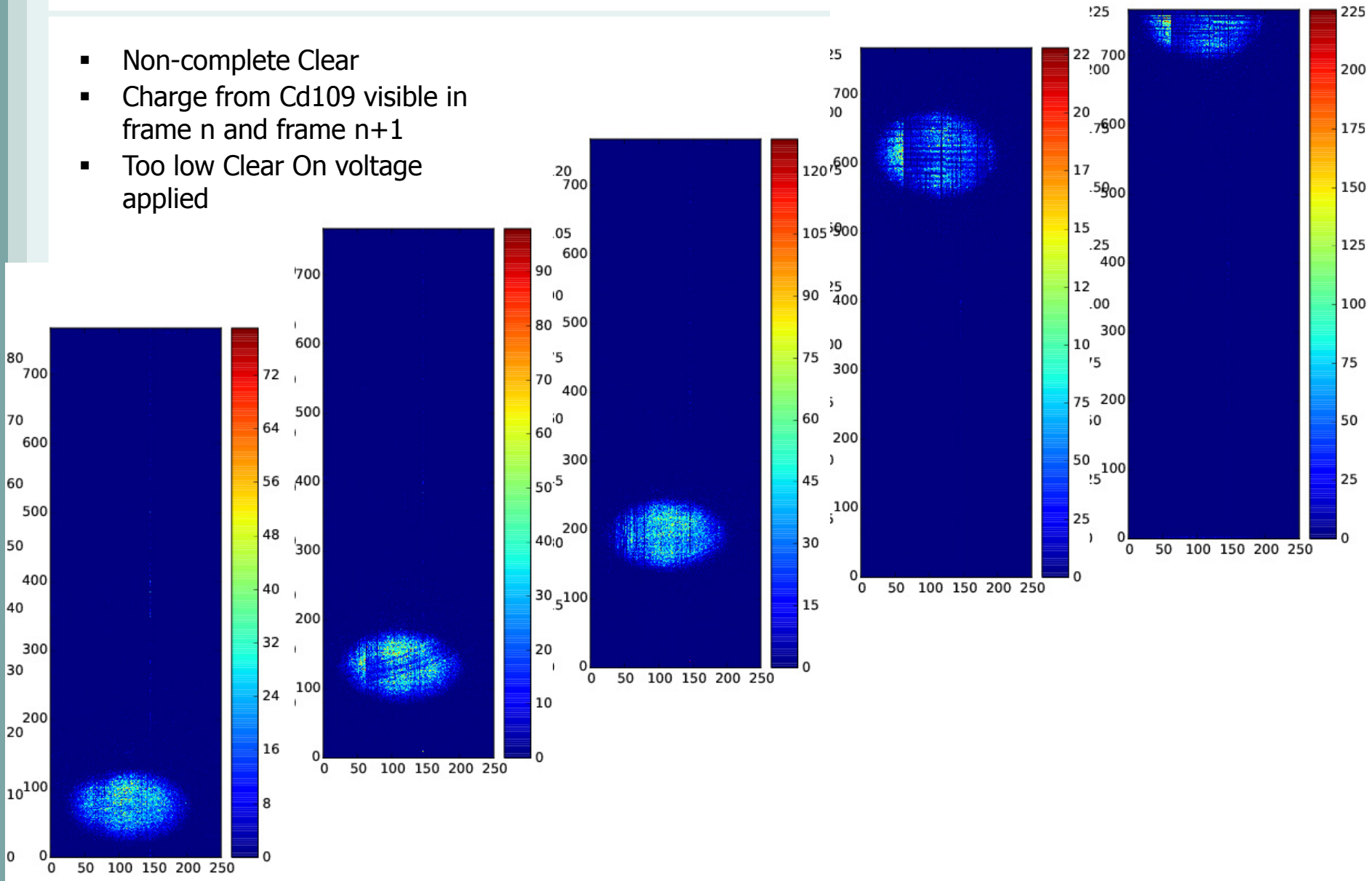
W30-OB1 Pedestal & Common Mode



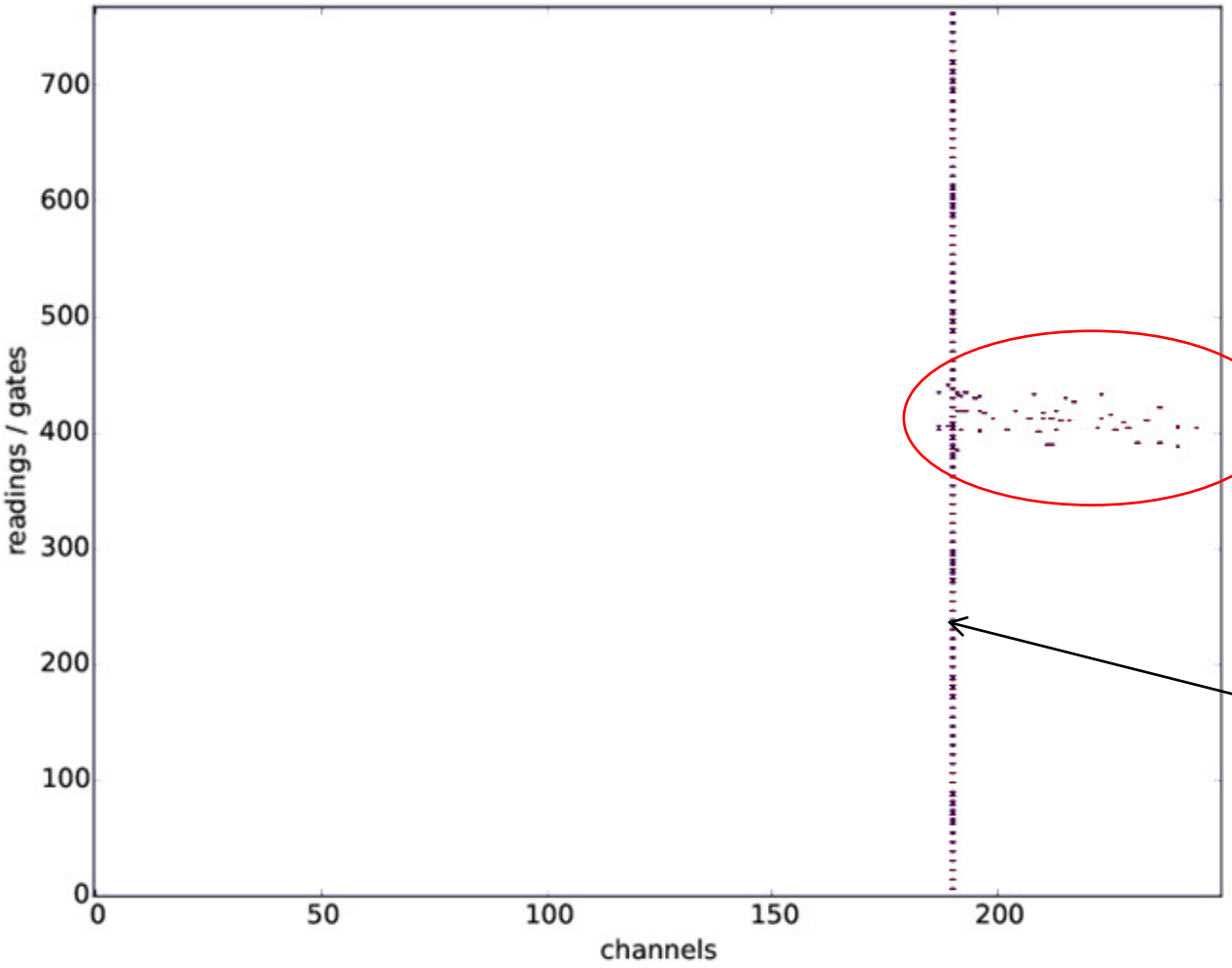
- Large common mode contribution
- Not visible @ PXD6 matrix

Cd109 Hitmap – Non-complete Clear

- Non-complete Clear
- Charge from Cd109 visible in frame n and frame n+1
- Too low Clear On voltage applied



Compare consecutive frames



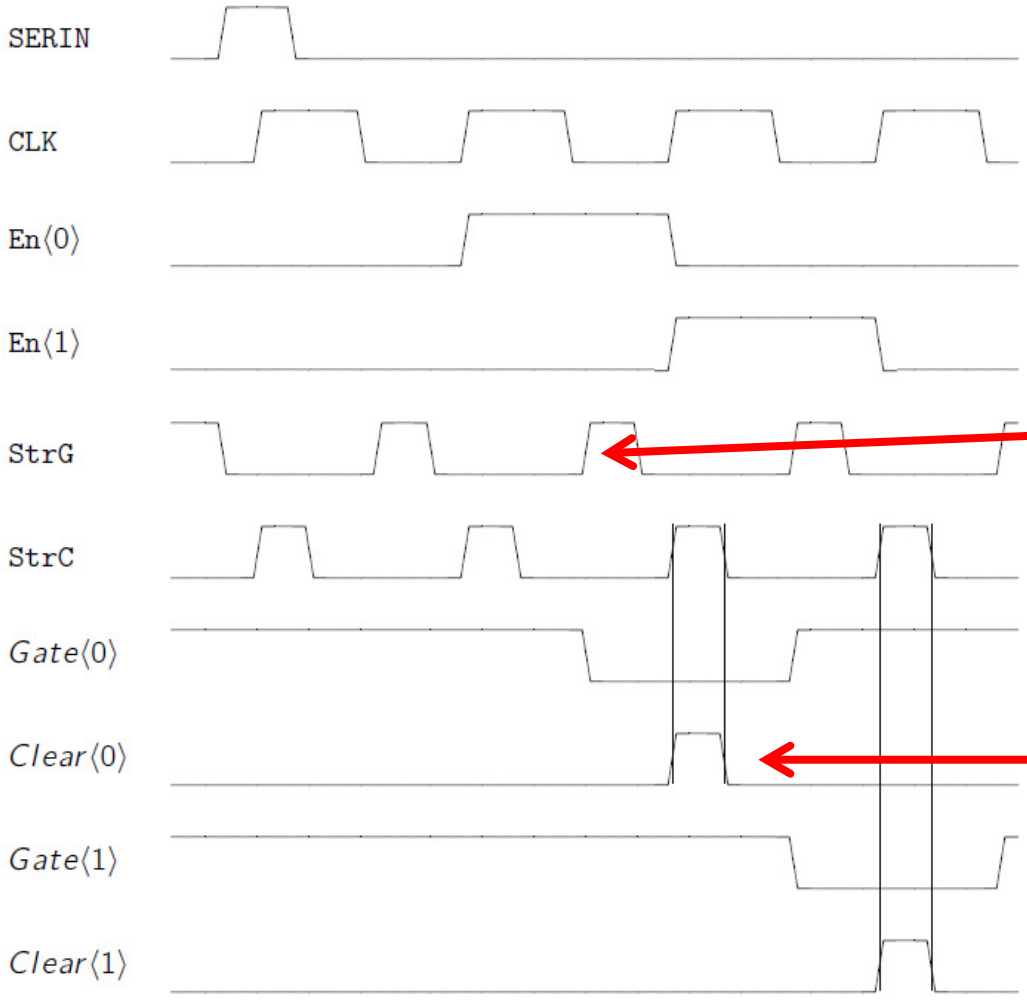
Comparison between frame n and frame n+1
Trigger length = 3072
only one DHPT read

Charge remained in internal gate in the next frame.

Vertical line is done on purpose to test the software

Switcher Control Signals

- StrC signal is the most critical of the control signals

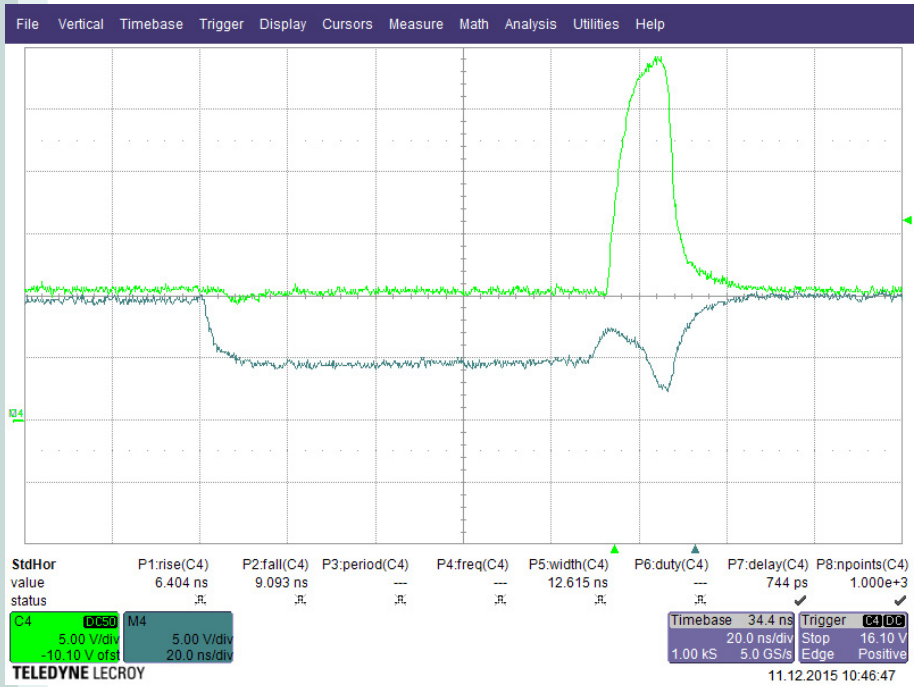


SwticherB gate output is sensitive to the rising edge of the StrG signal only

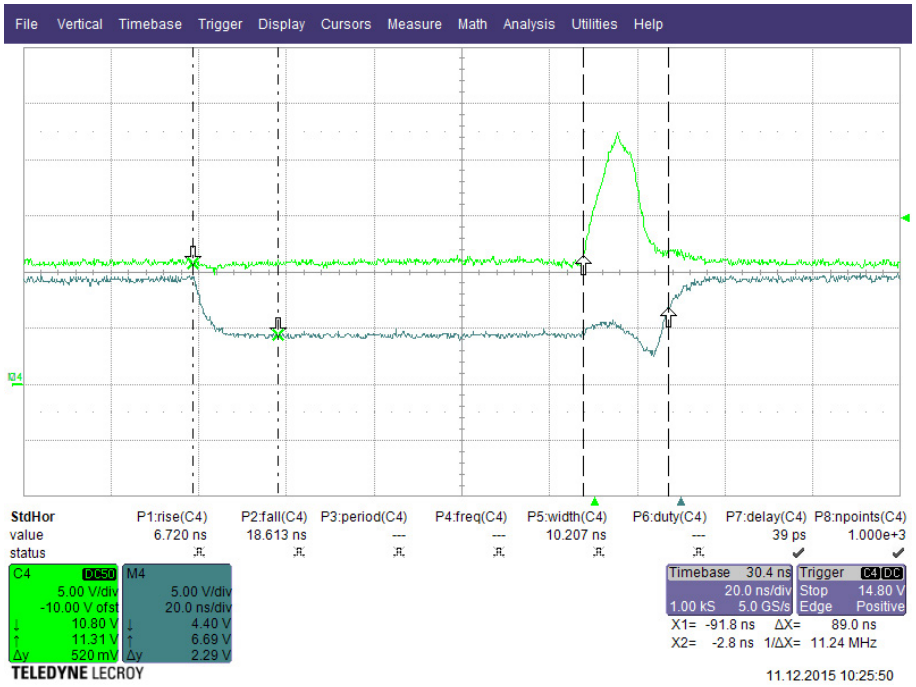
SwticherB clear output is sensitive to the rising and falling edge of the StrC signal

Switcher 1 and Switcher 6 – Clear and Gate output

- Clear pulse along the matrix

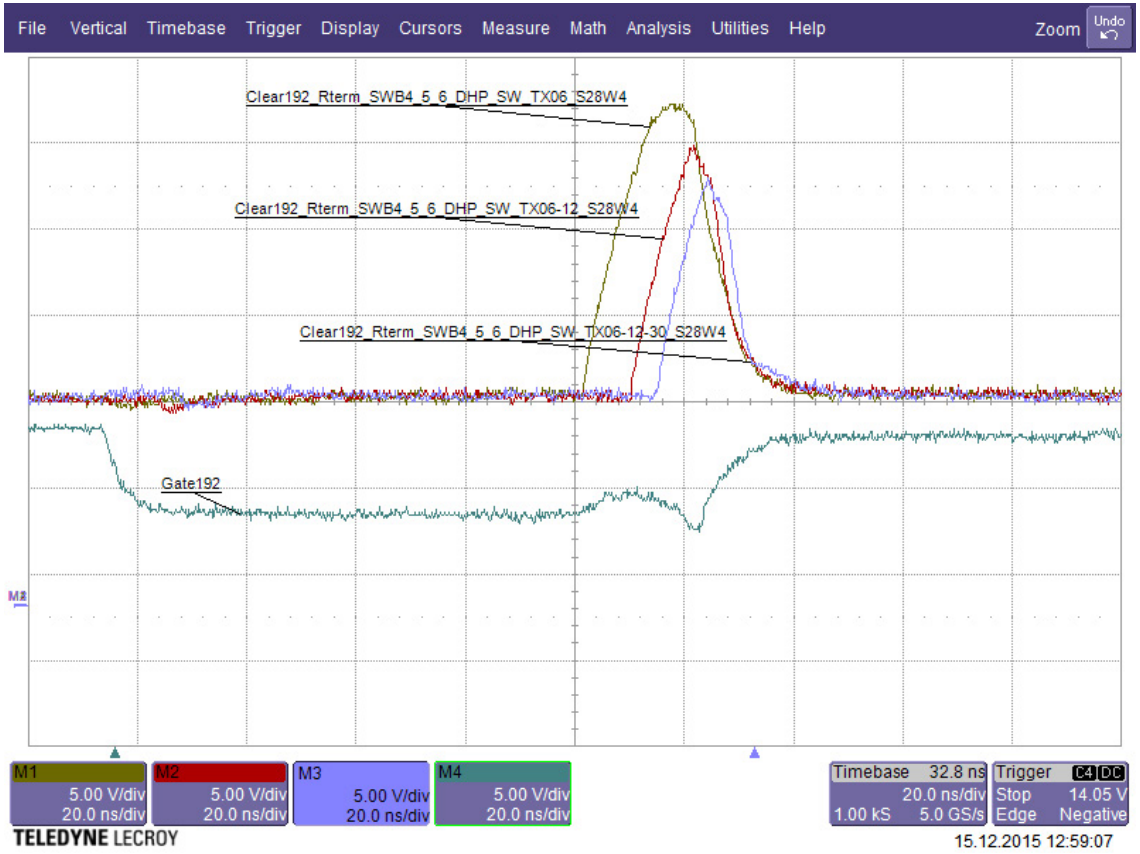


Switcher 1
Clear #1 and Gate #1



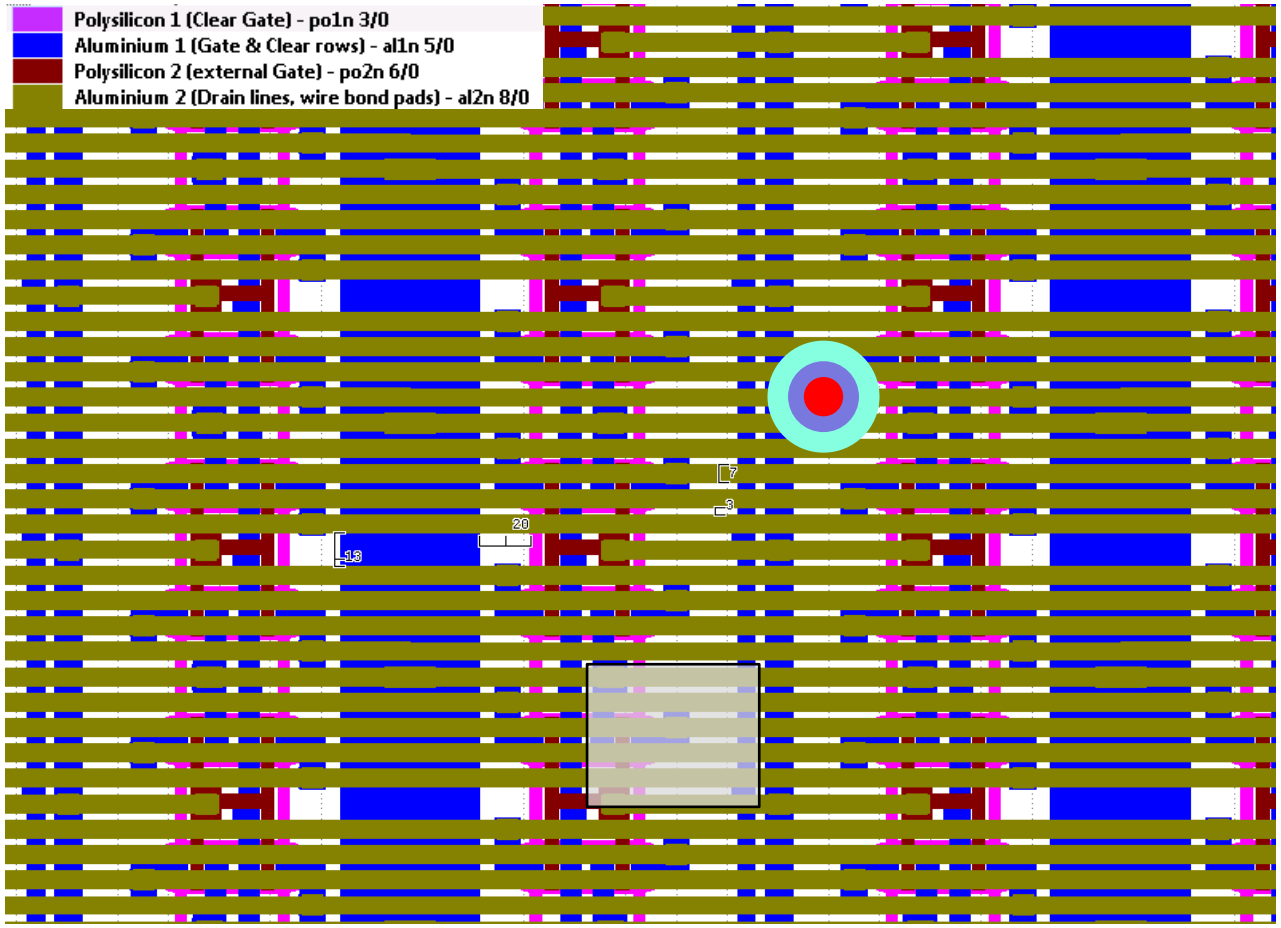
Switcher 6
Clear #192 and Gate #192

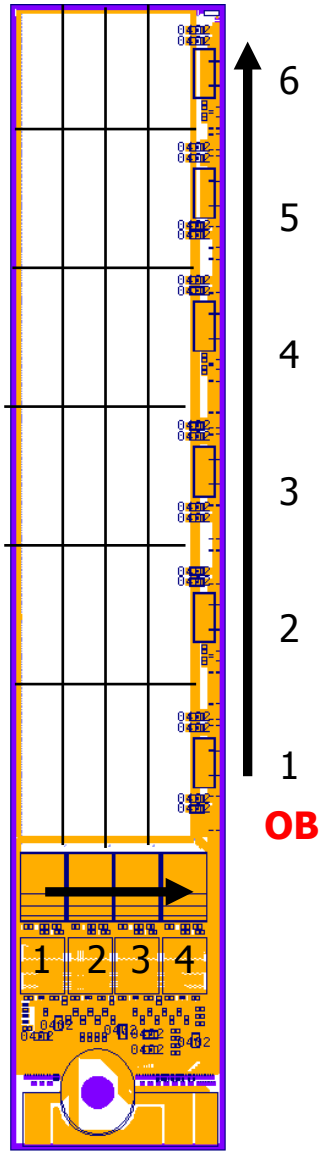
Optimizing the Clear pulse



- The signal integrity along the module is a **matter of optimization**
- Difficult because of limited access to outputs (only 2 out of 192 (clear&gate))
- Width of operation window/influence from routing not completely clear yet →simulations started
- Scan with a laser spot over the various matrix regions done for W30-OB1

Laser Scan



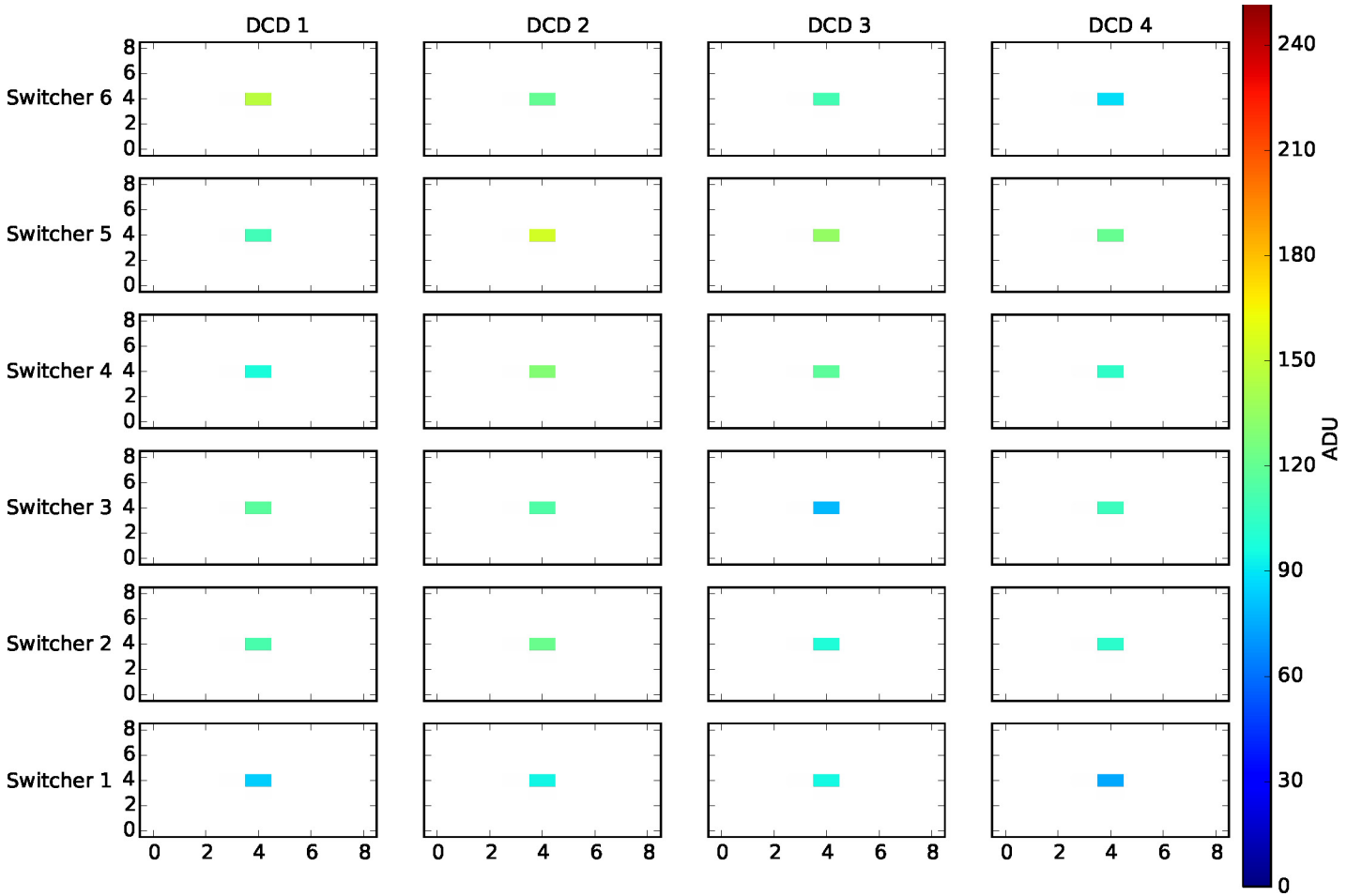


Laser can only shoot from the top side

Laser scan – W30/OB1

Laser signal ~2-4mip, **read out at full speed** with a noise of ~1.8 ADU (laser instability and system noise)

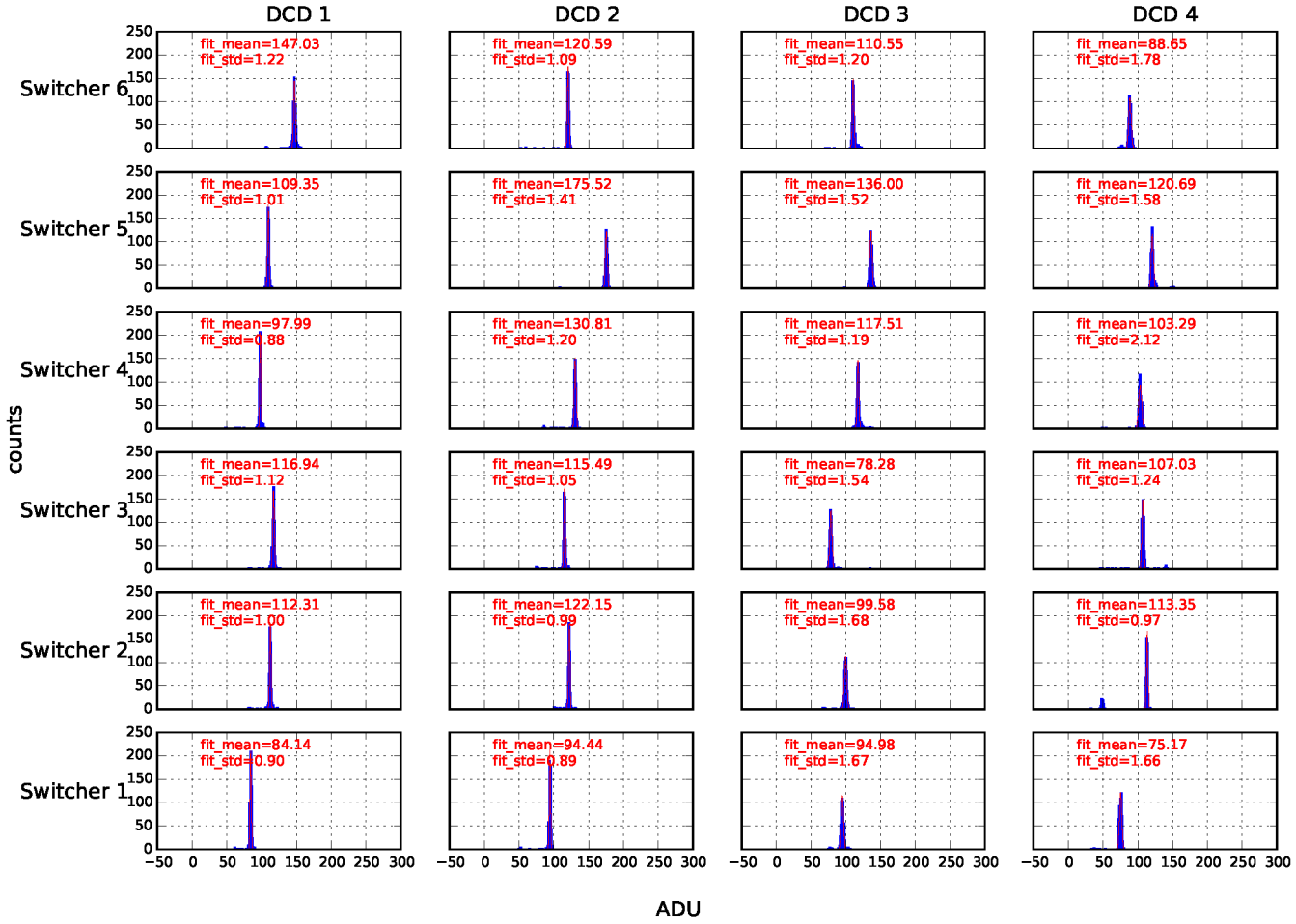
~105 ns/row, of which ~26ns are used for clear pulse (8 ticks of 32)



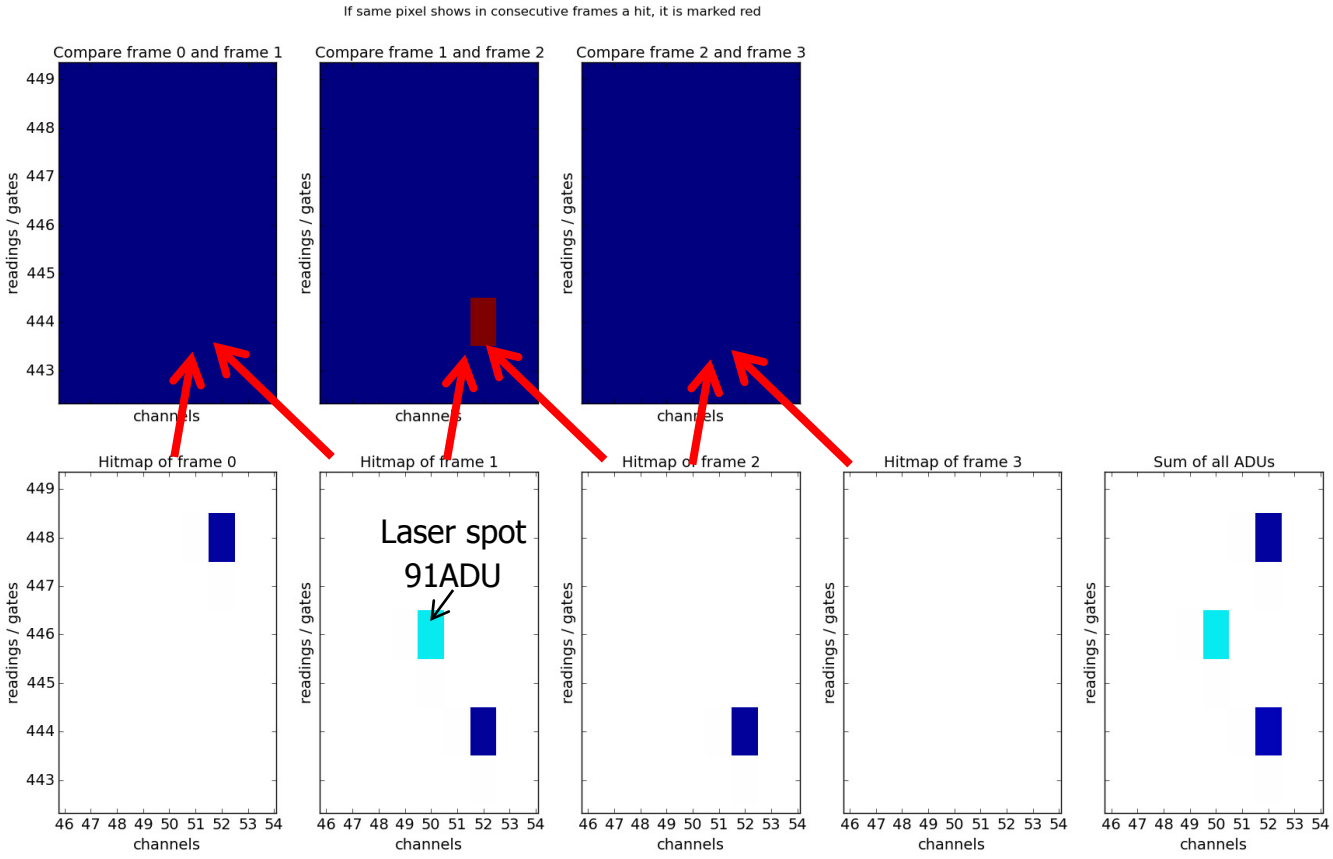
Laser scan over W30-OB1

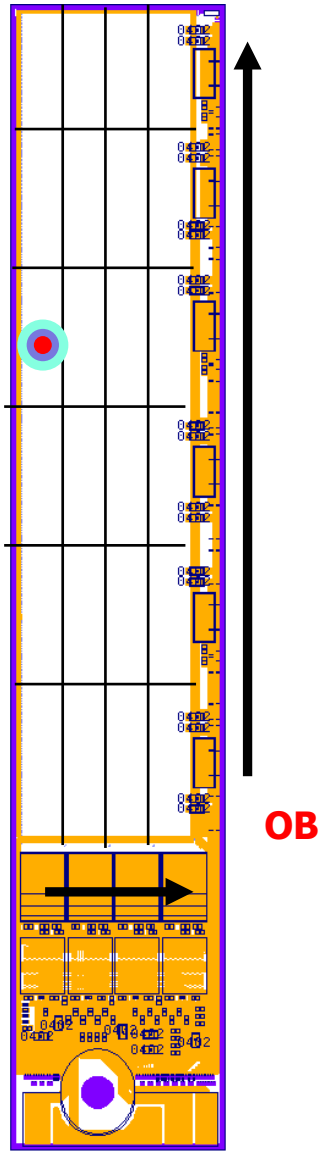
Laser signal ~2-4mip, **read out at full speed** with a noise of ~1.8 ADU (laser instability and system noise)

~105 ns/row, of which ~26ns are used for clear pulse (8 ticks of 32)



Laser scan over W30-OB1 – Clear Performance



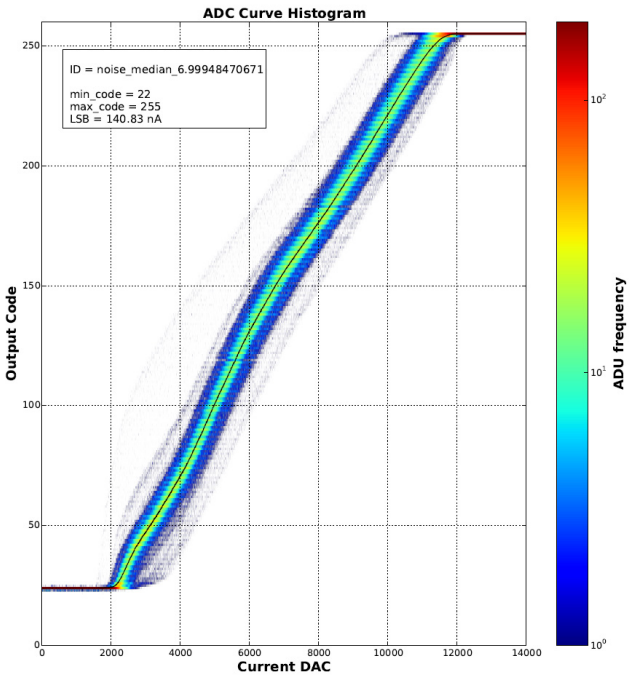


- Trigger width increase to 6144 – to transmit 4 consecutive frames
- Timing of the laser set to have one laser pulse within 4 frames
- Threshold of zero suppression in DHPT set to 5 ADU

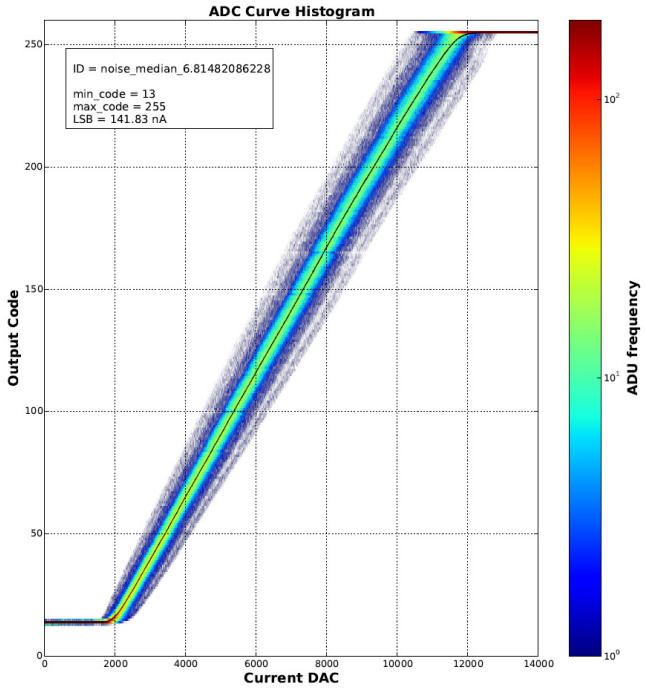
W30-OB1 ADC Transfer Curves – **DHE current source**

- 4 DCDs share one monitor line which is connected to a current source on the DHE
- Large noise contribution – probably due to length of the monitor line (kapton, patch-panel, Infiniband cables) + high common mode for the channel which is connected to the matrix
- Bow in the ADC curve of channel 1 due to small change of the DEPFET voltages

Channel 1 - connected to matrix



Channel 11 – **NOT** connected to matrix

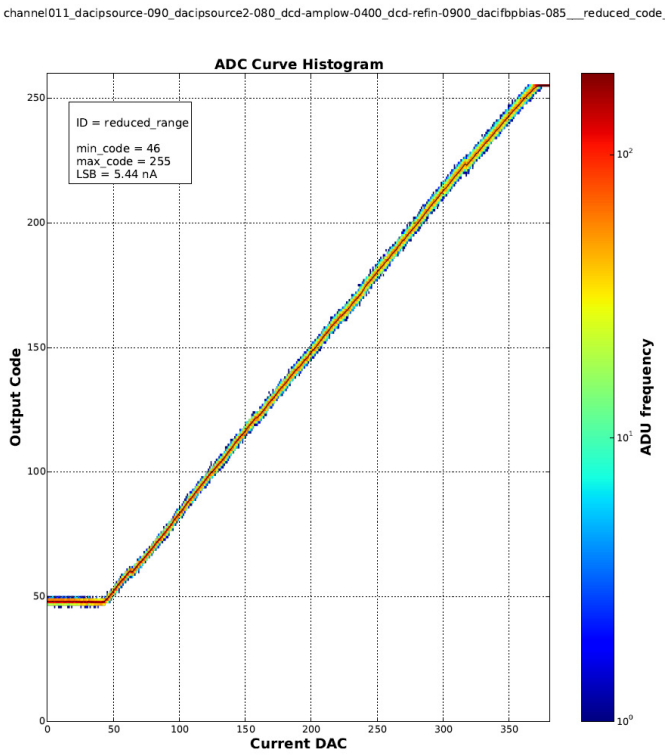


Clear-On: 12V
Clear-Off: 12V
Gate-On: 3V
Gate-Off: 3V
Source: 6V
Bulk: 10V

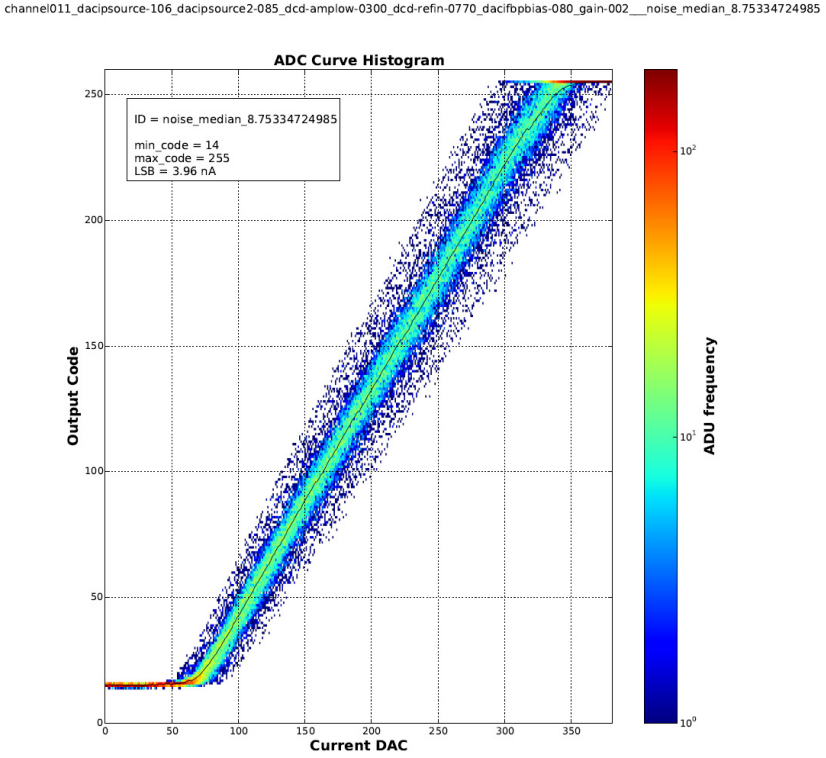
W30-OB1 ADC Transfer Curves – **DCD internal current source**

Channel 11 - not connected to matrix

DHE Current Source connection removed on patch panel



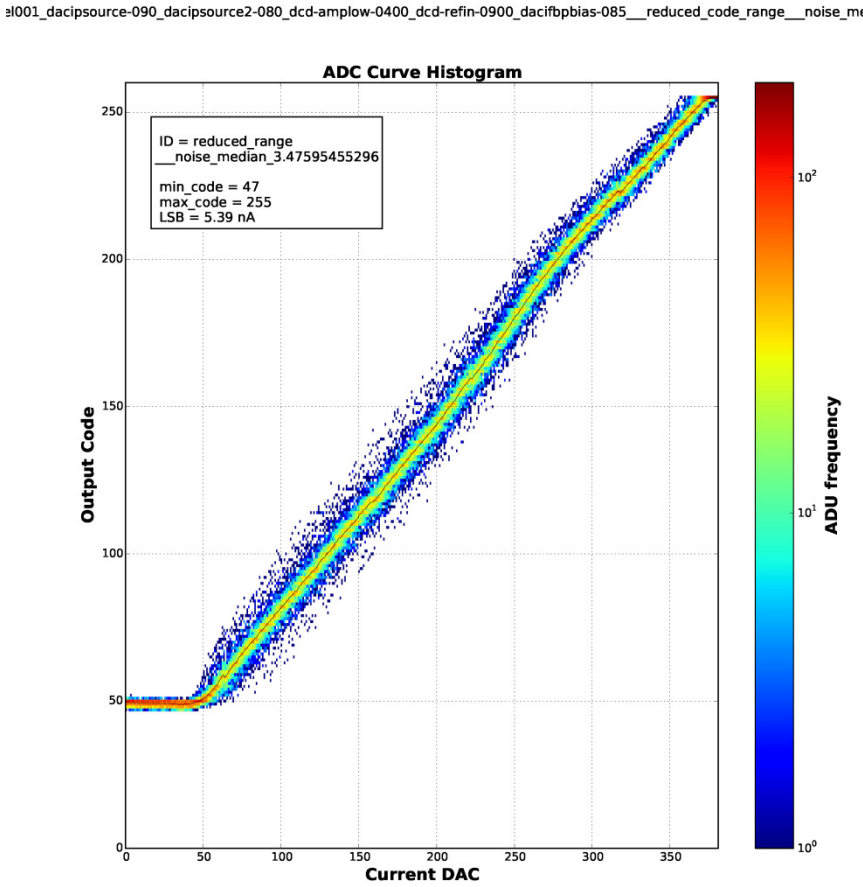
DHE Current Source connected but not used



→ Large noise with the external current source makes the analysis of the ADC curve and optimization of the DCD parameters very difficuilt

W30-OB1 ADC Transfer Curves – **DCD internal current source**

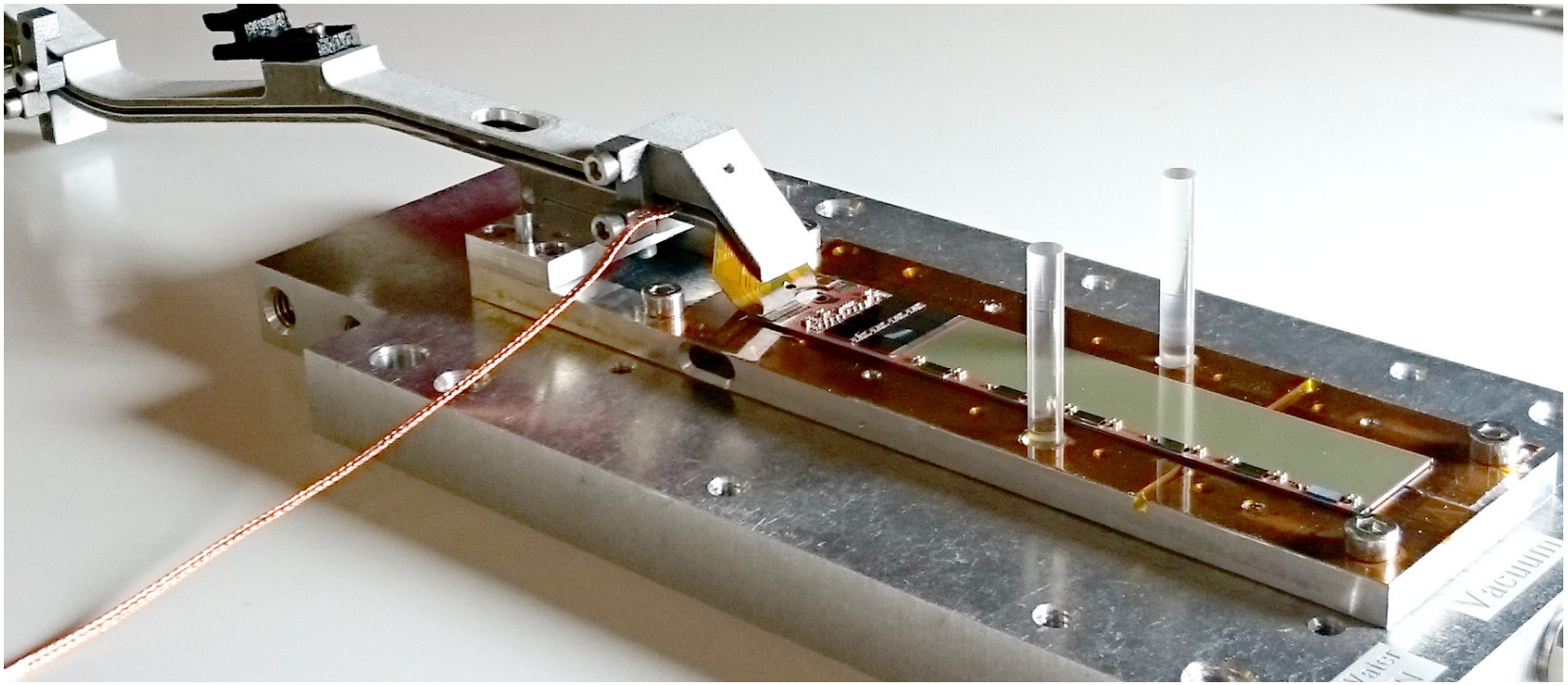
Channel 1 - connected to matrix
DHE Current Source connection removed on patch panel



- Scan with the DCD internal current source possible but much slower than with DHE external current source (probably can be improved by DHE firmware)
- Scan with DEPFET as current source under investigation (parallel scan of all DCD channels possible)

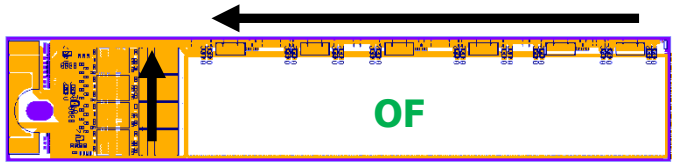
W30-OB2

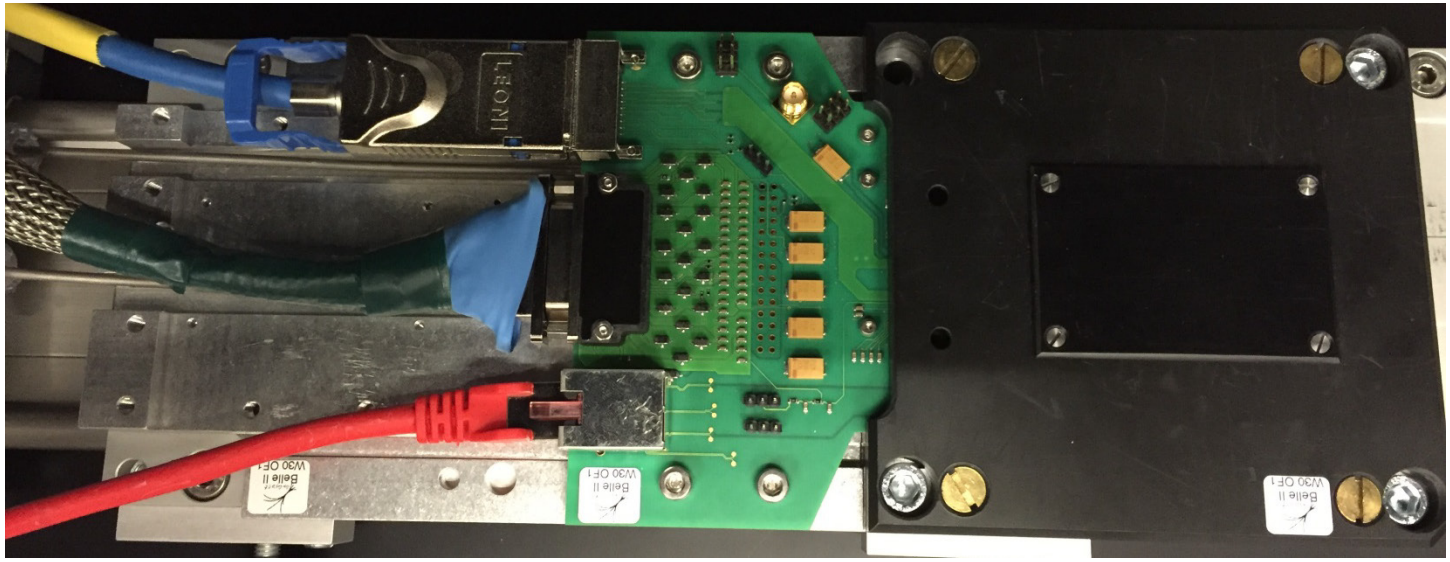
- In order to improve/understand the high common mode noise the GND/GNDA connection to the aluminum jig is done close to the PXD9 module (in a similar way as it is planned in the experiment)
- Testing will be done after the VXD meeting



W30-OF1

- Outer forward module assembled to Hybrid 7 (replaces Kapton)
- Change in firmware to invert the TRG line necessary (command line of the DHPT) – due to routing of the signals on the Hybrid7 PCB
- Having fixed the setup issues all High Speed links are up @ 1Gbps (full rate, GCK = 62.5MHz) and delay scans for all ASICs are ok (since Jan 11th)
- Next step is to measure Switcher Clear and Gate outputs with the oscilloscope (2 of 192)





Summary

- W30-OB1 shows a good clear performance over the entire matrix at full speed with reasonable long StrC signal!

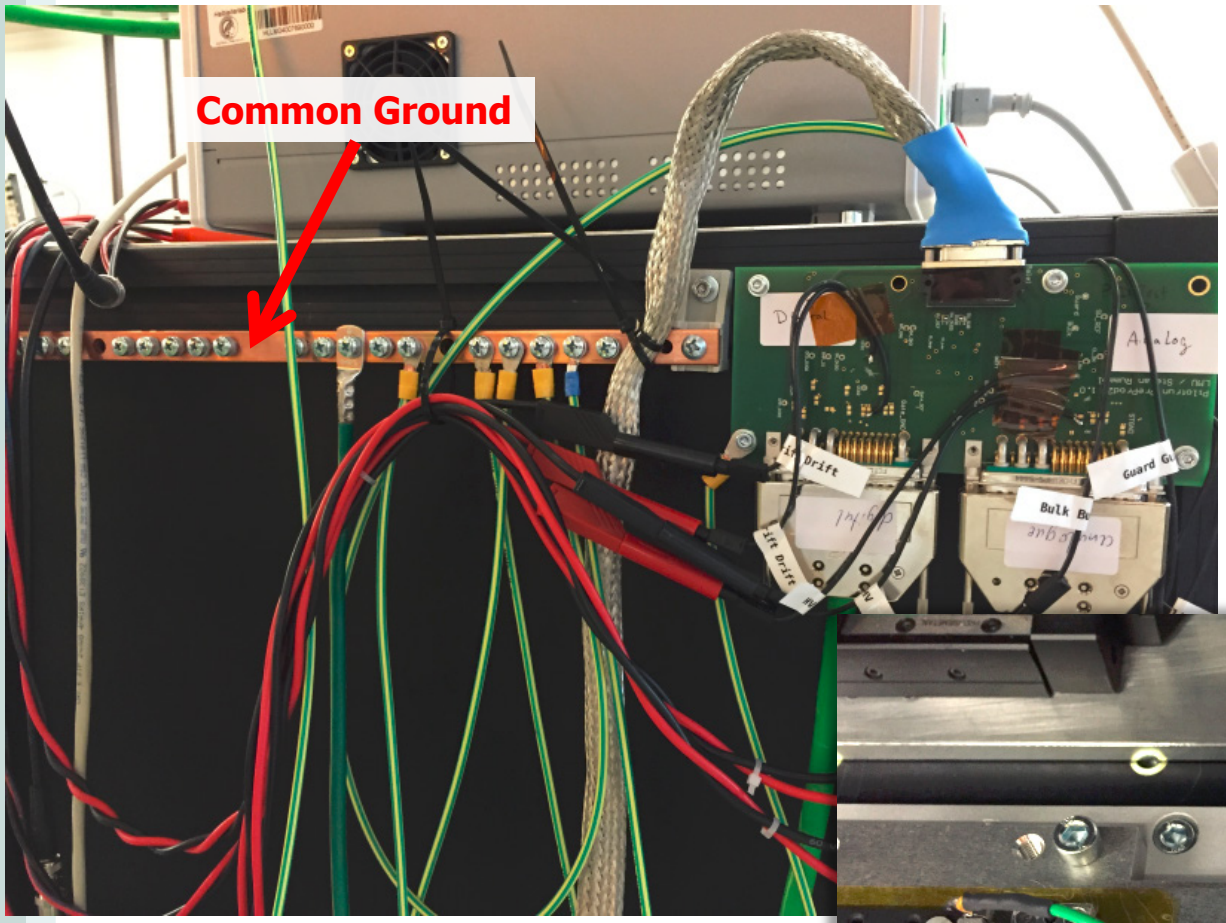
- Open topics before we proceed with alu1 metallization
  - **W30-OF1** (Hybrid7) Switcher output signals, pedestals and laser scan
  - **W30-OB1** radio active source @ GCK = 62.5 MHz (much less bit errors compared to GCK = 76.23MHz)
  - **W30-OB2** pedestal measurements (common mode)

- Gated Mode with DHPT and DHE (Hybrid5 and PXD9) needed to proceed with alu2 and copper!

- Changes introduced in the PXD9 layout & lessons learned
  - Increase spacing of the DCD-DHPT data lines (for pedestal upload, reference voltage and ADC data)
  - Summary of lessons learned: https://docs.google.com/spreadsheets/d/155aSvn3mvLV5qWFrh0GnLXhELrkM1Mf4Xqo_J7SGIs0/edit#gid=731047789

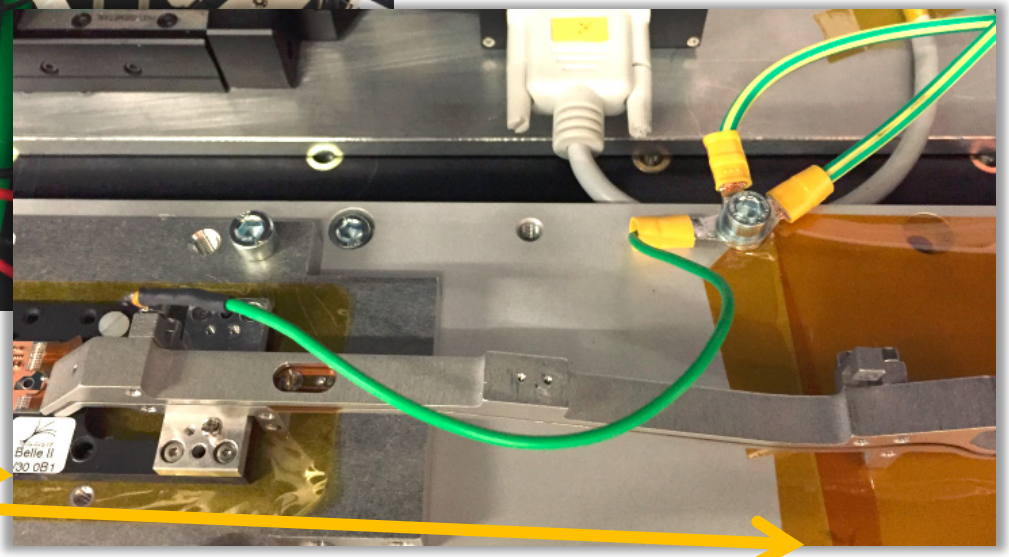
Backup

Grounding of PXD9 Pilot Run – W30-OB1



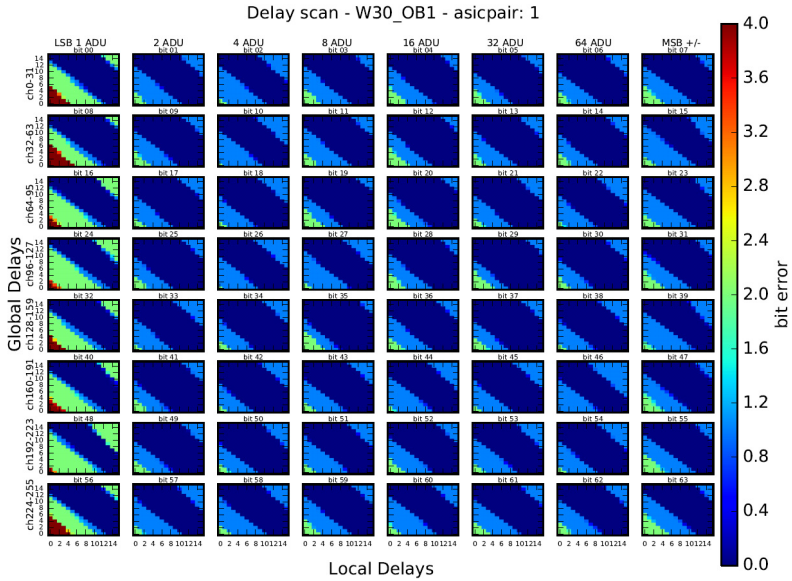
connected:

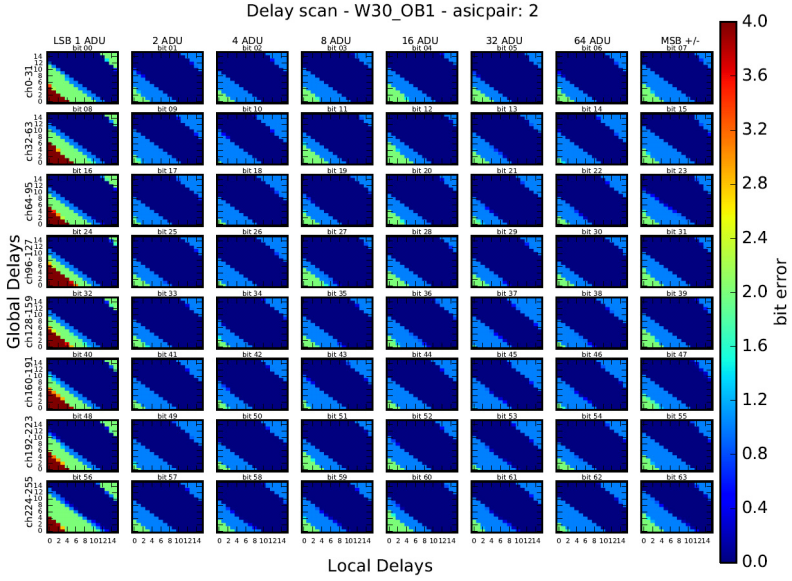
- House Ground (HLL)
- LMU Power Supply
- Shield of Glenair PS Cable
- Aluminum plate
- jig - capacitive coupled

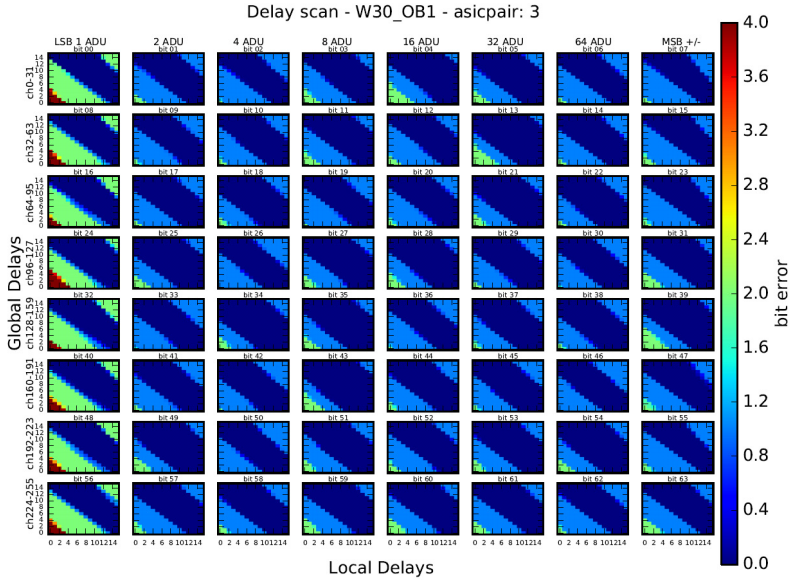


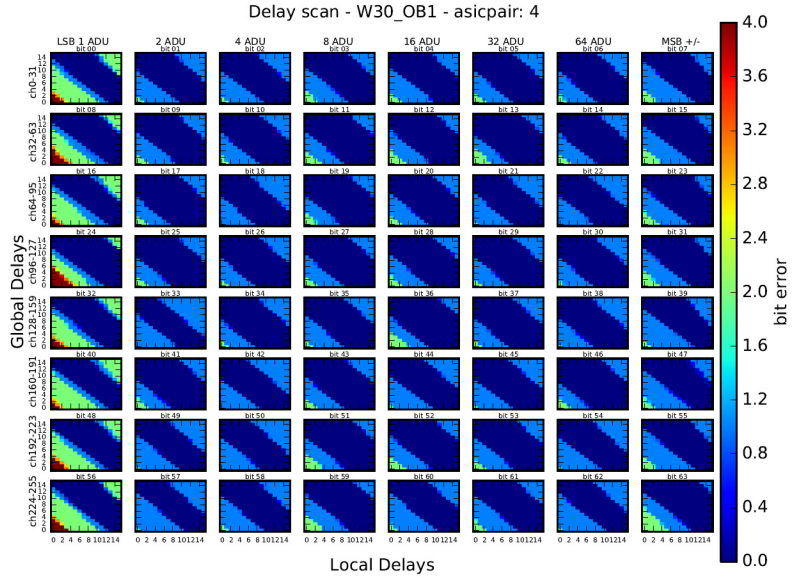
Kapton flex

Delays CLK_{DHE}62.5MHz (CLK_{DCD}250MHz)

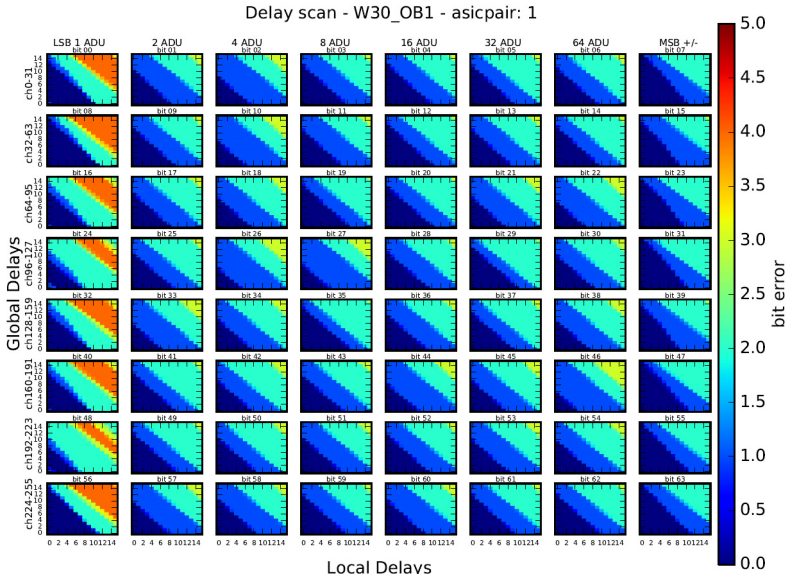


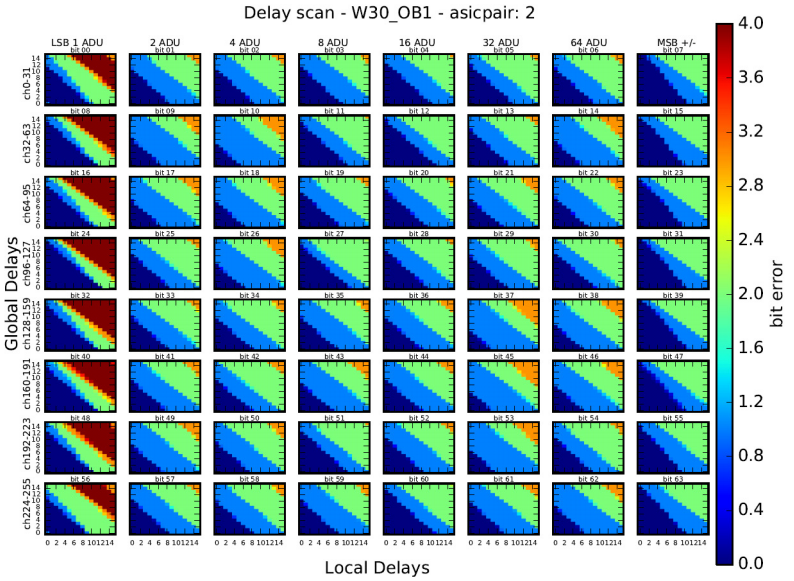


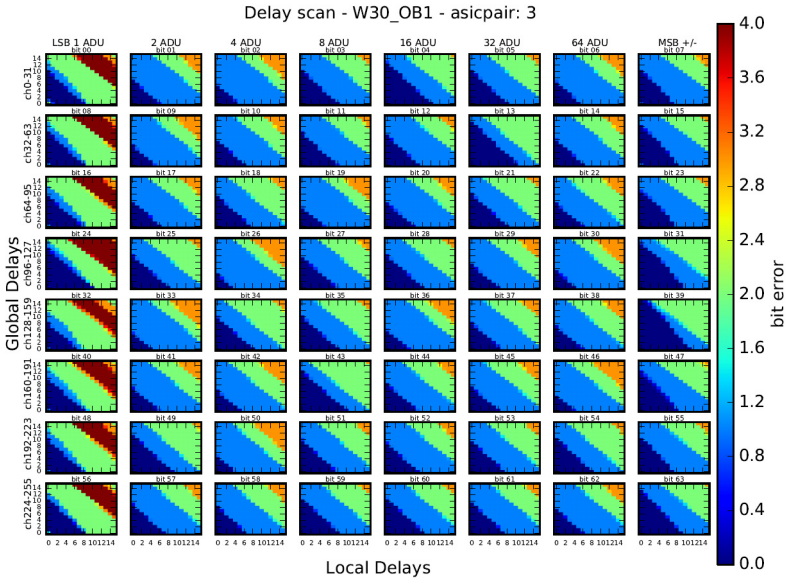


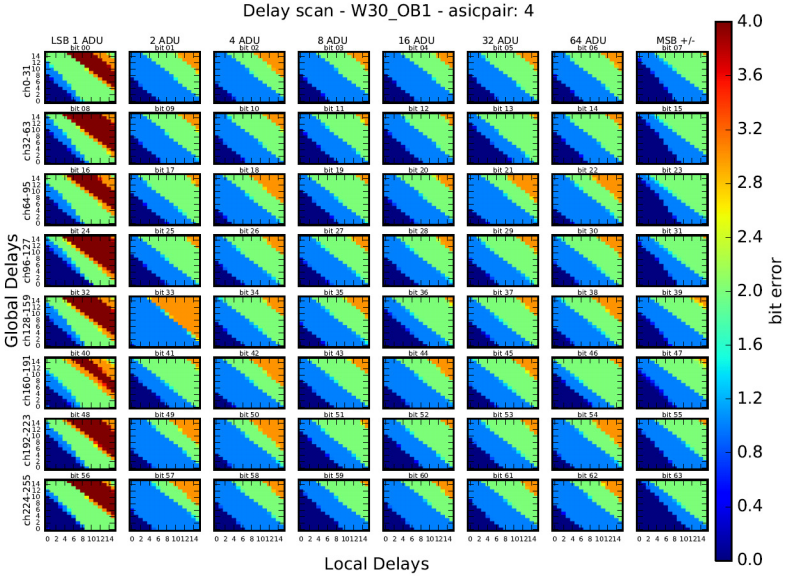


Delays CLK_{DHE}76.3MHz (CLK_{DCD}305MHz)

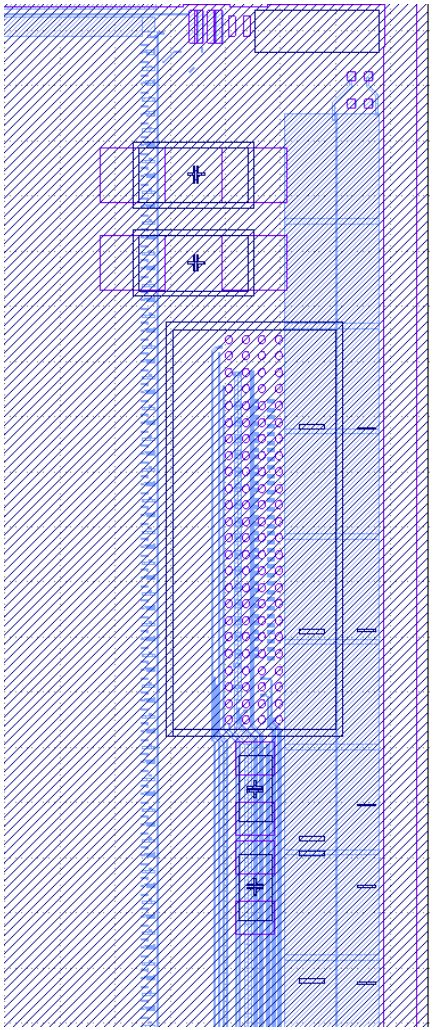








SWB Control

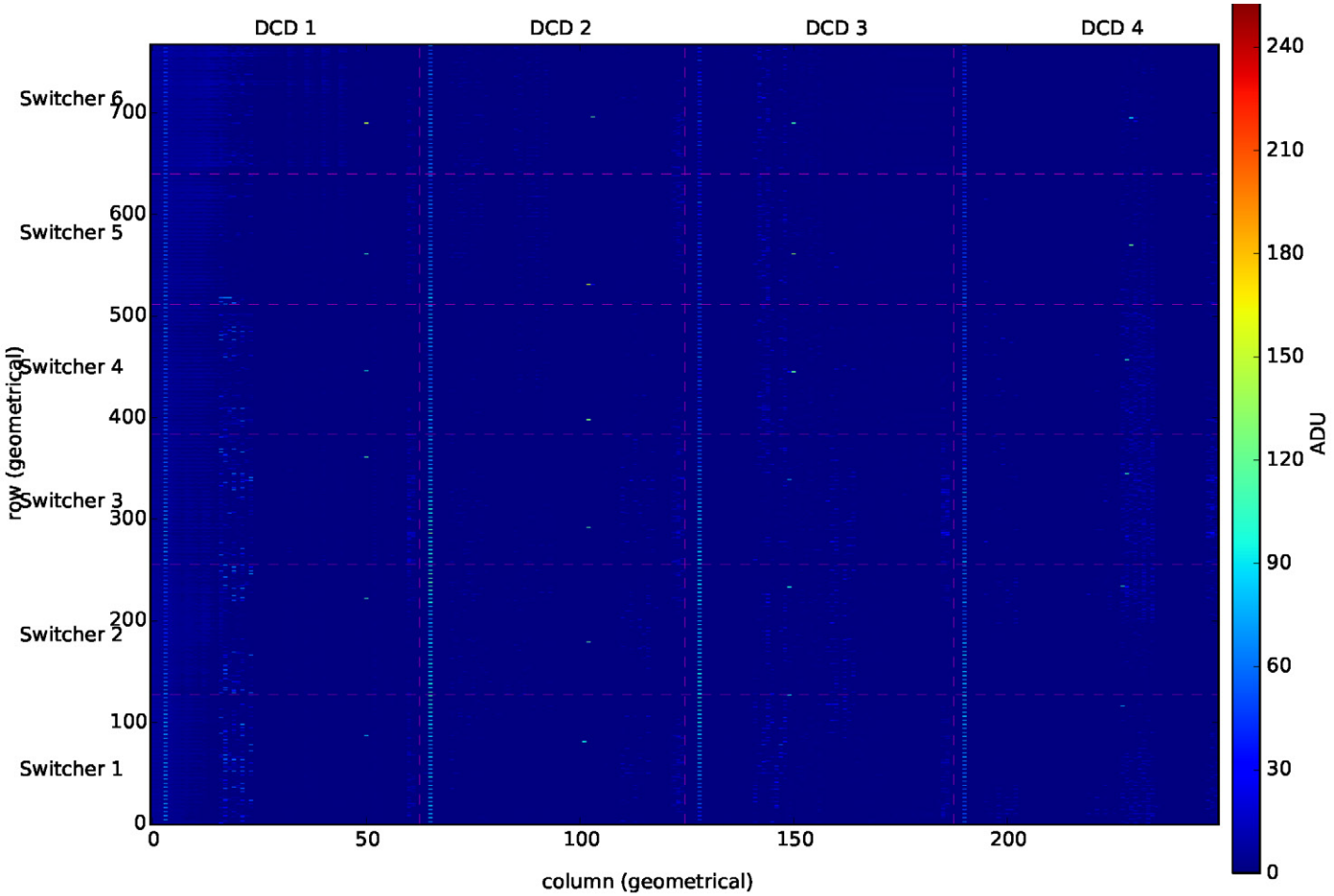


- Control signals SerIN, Clk, StrC, StrG generated by DHPT
- DHPT parameters for setting swing of the control signals sw_tx_06, sw_tx_12, sw_tx_30
- No SMD components for termination but internal resistors in Switcher ASICs

Laser scan over W30-OB1

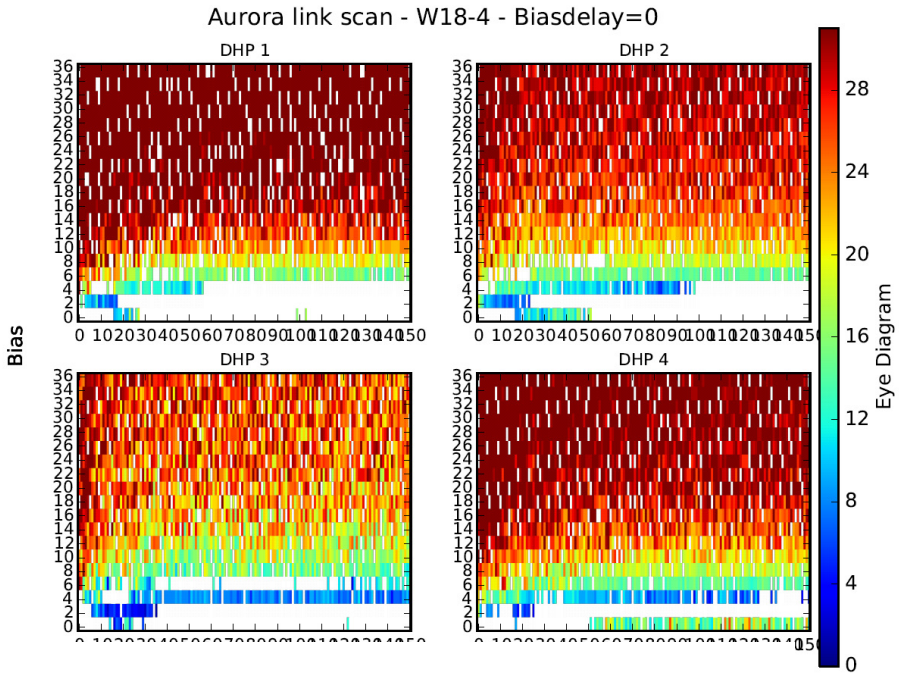
Laser signal ~2-4mip, **read out at full speed** with a noise of ~1.8 ADU (laser instability and system noise)

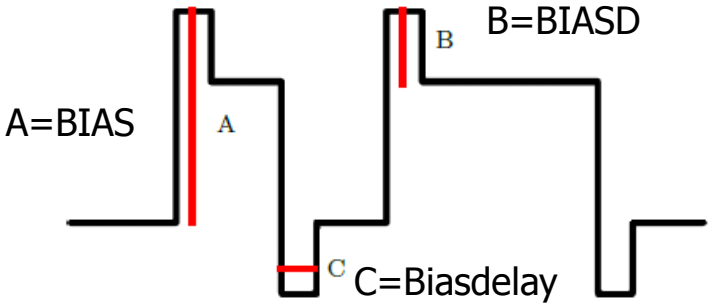
~105 ns/row, of which ~26ns are used for clear pulse (8 ticks of 32)



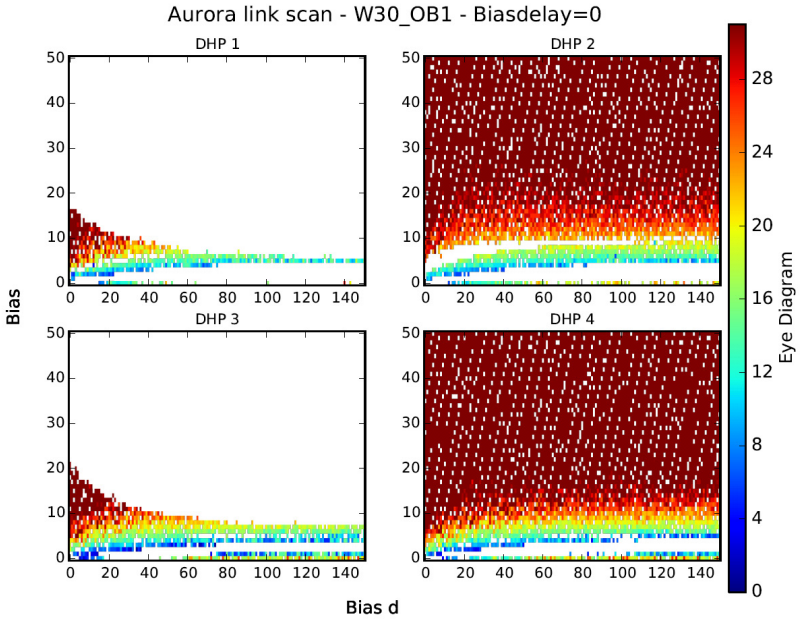
Aurora Link Optimization with DHPT1.0

EMCM

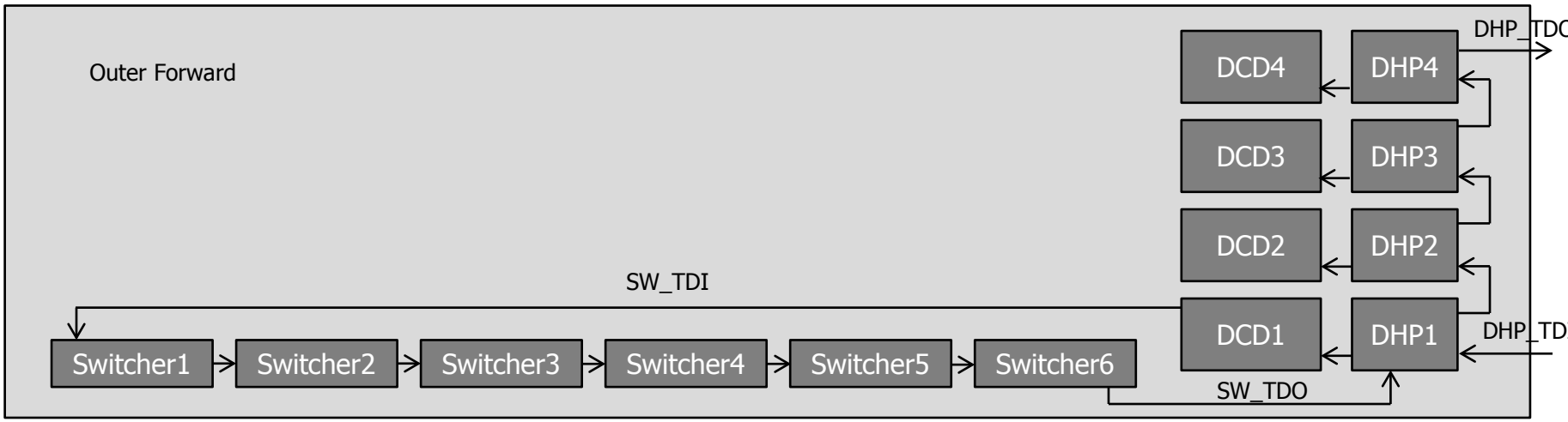




PXD9 Pilot Run



PXD9 Pilot Outer Forward – Boundary Scan (W30-OF1)



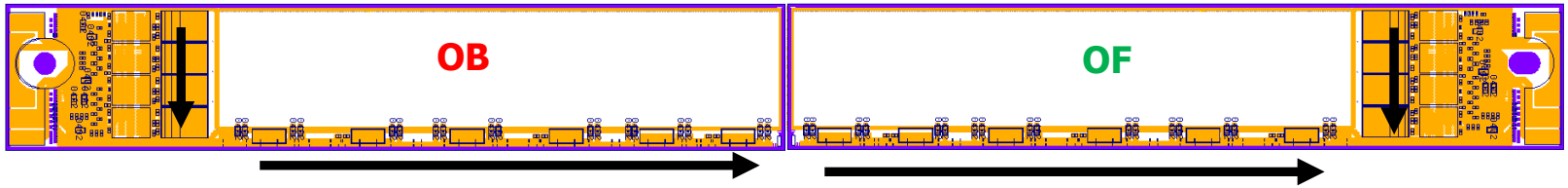
#11140

```
CONNTEST passed

Checking the integrity of the JTAG chain.
CheckChain passed

>>>> PASSED <<<<
```

NAME	RESULT		TIME
⊞ JTAG CON	Passed		1.152
⊞ JTAG Chain	Passed		0.234
TOTAL TIME			1.387

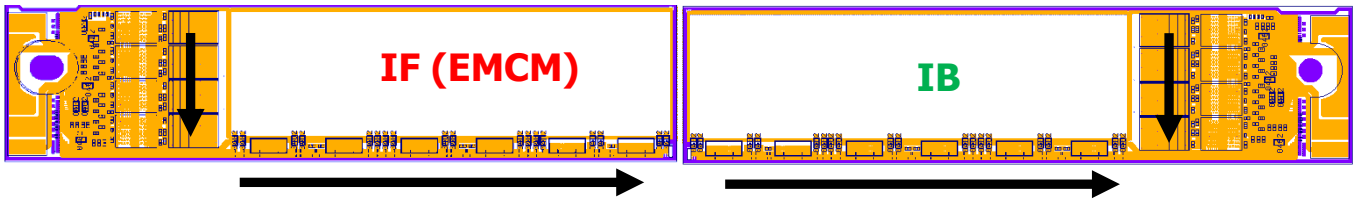
Boundary scan to verify that all ASICs bumps (of digital signals, not DEPFET drains, not switcher Gate & Clear) are properly connected

OB – OF comparison

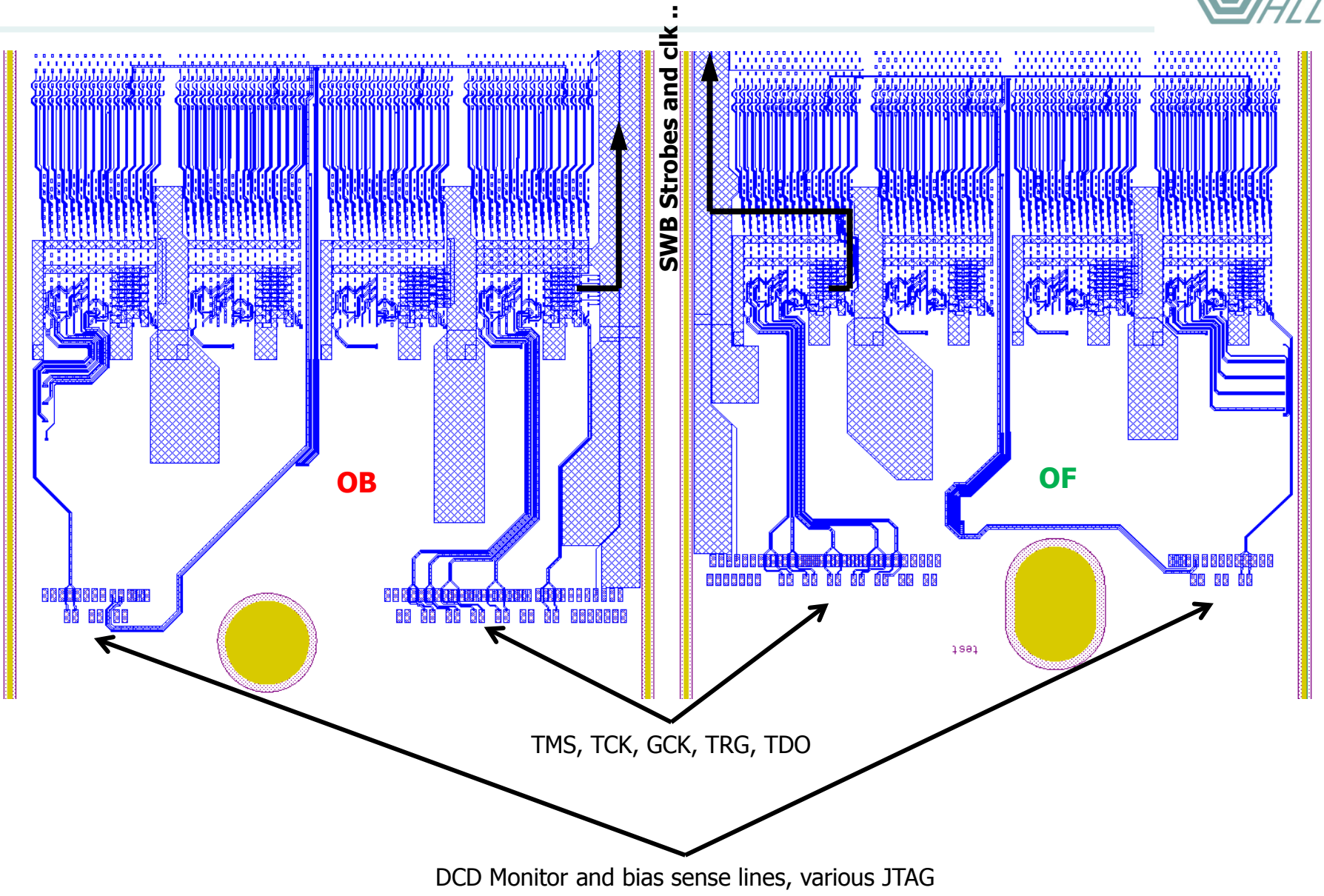


:- different in the direction of the rolling shutter
:- different in the topology of the JTAG chain
:- some differences in the routing of lines …

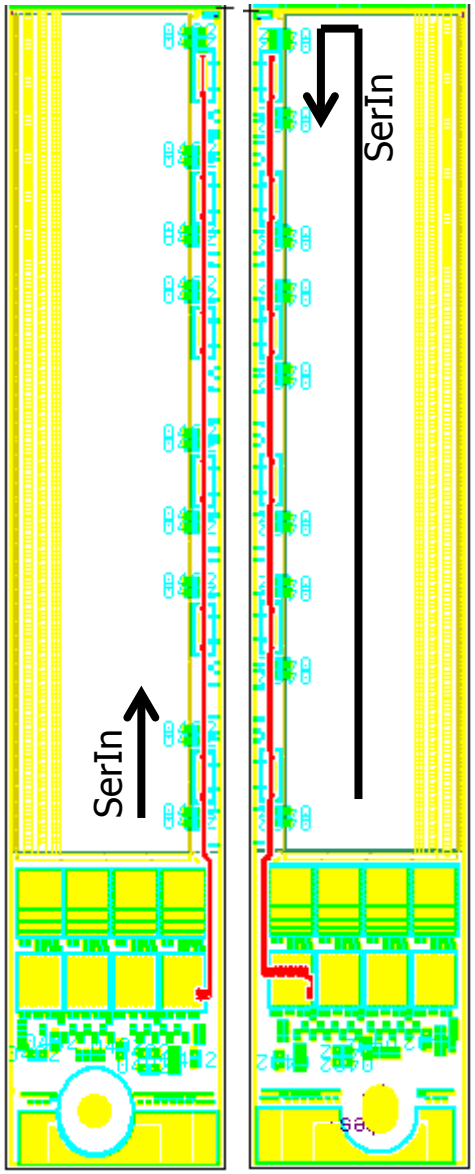
What is actually the difference in metal 1??

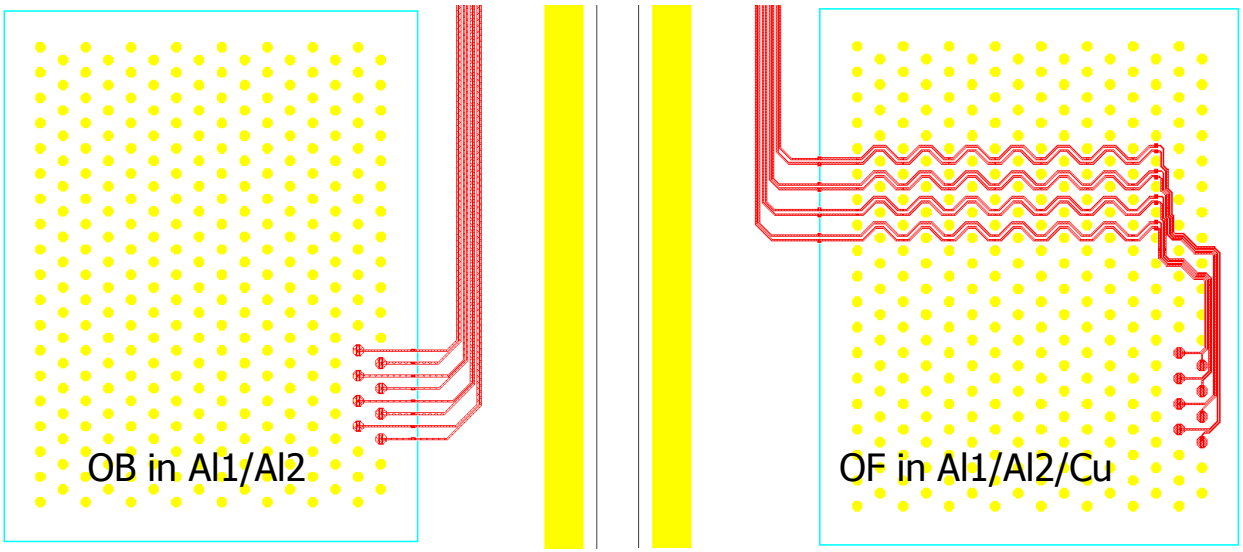


The EOS


SWB Strobes and clk ..
OB
OF
TMS, TCK, GCK, TRG, TDO
DCD Monitor and bias sense lines, various JTAG

OB – OF strobe lines





In addition from DHPT:
:- SerIn goes all the way up to last SWB at the end of OF
:- SerIn starts on SWB close to DHP on OB

Routing on balcony basically the same

→ And the JTAG lines are routed same as the SerIn

Detailed power up sequence (check list)

https://docs.google.com/spreadsheets/d/155aSvn3mvLV5qWFrh0GnLXhELrkM1Mf4Xqo_J7SGIs0/edit#gid=928068883

1	Power up ASICs
2	sanity check: voltages and currents
3	configure JTAG, set termination resistors in Switcher 6
4	sanity check: voltages and currents; DHPT temperature
5	Power Down, Add BoundaryScan Board, Repeat steps 1-4
6	check boundary scan (incl. DHPT-DCD links)
7	Power Down, Disconnect BoundaryScan Board, Repeat steps 1-4
8	scan DHPT link parameters (amplitude, boost, delay)
9	Set optimal aurora parameters into inifile
10	PowerCycle of System (ASICs, DHE, EPICS of DHH) - Repeat steps 1,4
11	digital test pattern, delay scan
12	program SWB sequence (192 channels) - switch DHPT output still on
13	increase DCDPP current limit
14	increase current limit of VDDA (3000mA), AmpLow (1300mA)
15	enable DCDPP analog part: analog CMC off, no pedestal correction

16	sanity check: voltages and currents
17	check test pattern again
18	Manual Delay tuning (raw data read-out => minimize noise)
19	Check electrical isolation between DEPFET and JIG
20	Increase current limit of Source to 150mA
21	Set GateOn in step 23 to 0V
22	power up DEPFET voltages
23	sanity check: voltages and currents;
24	raw data read-out, 1 single DHP
25	check: pedestal distribution, noise
26	check: response on light (laser)
27	set Gate_On to Gate_Off
28	sampling point scan
29	optimization of DEPFET voltages,
30	store pedestal values for 2-bit DAC offset correction
31	upload pedestals for zero suppressed readout
32	trigger zero suppressed frames (no data should arrive)
33	Laser spot (move laser accros the matrix)
34	Source measurement

PXD9 Pilot Verification Plan – out-dated

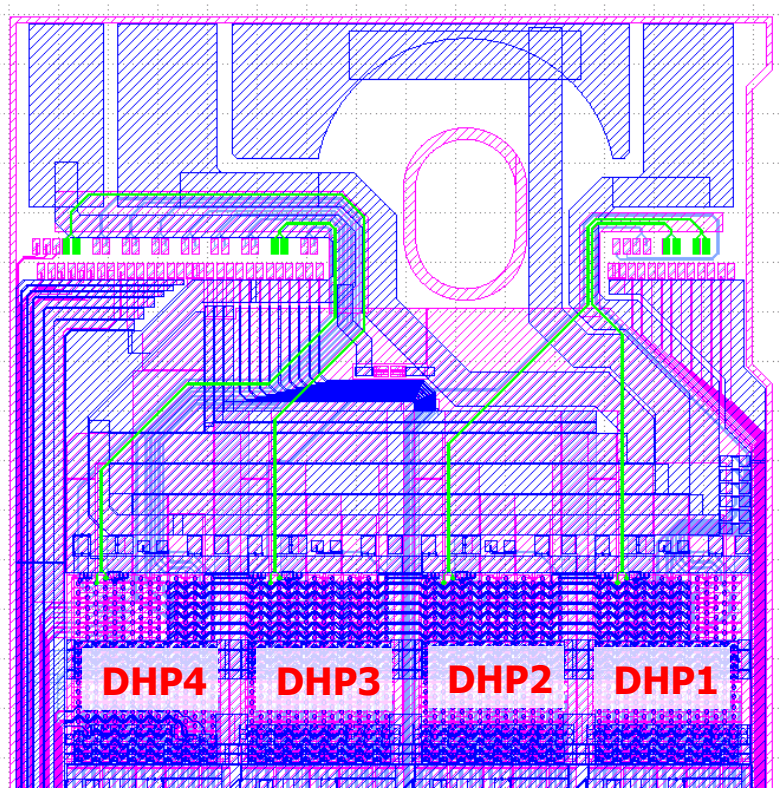
<table>
<tr><td></td><td>9.13. Nov</td><td>16.-20. Nov</td><td>23.-27. Nov</td><td>30. Nov - 4.Dec.</td><td>7. Dec. - 11. Dec.</td><td>14. Dec. - 18. Dec.</td><td>Dec. 2015 / Jan. 2016</td></tr>
<tr><td>CW</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td><td>51</td><td>47</td></tr>
<tr><td>HLL (pxdtest2)</td><td>sampling point scan</td><td>increase to nominal freq.</td><td>gated mode</td><td rowspan="5">PXD9 SeeVogh Meeting</td><td>DHPT serial link
- IBERT/oscilloscope</td><td rowspan="9">Go for PXD9 Alu1 metallization and agreement on the necessary changes

Technical Board Meeting

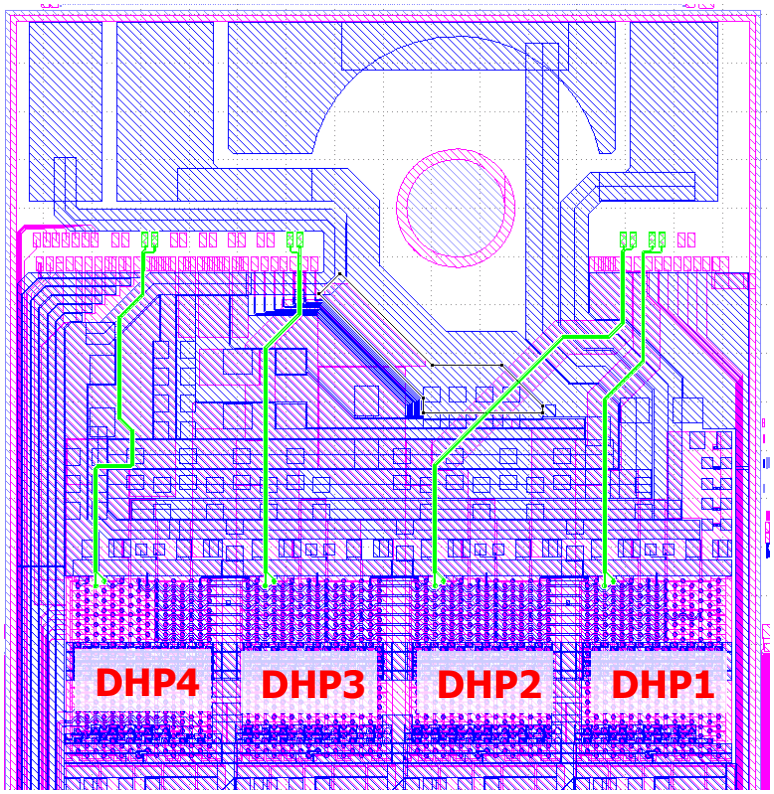
Dec. 15th</td><td>gated mode</td></tr>
<tr><td></td><td>pedestal/noise all DCDs</td><td>DHPT serial link
- IBERT/oscilloscope</td><td>pedestal compression</td><td>Cd109 spectrum
Clear voltages / sequence</td><td></td></tr>
<tr><td></td><td></td><td>DCD <-> DHPT (delay)</td><td>Cd109 spectrum</td><td>Common Mode Noise</td><td></td></tr>
<tr><td></td><td></td><td>sampling point scan</td><td>Laser spot</td><td></td><td></td></tr>
<tr><td></td><td></td><td>pedestal/noise all DCD</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>zero suppressed data</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>HLL (pxdtest4)</td><td colspan="3">Preparation Gated Mode Test
EMCM</td><td colspan="4">Hybrid 7 Testing
to verify OF/IB balcony and EOS layout</td></tr>
</table>

Aurora Link Scan

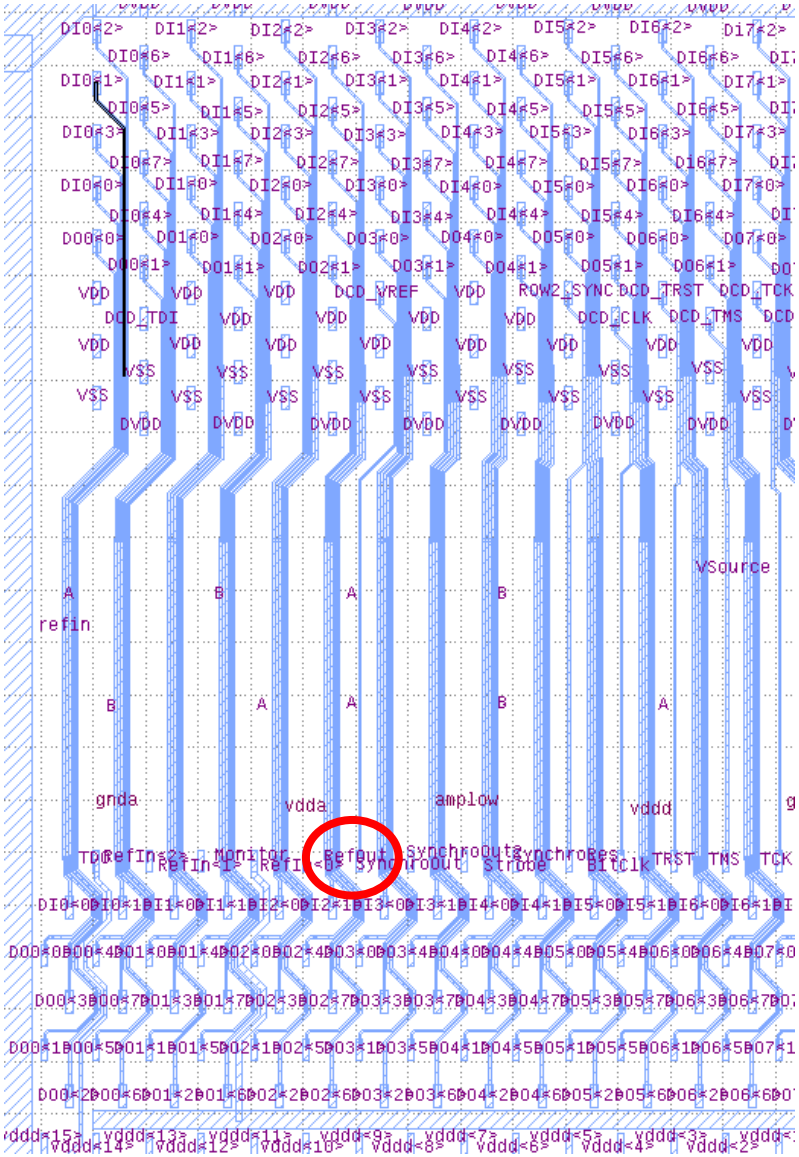
EMCM
High speed signal routing in Aluminum**1**



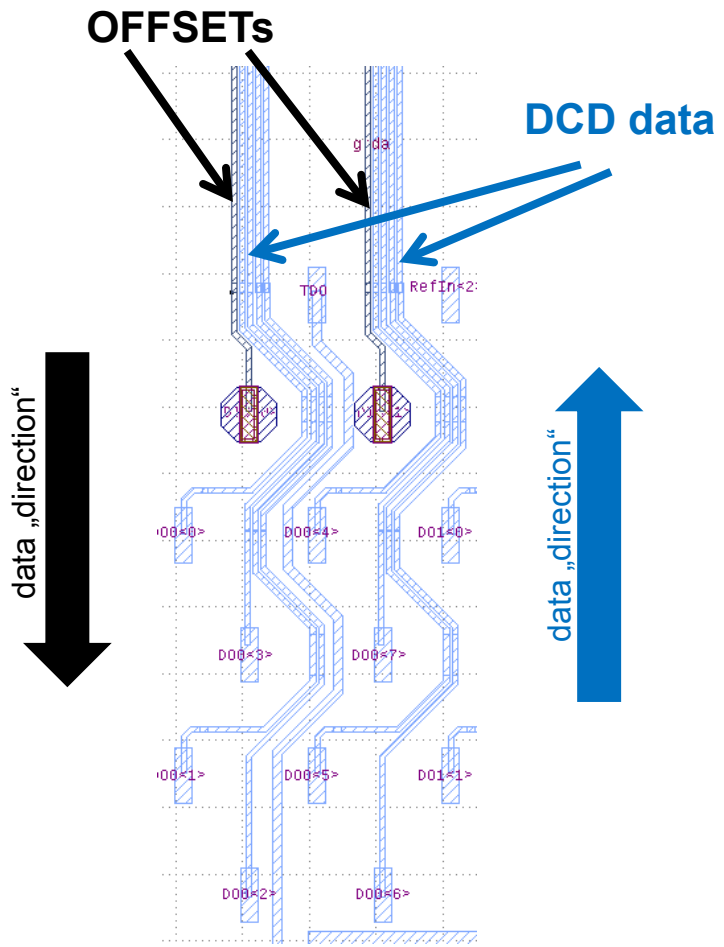
PXD9 Pilot Run
High speed signal routing in Aluminum**2**



Crosstalk-Offsets - Introduction

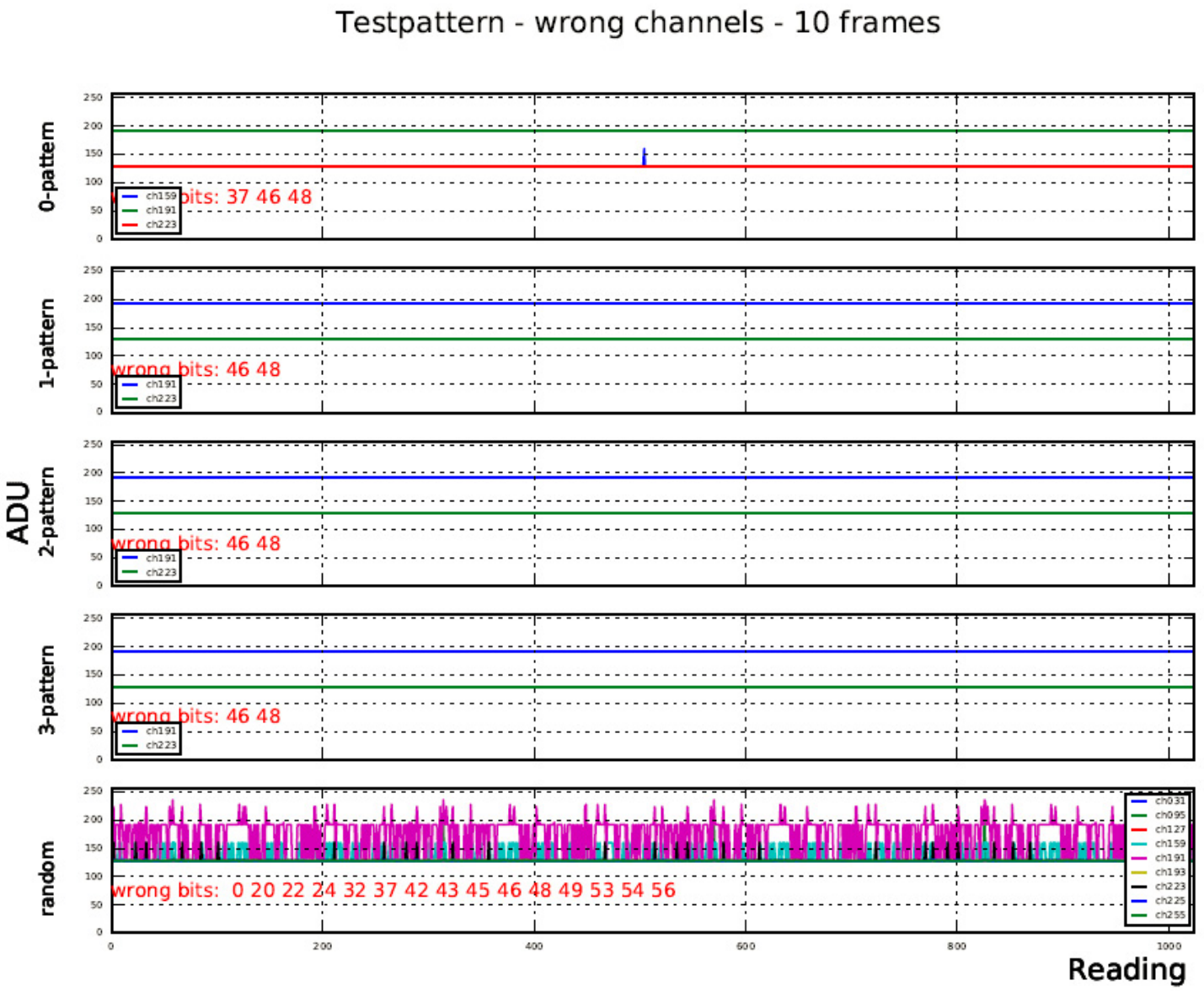


1 Columnpair, i.e. 32DCD channels

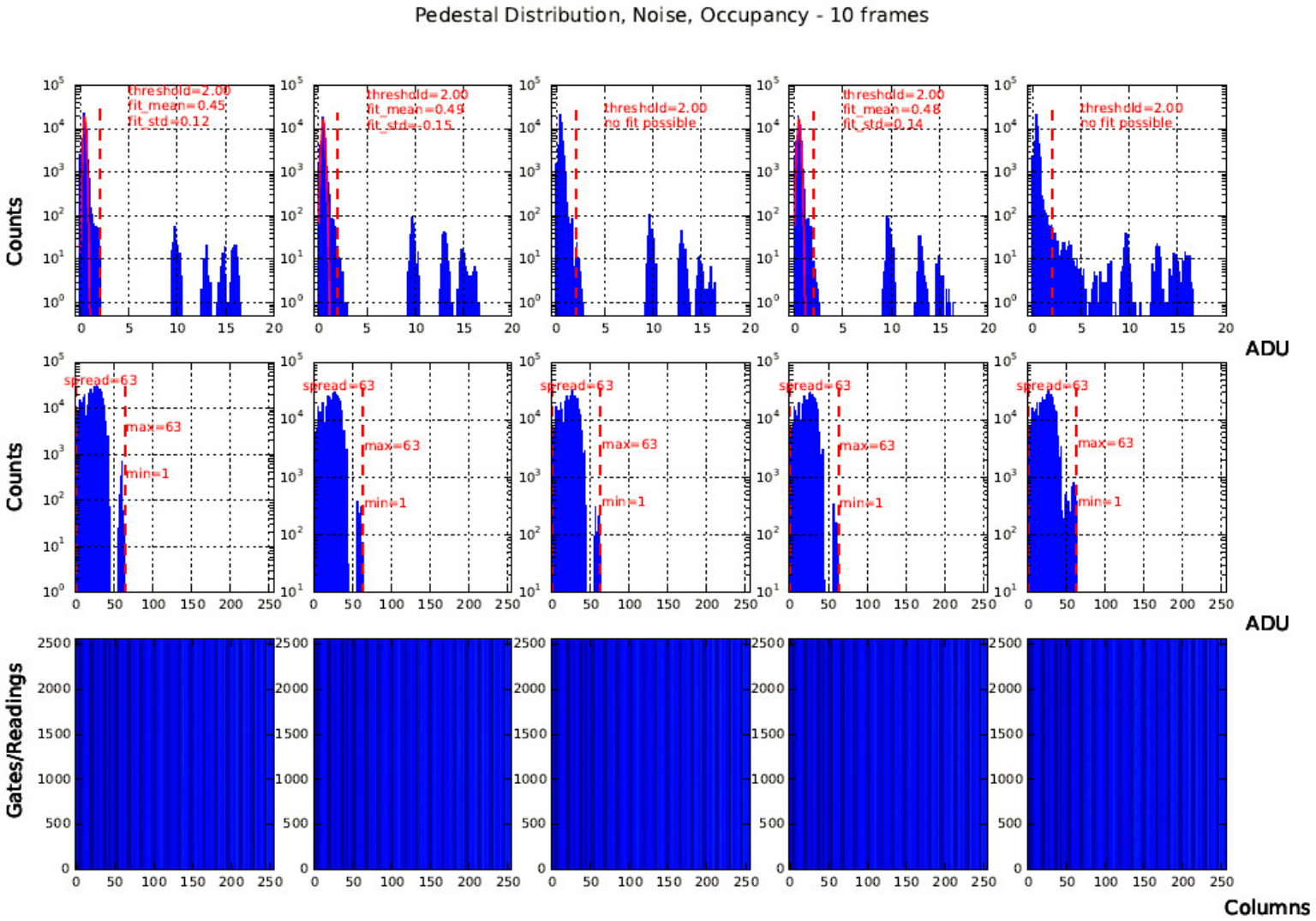


Is there a crosstalk between OFFSETs and DCD data?

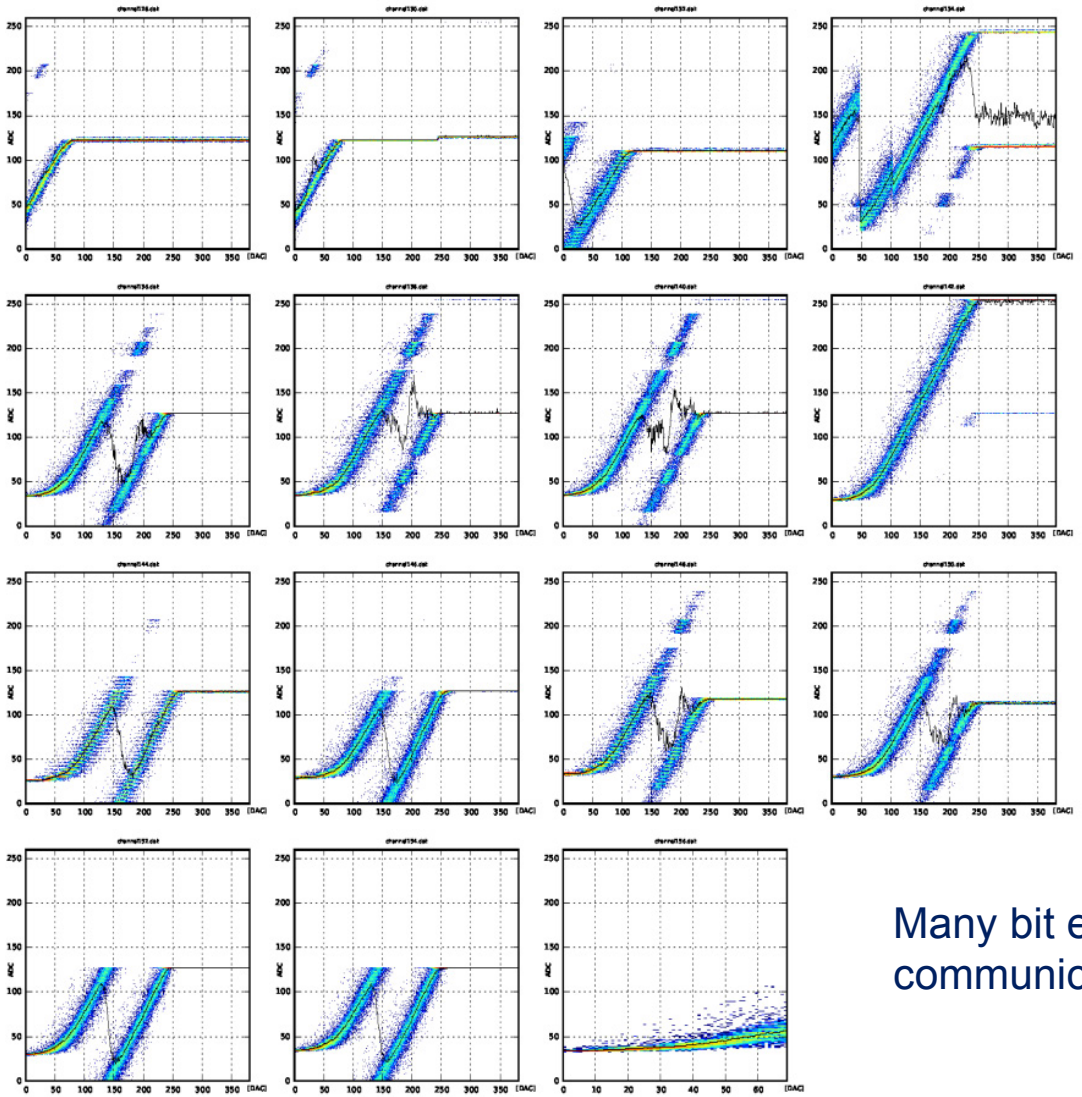
Cross Talk – EMCM W18_3 – 76.23MHz – DCD4



Cross Talk – EMCM W18_3 – 76.23MHz – DCD4



W30-OB1 ADC Transfer Curve



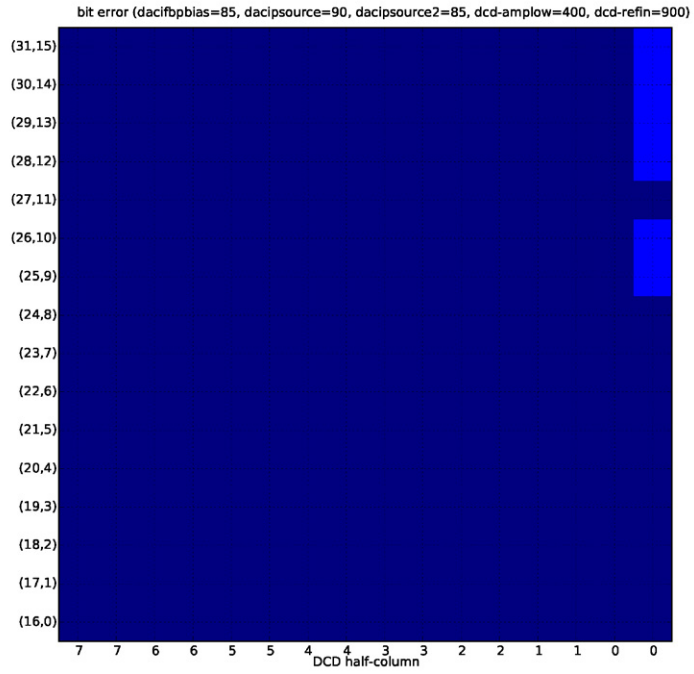
- GCK = 76.23 MHz
- DCD_DVDD = 1.9V, DHPT_IO = 1.8V, DHPT_Core = 1.64V

Many bit errors in the DCD-DHPT communication

W30-OB1 ADC Transfer Curve – increased supply voltage

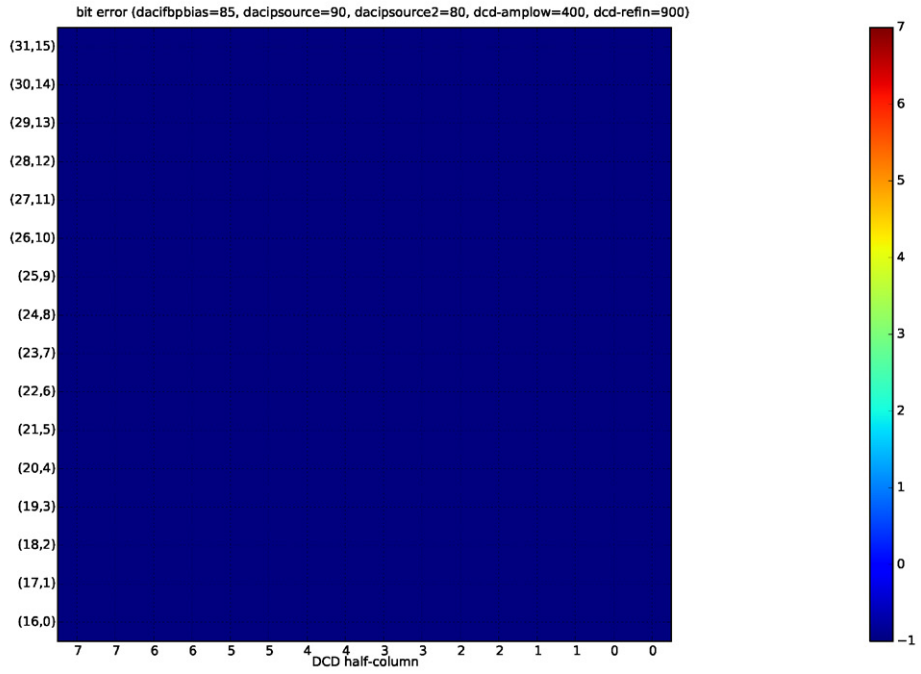
- GCK = 62.5 MHz
- DCD_DVDD = 2.2V, DHPT_IO = 2.1V, DHPT_Core = 1.64V
- Delay Scan using the DCD test pattern
- ADC transfer curves using the DCD internal current source I_Sig_Mirror
- ASIC-pairs 3 + 4 all channels (but only 2 x 2 IPSource/IPSource2 settings)

D3-R3



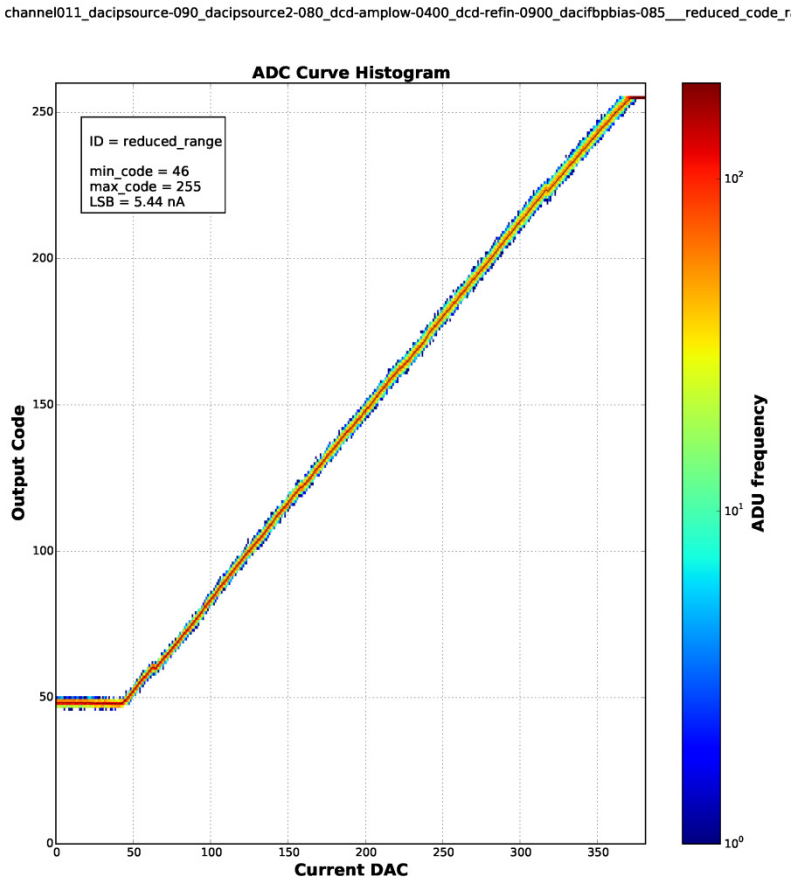
6 channels showed bit errors

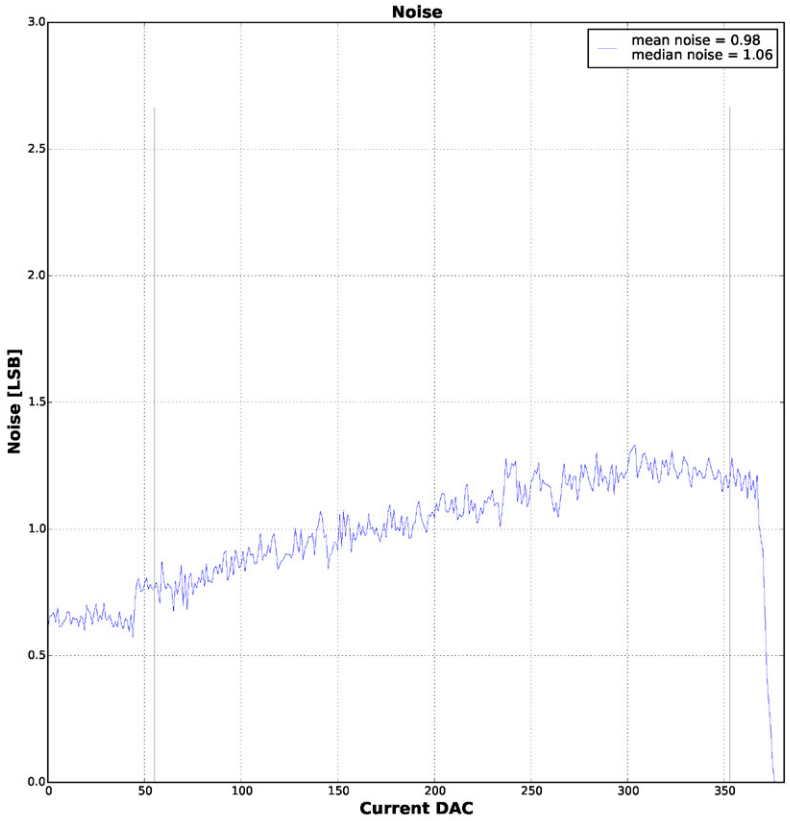
D4-R4



No bit errors

W30-OB1 ADC Transfer Curve – increased supply voltage





- R4 (asic-pair 4) channel not connected to DEPFET matrix
- GCK = 62.5 MHz