SI LAB
Silizium Labor Bonn

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DHPT 1.1 Testing

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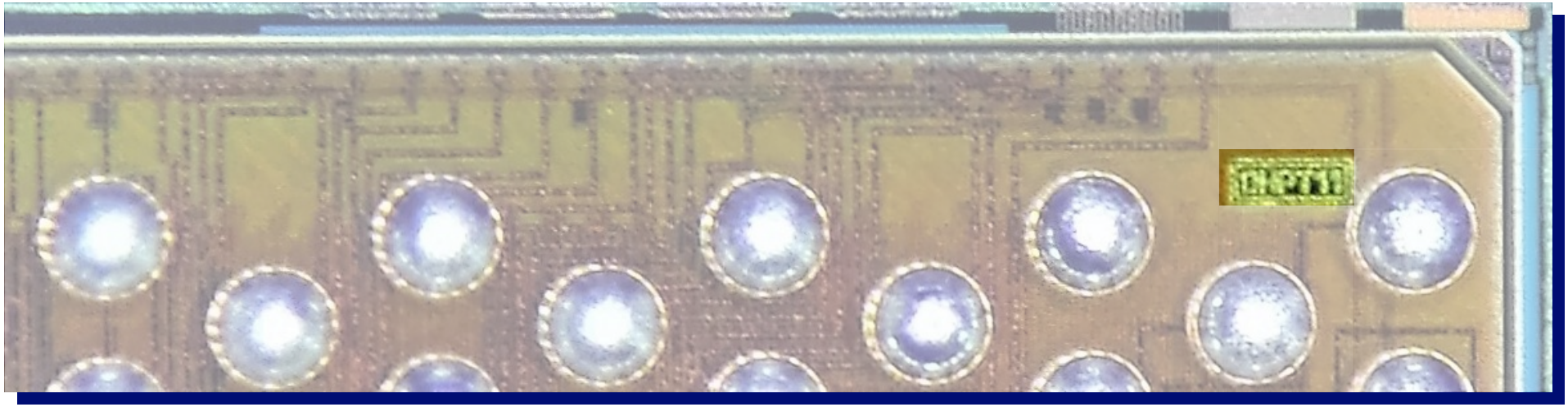
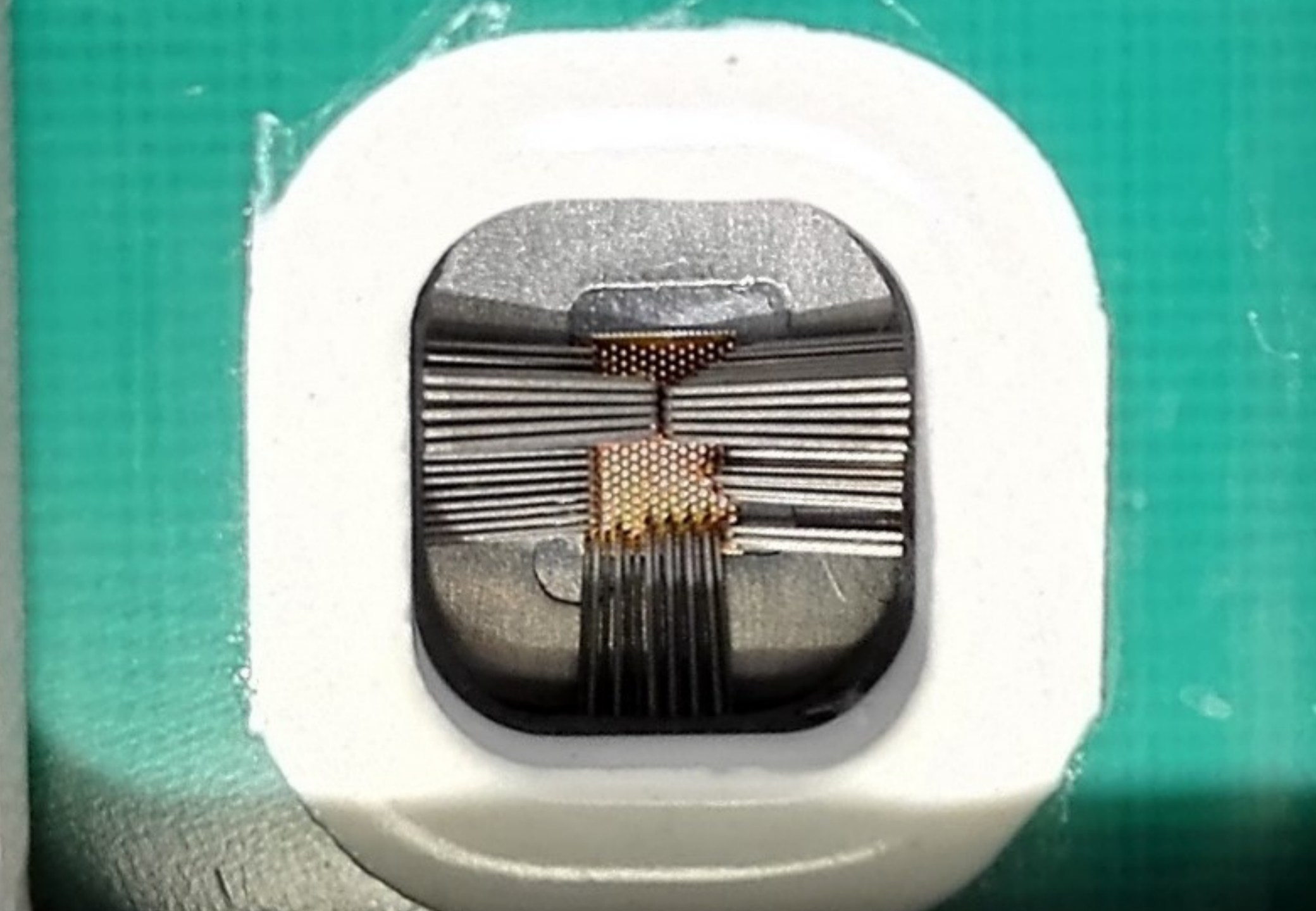
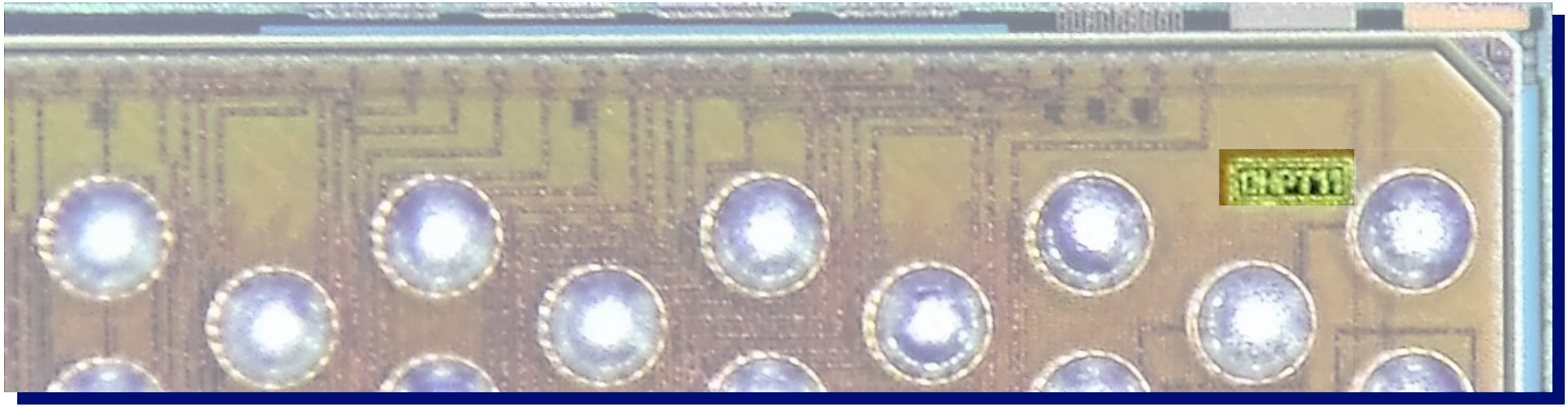




Changes from DHPT1.0 to DHPT1.1

Setup and test environment check



Results

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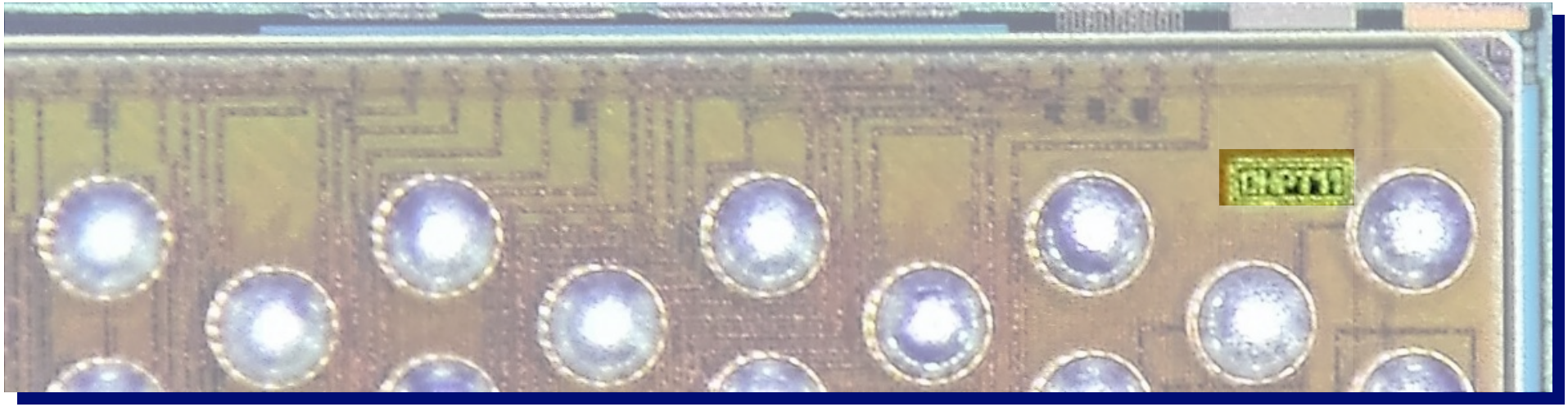
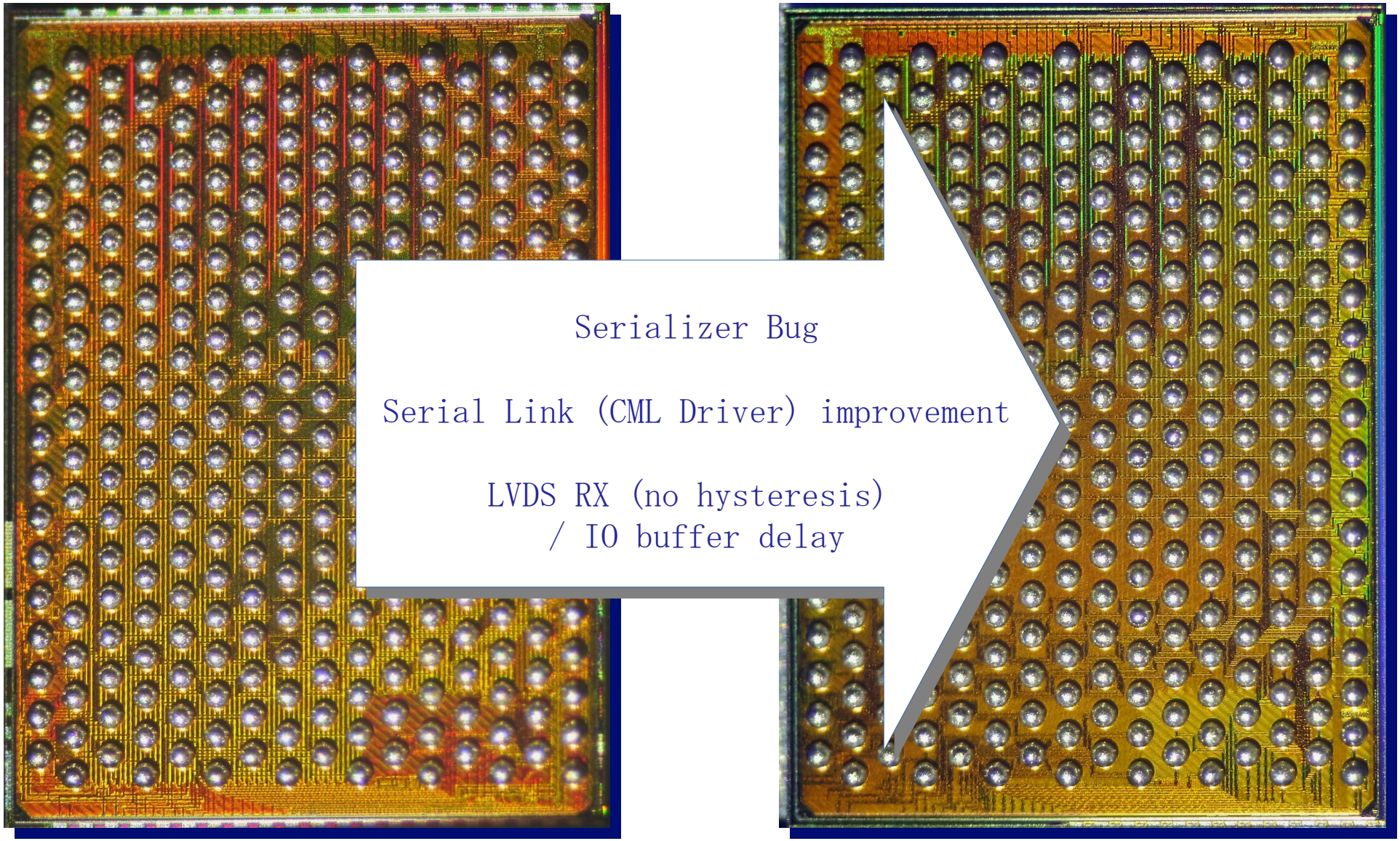
Changes from DHPT1.0 to DHPT1.1

Setup and test environment check



Results

Changes DHPT 1.0 → DHPT 1.1



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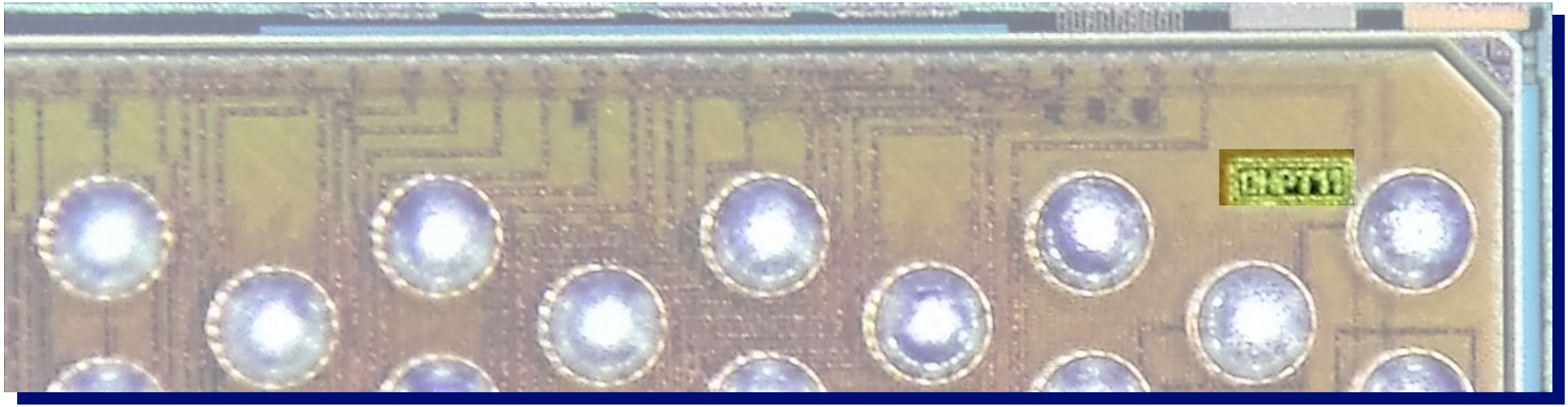


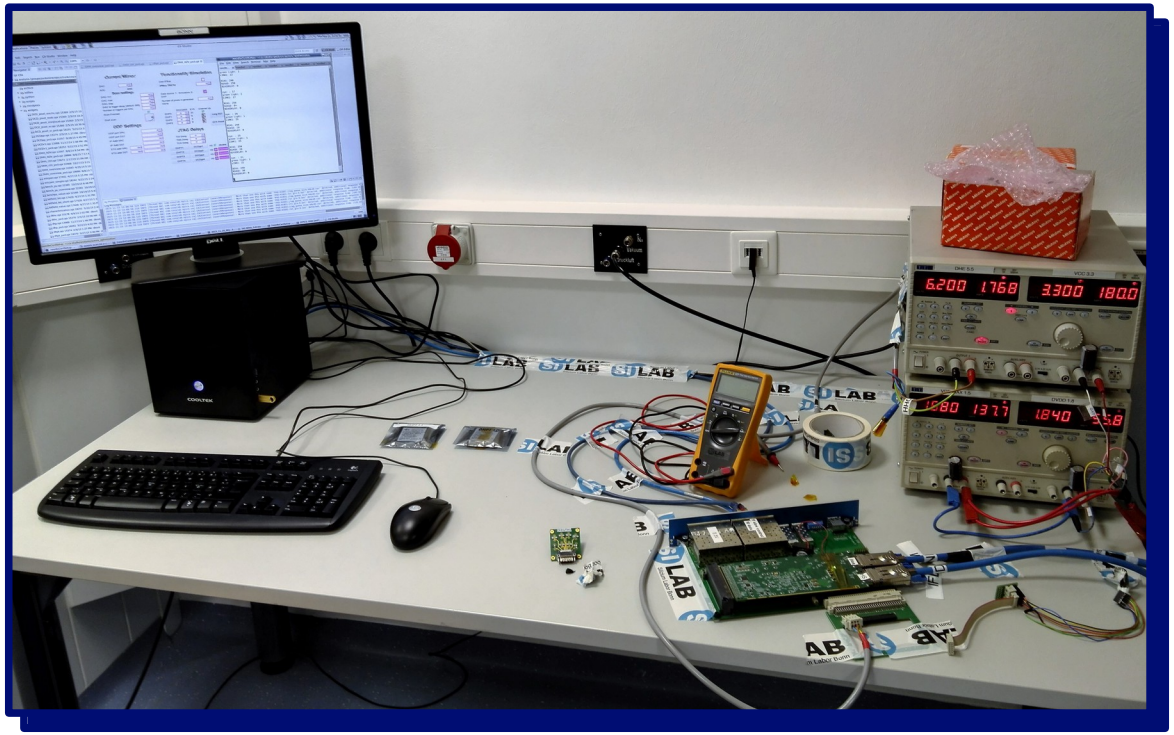
Results

PC
(EPICS - DHH software)

TTI PSU
(DHH, DHPT VDD,
DHPT DVDD, FPGA VCC)

DHE

2x TWP (10m Infiniband cable)



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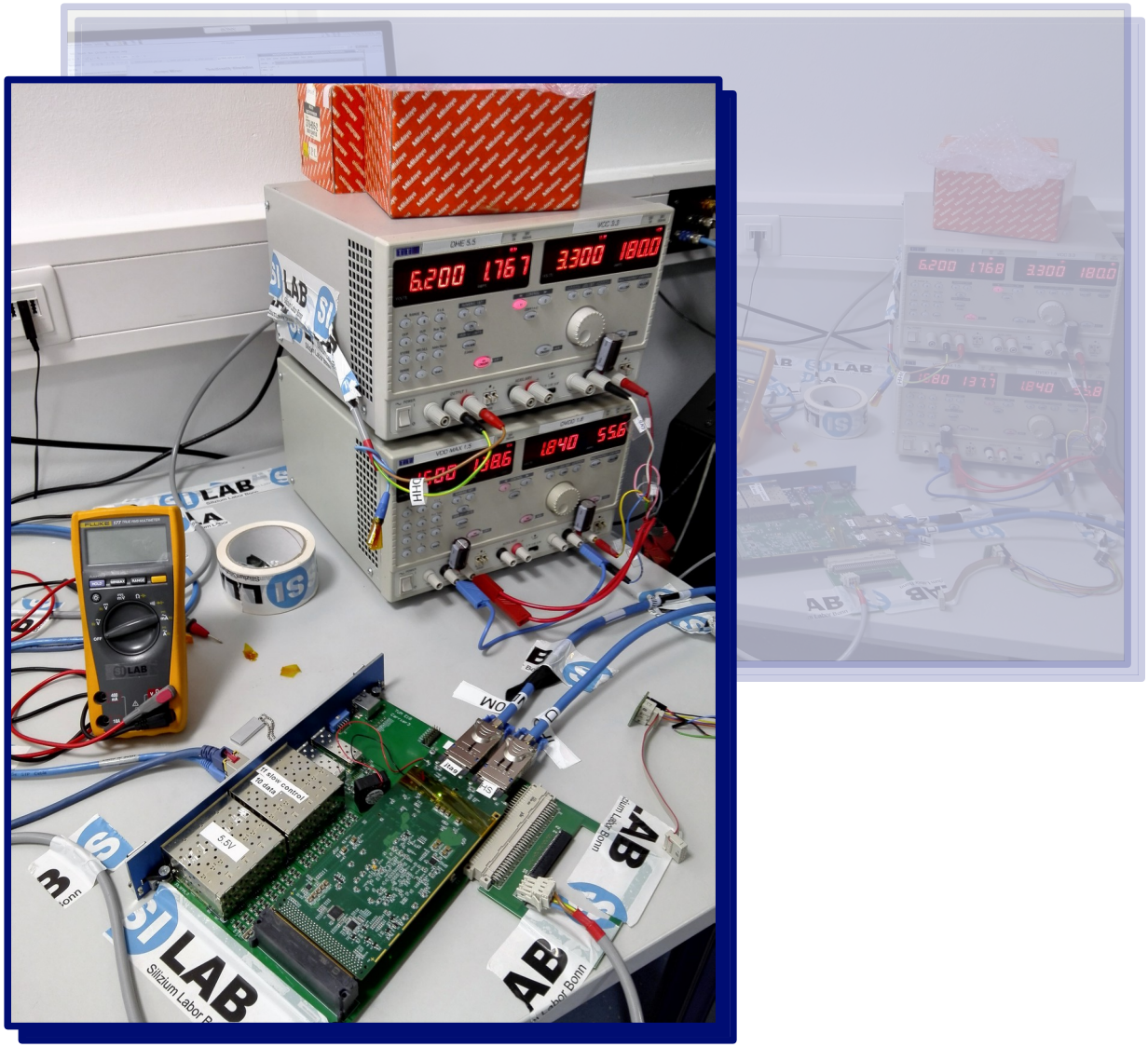
Voltages not sensed

VDD (*here DHPT 1.0)
1.68V

DVDD (*)
1.84V

DHE
6.2V (on board 5.4V)



Changes from DHPT1.0 to DHPT1.1

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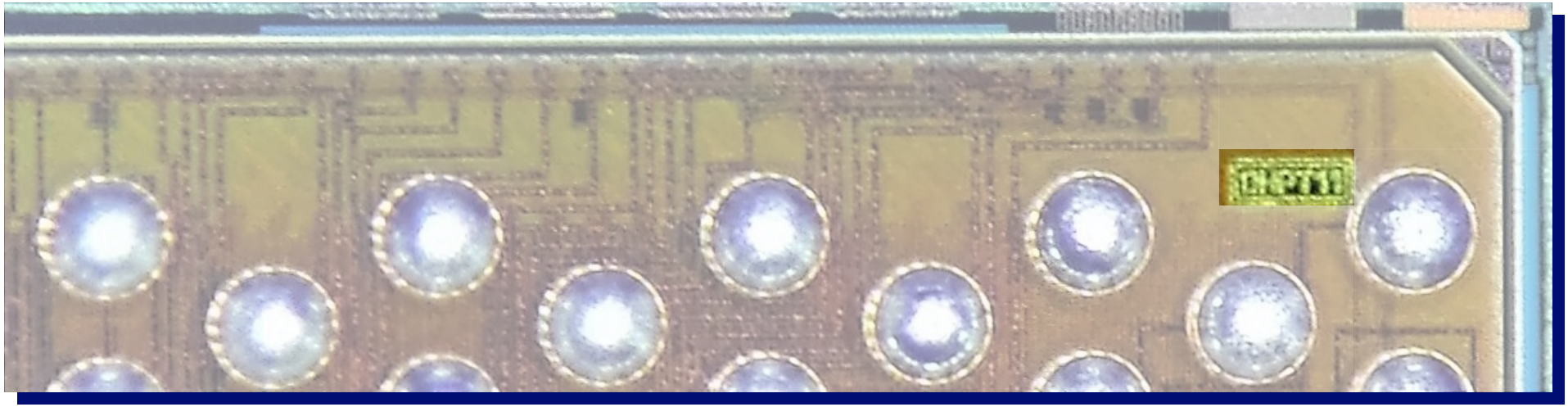


Results

Before DHPT 1.1 has been tested a DHPT 1.0 has been tested as reference

Digital checks for DHPT 1.1:

Jtag communication DHE & DHPT

Memory tests

Link established
(down to VDD 1.25V !unsensed!)
No do_cc dependence anymore
(clock compensation for aurora protocol)

CML driver parameter space improved

Large area with stable link (see next slide)

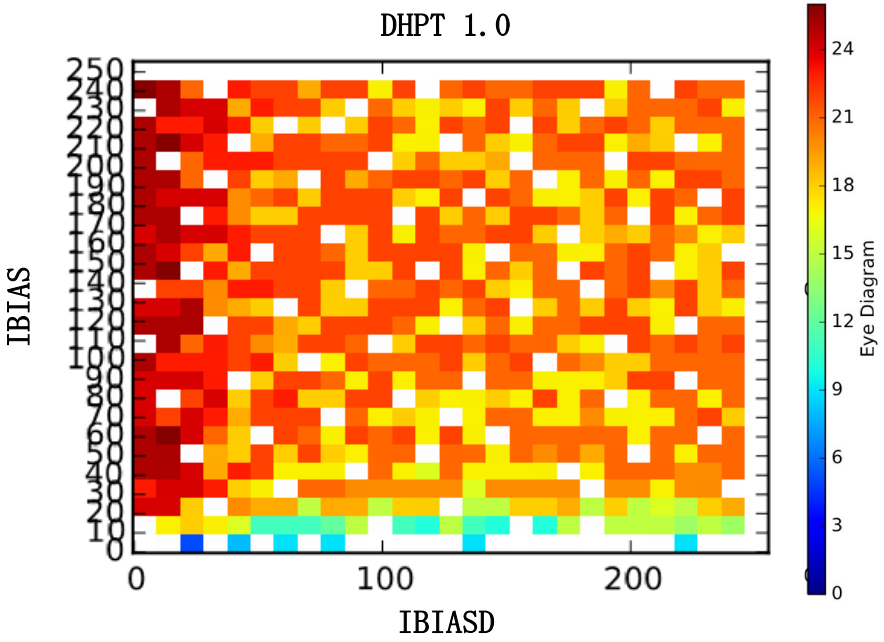
CML driver

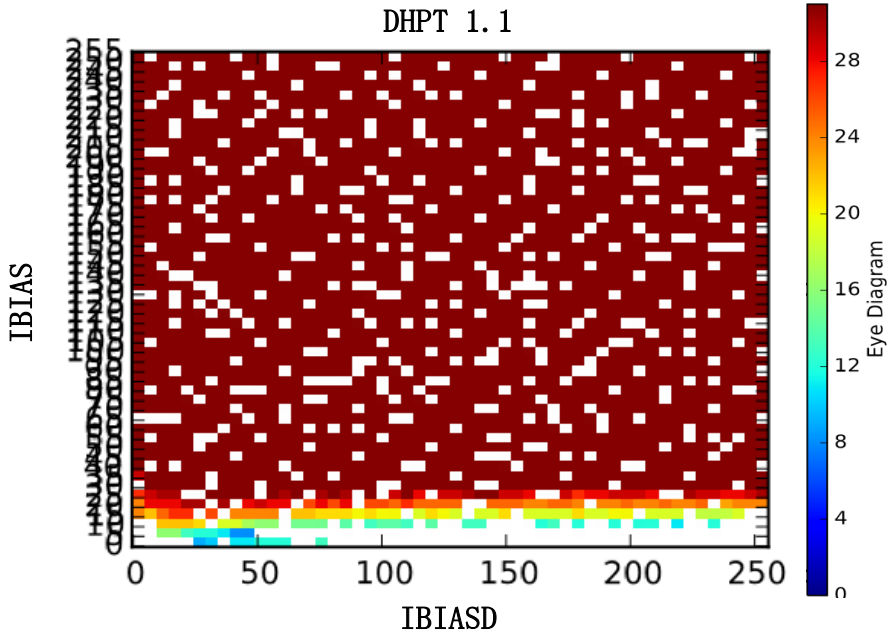
Scan over parameter space

IBIAS, IBIASD and pll_cml_dly

Without RXEQMIX usage (no receiver equalizing)

Examples for pll_cml_dly = 0 and GCK = 62.5 MHz





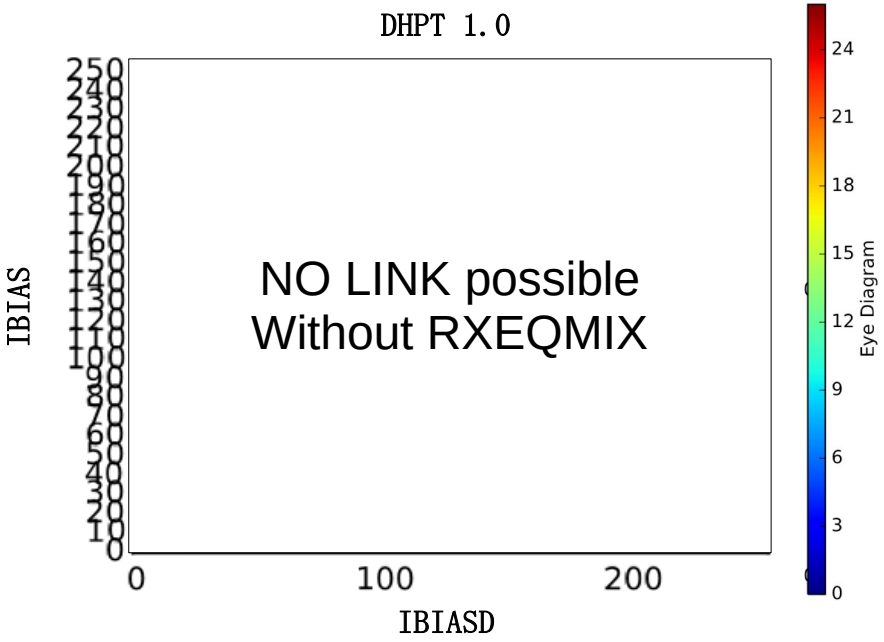
CML driver

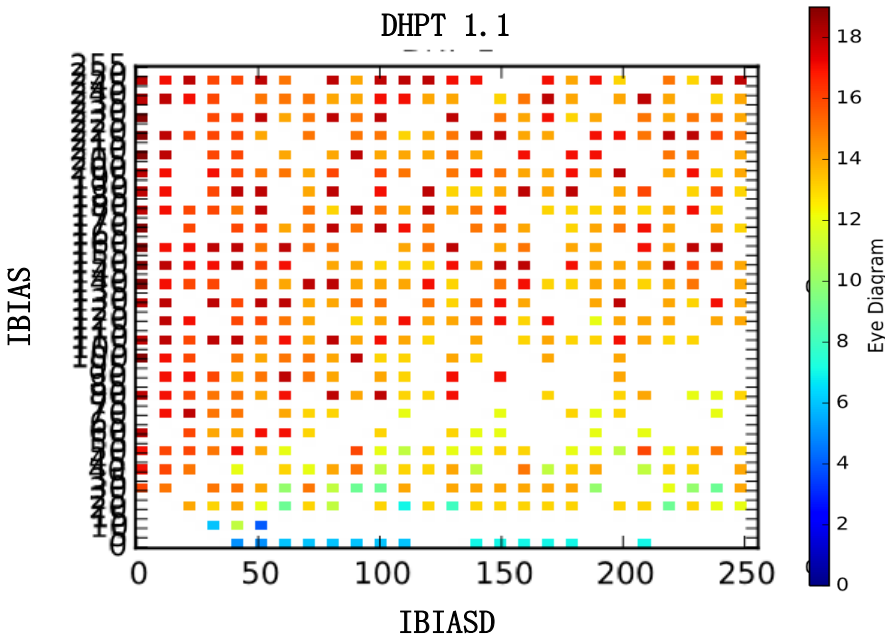
Scan over parameter space

IBIAS, IBIASD and pll_cml_dly

Without RXEQMIX usage (no receiver equalizing)

Examples for pll_cml_dly = 0 and GCK = 76.23 MHz





- For further verification (DHPT & DCD interface) test boards (Hybrid 5, DHPT standalone board, etc) are necessary!

- Signal integrity with final DAQ chain, i.e.
  Kapton + PatchPanel + Transmission line
  in order to investigate the margin of the CML driver working point

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Thank you

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