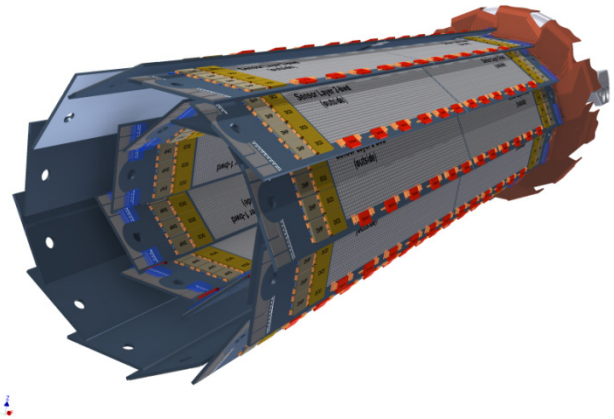
DEPFET-LAB
Dec 2, 2015

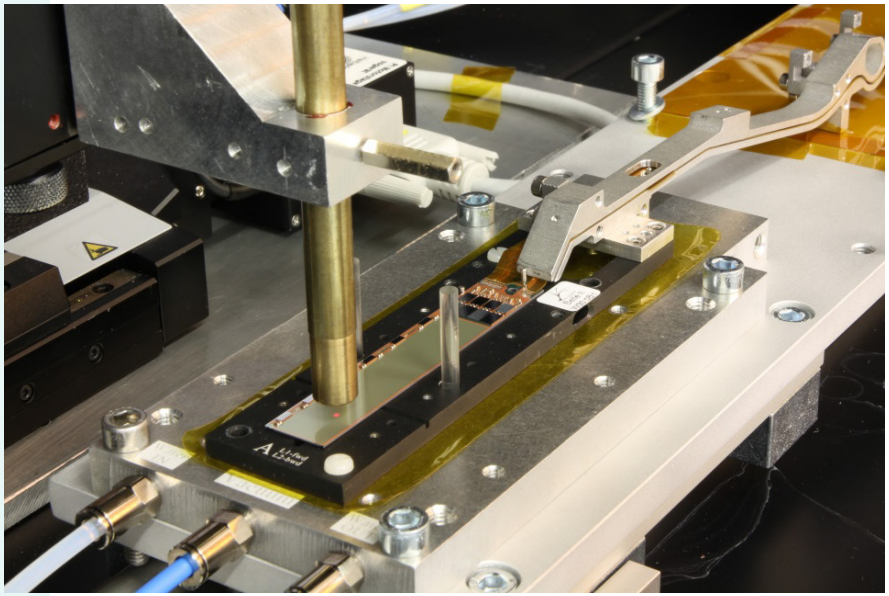
Pilot Run: PXD9 W30_OB1
(Outer Backward)

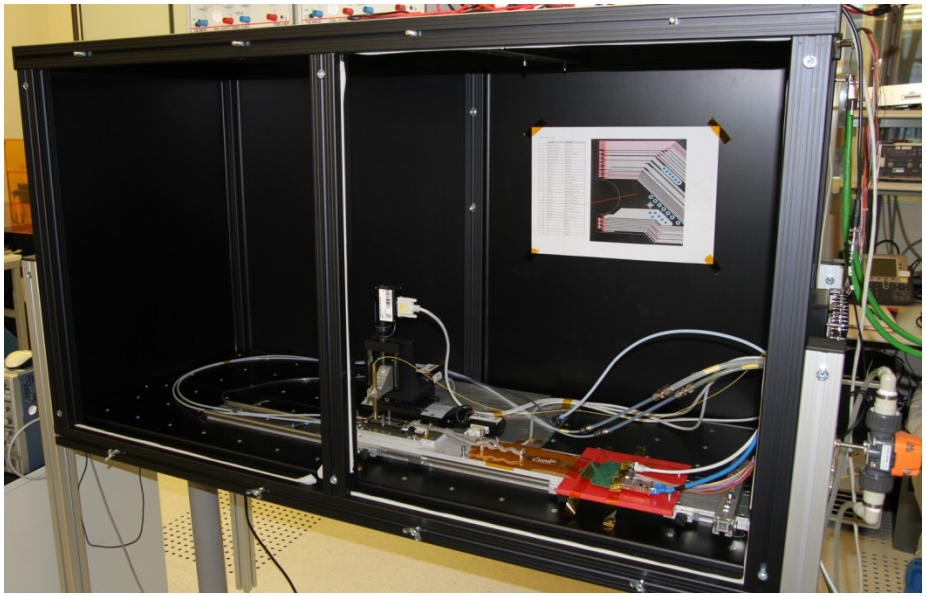


Overview

- Module overview
- Boundary Scan
- DHPT Serial Link Measurements
- Delays
- CrossTalk (EMCM)
- ADC Curve
- Sample Point Curve
  - Switcher Sequence
  - Dependency of Settling Time
  - Adjustment of GateOn/Off
  - Comparision to Hybrid6 (large matrix), EMCM & Hybrid5 (small matrix)
- Noise / Common Mode Contribution / Grounding Scheme
- Zero Suppressed Data taking (masking)
  - Radioactive Source
- PXD9 metal routing
- Open issues and discussion

Pilot Run – W30_OB1

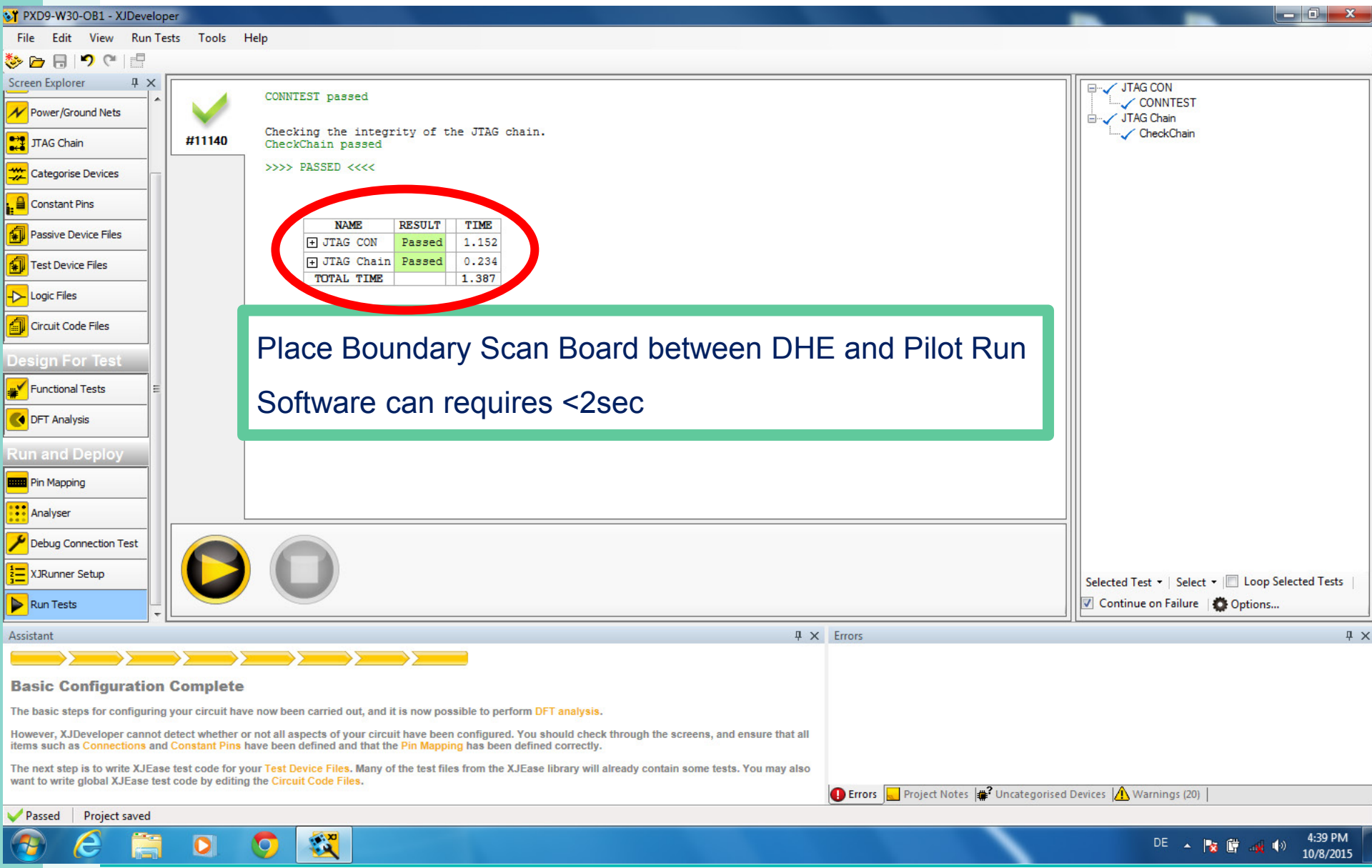




- Power-up ASICs – sanity check voltages + currents
- Configure ASICs via JTAG
- Boundary Scan
- DHPT serial link – parameters of the pre-emphasis
- DCD <-> DHPT communication – timing adjustment
- Sampling point scan
- Pedestal distribution for various GateOn voltages
- Measure DEPFET response (Source, Laser spot, homogeneously illuminated)

4x DHPT1.0
4x DCDpp
6x SwitcherB18v2

Boundary Scan

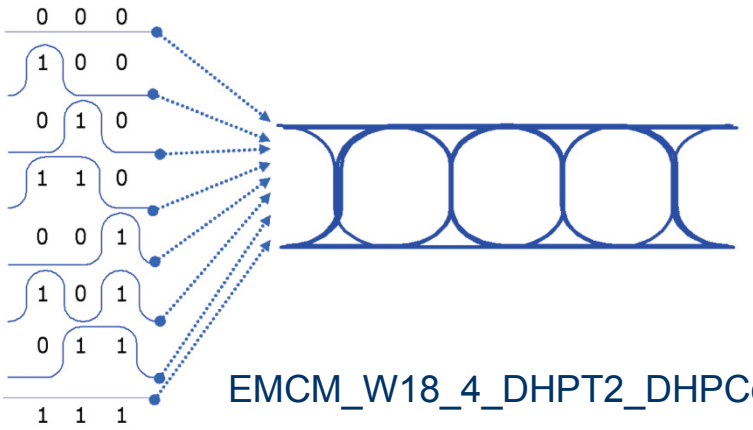


Place Boundary Scan Board between DHE and Pilot Run

Software can requires <2sec

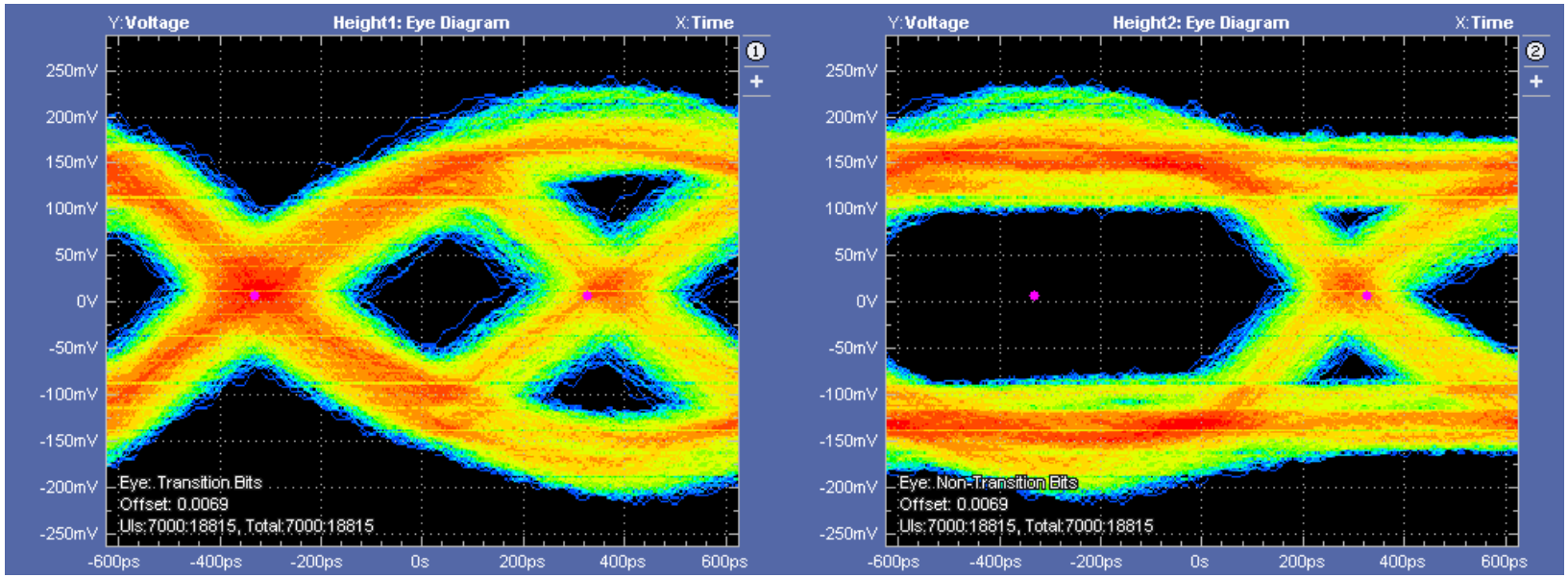
Data Eye - Basics

Tektronix – Application Note: Anatomy of an Eye Diagram 65W_26042_0_Letter



Overlaying of bit sequences to form an eye diagram

EMCM_W18_4_DHPT2_DHPCore1.2V_EyeOpen_50mV_Bias15_BiasD150.png

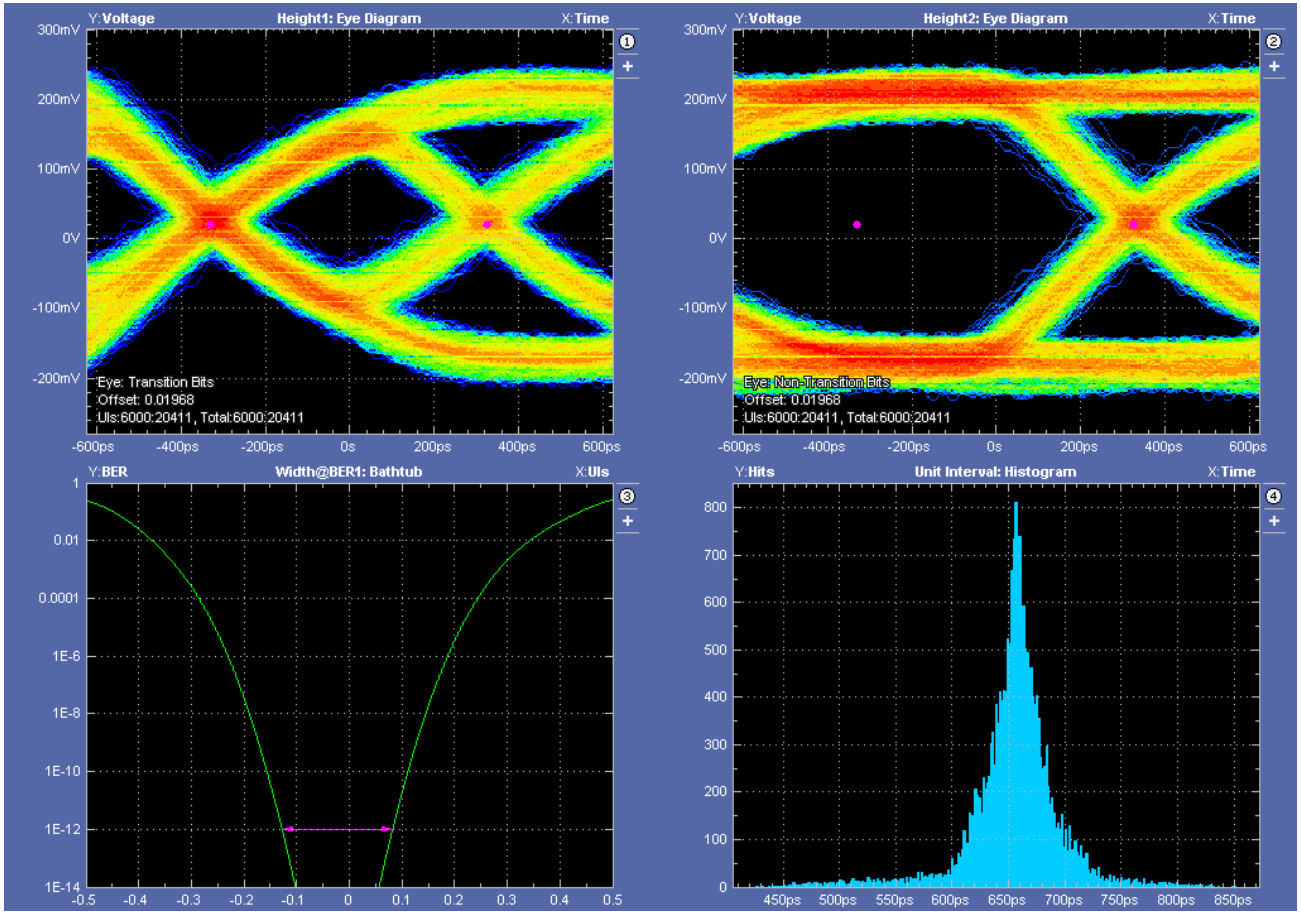


Eye diagram for transition bits and non transition bits (according to the PCI Express compliance).

Data Eye - EMCM

DHP3_1.2V_76.23MHz_Bias15_BiasD30BiasDelay50_bath_UI.pngg

- Using DHPT pseudo random bit pattern
- pll_cml_dly_sel = 0
- BiasDelay is not used in DHPT1.0
- 48cm Kapton + Patch Panel with Infiniband connector + 3m Infiniband cable

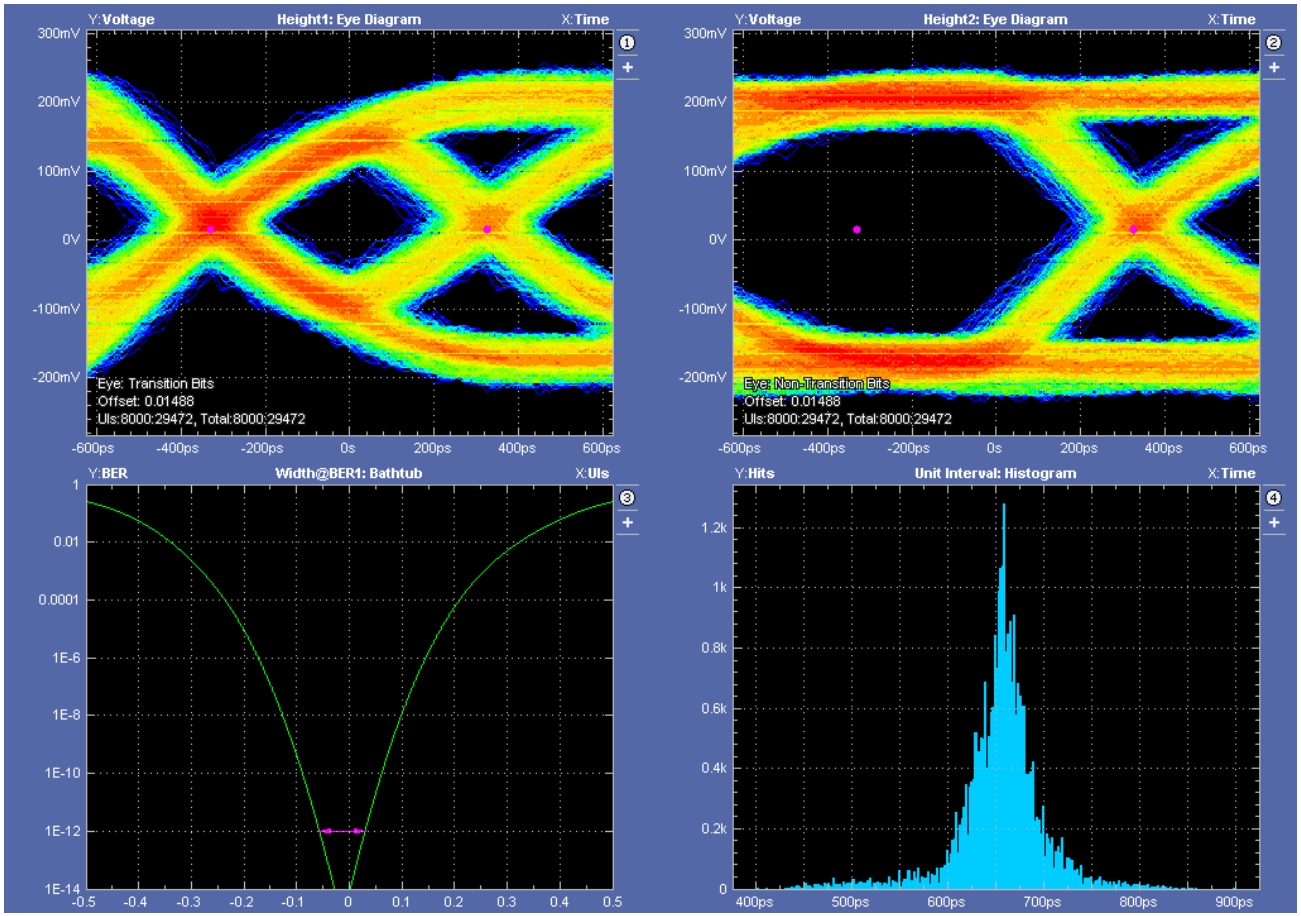


DCDs analog: OFF

Data Eye - EMCM

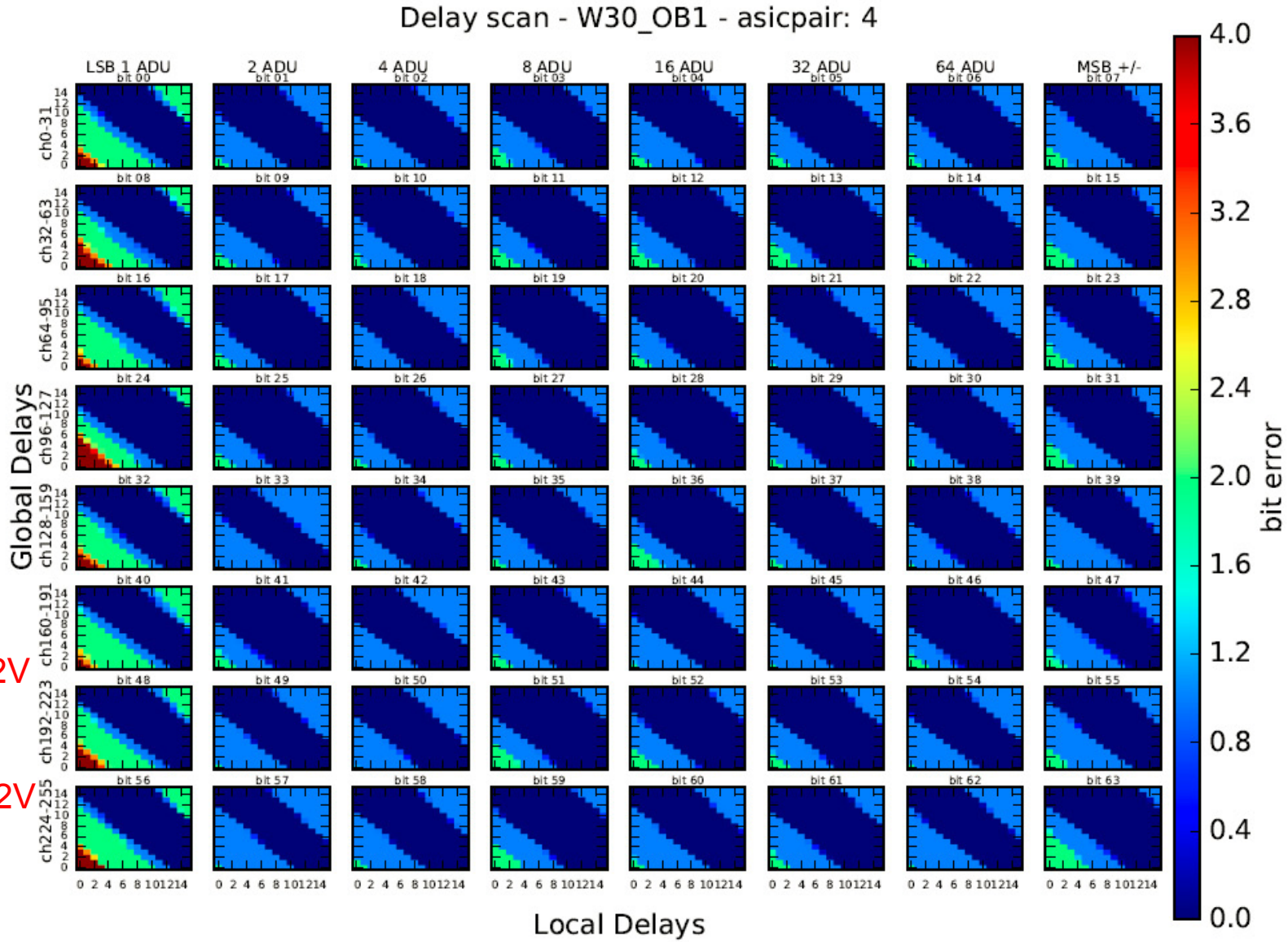
DHP3_1.2V_76.23MHz_Bias15_BiasD30BiasDelay50_bath_UI_allASICsOn.png

- 48cm Kapton + Patch Panel with Infiniband connector + 3m Infiniband cable
- DHP1,2,3 show similar data eye DHP4 not yet measured
- Differential peak-to-peak input voltage requirement of Virtex 6: 125mV



DCDs analog: ON

Delays – asicpair 4



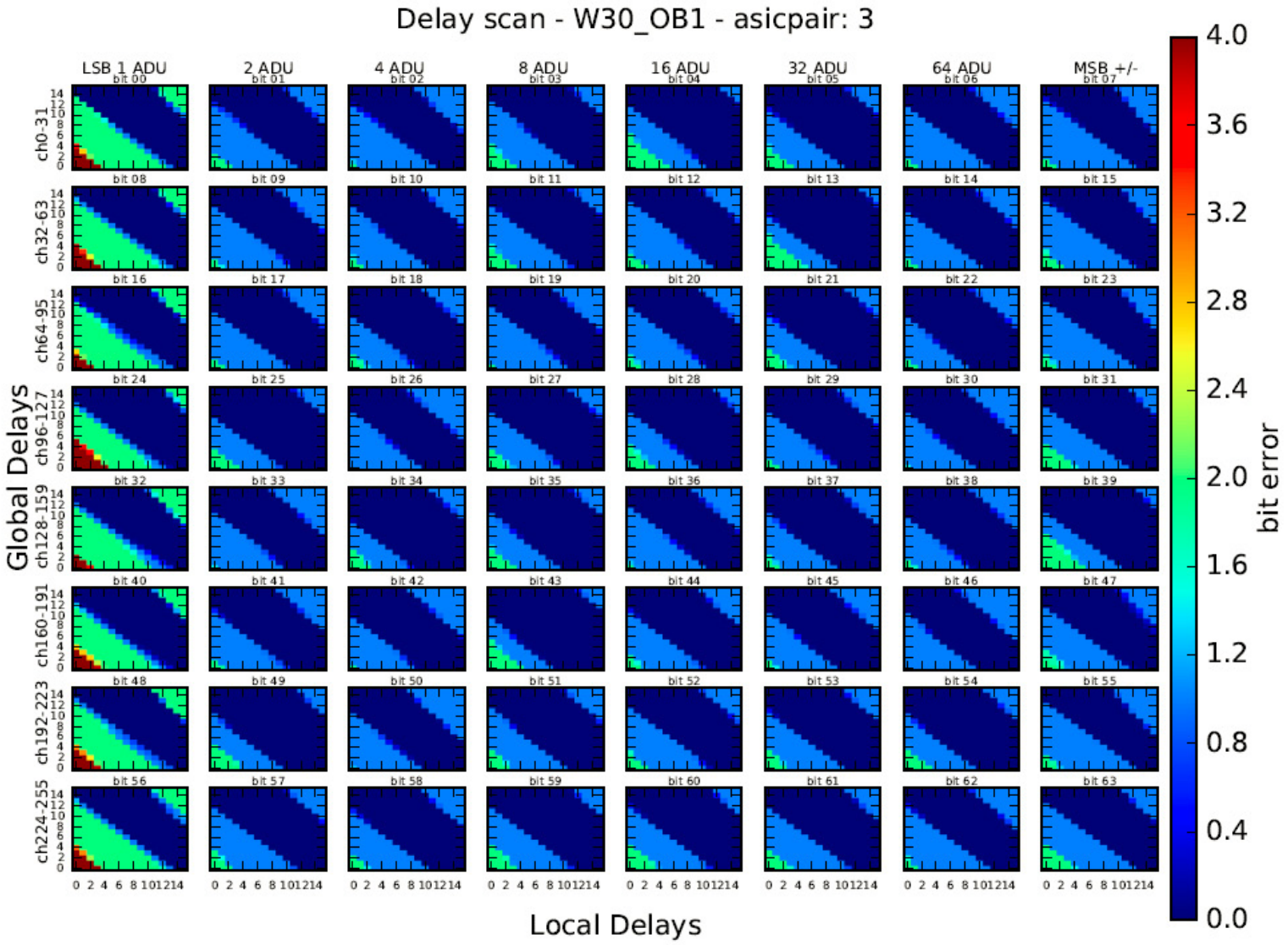
GCK=62.5MHz

DHP-Core=1.62V

DHP-IO=2.1V

DCD-DVDD=2.2V

Delays – asicpair 3



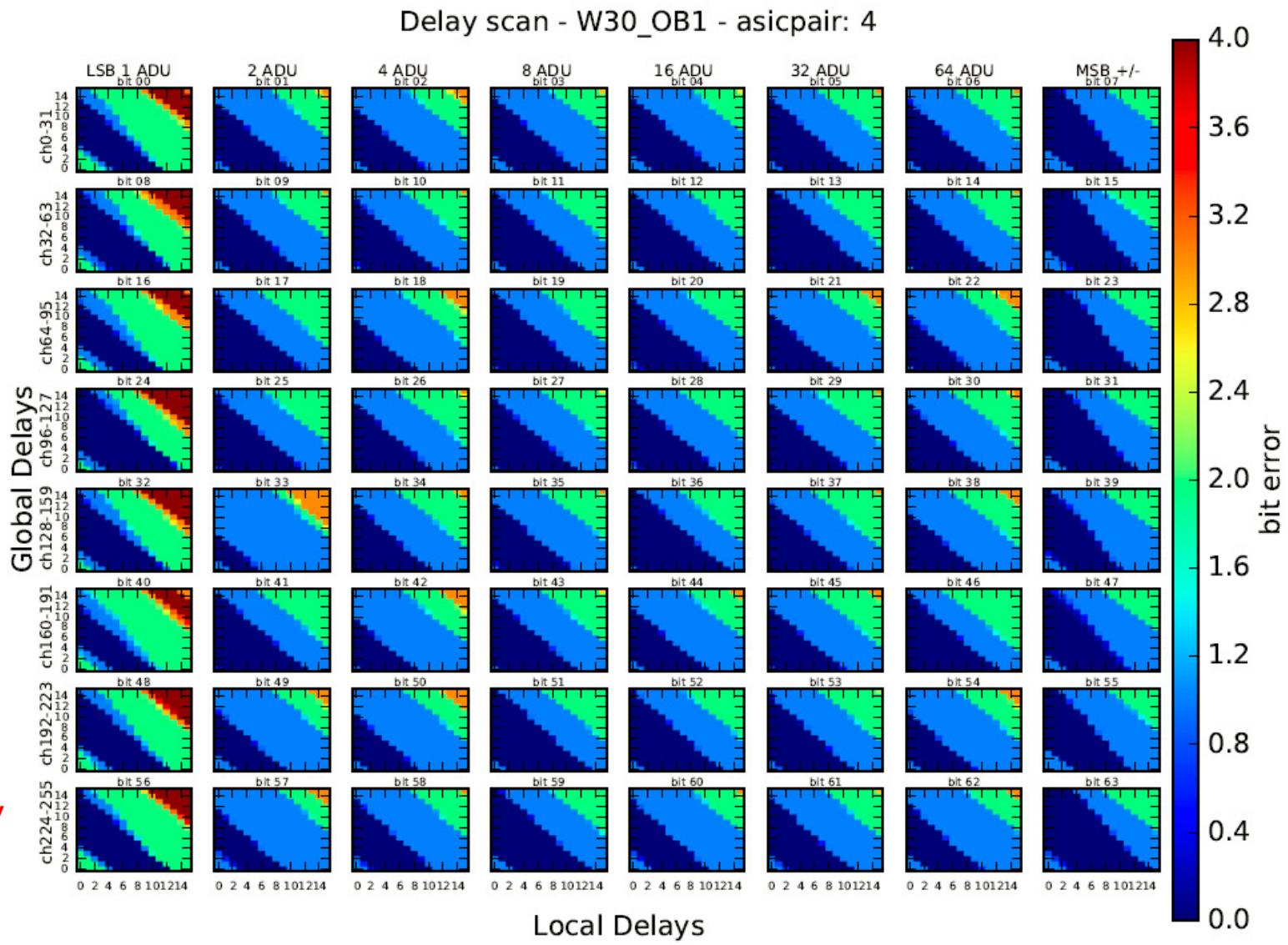
GCK=62.5MHz

DHP-Core=1.64V

DHP-IO=2.1V

DCD-DVDD=2.2V

Delays – asicpair 4



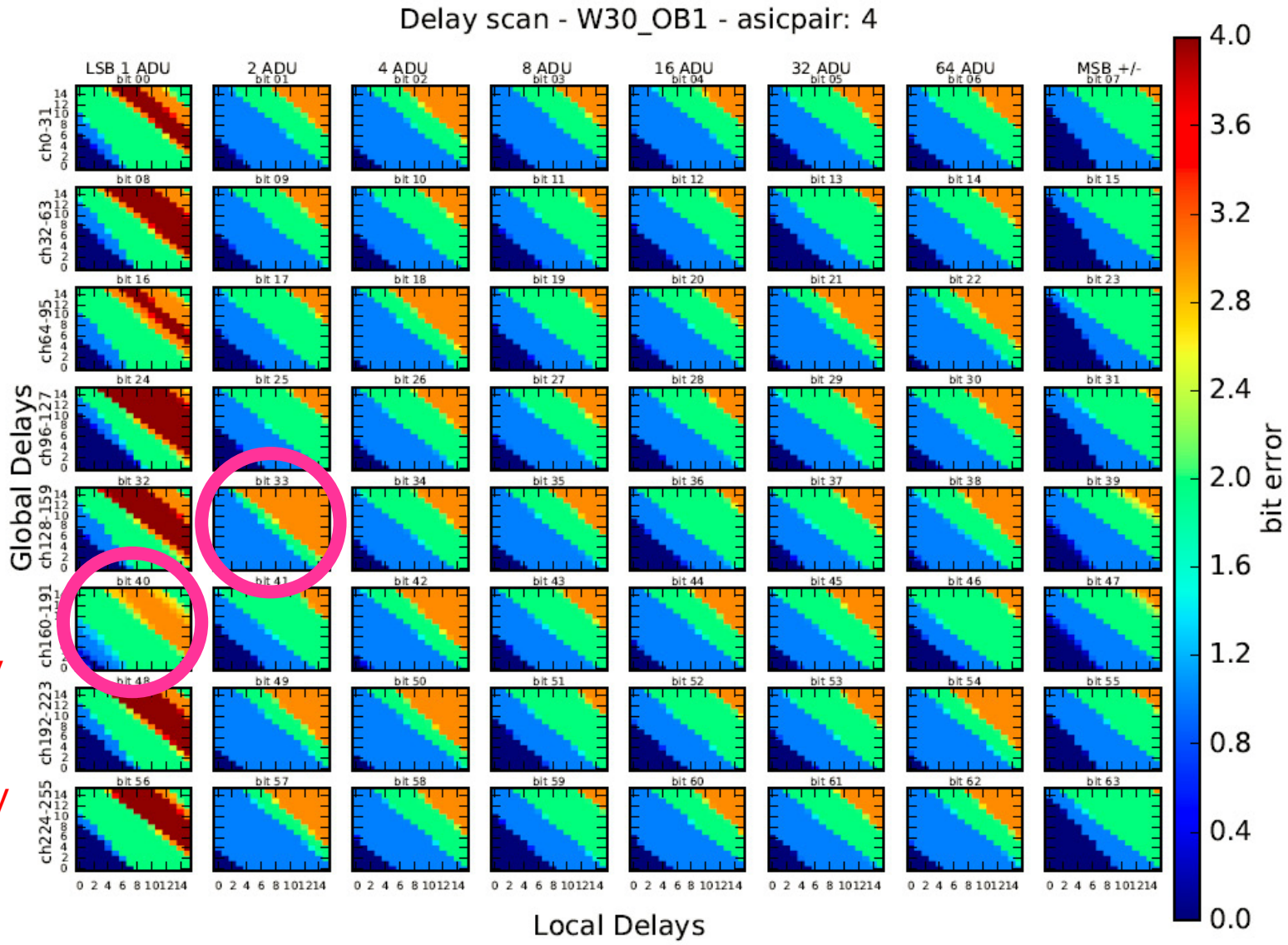
GCK=76.23MHz

DHP-Core=1.62V

DHP-IO=2.1V

DCD-DVDD=2.2V

Delay Scan – asicpair 4



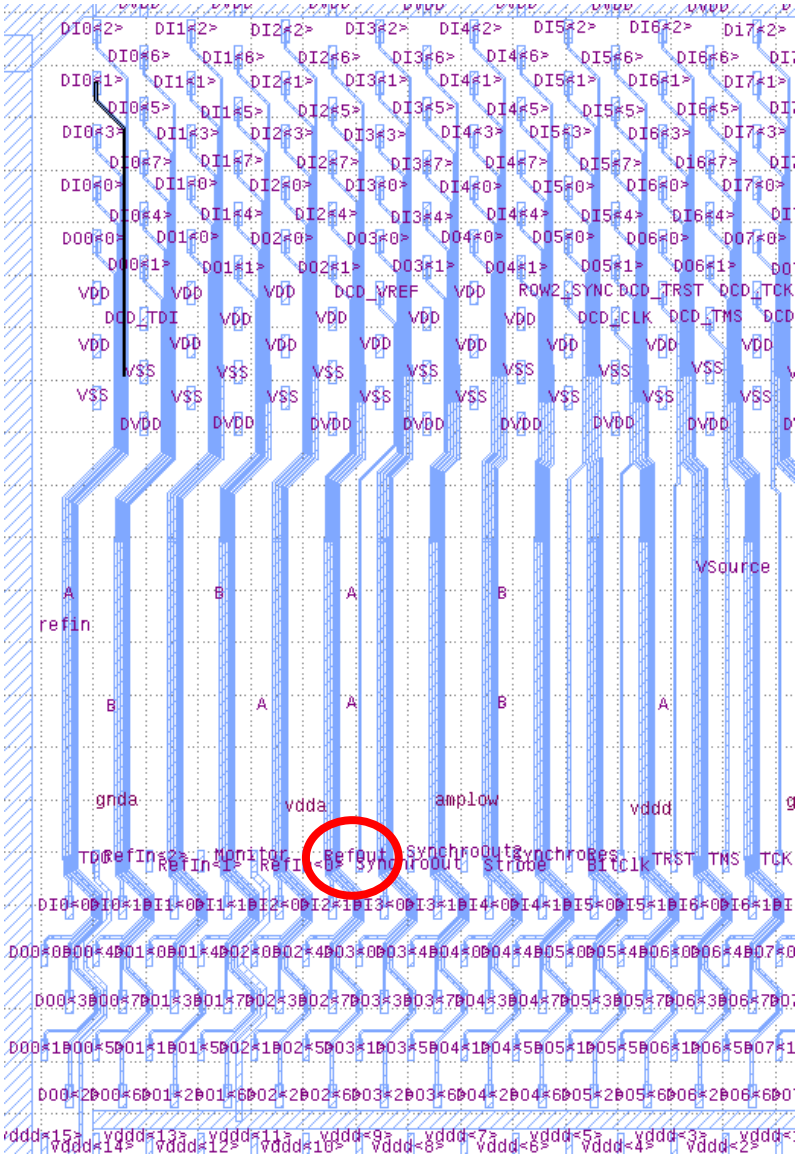
GCK=76.23MHz

DHP-Core=1.61V

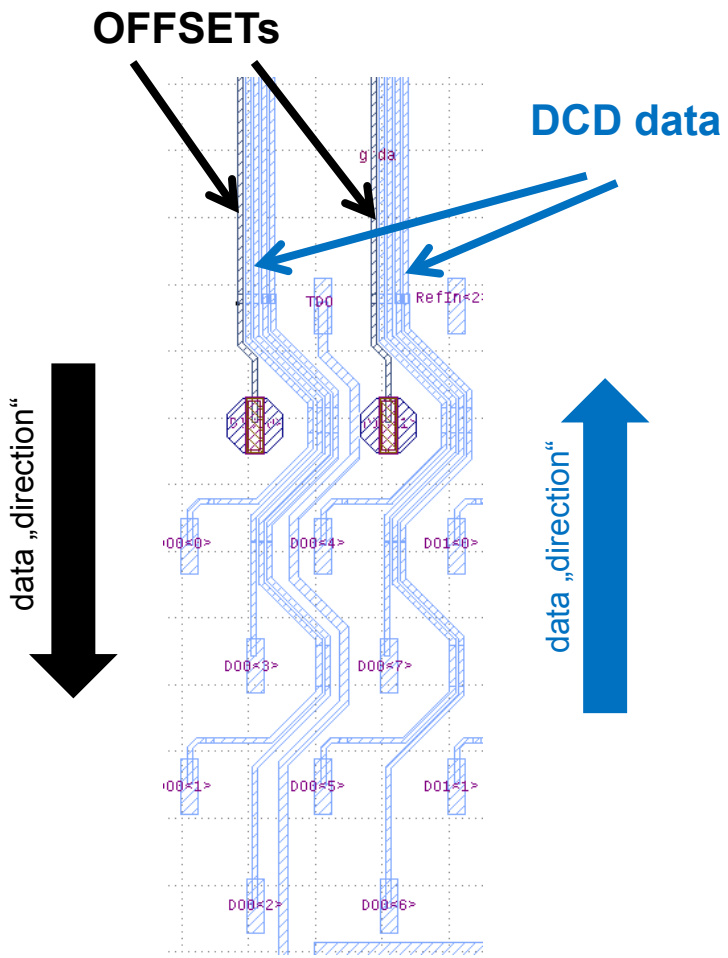
DHP-IO=1.8V

DCD-DVDD=1.9V

Crosstalk-Offsets - Introduction

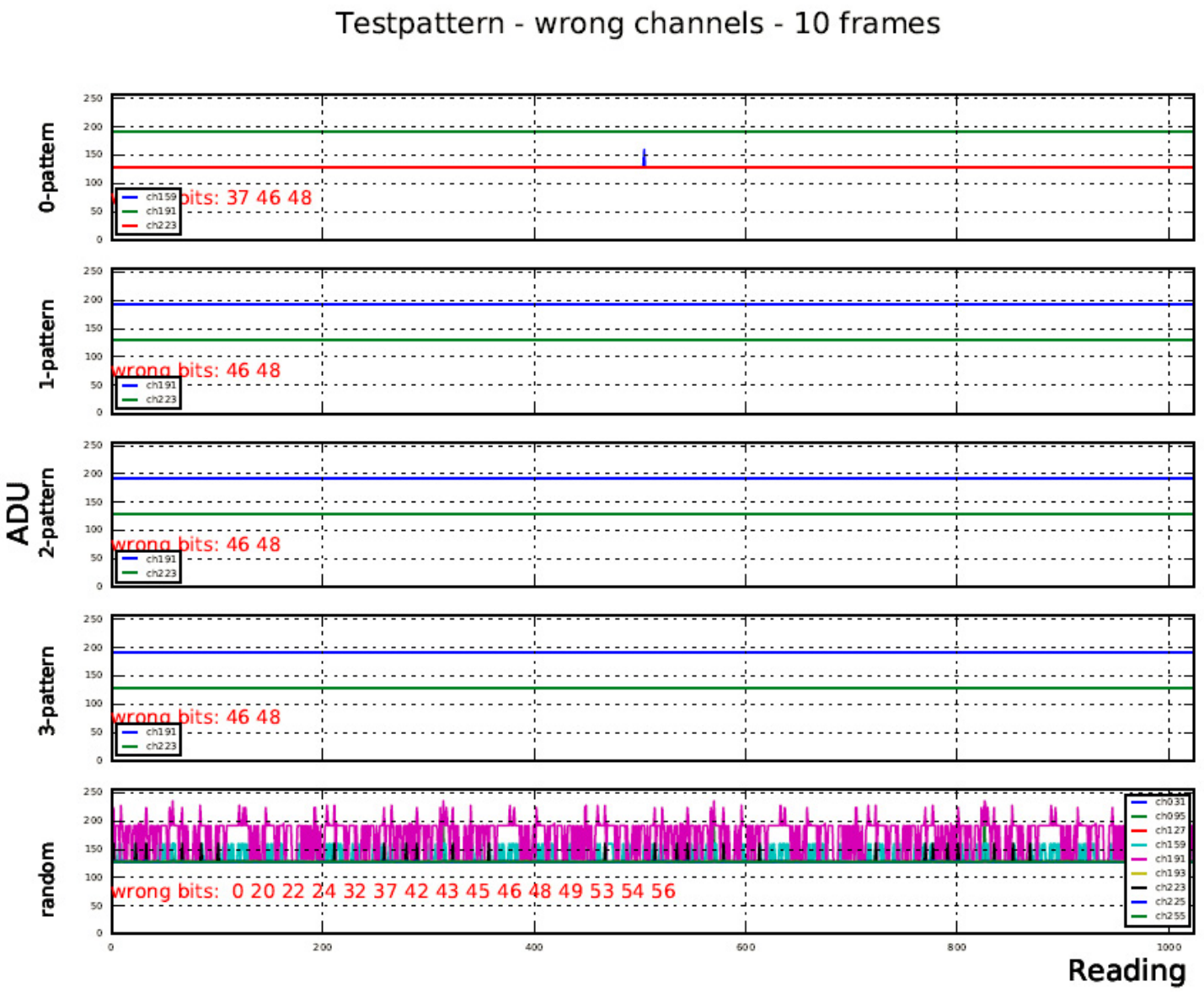


1 Columnpair, i.e. 32DCD channels

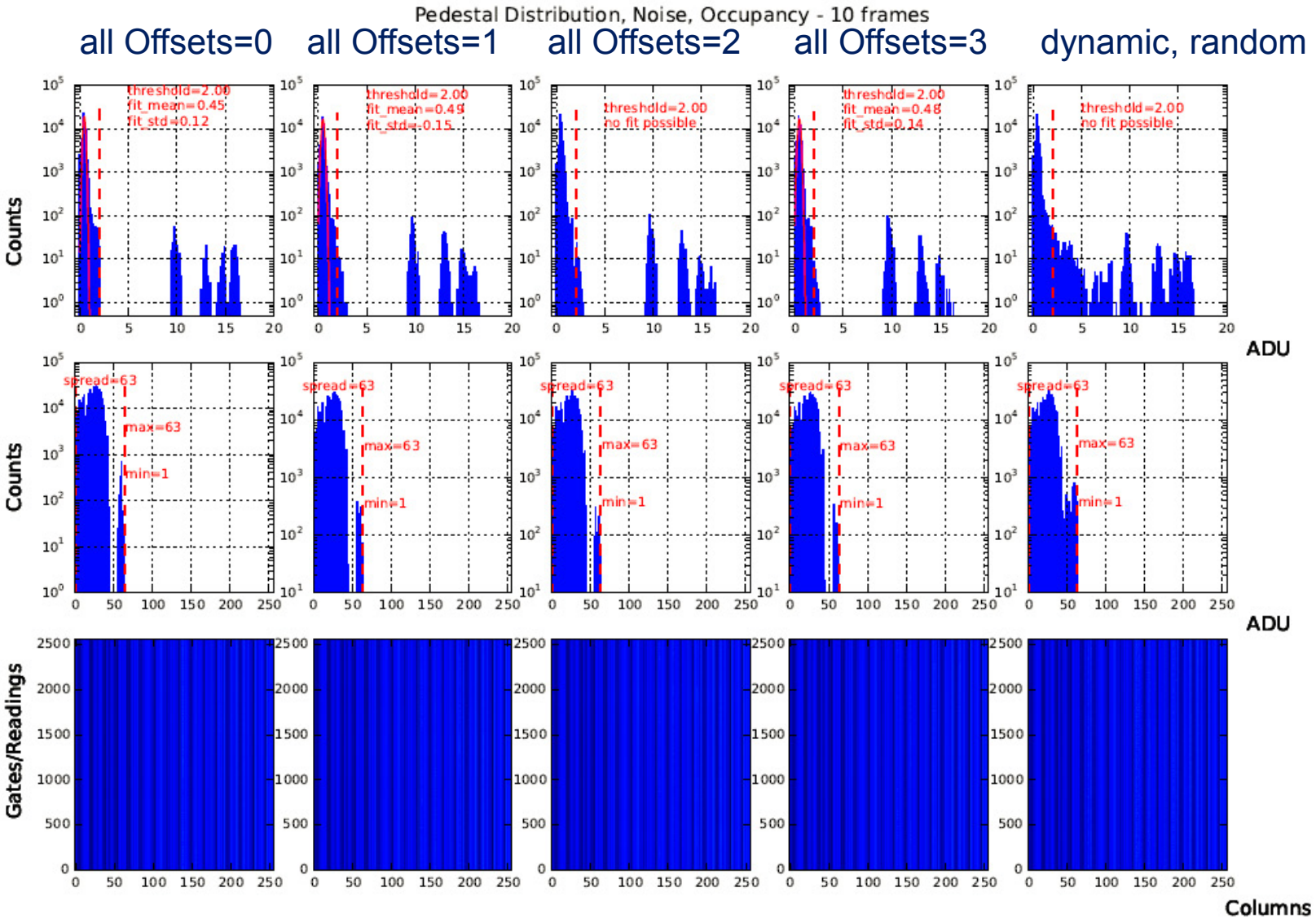


Is there a crosstalk between OFFSETs and DCD data?

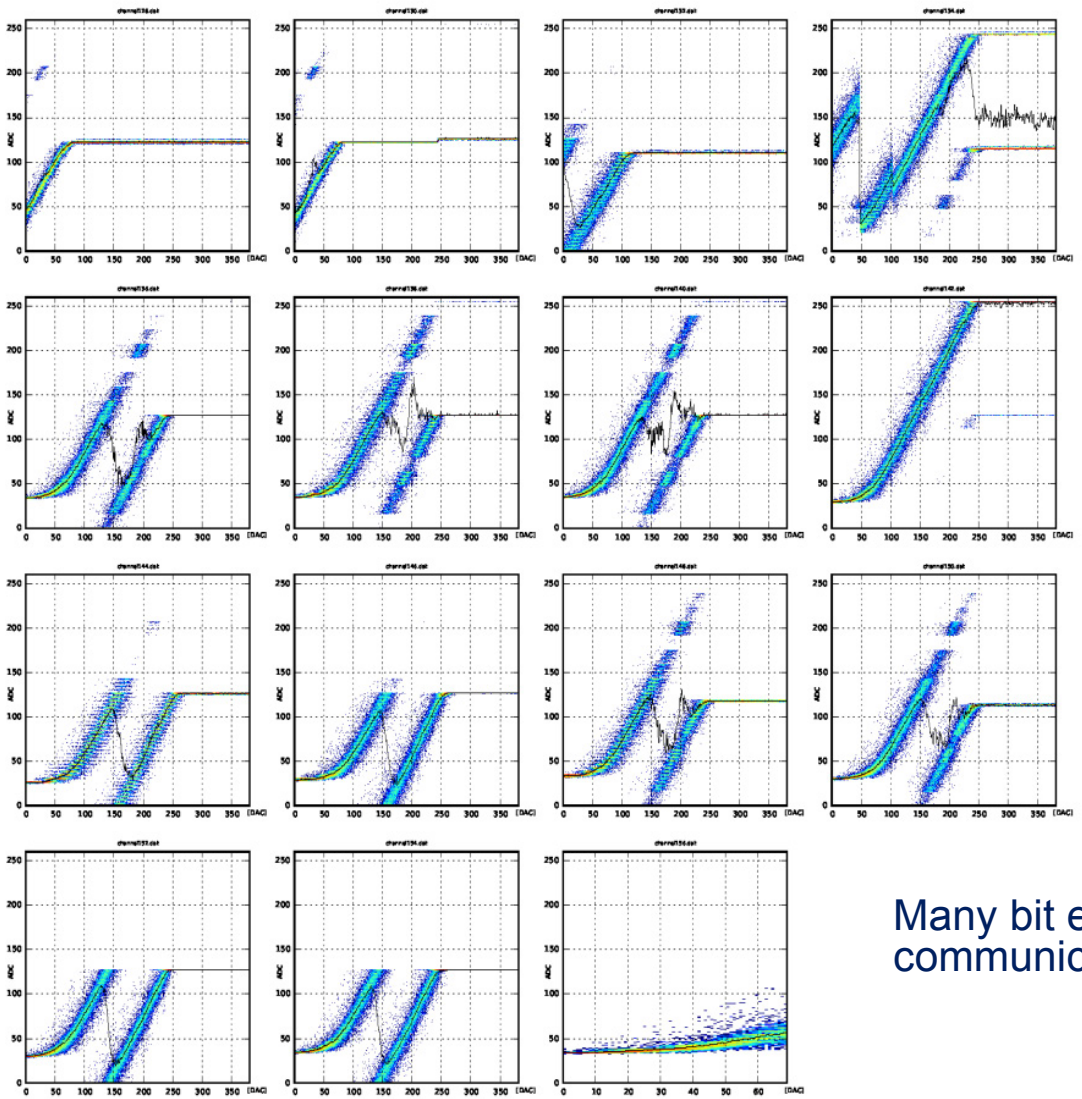
Cross Talk – EMCM W18_3 – 76.23MHz – DCD4



Cross Talk – EMCM W18_3 – 76.23MHz – DCD4



ADC Transfer Curve



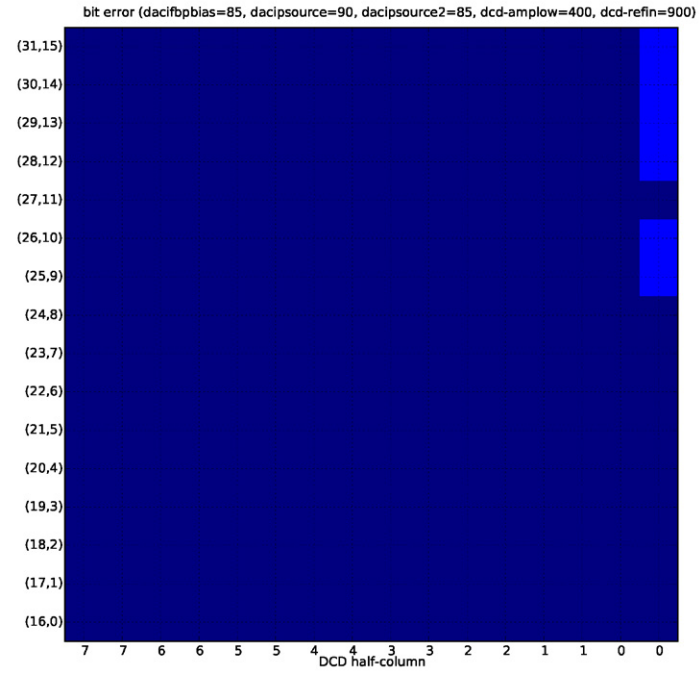
- GCK = 76.23 MHz
- DCD_DVDD = 1.9V, DHPT_IO = 1.8V, DHPT_Core = 1.64V

Many bit errors in the DCD-DHPT communication

ADC Transfer Curve

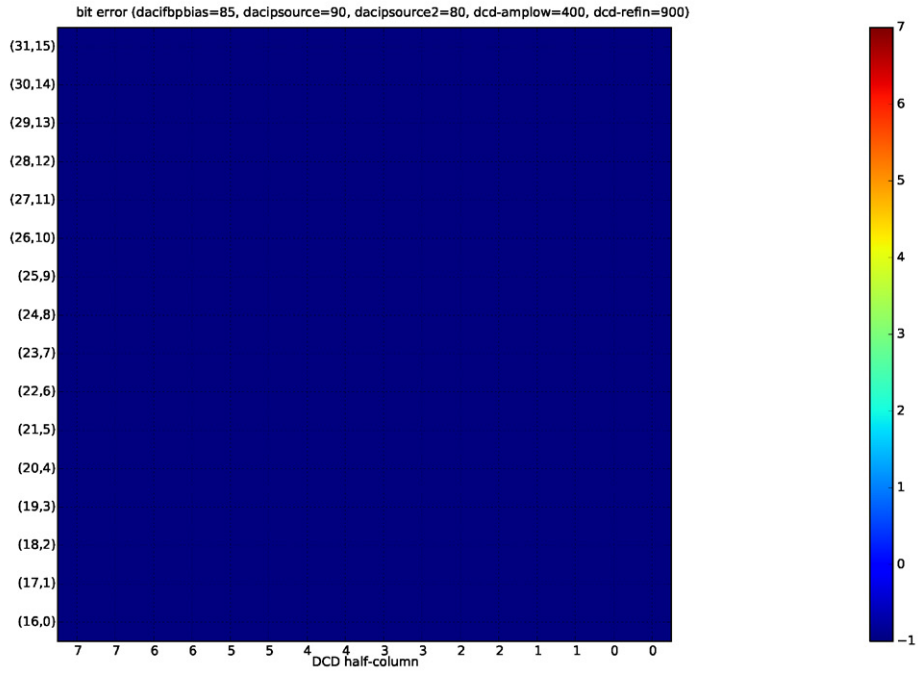
- GCK = 62.5 MHz
- DCD_DVDD = 2.2V, DHPT_IO = 2.1V, DHPT_Core = 1.64V
- Delay Scan using the DCD test pattern
- ADC transfer curves using the DCD internal current source I_Sig_Mirror
- ASIC-pairs 3 + 4 all channels (but only 2 x 2 IPSource/IPSource2 settings)

D3-R3



6 channels showed bit errors

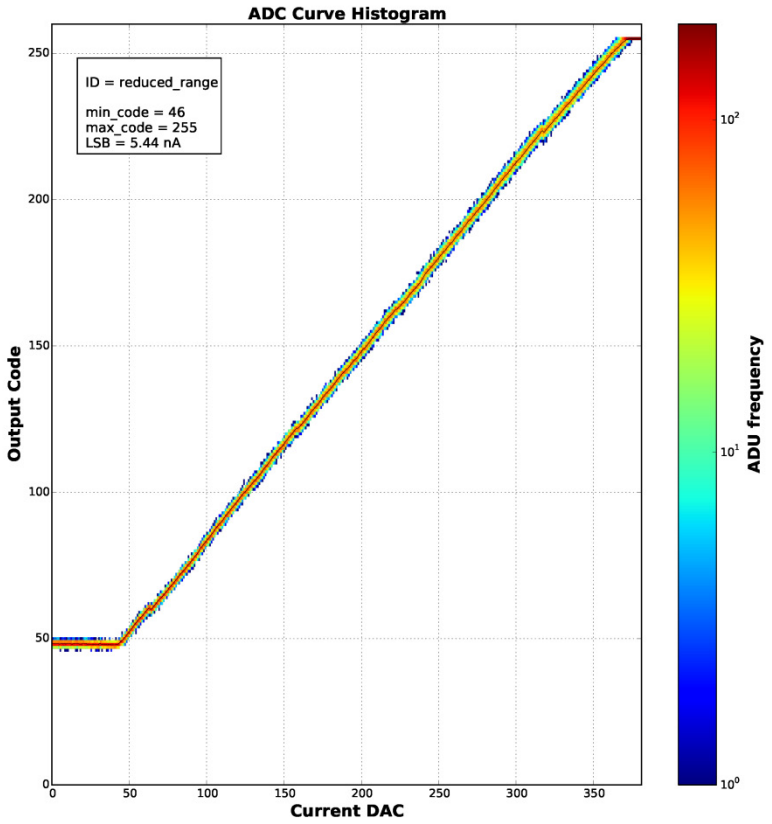
D4-R4

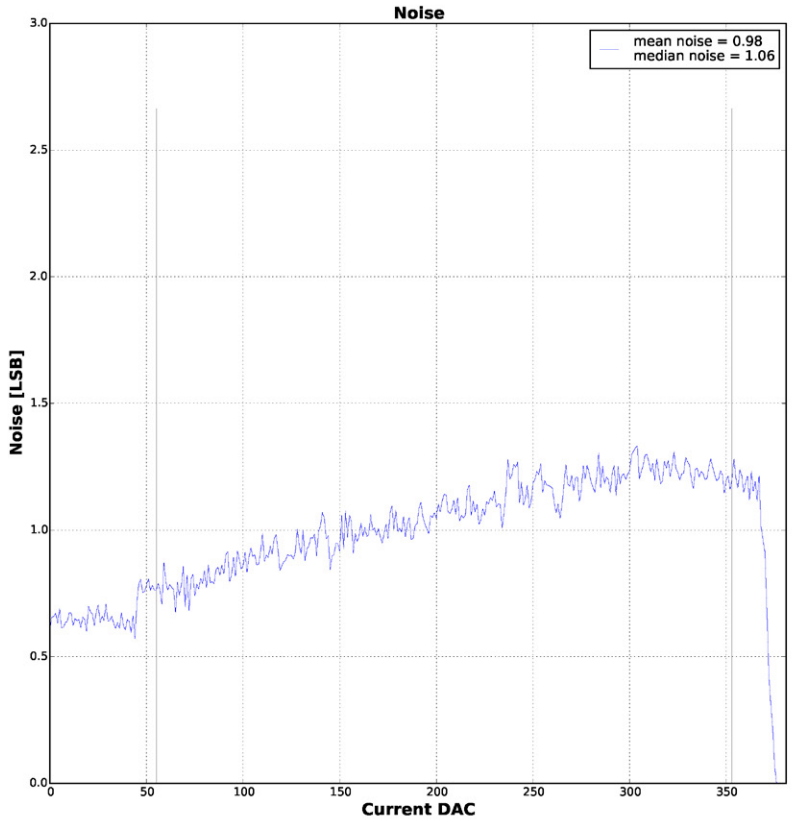


No bit errors

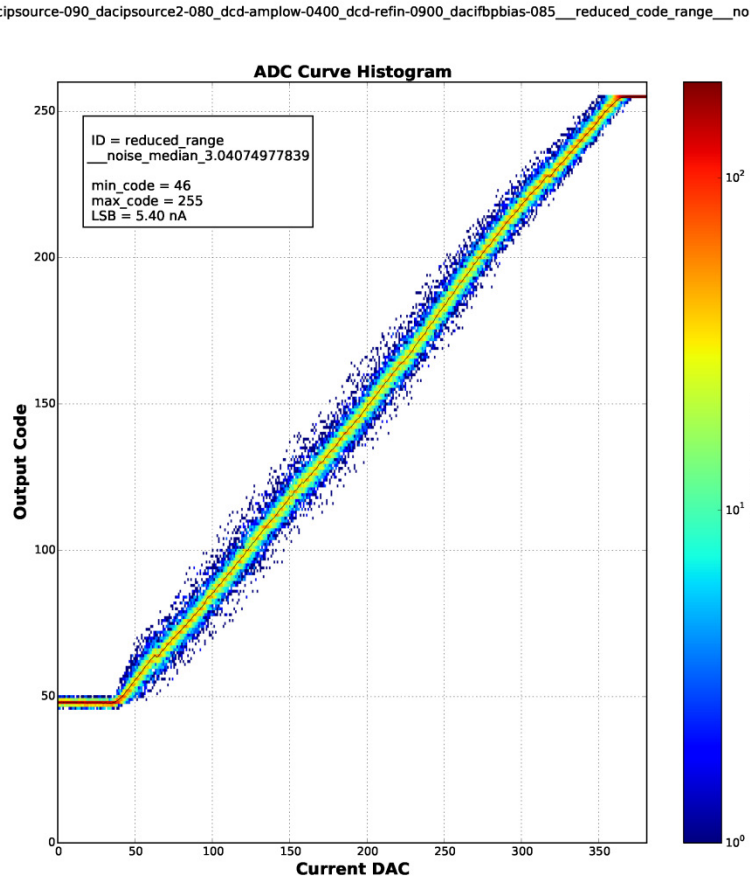
ADC Transfer Curve

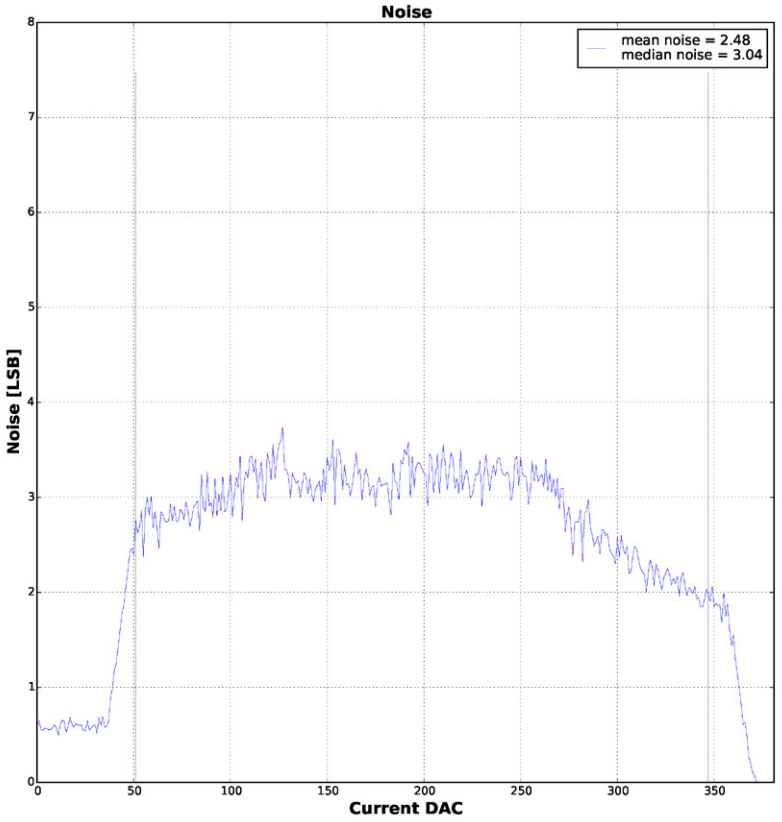
channel011_dacipsource-090_dacipsource2-080_dcd-amplow-0400_dcd-refin-0900_dacifbpbias-085___reduced_code_r





- R4 (asic-pair 4) channel not connected to DEPFET matrix
- GCK = 62.5 MHz

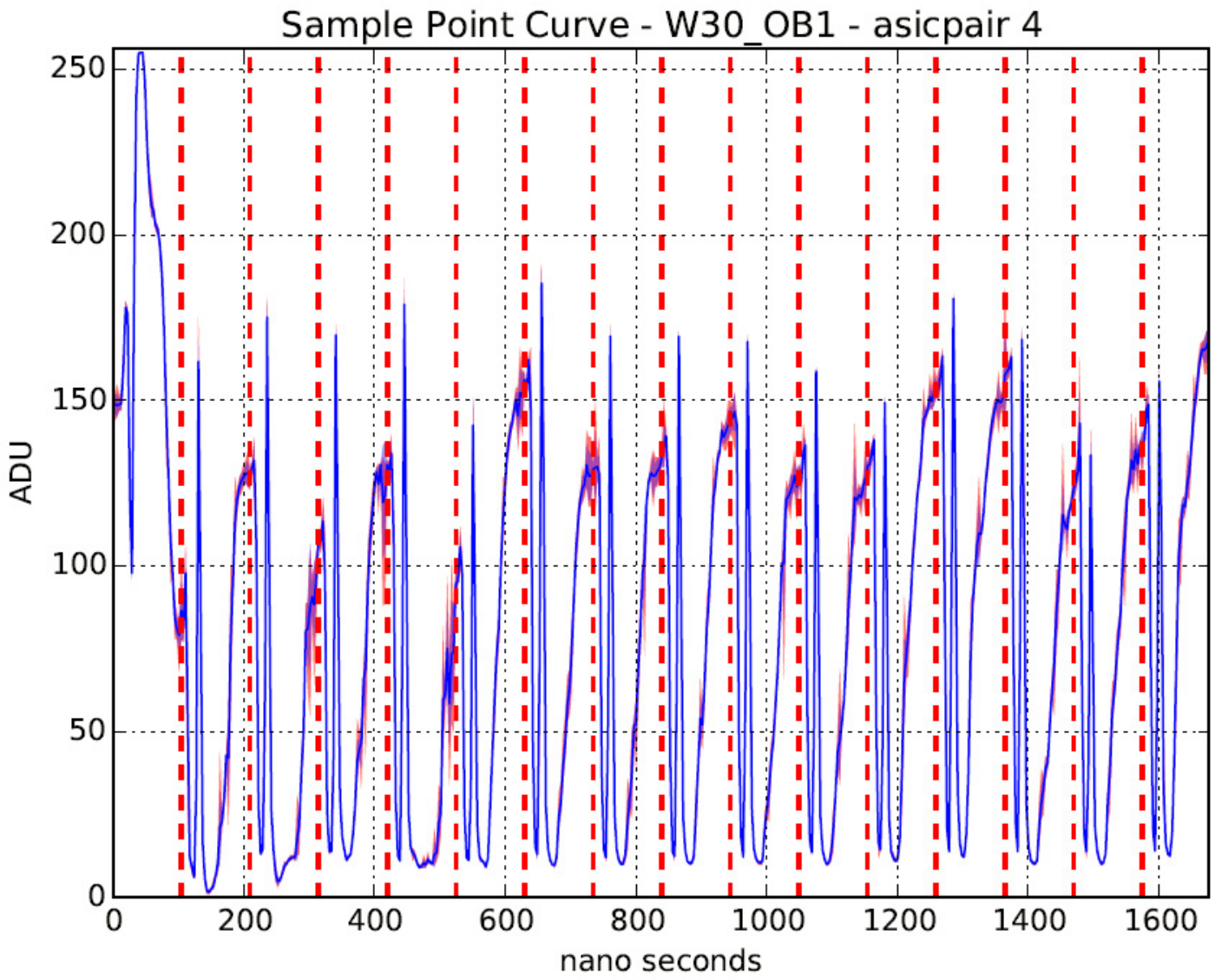




- R4 (asic-pair 4) channel connected to DEPFET matrix
- GCK = 62.5 MHz

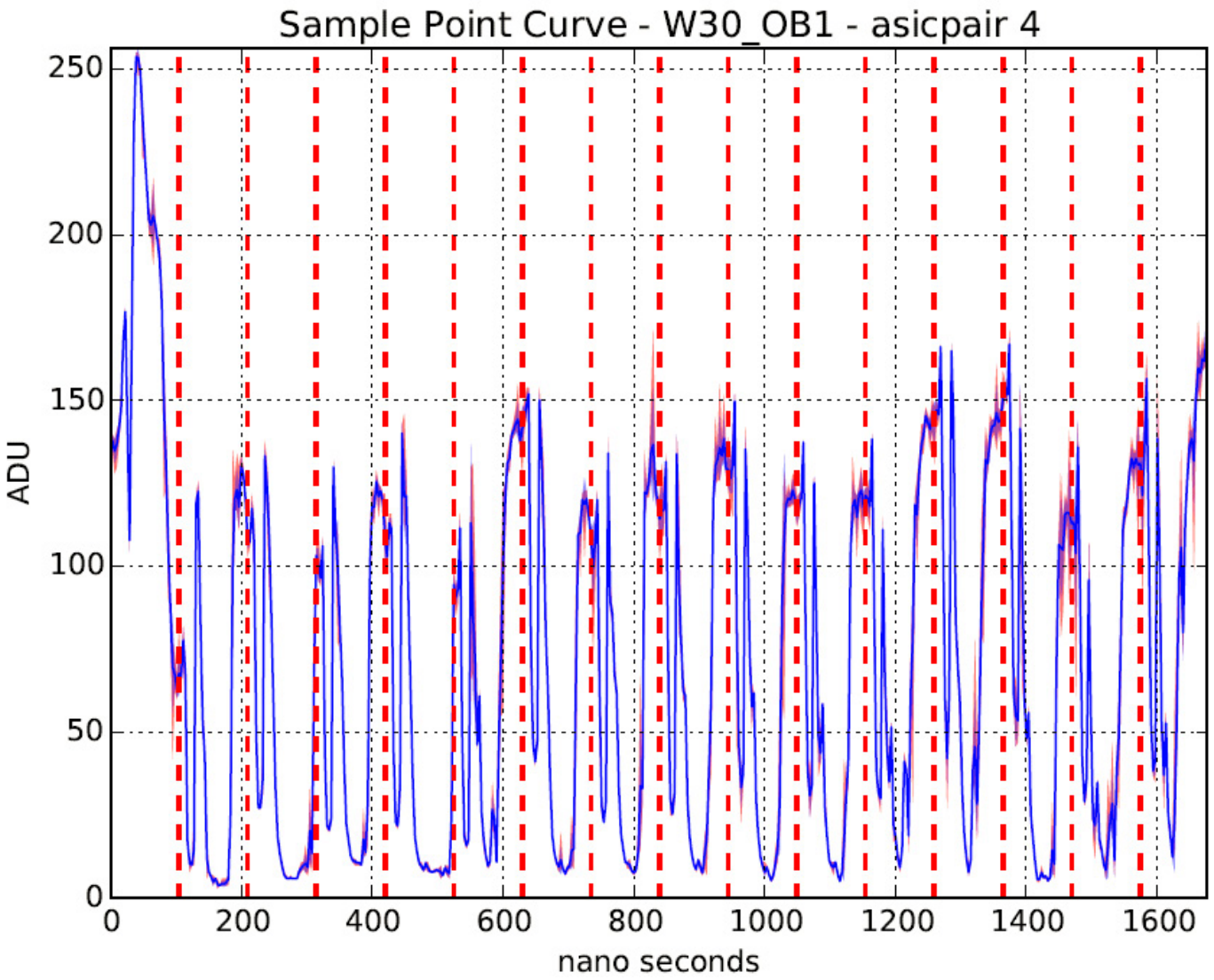
SCP

gateon1,2,3=-2500mV,
gateoff=2000mV
lowgain (gain=1),
deactivate caps
ITCPL=30

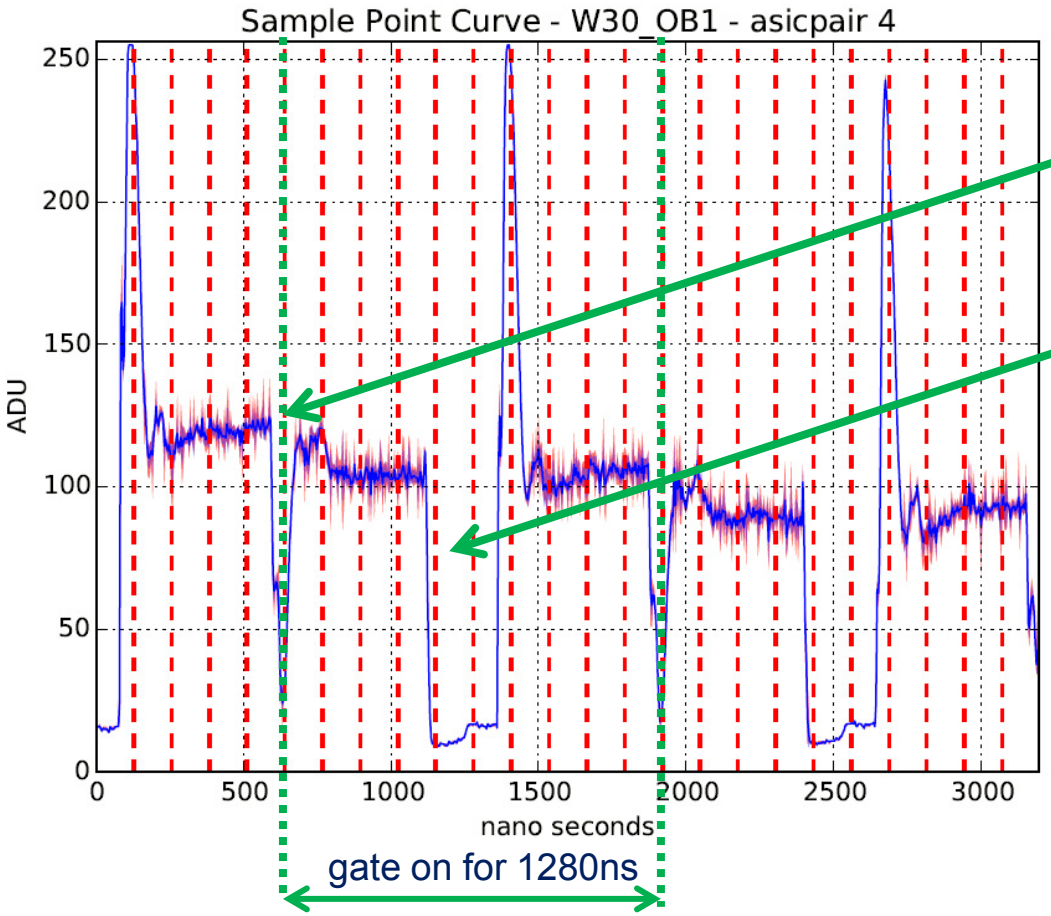


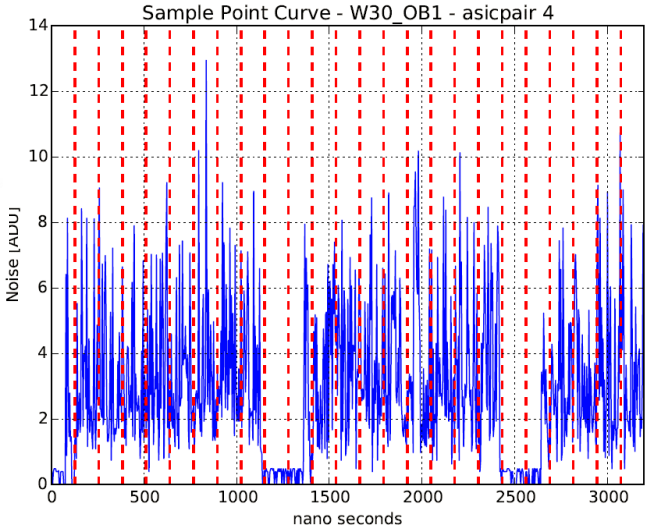
SCP

gateon1,2,3=-2500mV,
gateoff=2000mV
lowgain (gain=1),
deactivate caps
ITCPL=5



SPC – 1280ns integration time - noCM

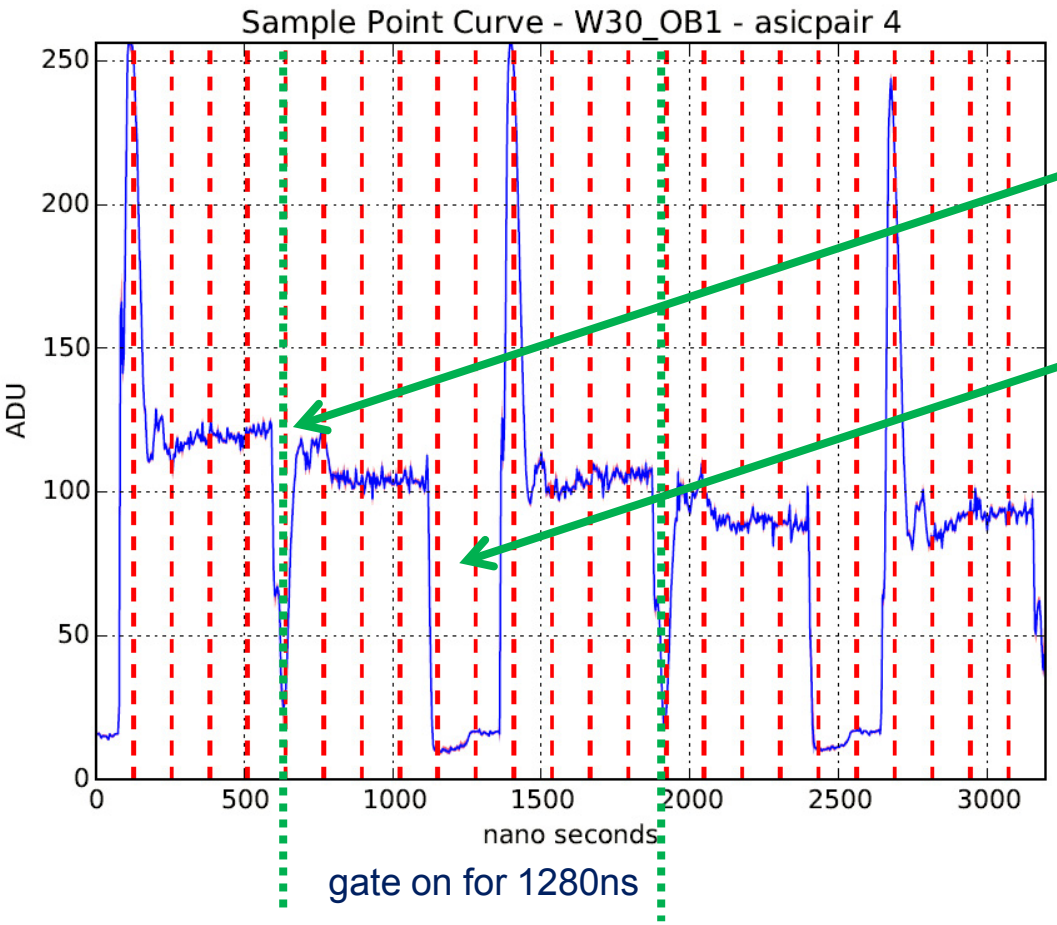




GCK (PLL) = 62.5 MHz
T_row = 1280ns

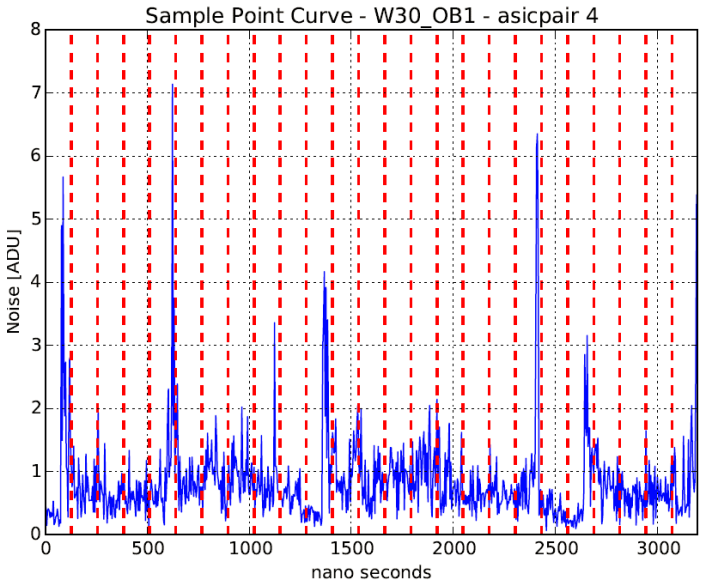
Measurement:
No offline Common Mode correction

SPC – 1280ns row time – CM correction



next row
gate on for 1280ns

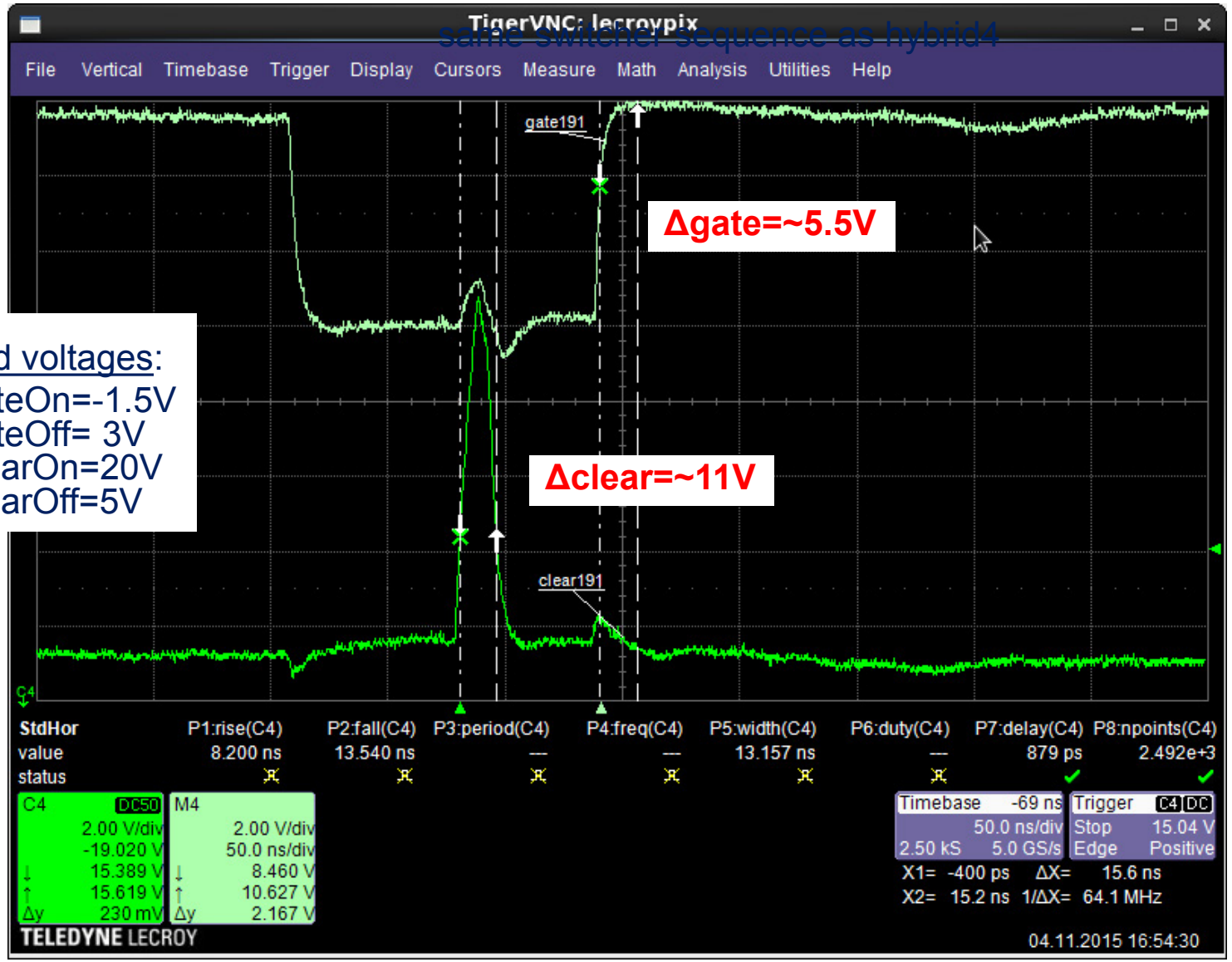
Clear (236ns)



GCK (PLL) = 62.5 MHz
T_row = 1280ns

Measurement:
Offline Common Mode correction

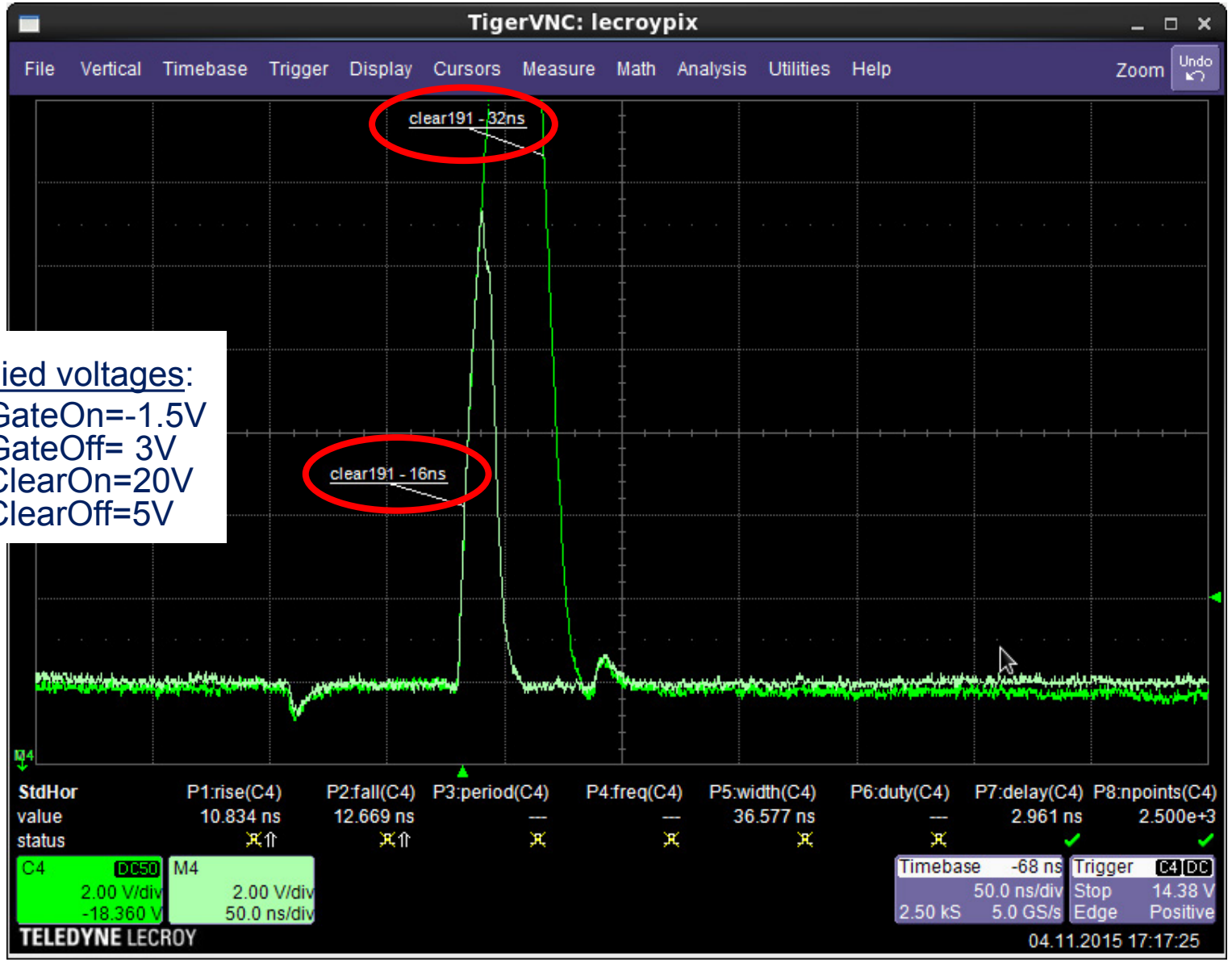
Pilot Run W30-OB1



applied voltages:

- GateOn=-1.5V
- GateOff= 3V
- ClearOn=20V
- ClearOff=5V

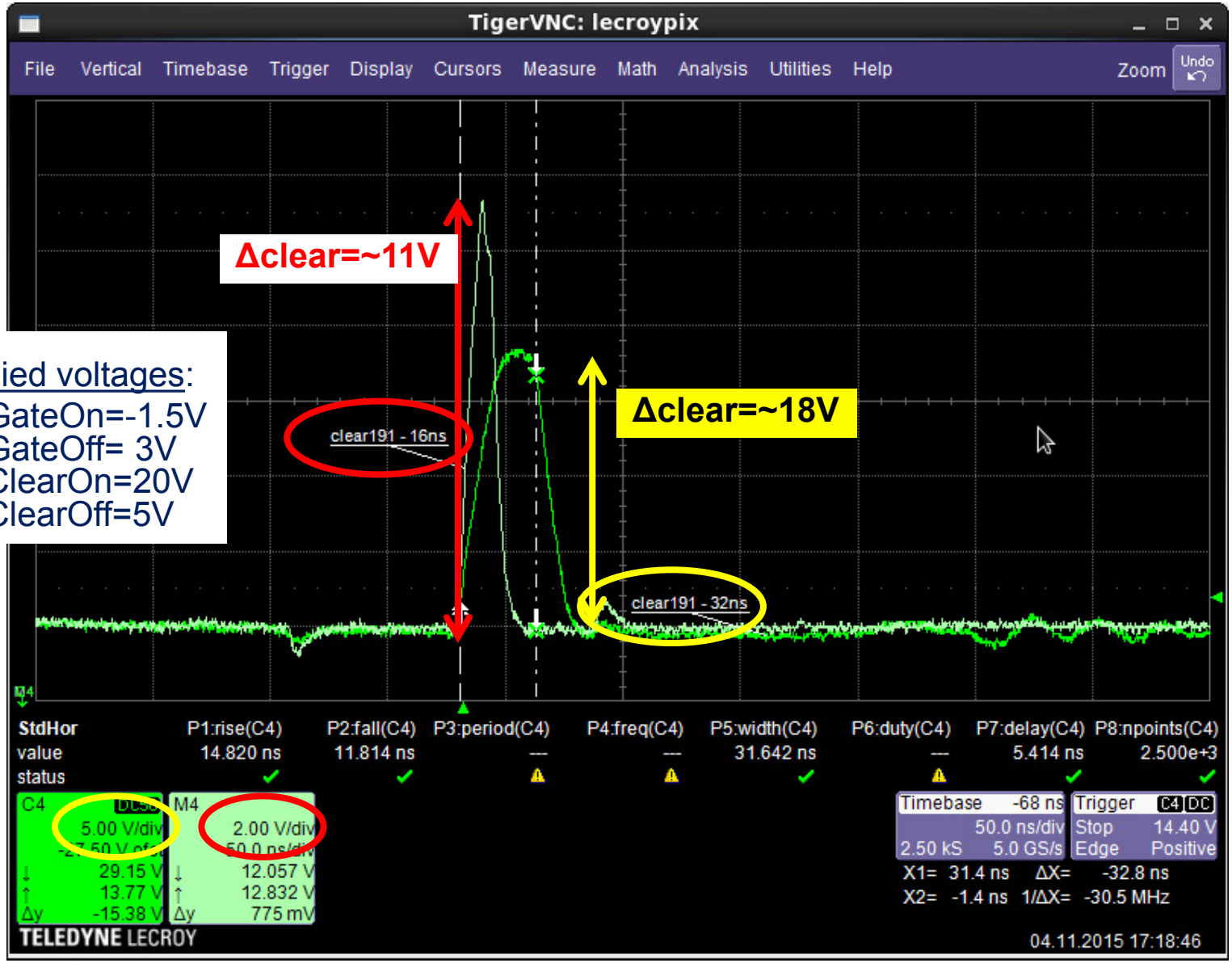
Pilot Run W30-OB1



applied voltages:

- GateOn=-1.5V
- GateOff= 3V
- ClearOn=20V
- ClearOff=5V

Pilot Run W30-OB1

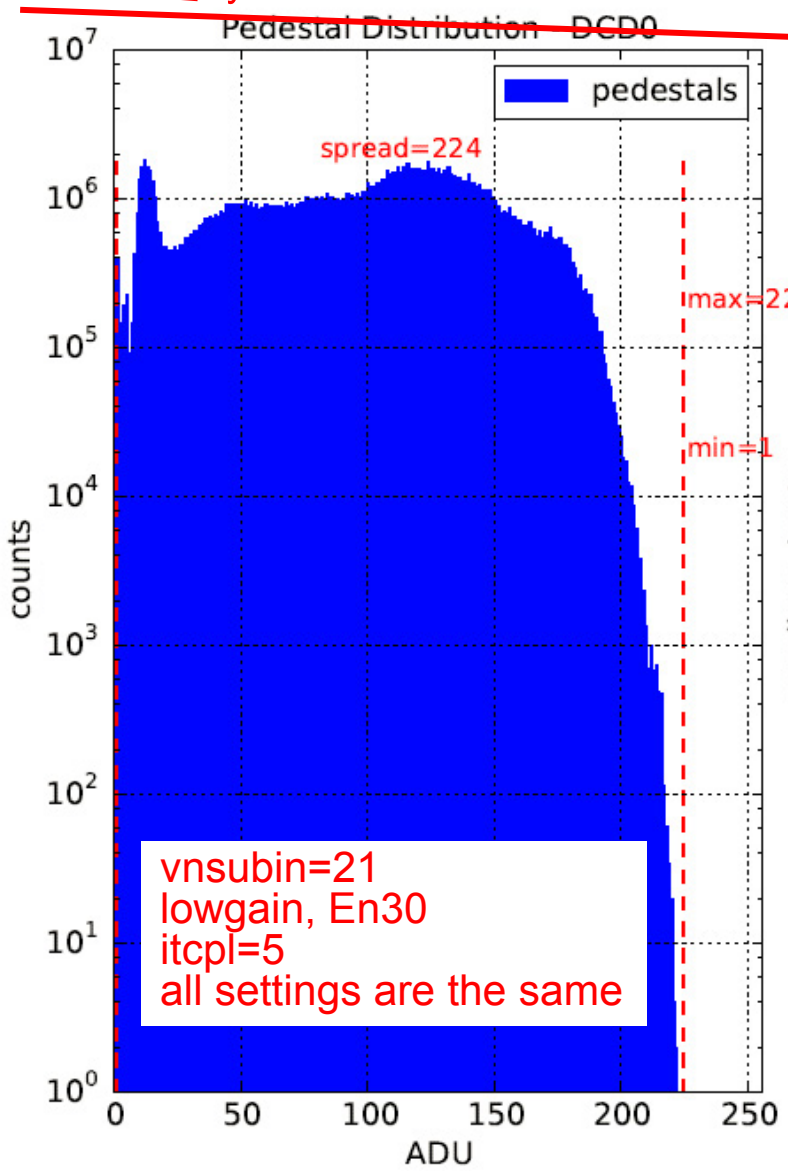


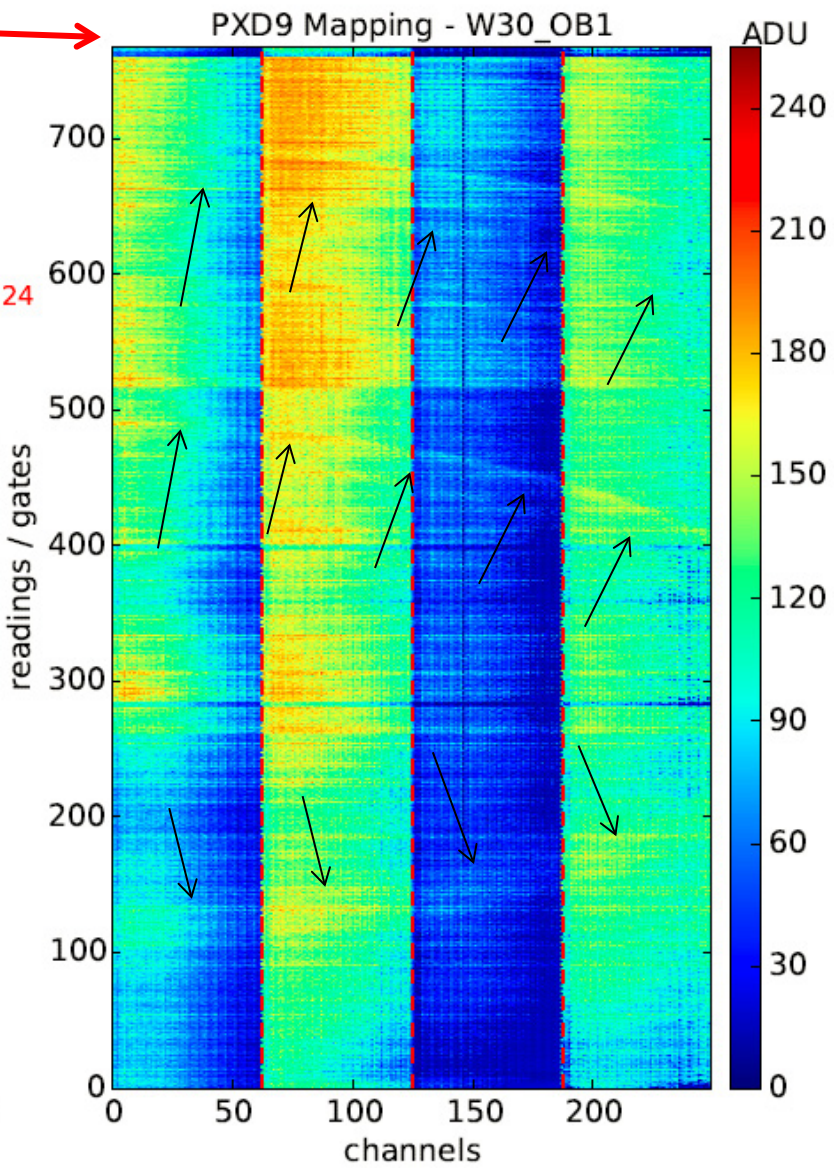
applied voltages:

- GateOn=-1.5V
- GateOff= 3V
- ClearOn=20V
- ClearOff=5V

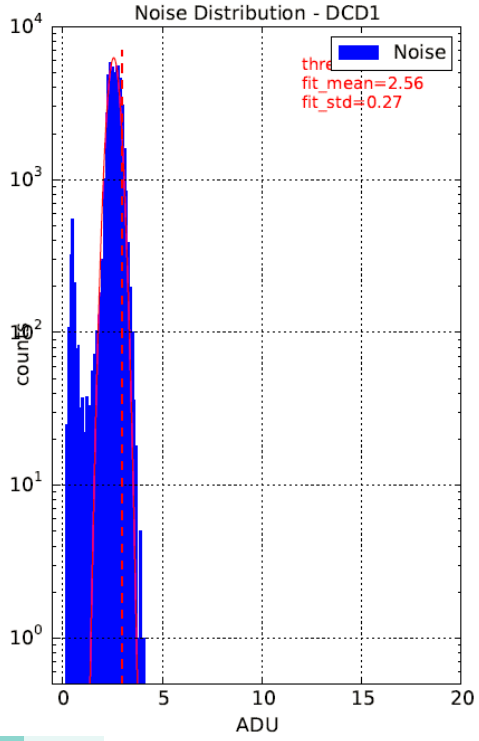
Pedestal Distribution

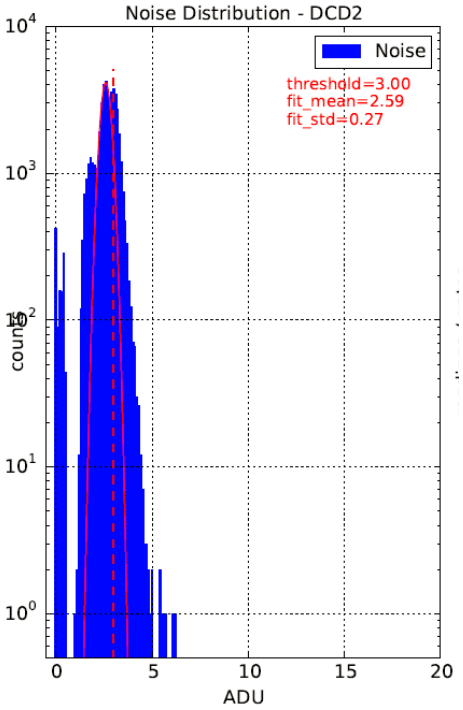
?sync_proc_dly?

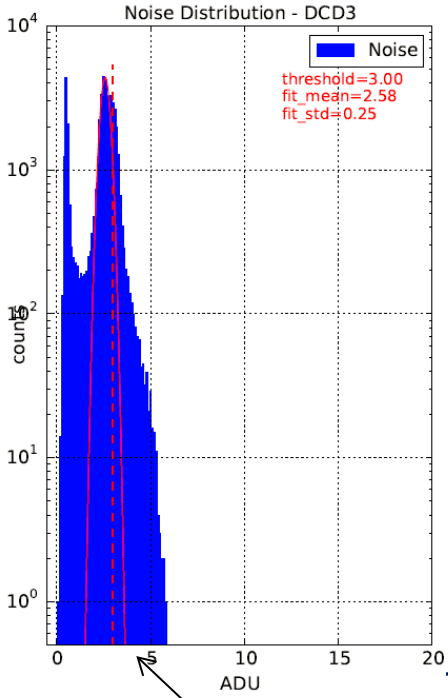


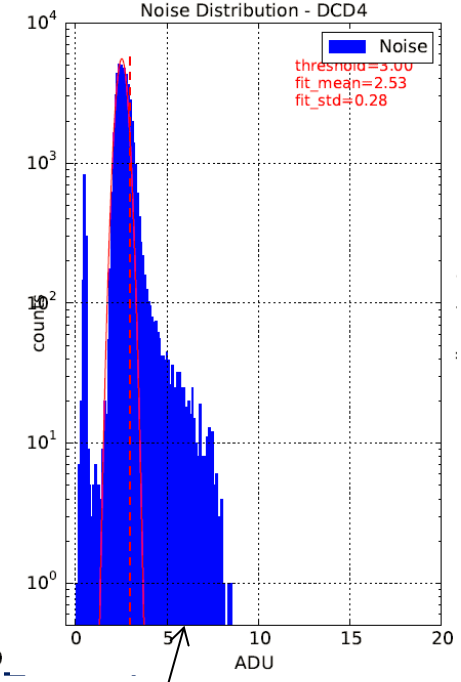


Noise Issues – GCK 62.5MHz







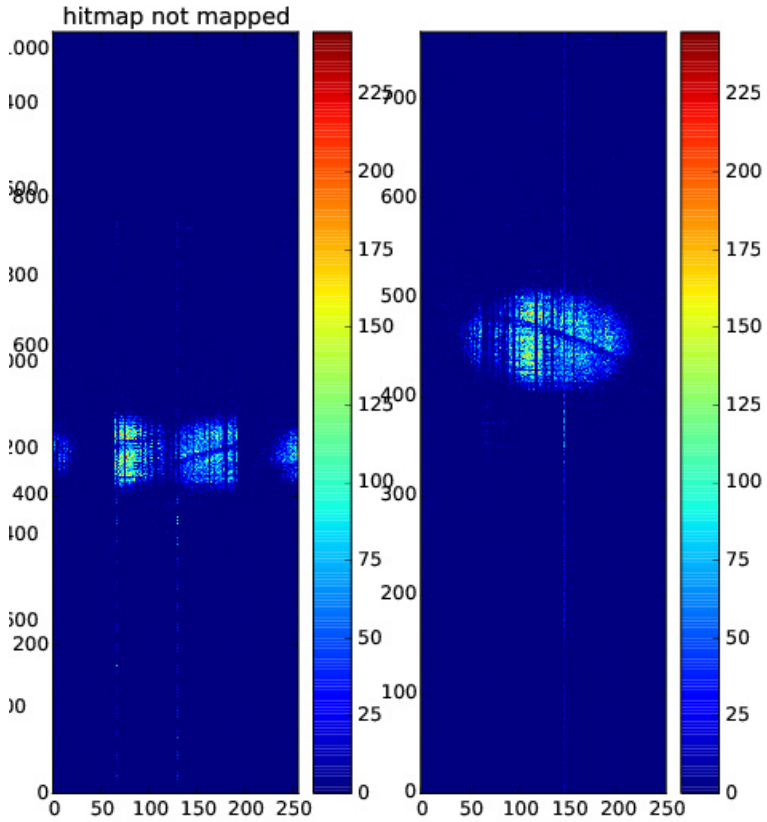


No CM Correction applied

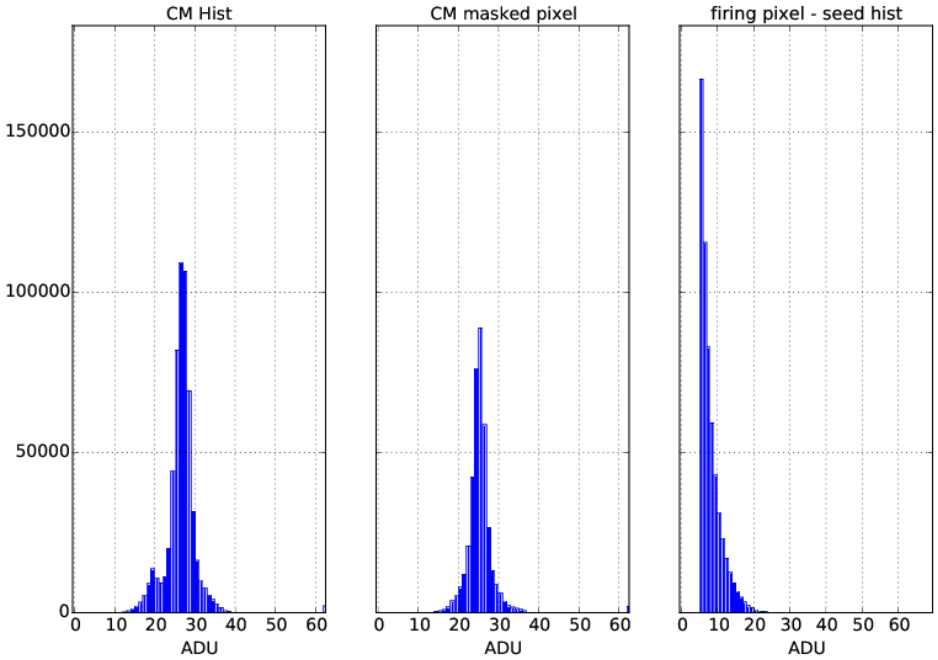
fits are applied for values< threshold

test pattern is not a good indicator for proper communication
Increased noise due to bot errors?

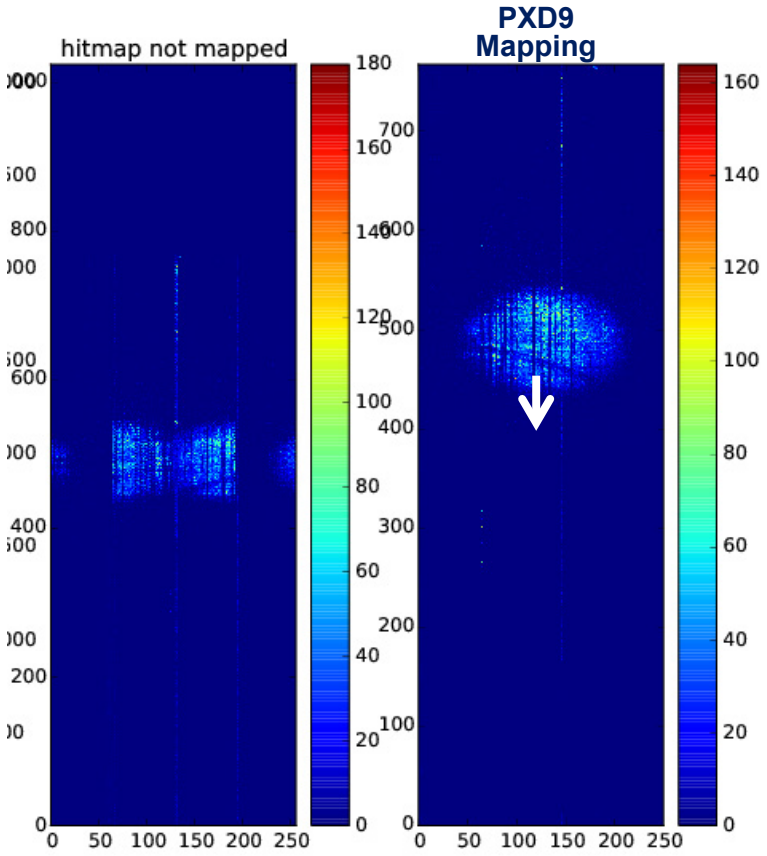
Cd109 Hitmap



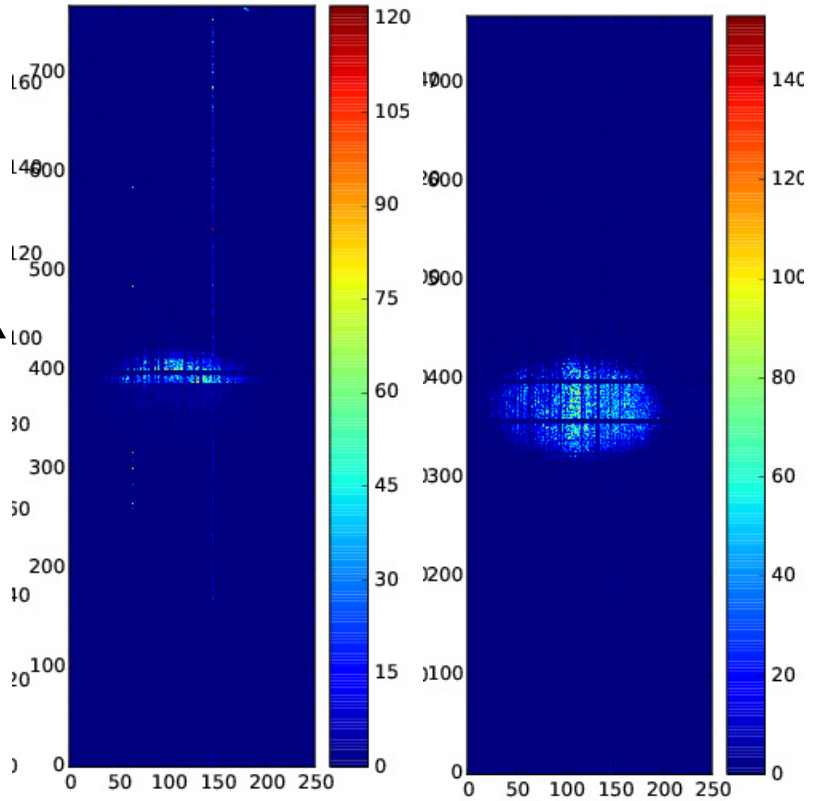
- All DHPTs read-out simultaneously
- GCK = 62.5 MHz
- Pedestals taken with data link: Full-rate
- ZS-data taken data link: Half-rate
- Threshold = 5
- Cut on CM (offline) to mask rows with large CM
- Ring of low sensitivity – as seen on Hybrid5



Cd109 Hitmap

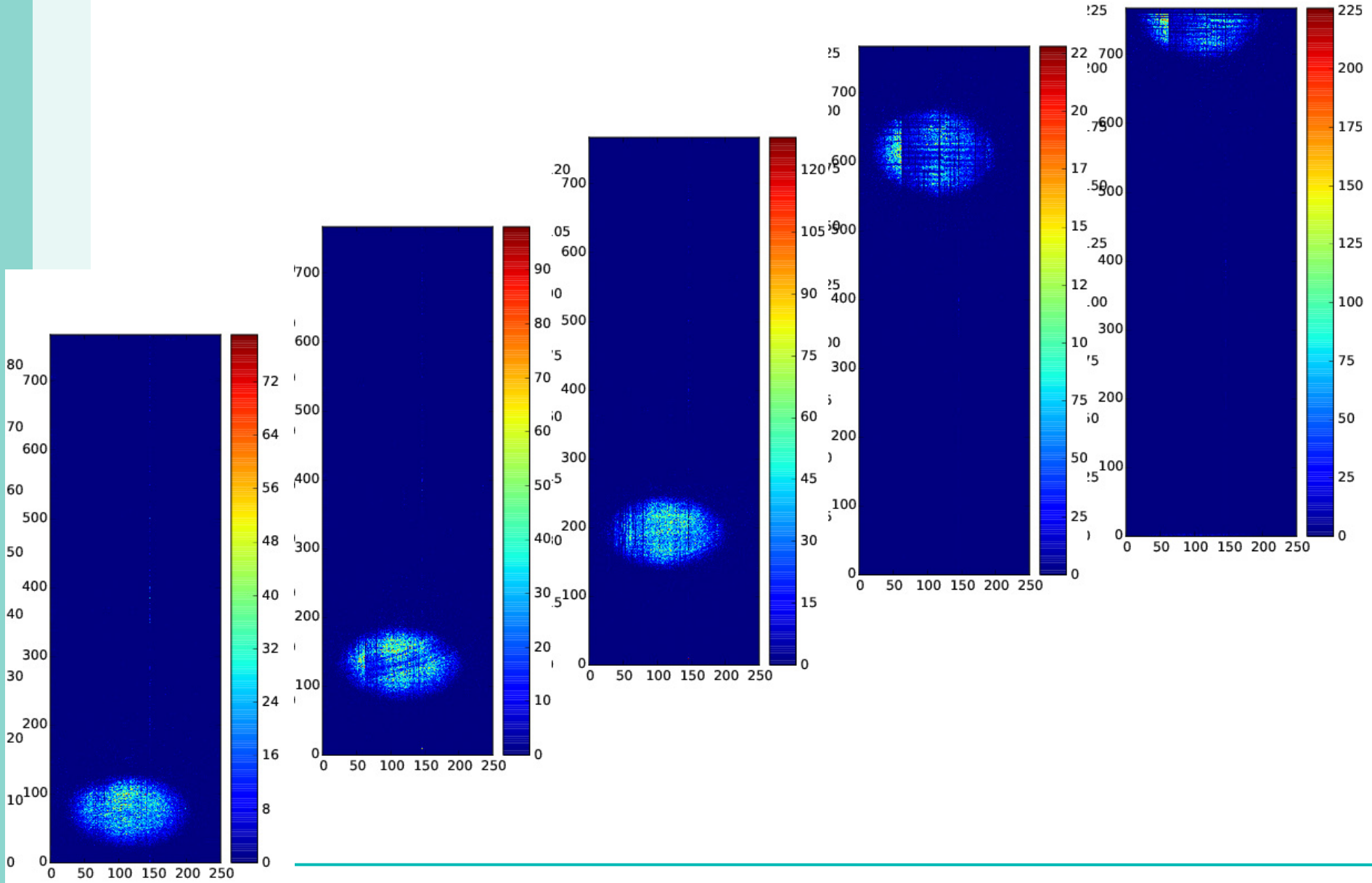


Source moved down
→ Much less sensitivity in the rows which are addressed by the 3rd Switcher



- Change the Clear On voltages helps

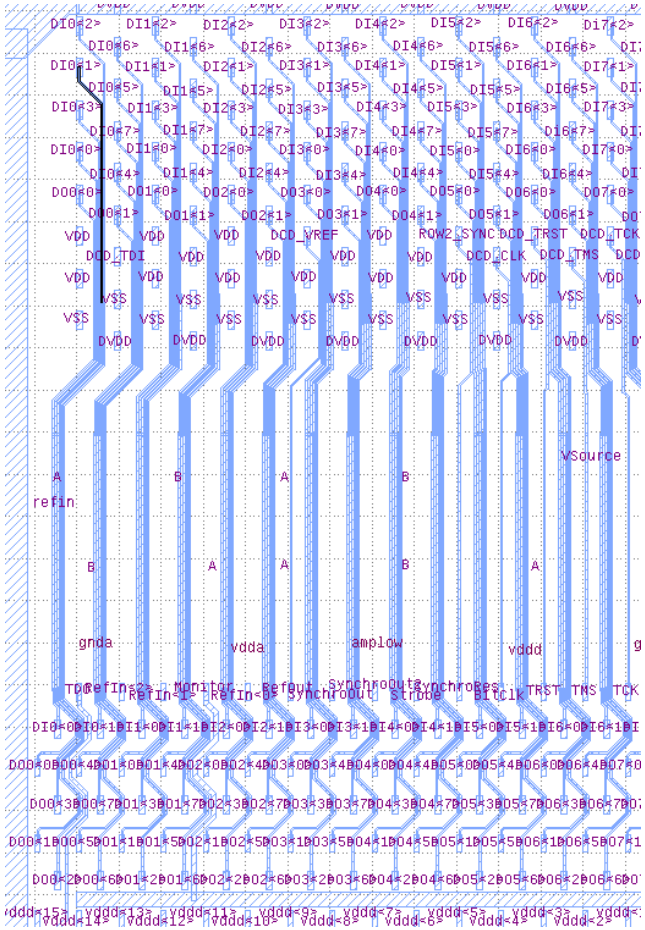
Cd109 Hitmap

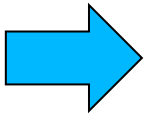


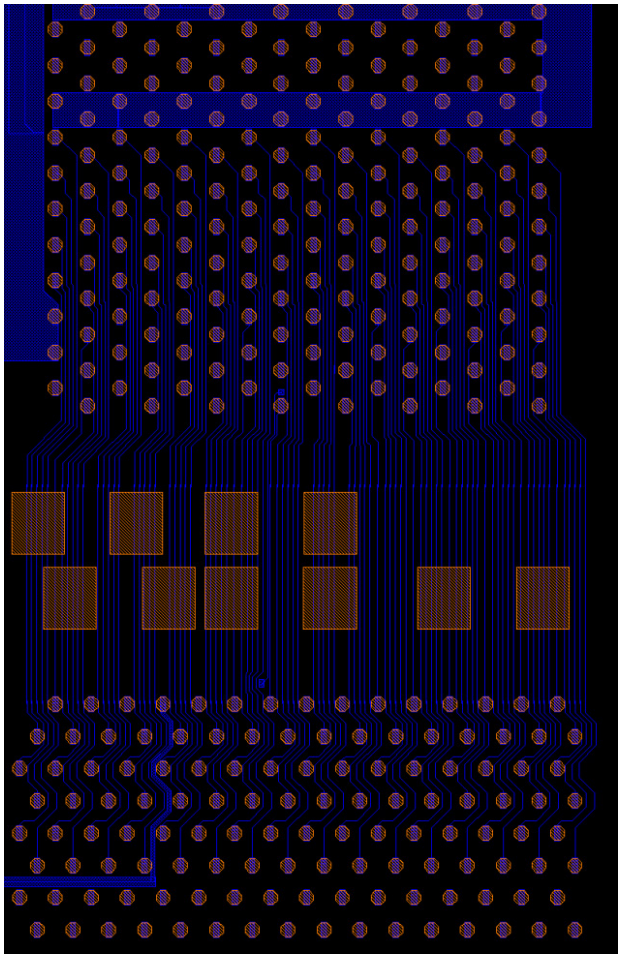
Felix Müller, Christian Koffmane

PXD9 Layout Changes

- Trace to trace distance for the digital lines between DHPT and DCD

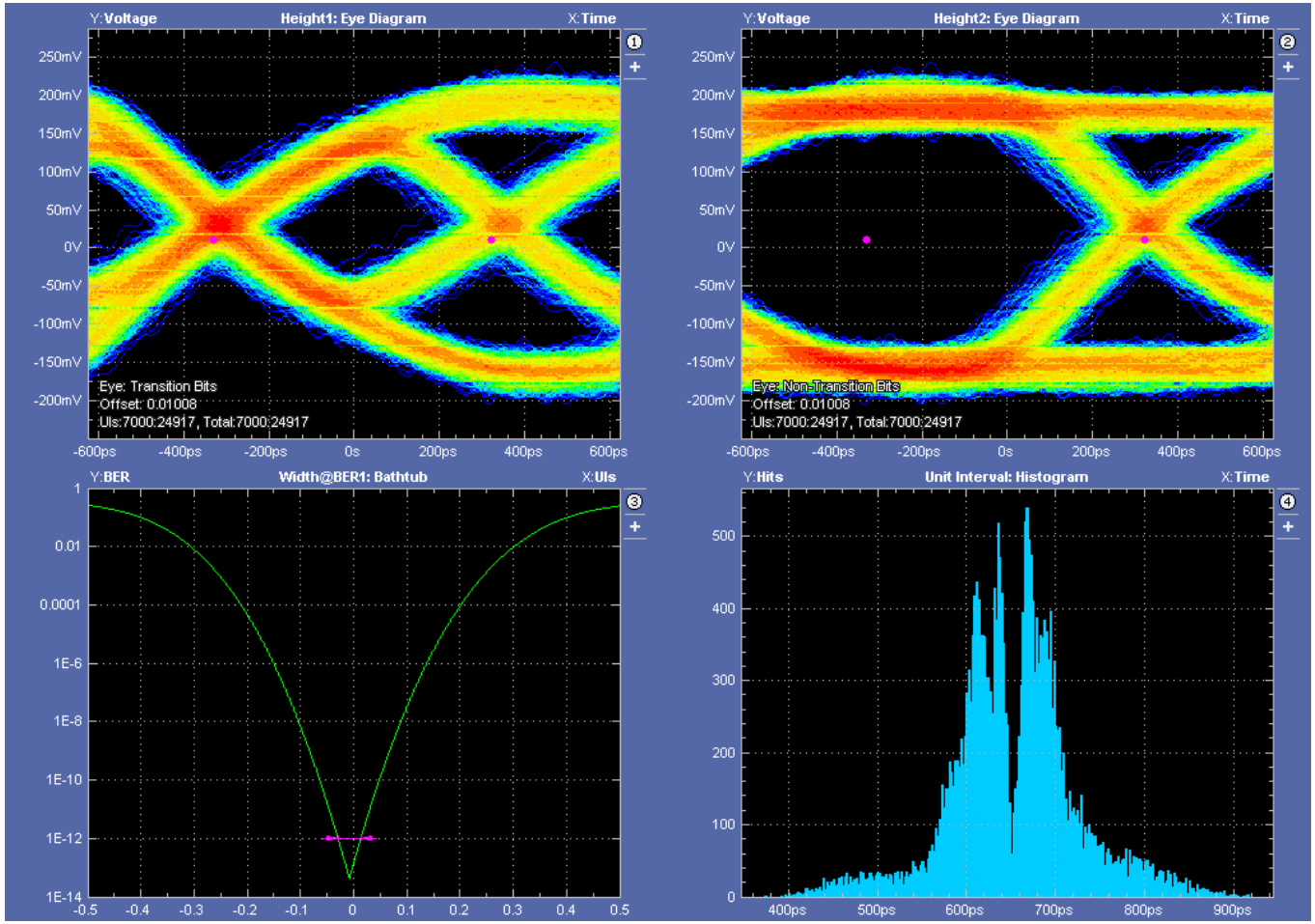






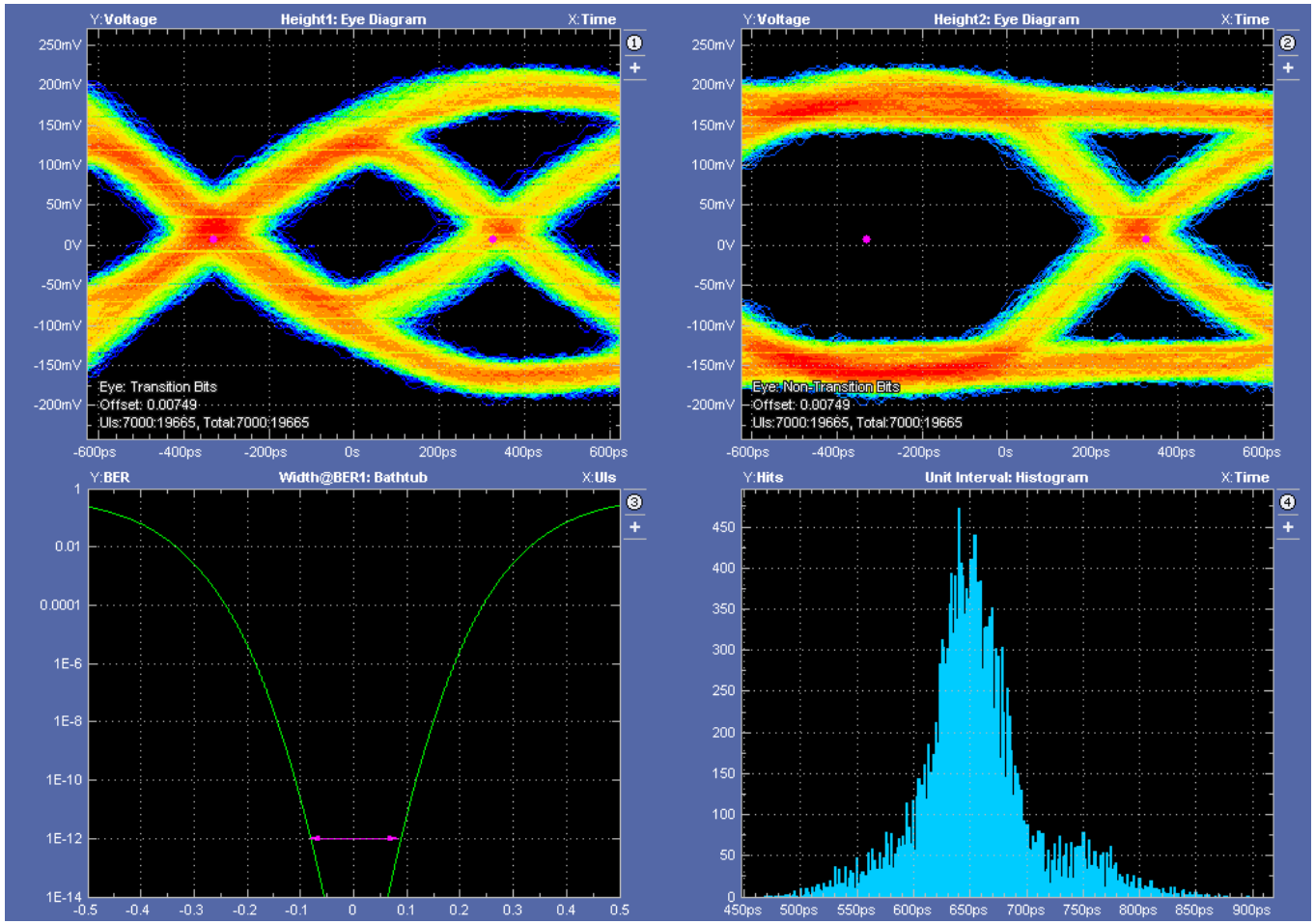
BACKUP

DHP1_1.2V_76.23MHz_Bias13_BiasD40BiasDelay50_Bath_UI_allASICsOn.png



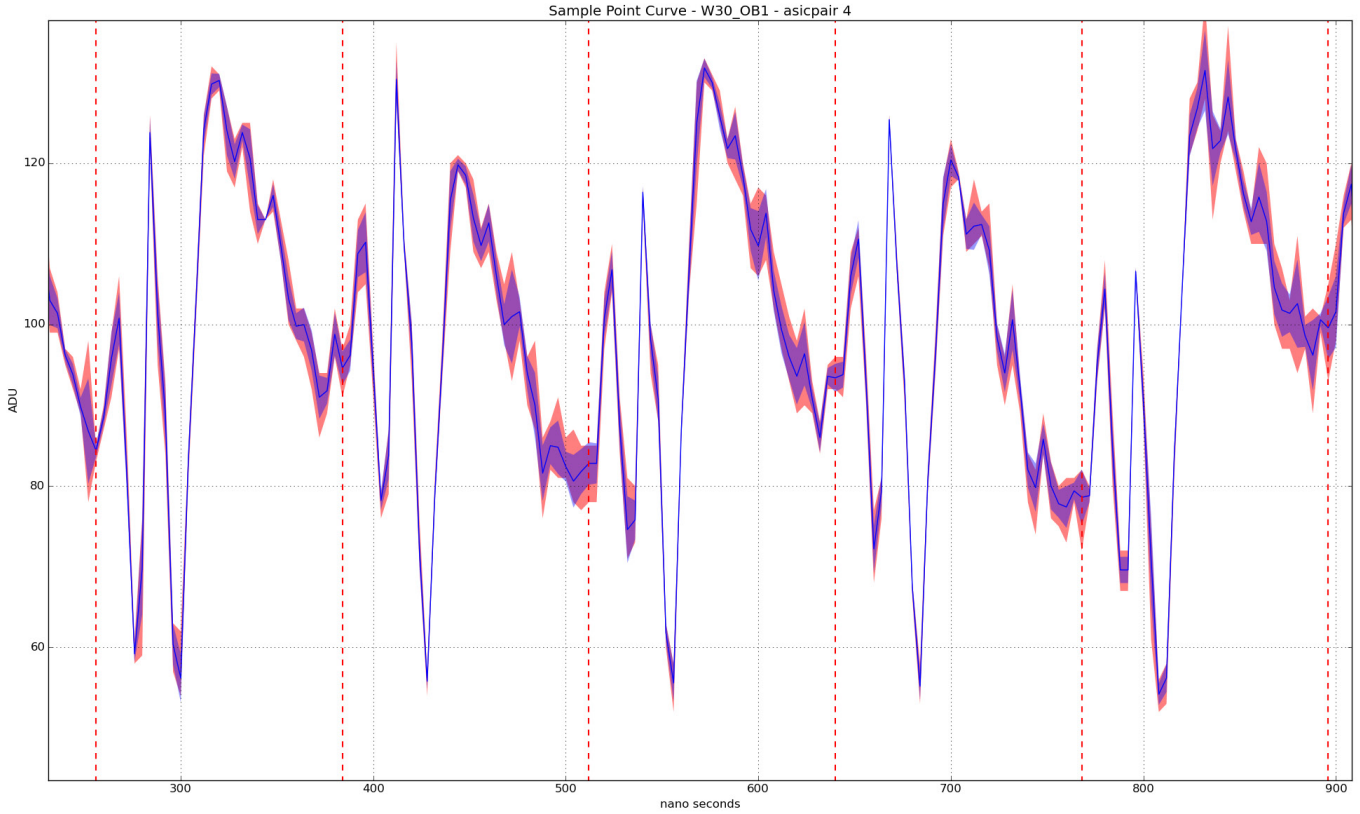
DCDs analog: ON

DHP2_1.2V_76.23MHz_Bias15_BiasD150BiasDelay50_bath_UI.png



DCDs analog: OFF

W30-OB-1 – bad ClearOn for SWB1-3



Backup – Laser Spot