PXD9 Pilot Module

Summary of Measurement Campaign of Pilot Module

PXD Belle II SeeVogh – December 08, 2015

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PXD9 Pilot Verification Plan

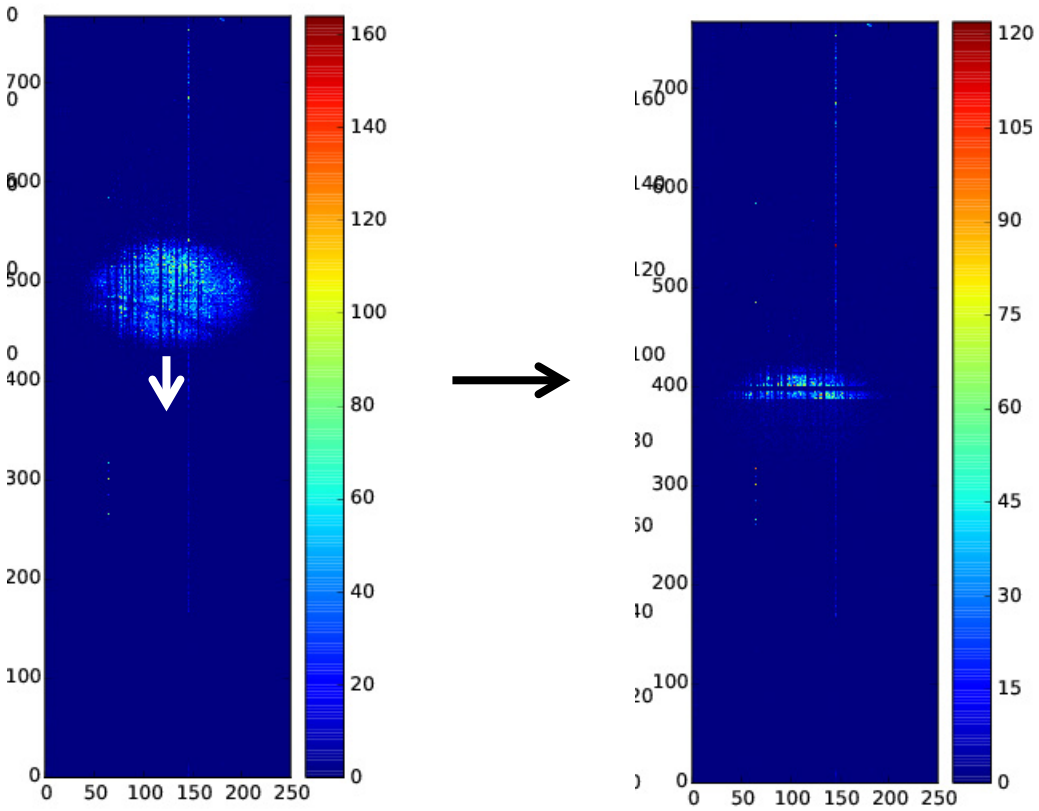
	26.-30. Oct	2.-6. Nov	9.13. Nov	16.-20. Nov	23.-27. Nov	30. Nov - 4.Dec.	Dec. 7th
CW	44	45	46	47	48	49	50
HLL (pxdtest2)	sampling point scan			increase to nominal freq.	gated mode	PXD9 SeeVogh Meeting	**Go for PXD9 metallization or agreement on the necessary changes** **Technical Board Meeting**
	pedestal/noise all DCDs			DHPT serial link - IBERT/oscilloscope	pedestal compression		
				DCD <-> DHPT (delay)	Cd109 spectrum		
				sampling point scan	Laser spot		
				pedestal/noise all DCD			
				zero suppressed data			
HLL (pxdtest4)			Preparation Gated Mode Test EMCM			Hybrid 7 Testing to verify OF/IB balcony and EOS layout	

PXD9 Pilot Verification Plan - updated

	9.13. Nov	16.-20. Nov	23.-27. Nov	30. Nov - 4.Dec.	7. Dec. - 11. Dec.	14. Dec. - 18. Dec.	Dec. 2015 / Jan. 2016
CW	46	47	48	49	50	51	47
HLL (pxdtest2)	sampling point scan	increase to nominal freq.	gated mode	**PXD9 SeeVogh Meeting**	DHPT serial link - IBERT/oscilloscope	**Go for PXD9 Alu1 metallization and agreement on the necessary changes** **Technical Board Meeting** **Dec. 15th**	gated mode
	pedestal/noise all DCDs	DHPT serial link - IBERT/oscilloscope	pedestal compression		Cd109 spectrum **Clear voltages / sequence**		
		DCD <-> DHPT (delay)	Cd109 spectrum		**Common Mode Noise**		
		sampling point scan	Laser spot				
		pedestal/noise all DCD					
		zero suppressed data					
HLL (pxdtest4)	Preparation Gated Mode Test EMCM			Hybrid 7 Testing to verify OF/IB balcony and EOS layout			

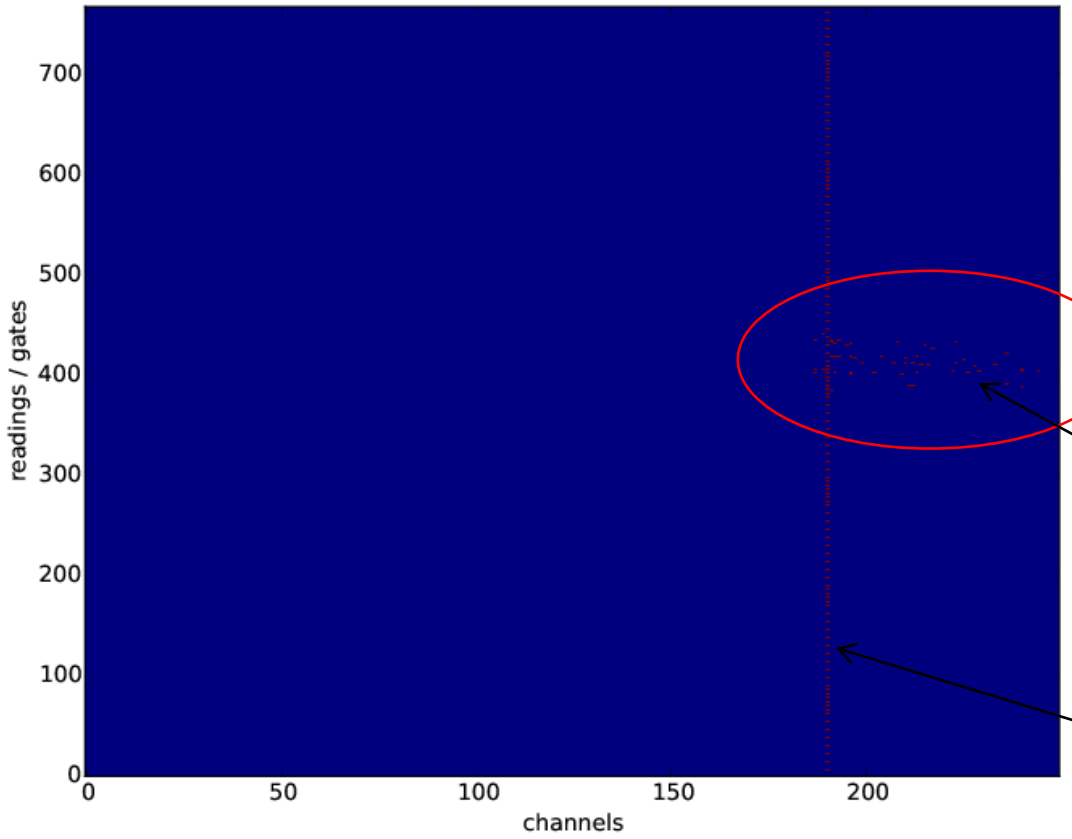
Cd109 Hitmap

- Hit map using a Cd109 source
- read-out of all ASIC simultaneously
- GCK = 62.5 MHz
- T_row = 128ns



- Change in the Clear performance between Switcher 3 and Switcher 4
- Non-complete Clear for Switcher 4, Switcher 5 and Switcher 6
- Charge from Cd109 visible in frame n and frame n+1
- Could be improved by changing the length of the StrC signal (32ns)
- Impact of the ClearOn and ClearGate voltages and timing of StrC signal is under investigation

Cd109 Hitmap



Comparison between frame n and frame n+1
Trigger length = 3072
only one DHPT read

Charge remained in internal gate in the next frame.

Vertical line is done on purpose to test the software

- Change in the Clear performance between Switcher 3 and Switcher 4
- Non-complete Clear for Switcher 4, Switcher 5 and Switcher 6
- Charge from Cd109 visible in frame n and frame n+1
- Could be improved by changing the length of the StrC signal (32ns)
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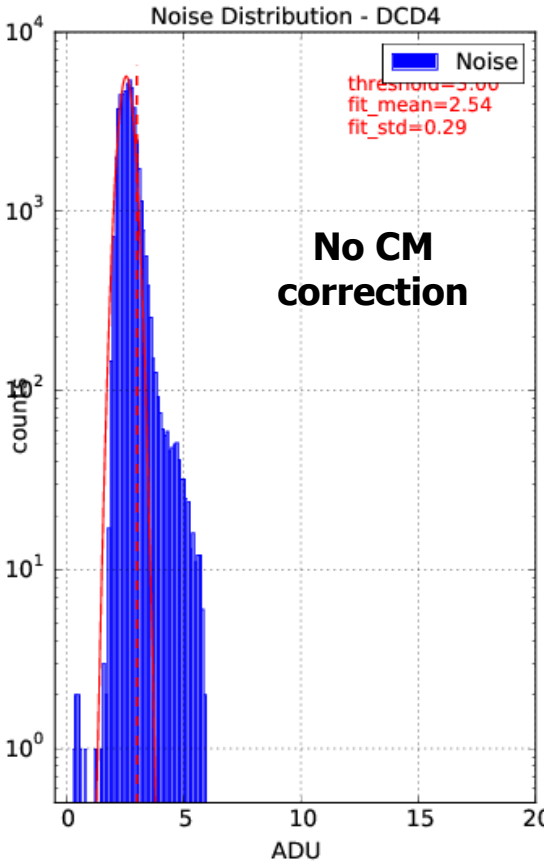
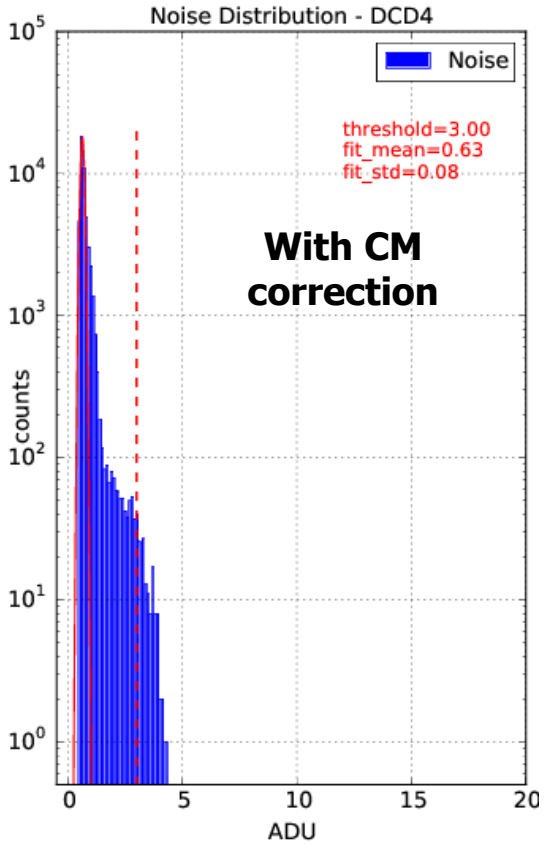
Common Mode Noise





- Tail probably still bit-errors in the DCD-DHPT data transmission
- No change of the CM when HV or grounding of the alu jig was modified
- Investigation on the CM when Switchers and DEPFETs are in steady state is ongoing

Summary

- Dedicated PXD9 Pilot SeeVogh last week – slides distributed to the mailing list and on today´s indico page
- We are working on the main open topics
  - CM noise
  - Different Clear performance between Switchers 1-3 and Switchers 4-6
  - Hybrid 7
- Technical board meeting to discuss the results of the PXD9 pilot measurements and the risk if we go ahead with the Alu1 metallization is planned for Tuesday next week

Backup

Cd109 Hitmap – Non-complete Clear

- Too low Clear On voltage applied
- Non-complete Clear
- Charge from Cd109 visible in frame n and frame n+1