Status of Copper Link Characterization
&
Switcher Control Lines on PXD Module

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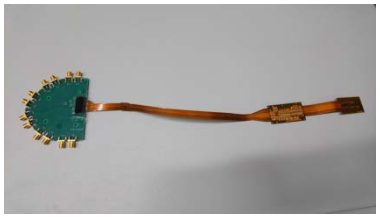
15.12.2015

Status of Copper Link Characterization

- Received all components of the link yesterday (14.12.2015 , one year after the initial request in Nov 2014).



Kapton cable with breakout board

Short (2m) TWP cable with soldered PP

Dock box patch panel

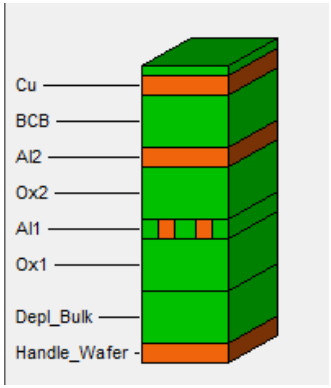
Long (12m) TWP cable

- To do
  - TDR measurements → check for impedance discontinuities (patch panels, connectors etc.)
  - S-parameter extraction → cable model for DHPT driver simulation
  - For measurements with DHPT and the full setup we would need **a EMCM with DHPT 1.1 and a production flex cable** connected.

Switcher Control Lines on PXD Module

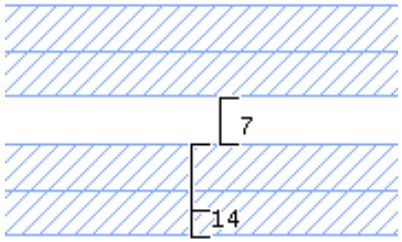
- Simplified layer stackup

Layer Name	Usage	Thickness um	Er
	Solder Mask	5	4
Cu	Plane	5	<Auto>
BCB	Substrate	3	3
Al2	Plane	1	<Auto>
Ox2	Substrate	1	4
Al1	Signal	1	<Auto>
Ox1	Substrate	1	4
Depl_Bulk	Substrate	75	11
Handle_Wafer	Plane	17.145	<Auto>



(HyperLynx limitations → 1µm min. layer thickness, no resistive reference planes)

- Differential Switcher control lines
  - Routing on Al1
  - Width = 14µm (over etching → 12µm)
  - Spacing = 7µm (over etching → 9µm)
  - DHPT to last Switcher: ~60 (50) mm length for inner (outer) module



TML Parameters

Calculation from simplified stackup (does not take routing details into account, i.e. AL2 doubling, accurate ILD thickness, etc…)

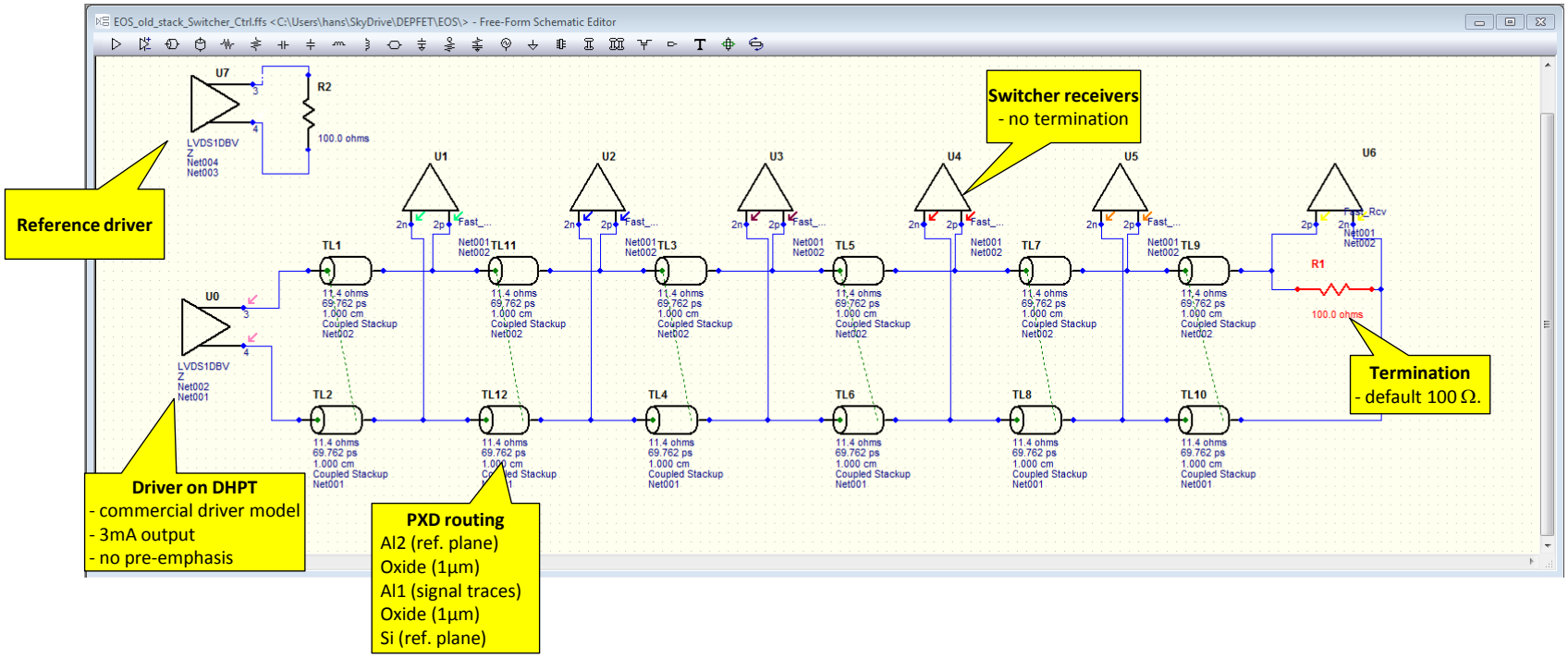
- Differential impedance $Z_{0\ diff}$ = 22 Ohm
- DC line resistance Z_{DC} : 14 Ohm/cm → ~80 Ohm per single line
- Ideal case: $Z_{DC} = 0\Omega$, $Z_{0\ diff} = 100\Omega$

➔ Impedance mismatch (100 Ohm termination vs. 22 Ohm TML impedance) is **not** the main issue

➔ The problem is the DC line resistance, i.e. the pronounced lossy behavior of the TML

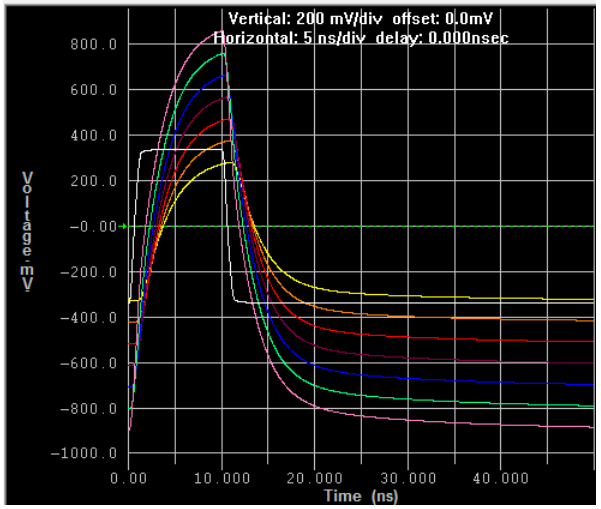
Simulation Environment

- Simulation tool: HyperLynx (➔ PCB signal integrity, not optimized for VLSI routing…)
- TML model: 1 cm coupled lines on PXD module stackup from one Switcher to the next
- LVDS driver model → SN65LVDS1 (switched 3 mA current source)

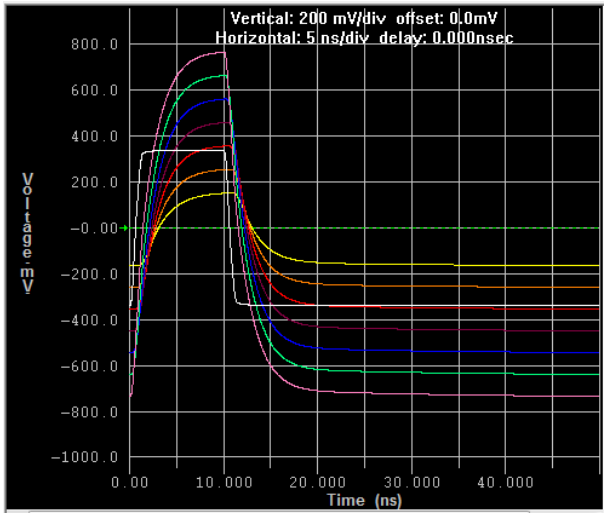


Simulation Results – Current Layout

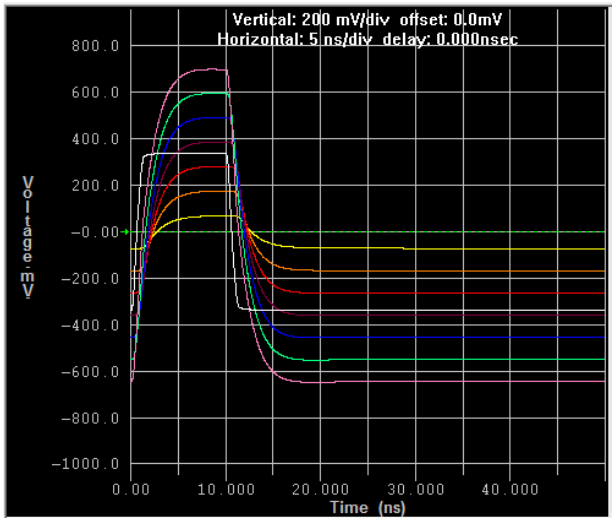
- Signal: 10ns pulse
- Sweep parameter: Switcher location
- Changed termination resistor values at end of the line (last Switcher)



100 Ohm



50 Ohm

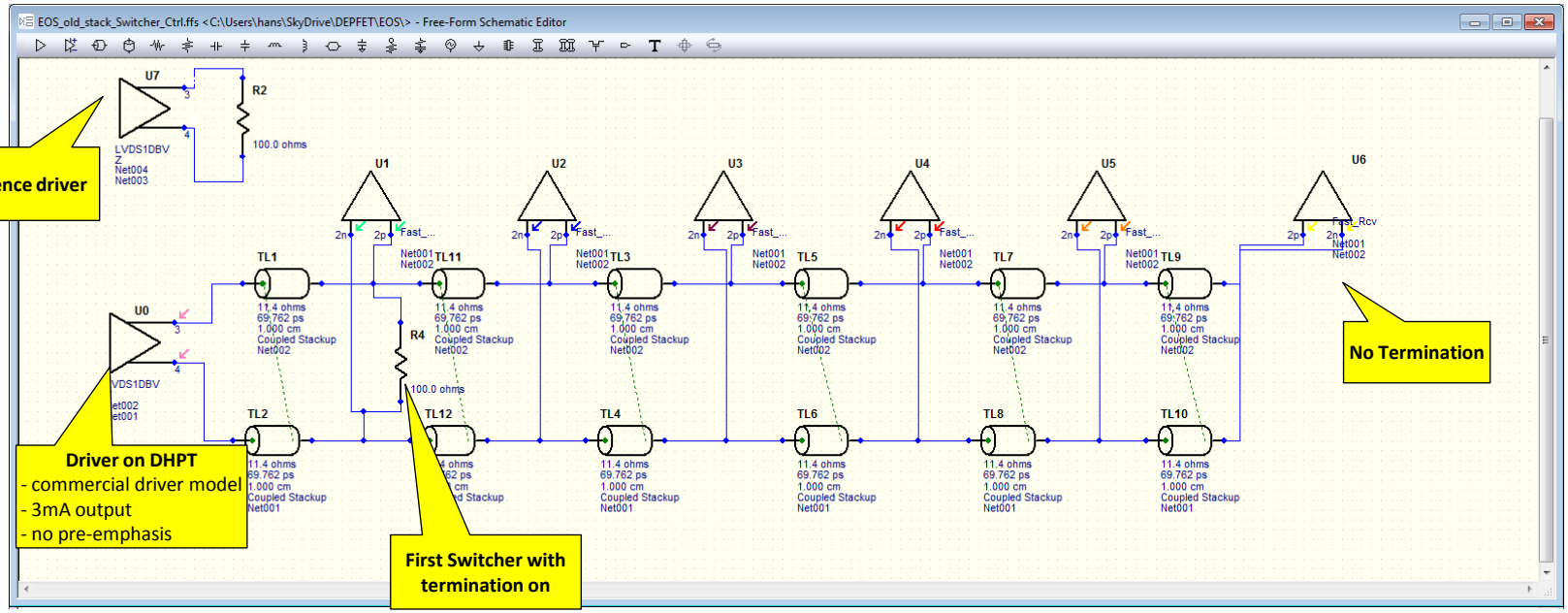


22 Ohm

➔ Smaller termination resistor improves rise time, but makes amplitude difference between first and last switcher worse

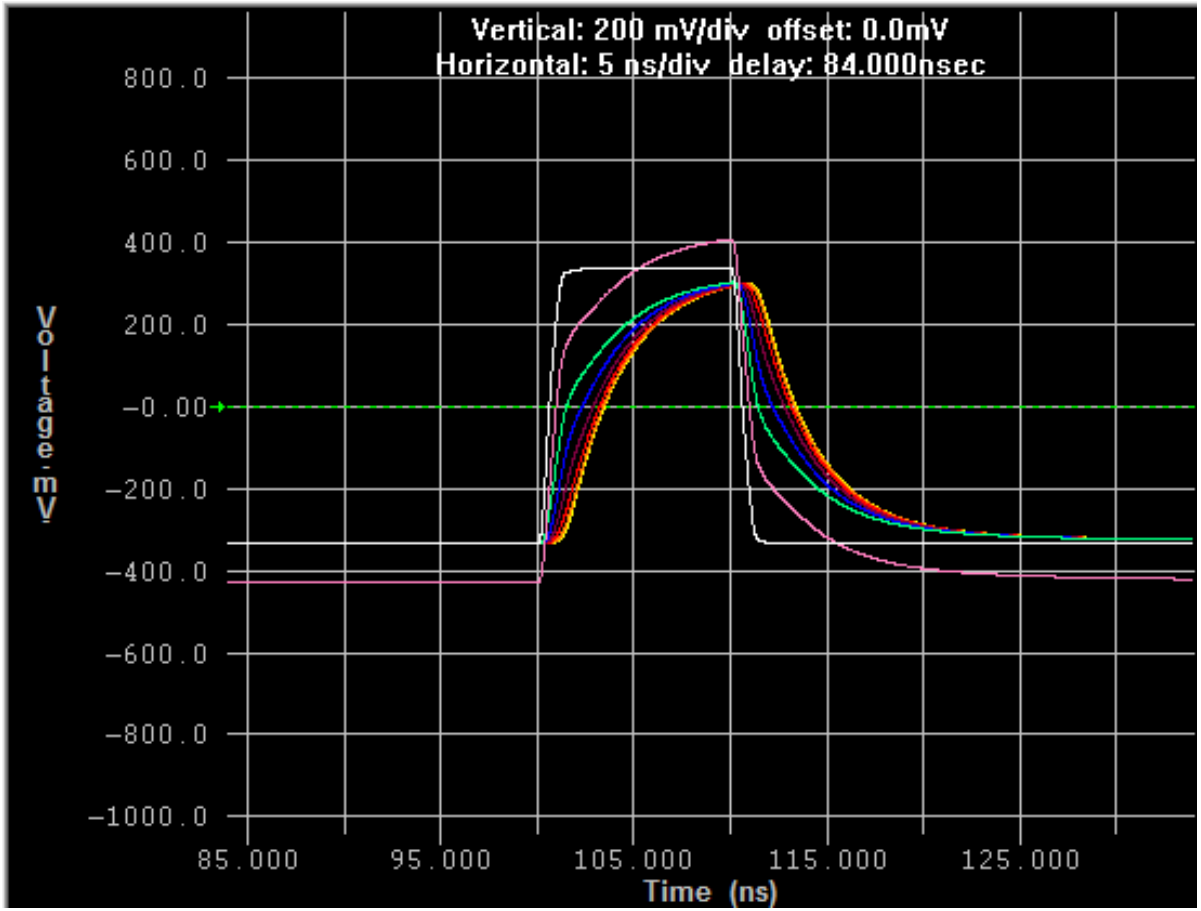
Adjusted Termination Scheme

- Removed termination from the last Switcher ➔ avoid the loss of the resistive divider
- Enabled the termination of the first Switcher ➔ convert output current of the LVDS driver to voltage swing
- Reflections possibly negligible due to the high damping of the TML



Waveforms with Adjusted Termination Scheme

- 100 Ohm termination enabled only for first Switcher, all others off



Preliminary Conclusion

- Non negligible DC resistance of the TML has two effects
  - Signal rise time becomes lower
  - Received signal amplitude becomes a function of the distance to the driver (resistive divider between DC line resistance and termination resistor)

- Possible solution: Enable termination on first Switcher only